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ICL7112

January 1998

12-Bit, High-Speed, CMOS μP-Compatible A/D Converter

Features

- **12-Bit Resolution and Accuracy**
- **No Missing Codes**
- **Microprocessor Compatible Byte-Organized Buffered Outputs**
- **Auto-Zeroed Comparator for Low Offset Voltage**
- **Low Linearity and Gain Errors**
- **Low Power Consumption (60mW)**
- **No Gain or Offset Adjustment Necessary**
- **Provides 3% Usable Overrange**
- **Fast Conversion (40μs)**

Description

The ICL7112 is a monolithic 12-bit resolution, fast successive approximation A/D converter. It uses thin film resistors and CMOS circuitry combined with an on-chip PROM calibration table to achieve 12-bit linearity without laser trimming. Special design techniques used in the DAC and comparator result in high speed operation, while the fully static silicon-gate CMOS circuitry keeps the power dissipation very low.

Microprocessor bus interfacing is eased by the use of standard memory $\overline{\text{WRite}}$ and $\overline{\text{ReaD}}$ cycle timing and control signals, combined with $\overline{\text{Chip}}$ $\overline{\text{Select}}$ and Address pins. The digital output pins are byte-organized and three-state gated for bus interface to 8-bit and 16-bit systems.

The ICL7112 provides separate Analog and Digital grounds for increased system accuracy. Operating with ±5V supplies, the ICL7112 accepts 0V to +10V input with a -10V reference or 0V to -10V input with a +10V reference.

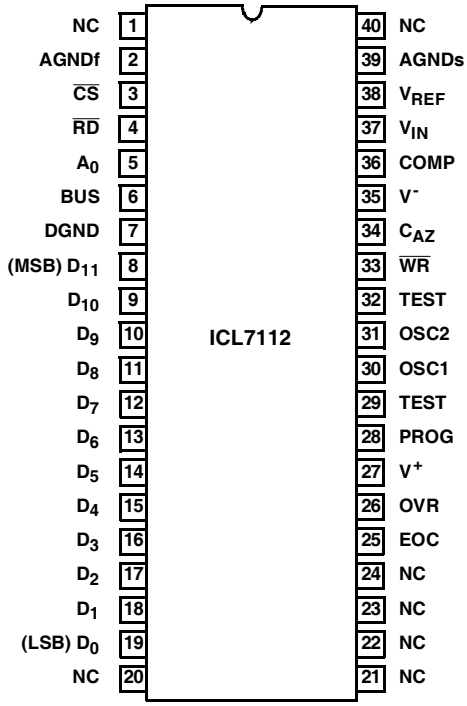
Ordering Information

PART NO.	TEMP. RANGE (^{o}C)	PACKAGE	RESOLUTION WITH NO MISSION CODES
ICL7112JCDL	0 to 70	40 Ld CERDIP	11-Bit
ICL7112KCDL	0 to 70	40 Ld CERDIP	12-Bit
ICL7112LCDL	0 to 70	40 Ld CERDIP	12-Bit (Note)±
ICL7112JIDL	-25 to 85	40 Ld CERDIP	11-Bit
ICL7112KIDL	-25 to 85	40 Ld CERDIP	12-Bit
ICL7112LIDL	-25 to 85	40 Ld CERDIP	12-Bit (Note)±
ICL7112JMDL	-55 to 125	40 Ld CERDIP	11-Bit
ICL7112KMDL	-55 to 125	40 Ld CERDIP	12-Bit
ICL7112LMDL	-55 to 125	40 Ld CERDIP	12-Bit (Note)±

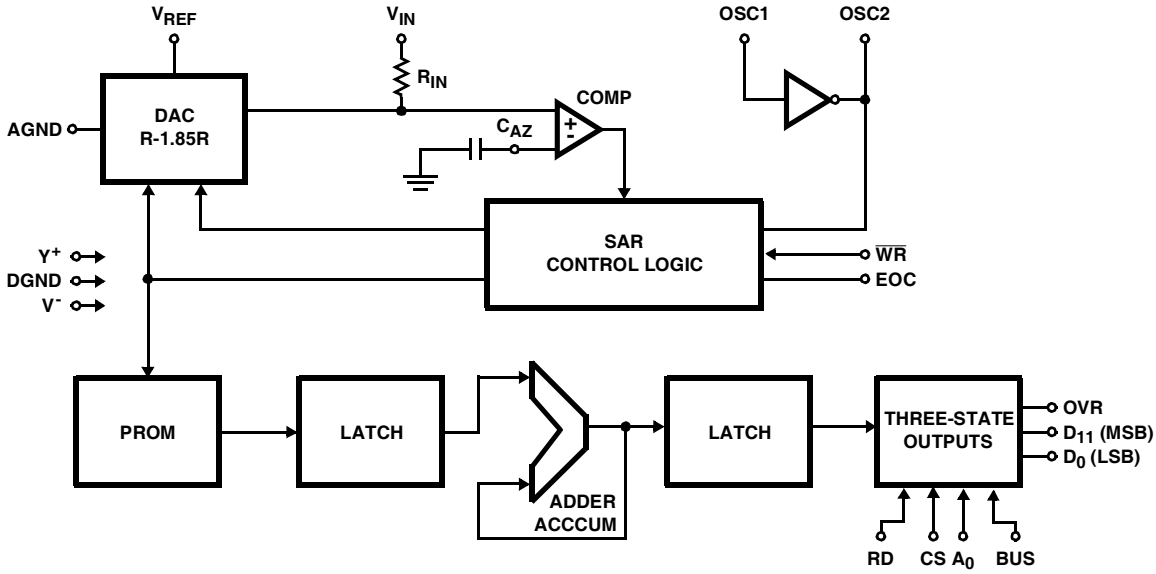
NOTE: Over operating temperature range.

Pinout

ICL7112
TOP VIEW



Functional Block Diagram



Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage (V^+ to DGND) . . . . . -0.3V to +6.5V
Supply Voltage (V^- to DGND). . . . . +0.3V to -6.5V
V_{REF}, V_{IN} to DGND . . . . . ±25V
AGND to DGND . . . . . +1V to -1V
V_{REF}, V_{IN}, AGND Current 25mA
Digital I/O Pin Voltages. . . . . -0.3V to V+ +0.3V
PROG to DGND Voltage . . . . . V^- to (V+ +0.3V)

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
CERDIP Package	___	___

Maximum Power Dissipation (Note 2). 500mW
Derate above 70^oC at $10mW/^oC$
Maximum Junction Temperature (Ceramic Package) . . . . . 175^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s). . . . . 300^oC

Operating Conditions

ICL7112XCXX. . . . . 0 to 70
ICL7112XIXX . . . . . -25 to 70
ICL7112XMXX . . . . . -55 to 125

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
2. All voltages with respect to DGND, unless otherwise noted.
3. Assumes all leads soldered or welded to printed circuit board.

Electrical Specifications

Test Conditions: V+ = +5V, V- = -5V, V_{REF} = -10V, $T_A = 25^oC$, f_{CLK} = 500kHz, Unless Otherwise Noted

PARAMETER	SYMBOL	TEST CONDITIONS	J			K			L			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
ACCURACY												
Resolution	RES				12							Bits
Resolution with No Missing Codes	RES (NMC)	Notes 4, 5, 6 R_M T_{MIN} -T_{MAX}	11 10	-	-	12 11	-	-	12 12	-	-	Bits
Integral Linearity Error	I_{LE}	Notes 4, 5 R_M T_{MIN} -T_{MAX}	-	-	±0.024 ±0.030	-	-	±0.012 ±0.020	-	-	±0.012 ±0.020	%FSR
Unadjusted Full Scale Error	FSE	Adjust-able to Zero; C; R_M T_{MIN} T_{MAX}	-	-	±0.10 ±0.12	-	-	±0.08 ±0.10	-	-	±0.08 ±0.10	%FSR
		I; R_M T_{MIN} -T_{MAX}	-	-	±0.10 ±0.13	-	-	±0.08 ±0.11	-	-	±0.08 ±0.11	
		M; R_M T_{MIN} -T_{MAX}	-	-	±0.10 ±0.14	-	-	±0.08 ±0.12	-	-	±0.08 ±0.12	
Zero Error	ZE	Notes 4, 5 R_M T_{MIN} -T_{MAX}	-	-	±1 ±1.5	-	-	±1 ±1.5	-	-	±1 ±1.5	
ANALOG INPUT												
Analog Input Range	V_{IN}		0	-	10.3	0	-	10.3	0	-	10.3	V
Input Resistance	R_{IN}	Notes 5, 8	4	-	9	4	-	9	4	-	9	kΩ
Temperature Coefficient of R_{IN}	T_C (R_{IN})	T_{MIN} -T_{MAX}	-	-300	-	-	-300	-	-	-300	-	$ppm/^oC$
REFERENCE INPUT												
Analog Reference	V_{REF}		-	-10.0	-	-	-10.0	-	-	-10.0	-	V
Reference Resistance	R_{REF}		-	5	-	-	5	-	-	5	-	kΩ
POWER SUPPLY SENSITIVITY												
Power Supply Rejection Ration	PSRR	V^+, V^- = 4.5 -5.5V RM T_{MIN} -T_{MAX}	-	±0.5	±1 ±2	-	±0.5	±1 ±2	-	±0.5	±1 ±2	LSB
LOGIC INPUT												
Low State Input Voltage	V_{IL}	T_{MIN} -T_{MAX}	-	-	0.8	-	-	0.8	-	-	0.8	V

Electrical Specifications Test Conditions: V+ = +5V, V- = -5V, V_{REF} = -10V, T_A = 25°C, f_{CLK} = 500kHz, Unless Otherwise Noted

PARAMETER	SYMBOL	TEST CONDITIONS	J			K			L			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
High State Input Voltage	V_{IH}	T_{MIN} -T_{MAX}	2.4	-	-	2.4	-	-	2.4	-	-	V
Logic Input Current	I_{LIH}	$0 < V_{IN} < V^+$	-	1	10	-	1	10	-	1	10	µA
Logic Input Capacitance	C_{IN}		-	15	-	-	15	-	-	15	-	pF
LOGIC OUTPUT												
Low State Output Voltage	V_{OL}	I_{OUT} = 1.6mA T_{MIN} -T_{MAX}	-	-	0.4	-	-	0.4	-	-	0.4	V
High State Output Voltage	V_{OH}	I_{OUT} = -200µA T_{MIN} -T_{MAX}	2.8	-	-	2.8	-	-	2.8	-	-	V
Three-State Output Current	I_{OX}	$0 < V_{OUT} < V^+$	-	1	-	-	1	-	-	1	-	µA
Logic Output Capacitance	C_{OUT}	Three-State	-	15	-	-	15	-	-	15	-	pF
POWER REQUIREMENTS												
Supply Voltage Range	V_{SUPPLY}	Functional Operation Only	±4.5	-	±6.0	±4.5	-	±6.0	±4.5	-	±6.0	V
Supply Current, I+, I-	I_{SUPPLY}	R_M T_{MIN} -T_{MAX}	-	2	4 6	-	2	4 6	-	2	4 6	mA

NOTES:

4. Full scale range (FSR) is 10V (reference adjusted).
5. Assume all leads are soldered or welded to printed circuit board.
6. "J" and "K" versions not production tested. Guaranteed by Integral Linearity Test.
7. Typical values are not tested, for reference only.
8. Not production tested. Guaranteed by design.

AC Electrical Specifications Test Conditions V+ = +5V, V- = -5V, T_A = 25°C, f_{CLK} = 500kHz, unless otherwise noted. Data derived from extensive characterization testing. Parameters are not production tested

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
READ CYCLE TIMING						
Propagation Delay $\overline{CS}$ to Date	t_{cd}	$\overline{RD}$ Low, A_0 Valid	-	-	200	ns
Propagation Delay A_0 to Data	t_{ad}	$\overline{CS}$ Low, $\overline{RD}$ Low	-	-	200	
Propagation Delay $\overline{RD}$ to Data	t_{rd}	$\overline{CS}$ Low, A_0 Valid	-	-	200	
Propagation Delay Data to Three-State	t_{rx}		-	-	150	
Propagation Delay EOC High to Data	t_{ed}		-	-	200	
WRITE CYCLE TIMING						
$\overline{WR}$ Low Time	t_{wr}		150	-	-	ns
Propagation Delay $\overline{WR}$ Low to EOC Low	t_{we}	Wait Mode	1	-	2	
EOC High Time	t_{eo}	Free Run Mode	0.5	-	1.5	$1/f_{CLK}$
Conversion Time	t_{conv}		-	-	20	
Clock Frequency Range	f_{CLK}	Functional Operation Only	-	500	-	kHz

NOTE:

9. All typical values have been characterized, but are not tested.

Pin Descriptions

PIN NO.	NAME	DESCRIPTION	
1		No connection.	
2	$AGND_f$	FORCE input for analog ground.	
3	$\overline{CS}$	Chip Select enables reading and writing (active low).	
4	$\overline{RD}$	$\overline{ReaD}$ (active low).	
5	A_0	Byte select (low = D_0 -D_7, high = D_8 -D_{11}, OVR).	
6	BUS	Bus select (low = outputs enabled by A_0, high = all outputs enabled together).	
7	DGND	Digital GrouND return.	
8	D_{11}	Bit 11 (most significant bit).	High Byte
9	D_{10}	Bit 10	
10	D_9	Bit 9	
11	D_8	Bit 8	
12	D_7	Bit 7	
13	D_6	Bit 6	
14	D_5	Bit 5	Low Byte
15	D_4	Bit 4	
16	D_3	Bit 3	
17	D_2	Bit 2	
18	D_1	Bit 1	
19	D0	Bit 0 (least significant bit).	
20		No connection.	
21		No connection.	
22		No connection.	
23		No connection.	
24		No connection.	
25	EOC	End of conversion flag (low = busy, high = conversion complete).	
26	OVR	OVerRange flag (valid at end of conversion when output code exceeds full-scale; three-state output enabled with high byte).	
27	V^+	Positive power supply input.	
28	PROG	Used for programming only. Must tie to V^+ for normal operation.	
29	TEST	Used for programming only. Must tie to V^+ for normal operation.	
30	OSC1	Oscillator inverter input.	
31	OSC2	Oscillator inverter output.	
32	TEST	Must tie to V^+ for normal operation.	
33	$\overline{WR}$	$\overline{WRite}$ pulse input (low starts new conversion).	
34	C_{AZ}	Auto-zero capacitor connection (Note).	
35	V^-	Negative power supply input.	
36	COMP	Used in test, tie to V^-.	
37	V_{IN}	SENSE line for input voltage.	
38	V_{REF}	SENSE line for reference input.	
39	$AGND_s$	SENSE line for analog ground.	
40		No connection	

Output Data Bits (High =True)

NOTE: The voltage of CAZ is driven; NEVER connect directly to ground.

Timing Diagrams

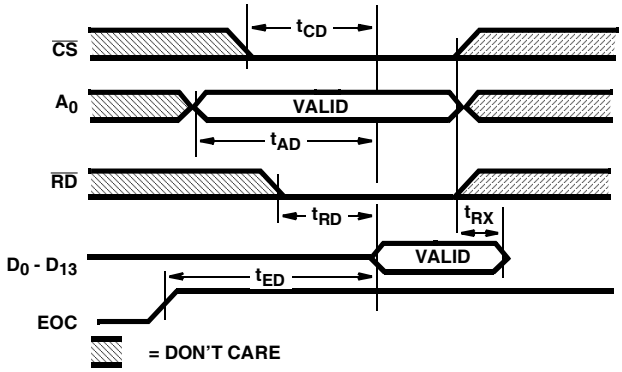


FIGURE 1. READ CYCLE TIMING

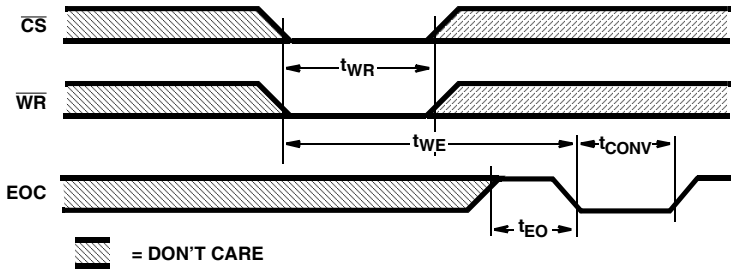


FIGURE 2. WRITE CYCLE TIMING

TABLE 2: I/O CONTROL

$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	A_0	BUS	FUNCTION
0	0	x	x	x	Initiates a conversion.
1	x	x	x	x	Disables all chip commands.
0	x	0	0	0	Low byte is enabled.
0	x	0	1	0	High byte is enabled.
0	x	0	x	1	Low and High bytes enabled together.
x	x	1	x	x	Disables outputs (high-impedance).

TABLE 3: TRANSFER FUNCTION

INPUT VOLTAGE	EXPECTED OUTPUT CODE			
V_{REF} = -10.0V	OVR	MSB		LSB
0	0	0	0000000000	0
+0.00244	0	0	0000000000	1
+0.30029	0	0	0000111101	1
+4.99756	0	0	1111111111	1
+5.00000	0	1	0000000000	0
+9.99512	0	1	1111111111	0
+9.99756	0	1	1111111111	1
+10.00000	1	0	0000000000	0
+10.00244	1	0	0000000000	1
+10.29000	1	0	0000111101	1

Detailed Description

The ICL7112 is basically a successive approximation A/D converter with an internal structure much more complex than a standard SAR-type converter. The Functional Block Diagram shows the functional diagram of the ICL7112 12-bit A/D converter. The additional circuitry incorporated into the ICL7112 is used to perform error correction and to maintain the operating speed in the 40μs range.

The internal DAC of the ICL7112 is designed around a radix of 1.85, rather than the traditional 2.00. This radix gives each bit of the DAC a weight of approximately 54% of the previous bit. The result is a usable range that extends to 3% beyond the full-scale input of the A/D. The actual value of each bit is measured and stored in the on-chip PROM. The absolute value of each bit weight then becomes relatively unimportant because of the error correction action of the ICL7112.

The output of the high-speed auto-zeroed comparator is fed to the data input of a successive approximation register (SAR). This register is uniquely designed for the ICL7112 in that it tests bit pairs instead of individual bits in the manner of a standard SAR. At the beginning of the conversion cycle, the SAR turns on the MSB (D_{11}) and the MSB 4-bit (D_7). The sequence continues for each bit pair, B_X and B_{x-4}, until only the four LSBs remain. The sequence concludes by testing the four LSBs individually.

The SAR output is fed to the DAC register and to the preprogrammed PROM where it acts as PROM address. PROM data is fed to a full-adder/accumulator where the decoded results from each successive phase of the conversion are summed with the previous results. After 20 clock cycles, the accumulator contains the final binary data which is latched and sent to the three-state output buffers. The accuracy of the A/D converter depends primarily upon the accuracy of the data that has been programmed into the PROM during

the final test portion of the manufacturing process.

The error correcting algorithm built into the ICL7112 reduces the initial accuracy requirements of the DAC. The overlap in the testing of bit pairs reduces the accuracy requirements on the comparator which has been optimized for speed. Since the comparator is auto-zeroed, no external adjustment is required to get ZERO code for ZERO input voltage.

Twenty clock cycles are required for the complete 12-bit conversion. The auto-zero circuitry associated with the comparator is employed during the last three clock cycles of the conversion to cancel the effect of offset voltage. Also during this time, the SAR and accumulator are reset in preparation for the start of the next conversion.

The overflow output of the full-adder is also the OVer Range (OVR) output of the ICL7112. Unlike standard SAR type A/D converters, the ICL7112 has the capability of providing valid usable data for inputs that exceed the fullscale range by as much as 3%.

Optimizing System Performance

When using A/D converters with 12 or more bits of resolution, special attention must be paid to grounding and the elimination of potential ground loops. A ground loop can be formed by allowing the return current from the ICL7112's DAC to flow through traces that are common to other analog circuitry. If care is not taken, this current can generate small unwanted voltages that add to or detract from the reference or input voltages of the A/D converter.

Figure 3 and Figure 4 show two different grounding techniques. Although the difference between the two circuits may not be readily apparent, the circuit of Figure 3 is very likely to have significant ground loop errors which the circuit of Figure 4 avoids. In Figure 3, the supply currents for analog ground, digital ground, and the reference voltage all flow through a lead, common to the input. This will generate a DC offset voltage due to the currents flowing in the resistance of the common lead. This offset voltage will vary with the input voltage and with the digital output. Even the auto-zero loop of the ICL7112 cannot remove this error.

Figure 4 shows a much better arrangement. The ground and reference currents do not flow through the input common lead, eliminating any error voltages. Note that the supply currents and any other analog system currents must also be returned carefully to analog ground. The clamp diodes will protect the ICL7112 against signals which could result from separate analog and digital grounds. The absolute maximum voltage rating between AGND and DGND is ±1.0V. The two inverse-parallel diodes clamp this voltage to less than ±0.7V.

Input Warning

As with any CMOS integrated circuit, no input voltages should be applied to the ICL7112 until the ±5V power supplies have stabilized.

Interfacing To Digital Systems

The ICL7112 provides three-state data output buffers, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, and bus select inputs (A_0 and BUS) for interfacing to a wide variety of microcomputers and digital systems. The I/O Control Truth Table shows the functions of the digital control lines. The BUS select and A_0 lines are provided to enable the output data onto either 8-bit or 16-bit data buses. A conversion is initiated by a $\overline{WR}$ pulse (pin 33) when $\overline{CS}$ (pin 3) is low. Data is enabled on the bus when the chip is selected and $\overline{RD}$ (pin 4) is low.

Figure 5 illustrates a typical interface to an 8-bit microcomputer. The "Start and Wait" operation requires the fewest external components and is initiated by a low level on the $\overline{WR}$ input to the ICL7112 after the I/O or memory mapped address decoder has brought the $\overline{CS}$ input low. After executing a delay or utility routine for a period of time greater than the conversion time of the ICL7112, the processor issues two consecutive bus addresses to read output data into two bytes of memory. A low level on A_0 enables the LSBs, and a high level enables the MSBs.

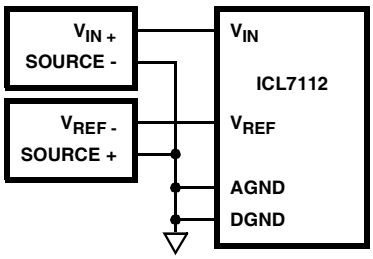


FIGURE 3. IMPROPER GROUNDING TECHNIQUE WILL CAUSE GROUND LOOP ERRORS

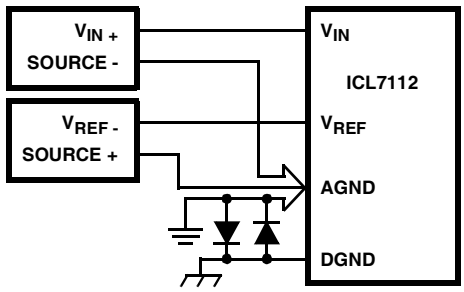


FIGURE 4. RECOMMENDED GROUNDING TECHNIQUE TO ELIMINATE GROUND LOOP ERRORS

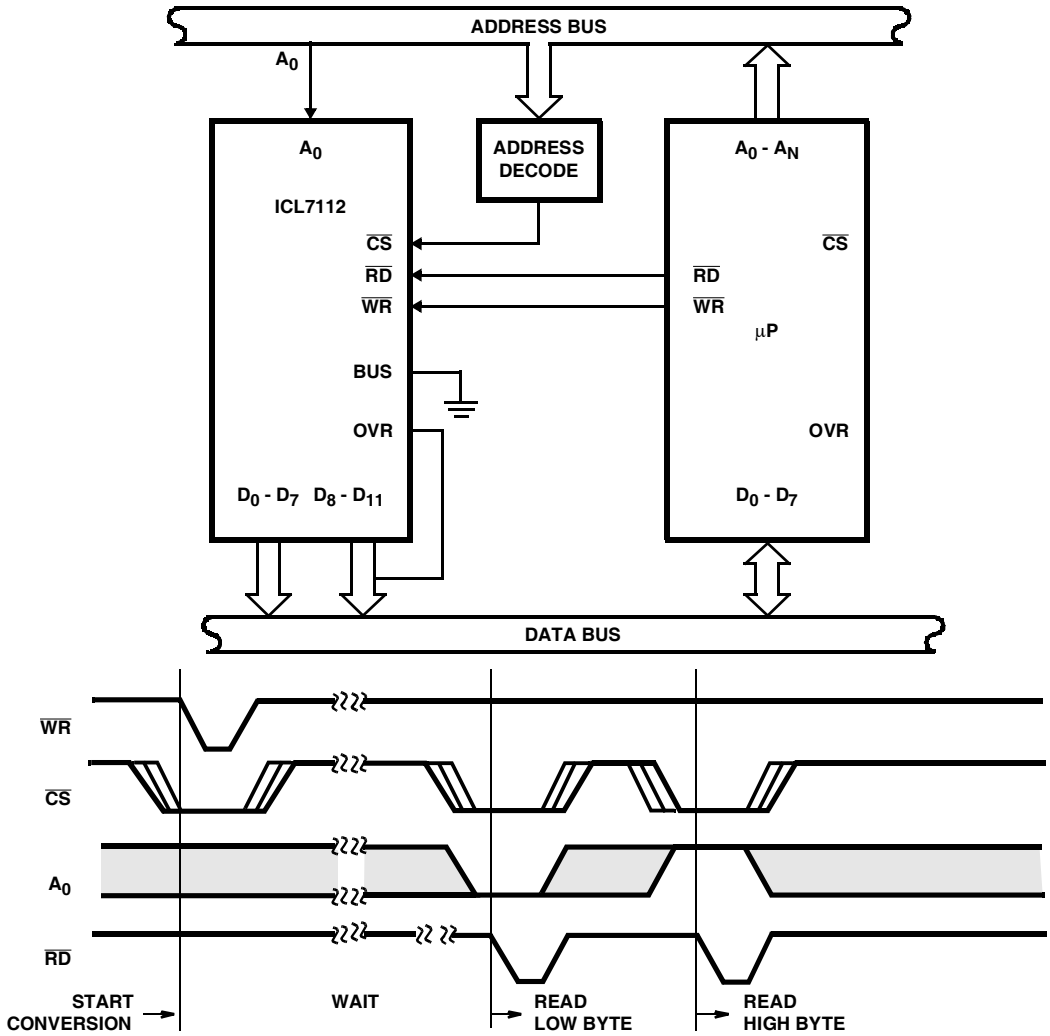


FIGURE 5. "START AND WAIT" OPERATION

By adding a three-state buffer and two control gates, the End-of-Conversion (EOC) output can be used to control a "Start and Poll" interface (Figure 6). In this mode, the A_0 and $\overline{CS}$ lines connect the EOC output to the data bus along with the most significant byte of data. After pulsing the $\overline{WR}$ line to initiate a conversion, the microprocessor continually reads the most significant byte until it detects a high level on the EOC bit. The "Start and Poll" interface increases data throughput compared with the "Start and Wait" method by eliminating delays between the conversion termination and the microprocessor read operation.

Other interface configurations can be used to increase data throughput without monopolizing the microprocessor during waiting or polling operations by using the EOC line as an interrupt generator as shown in Figure 7. After the conversion cycle is initiated, the microprocessor can continue to execute routines that are independent of the A/D converter until the converter's output register actually holds valid data. For fastest data throughput, the ICL7112 can be connected directly to the data bus but controlled by way of a Direct

Memory Access (DMA) controller as shown in Figure 8.

Applications

Figure 9 shows a typical application of the ICL7112 12- bit A/D converter. A bipolar input voltage range of +10V to -10V is the result of using the current through R_2 to force a 1/2 scale offset on the input amplifier (A_1). The output of A_1 swings from 0V to -1 0V. The overall gain of the A/D is varied by adjusting the 100Ω trim resistor, R_5. Since the ICL7112 is automatically zeroed every conversion, the system gain and offset stability will be superb as long as a reference with a tempco of 1ppm/^{o}C and stable external resistors are used.

If is important to note that since the 7112's DAC current flows in A_1, the amplifier should be a wideband (GBW > 20MHz) type to minimize errors.

The clock for the ICL7112 is taken from whatever system clock is available and divided down to the level for a conversion time of 40μs. Output data is controlled by the BUS and A_0 inputs. Here they are set for 8-bit bus operation with BUS grounded and A_0 under the control of the address decode section of the external system.

Because the ICL7112's internal accumulator generates accurate output data for input signals as much as 3% greater than full-scale, and because the converter's OVR output flags overrange inputs, a simple microprocessor routine can be employed to precisely measure and correct for system gain and offset errors. Figure 10 shows a typical data acquisition system that uses a 10V reference, input signal multiplexer, and input signal Track/Hold amplifier. Two of the multiplexer's input channels are dedicated to sampling the system analog ground and reference voltage. Here, as in Figure 9, bipolar operation is accommodated by an offset resistor between the reference voltage and the summing junction of A_1. A flip-flop in IC_3 sets 1_{C2}'s Track/Hold input after the microprocessor has initiated a WR command, and resets when EOC goes high at the end of the conversion.

The first step in the system calibration routine is to select the multiplexer channel that is connected to system analog ground and initiate a conversion cycle for the ICL7112. The results represent the system offset error which comes from the sum of the offsets from IC_1, IC_2, and A_1. Next the channel connected to the reference voltage is selected and measured. These results, minus the system offset error, represent the system full-scale range. A gain error correction factor can be derived from this data. Since the ICL7112 provides valid data for inputs that exceed full-scale by as much as 3%, the OVR output can be thought of as a valid 13th data bit. Whenever the OVR bit is high, however, the total 12-bit result should be checked to ensure that it falls within 100% and 103% of full-scale. Data beyond 103% of full-scale should be discarded.

Clock Considerations

The ICL7112 provides an internal inverter which is brought out to pins OSC1 and OSC2, for crystal or ceramic resonator oscillator operation. The clock frequency is calculated from:

$$f_{CLK} = \frac{20}{t_{CONV}}$$

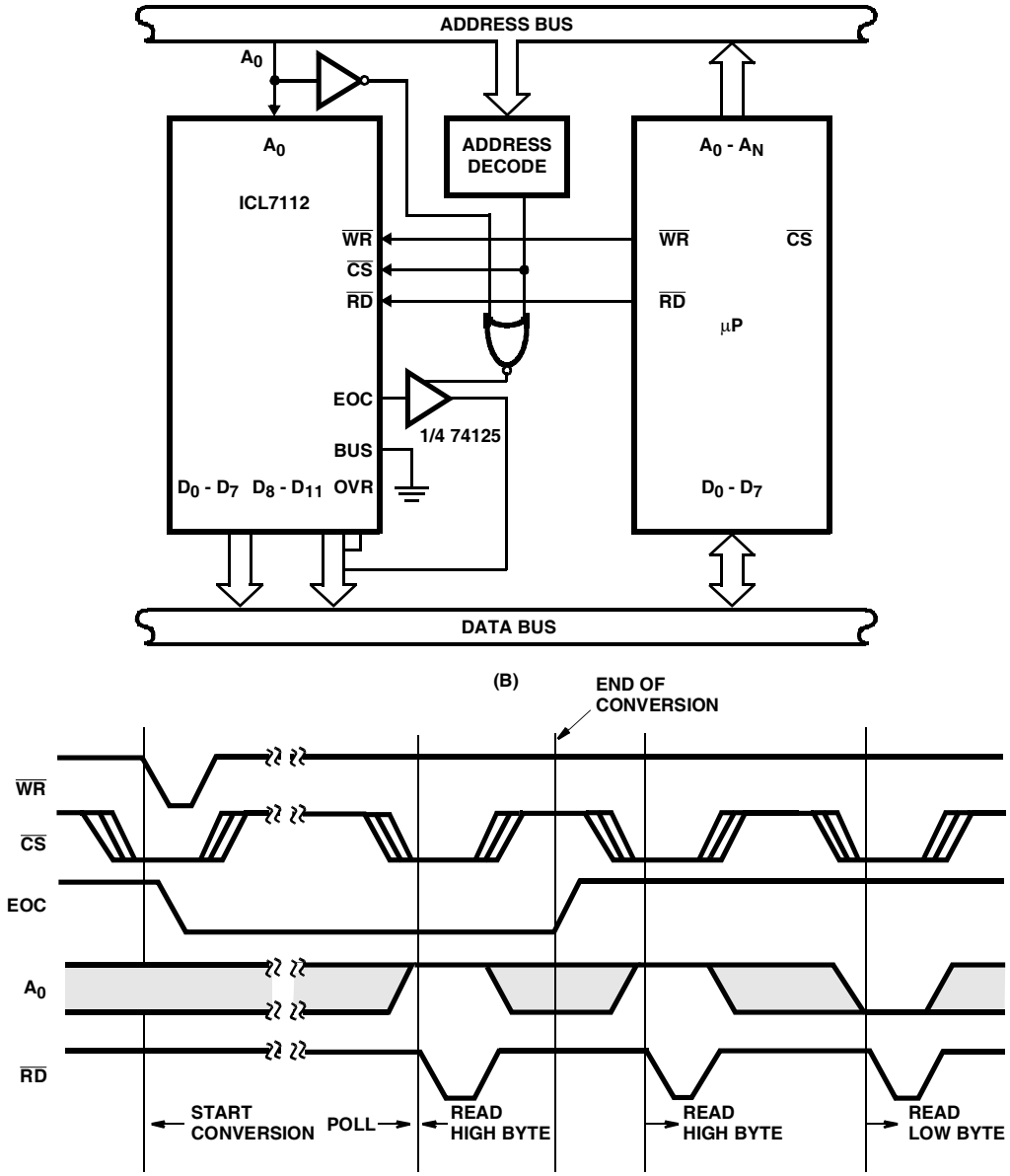
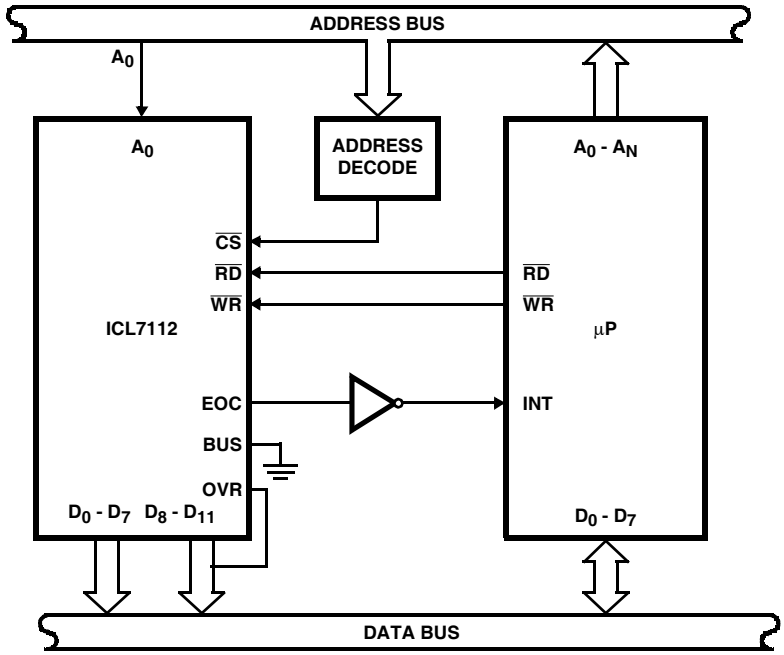


FIGURE 6. START AND POLL" OPERATION



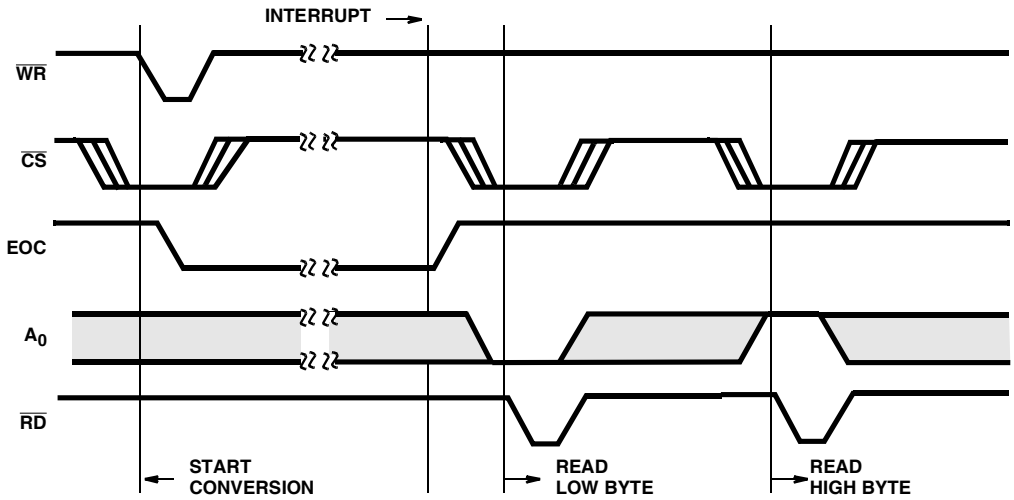
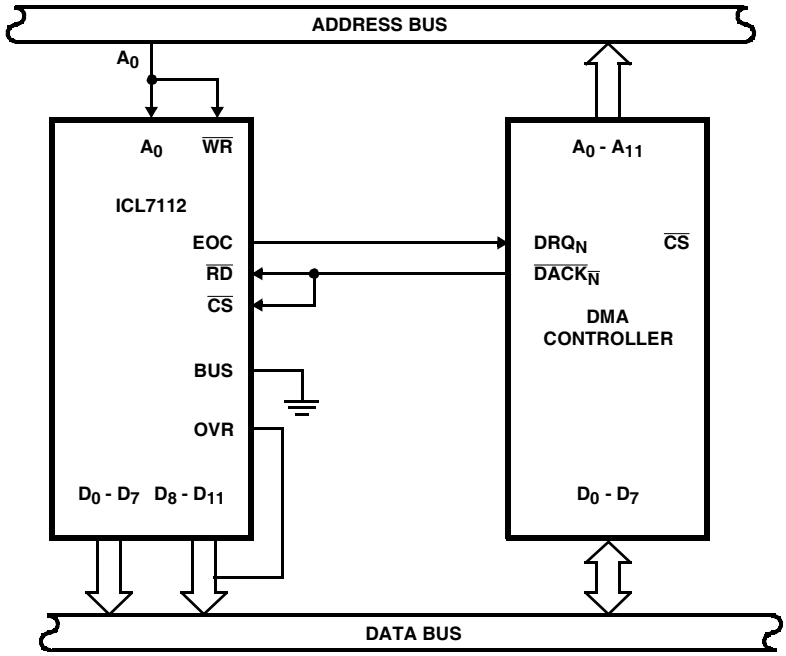


FIGURE 7. USING EOC AS AN INTERRUPT



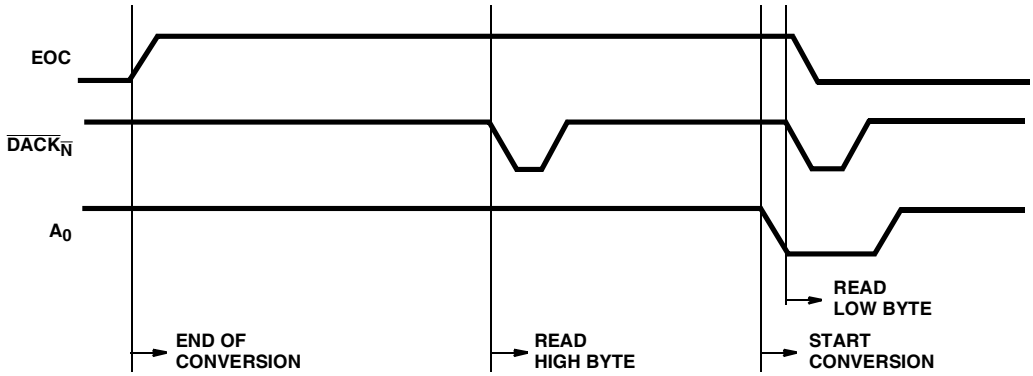


FIGURE 8. DATA TO MEMORY VIA DMA CONTROLLER

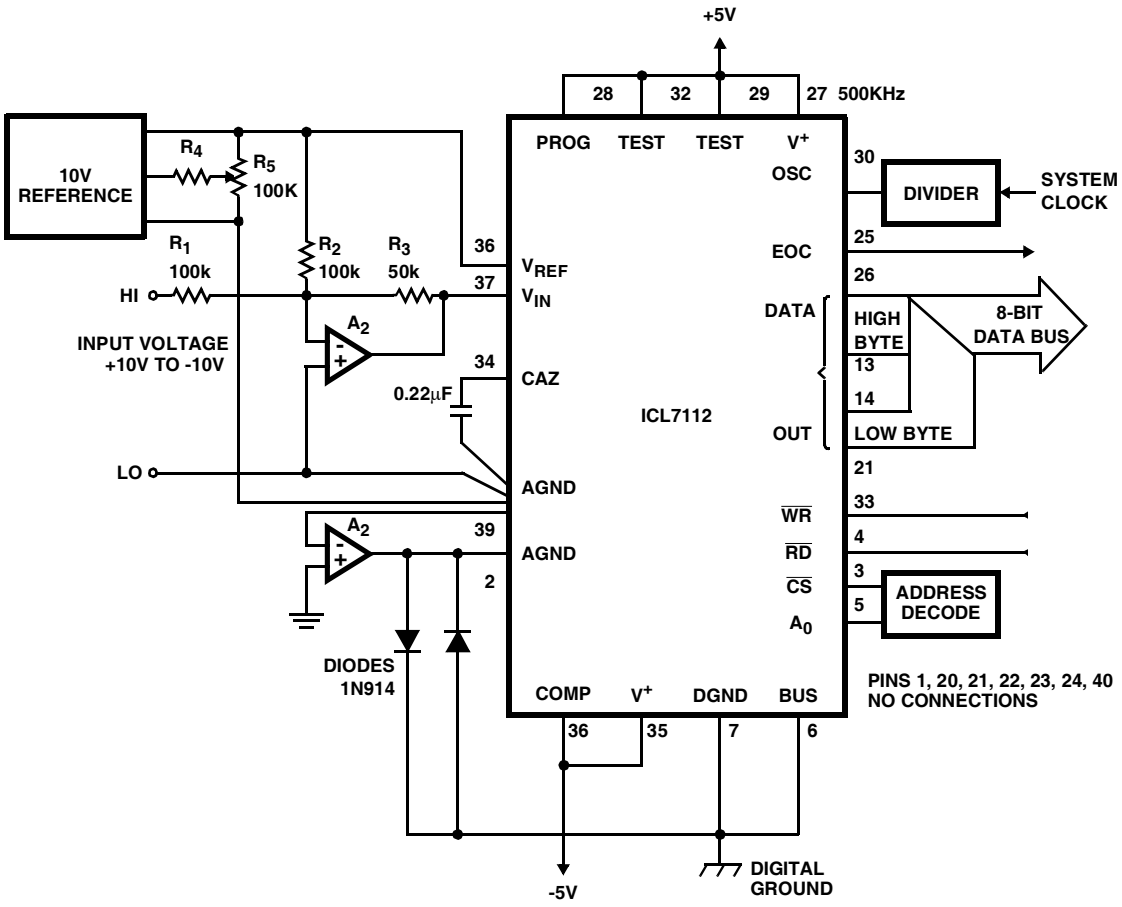


FIGURE 9. TYPICAL APPLICATION WITH BIPOLAR INPUT RANGE, FORCED GROUND, AND 10V ULTRA STABLE REFERENCE

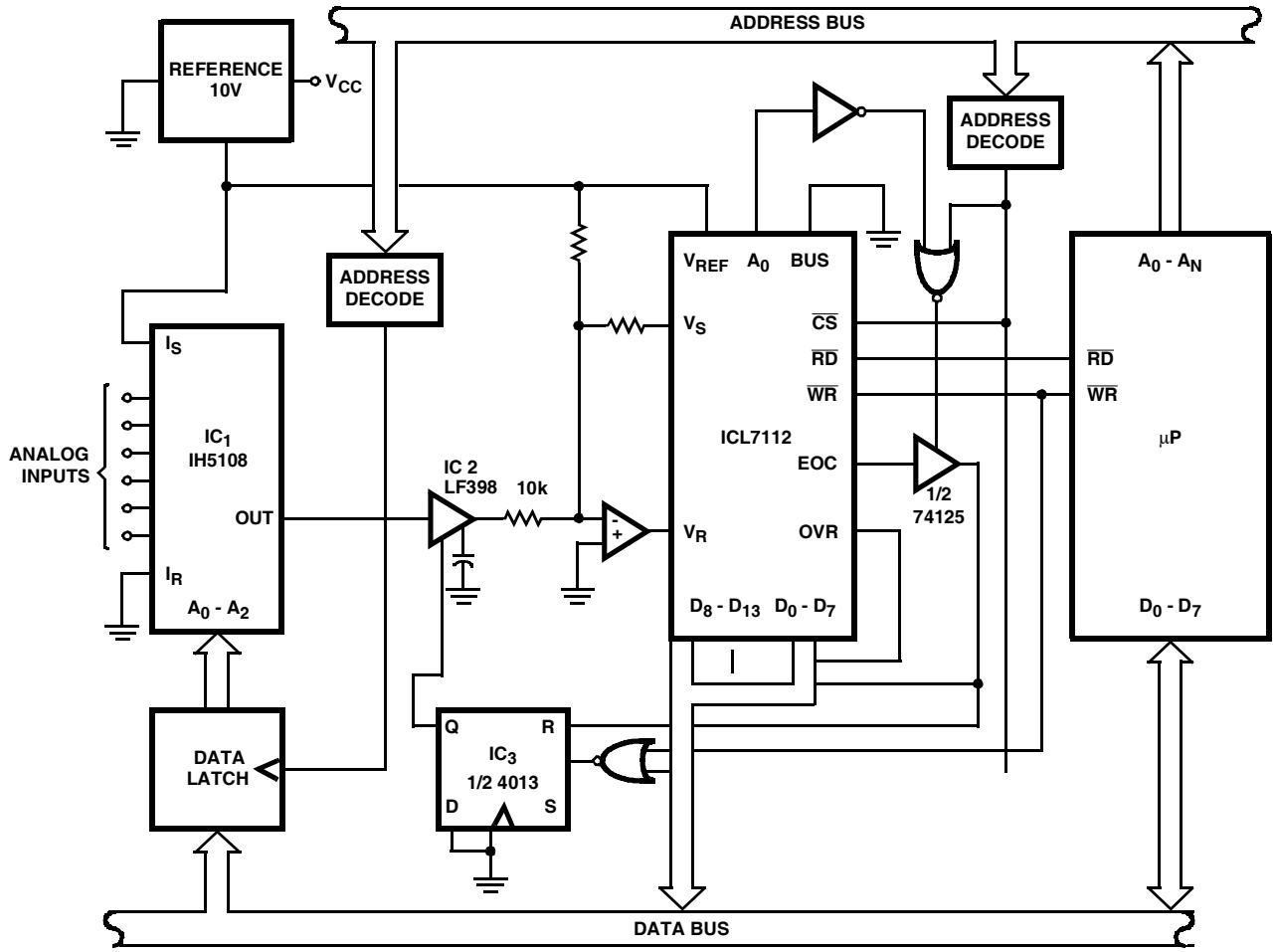


FIGURE 10. MULTI-CHANNEL DATA ACQUISITION SYSTEM WITH ZERO AND REFERENCE LINES BROUGHT TO MULTIPLEXER FOR SYSTEM GAIN AND OFFSET ERROR CORRECTION