SONY

ICX075AL

1/2-inch Progressive Scan CCD Image Sensor with Square Pixel for CCIR B/W Video Cameras

Description

The ICX075AL is an interline CCD solid-state image sensor suitable for CCIR black-and-white video cameras. Progressive scan allows all pixels signals to be output independently within approximately 1/50 second. This chip features an electronic shutter with variable charge-storage time which makes it possible to realize full-frame still image without mechanical shutter. Individual pixels in a square matrix make this device suitable for image input and processing applications.

High sensitivity and low dark current are achieved through the adoption of HAD (Hole-Accumulation Diode) sensors.

Features

• Progressive scan allows individual readout of the image signals from all pixels.
• High vertical resolution (580TV-lines) still picture without mechanical shutter.
• Square pixel unit cell
• High resolution, high sensitivity, low dark current
• Continuous variable-speed shutter
• Low smear
• Excellent antiblooming characteristics
• Reset gate: 5V drive (bias: no adjustment)

Device Structure

• Optical size: 1/2-inch format
• Number of effective pixels: 782 (H) × 582 (V)   approx. 460K pixels
• Total number of pixels: 823 (H) × 592 (V)   approx. 490K pixels
• Interline CCD image sensor
• Chip size: 8.10mm (H) × 6.33mm (V)
• Unit cell size: 8.3μm (H) × 8.3μm (V)
• Optical black: Horizontal (H) direction: Front 3 pixels, rear 38 pixels
         Vertical (V) direction: Front 8 pixels, rear   2 pixels
• Number of dummy bits: Horizontal 19
         Vertical 5
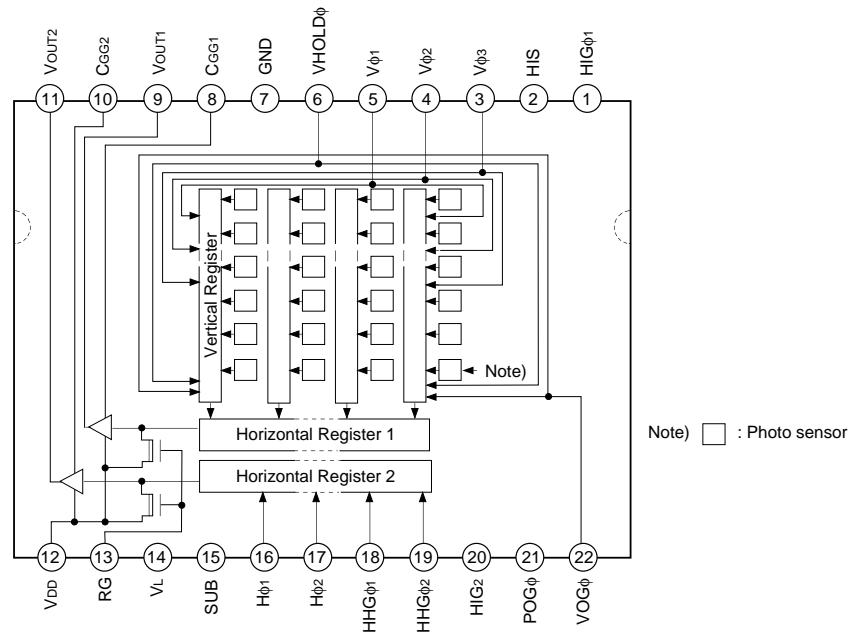• Substrate material: Silicon

22 pin DIP (Cer-DIP)
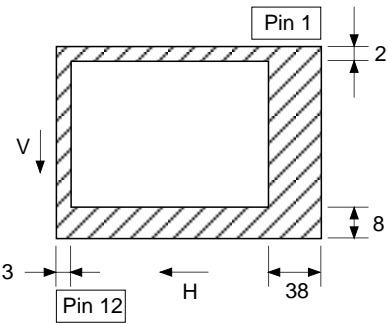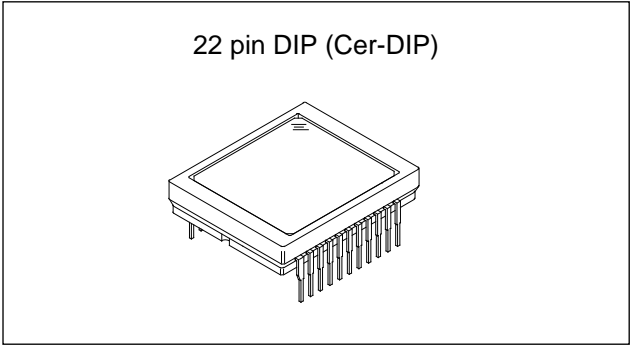
Optical black position
(Top View)

E95309D72-PS

Block Diagram and Pin Configuration

(Top View)

Note) ☐ : Photo sensor

Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	$HIG\phi_1$	Test pin *2	12	V_{DD}	Supply voltage
2	HIS	Test pin *2	13	RG	Reset gate clock
3	$V\phi_3$	Vertical register transfer clock	14	V_L	Protective transistor bias
4	$V\phi_2$	Vertical register transfer clock	15	SUB	Substrate (overflow drain)
5	$V\phi_1$	Vertical register transfer clock	16	$H\phi_1$	Horizontal register transfer clock
6	$VHOLD\phi$	Vertical register final stage accumulation clock	17	$H\phi_2$	Horizontal register transfer clock
7	GND	GND	18	$HHG\phi_1$	Inter-horizontal register transfer clock
8	C_{GG1}	Output amplifier 1 gate *1 decoupling capacitor	19	$HHG\phi_2$	Inter-horizontal register transfer clock
9	V_{OUT1}	Signal output 1	20	HIG_2	Test pin *2
10	C_{GG2}	Output amplifier 2 gate *1 decoupling capacitor	21	$POG\phi$	Test pin *2
11	V_{OUT2}	Signal output 2	22	$VOG\phi$	Vertical register final stage transfer clock

*1 DC bias is applied within the CCD, so that this pin should be grounded externally through a capacitance of 1μF or more.

*2 Regarding the test pins: apply the same voltage as the supply voltage to HIS, and ground $HIG\phi_1$, HIG_2, and $POG\phi$.

Absolute Maximum Ratings

Item		Ratings	Unit	Remarks
Substrate voltage SUB – GND		−0.3 to +55	V	
Supply voltage	V_{DD}, V_{OUT1}, V_{OUT2}, HIS, C_{GG1}, C_{GG2} – GND	−0.3 to +18	V	
	V_{DD}, V_{OUT1}, V_{OUT2}, HIS, C_{GG1}, C_{GG2} – SUB	−55 to +10	V	
Clock input voltage	$V\phi_1$, $V\phi_2$, $V\phi_3$, VHOLDϕ, VOGϕ – GND	−15 to +20	V	
	$V\phi_1$, $V\phi_2$, $V\phi_3$, VHOLDϕ, VOGϕ – SUB	to +10	V	
Voltage difference between vertical clock input pins		to +15	V	*1
Voltage difference between horizontal clock input pins		to +17	V	
$H\phi_1$, $H\phi_2$ – VOGϕ		−17 to +17	V	
$H\phi_1$, $H\phi_2$ – GND		−10 to +15	V	
$H\phi_1$, $H\phi_2$ – SUB		−55 to +10	V	
V_L – SUB		−65 to +0.3	V	
$V\phi_2$, $V\phi_3$, V_{DD}, V_{OUT1}, V_{OUT2}, HIS, HIGϕ_1, HIG2, POGϕ – V_L		−0.3 to +27.5	V	
RG – GND		−0.3 to +22.5	V	
$V\phi_1$, C_{GG1}, C_{GG2}, $H\phi_1$, $H\phi_2$, HHGϕ_1, HHGϕ_2, VOGϕ, VHOLDϕ – V_L		−0.3 to +17.5	V	
Storage temperature		−30 to +80	°C	
Operating temperature		−10 to +60	°C	

*1 +27V (Max.) when clock width < 10µs, clock duty factor < 0.1%.

Bias Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage	V_{DD}	14.55	15.0	15.45	V	
Substrate voltage adjustment range	V_{SUB}	9.0		18.5	V	*1
Substrate voltage adjustment precision		Indicated voltage – 0.1	Indicated voltage	Indicated voltage + 0.1	V	
Protective transistor bias	V_L		*2			

DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply current	I_{DD}		10		mA	
Input current	I_{IN1}			1	µA	*3
Input current	I_{IN2}			10	µA	*4

*1 Indications of substrate voltage (V_{SUB}) setting value
The setting value of the substrate voltage is indicated on the back of image sensor by a special code. Adjust the substrate voltage (V_{SUB}) to the indicated voltage.

V_{SUB} code – two characters indication ☐ ☐
↑ ↑
Integer portion   Decimal portion
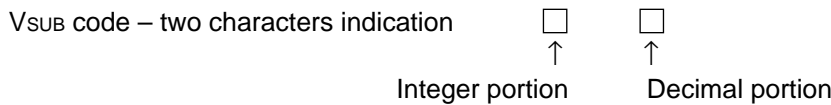
The integer portion of the code and the actual value correspond to each other as follows.

Integer portion of code	9	A	C	d	E	f	G	h	J	K
Value	9	10	11	12	13	14	15	16	17	18

<Example> "A5" → V_{SUB} = 10.5V

*2 V_L setting is the V_{VL} voltage of the vertical transfer clock waveform, or the same power supply as the V_L power supply for the V driver should be used.

*3 (1) Current to each pin when 18V is applied to V_{DD}, V_{OUT1}, V_{OUT2}, HIS, RG, C_{GG1}, C_{GG2}, GND and SUB pins, while pins that are not tested are grounded.
(2) Current to each pin when 20V is applied sequentially to $V\phi1$, $V\phi2$ and $V\phi3$ pins, while pins that are not tested are grounded. However, 20V is applied to SUB pin.
(3) Current to each pin when 15V is applied sequentially to RG, $H\phi1$ and $H\phi2$ pins, while pins that are not tested are grounded. However, 15V is applied to SUB pin.
(4) Current to V_L pin when 25V is applied to $V\phi2$, $V\phi3$, $POG\phi$, $HIG\phi1$, HIG2, V_{DD}, V_{OUT1} and V_{OUT2} pins or when, 15V is applied to $V\phi1$, $VHOLD\phi$, $VOG\phi$, C_{GG1}, C_{GG2}, $H\phi1$, $H\phi2$, $HHG\phi1$ and $HHG\phi2$ pins, while V_L pin is grounded. However, GND and SUB pins are left open.
(5) Current to GND pin when 20V is applied to the RG pin and the GND pin is grounded.

*4 Current to SUB pin when 55V is applied to SUB pin, while all pins that are not tested are grounded.

Clock Voltage Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Readout clock voltage	V_{VT}	14.55	15.0	15.45	V	1	
Vertical transfer clock voltage	V_{VH02}	−0.05	0	0.05	V	2	$V_{VH} = V_{VH02}$
	V_{VH1}, V_{VH2}, V_{VH3}	−0.2	0	0.05	V	2	
	V_{VL1}, V_{VL2}, V_{VL3}	−8.0	−7.5	−7.0	V	2	$V_{VL} = (V_{VL01} + V_{VL03})/2$
	$V\phi V$	6.8	7.5	8.05	V	2	$V\phi V = V_{VHn} - V_{VLn}$ (n = 1 to 3)
	| $V_{VL1} - V_{VL3}$ |			0.1	V	2	
	V_{VHH}			0.5	V	2	High-level coupling
	V_{VHL}			0.5	V	2	High-level coupling
	V_{VLH}			0.5	V	2	Low-level coupling
	V_{VLL}			0.5	V	2	Low-level coupling
Horizontal transfer clock voltage	$V\phi H$	4.75	5.0	5.25	V	3	
	V_{HL}	−0.05	0	0.05	V	3	
Reset gate clock voltage	$V\phi RG$	4.5	5.0	5.5	V	4	Input through 0.01μF capacitance
	$V_{RGLH} - V_{RGLL}$			0.8	V	4	Low-level coupling
	V_{RGH}	V_{DD} + 0.4	V_{DD} + 0.6	V_{DD} + 0.8	V	4	
Substrate clock voltage	$V\phi SUB$	21.5	22.5	23.5	V	5	
Vertical final stage accumulation clock voltage /transfer clock voltage	V_{VHOLDH}, V_{VOGH}	−0.05	0	0.05	V	6	
	V_{VHOLDL}, V_{VOGL}	−8.0	−7.5	−7.0	V	6	
Inter-horizontal register transfer clock voltage	V_{HHG1H}, V_{HHG2H}	4.75	5.0	5.25	V	7	
	V_{HHG1L}, V_{HHG2L}	−8.0	−7.5	−7.0	V	7	
	V_{HHG1M}, V_{HHG2M}	−0.05	0	0.05	V	7	

Clock Equivalent Circuit Constant

| Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C\phi_{V1}$		820		pF	
	$C\phi_{V2}$		820		pF	
	$C\phi_{V3}$		820		pF	
Capacitance between vertical transfer clocks	$C\phi_{V12}$		3300		pF	
	$C\phi_{V23}$		2200		pF	
	$C\phi_{V31}$		2200		pF	
Capacitance between vertical final stage accumulation clock and GND	$C\phi_{VHOLD}$		19		pF	
Capacitance between vertical final stage transfer clock and GND	$C\phi_{VOG}$		12		pF	
Capacitance between inter-horizontal register transfer clock and GND	$C\phi_{HHG1}$		19		pF	
	$C\phi_{HHG2}$		19		pF	
Capacitance between horizontal transfer clock and GND	$C\phi_{H1}$		68		pF	
	$C\phi_{H2}$		68		pF	
Capacitance between horizontal transfer clocks	$C\phi_{HH}$		47		pF	
Capacitance between reset gate clock and GND	$C\phi_{RG}$		10		pF	
Capacitance between substrate clock and GND	$C\phi_{SUB}$		400		pF	
Vertical transfer clock series resistor	R_1, R_2, R_3		22		Ω	
Vertical transfer clock ground resistor	R_{GND}		15		Ω	
Horizontal transfer clock series resistor	$R\phi_{H1}$		24		Ω	
	$R\phi_{H2}$		24		Ω	
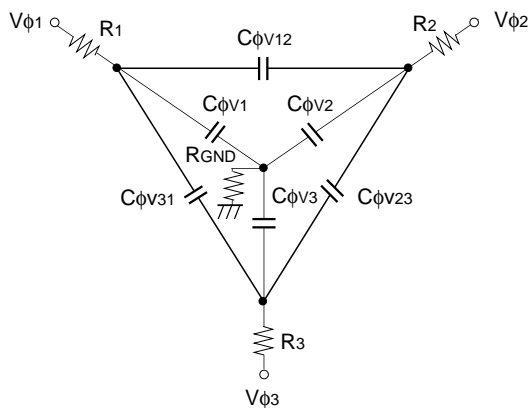
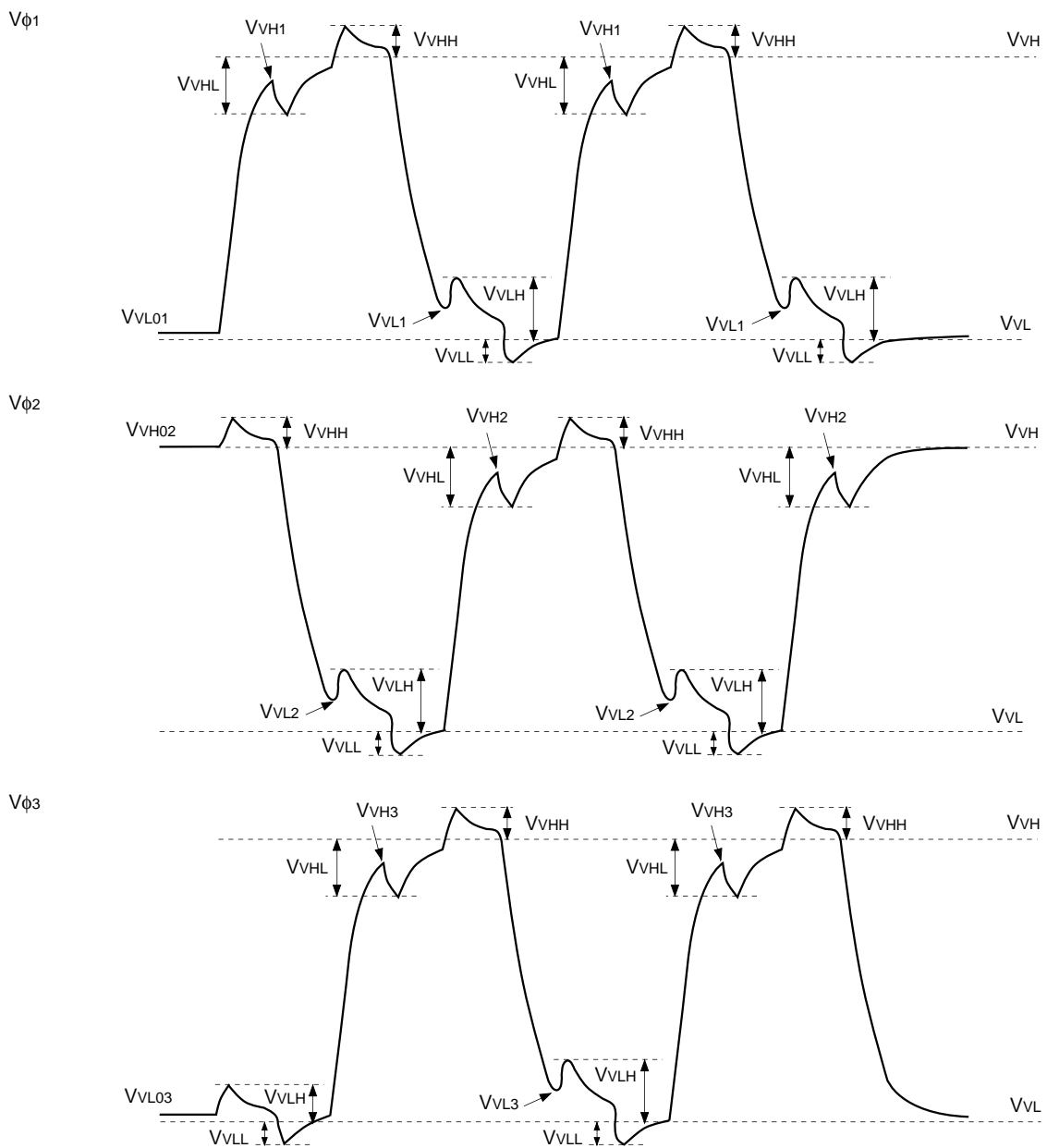**Vertical transfer clock equivalent circuit**
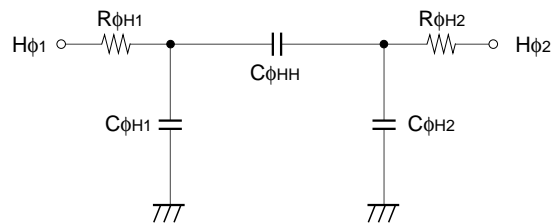
Horizontal transfer clock equivalent circuit

Drive Clock Waveform Conditions

(1) Readout clock waveform
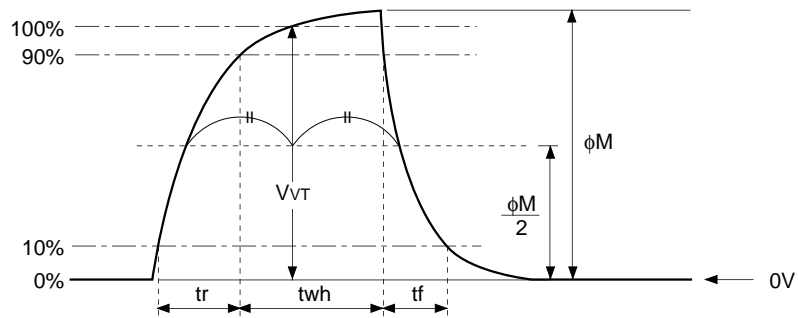
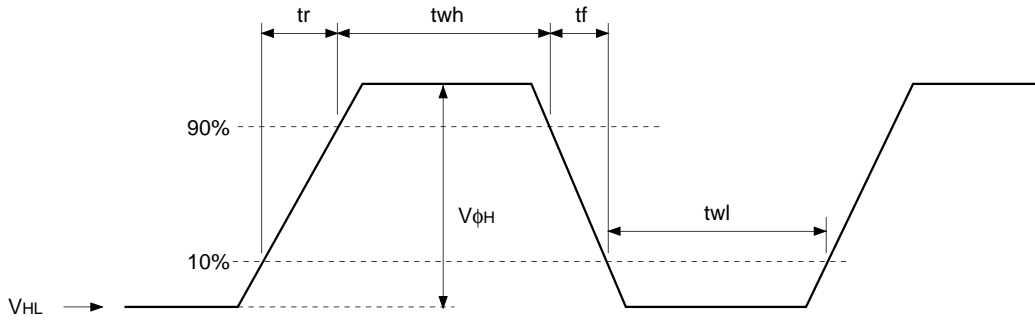### (2) Vertical transfer clock waveform

$$V_{VH} = V_{VH02}$$
$$V_{VL} = (V_{VL01} + V_{VL03})/2$$
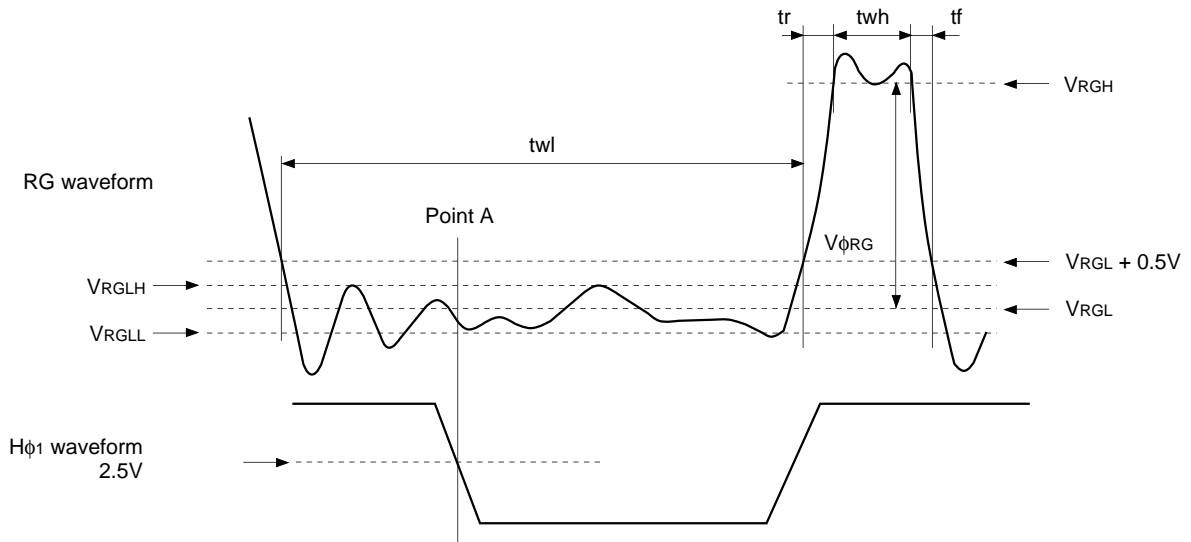
$$V_{\phi V1} = V_{VH1} - V_{VL01}$$
$$V_{\phi V2} = V_{VH02} - V_{VL2}$$
$$V_{\phi V3} = V_{VH3} - V_{VL03}$$

(3) Horizontal transfer clock waveform

## (4) Reset gate clock waveform

V_{RGLH} is the maximum value and V_{RGLL} is the minimum value of the coupling waveform during the period from Point A in the above diagram until the rising edge of RG. In addition, V_{RGL} is the average value of V_{RGLH} and V_{RGLL}.

$$V_{RGL} = (V_{RGLH} + V_{RGLL})/2$$

Assuming V_{RGH} is the minimum value during the interval twh, then:

$$V\phi_{RG} = V_{RGH} - V_{RGL}$$

(5) Substrate clock waveform
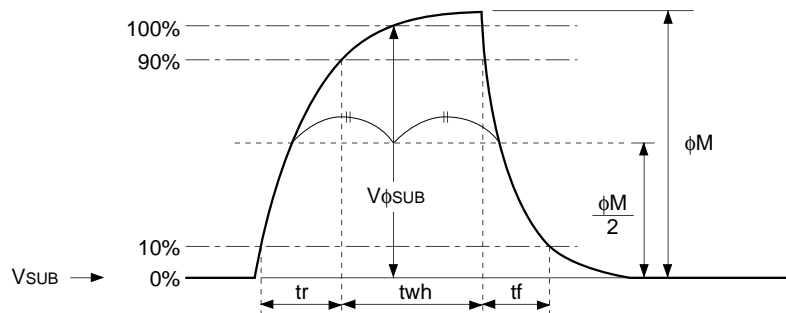
(6) Vertical final stage accumulation clock waveform · Vertical final stage transfer clock waveform

VHOLDφ, VOGφ

tr   tf

V_{VHOLDH}, V_{VOGH}

90%

10%

V_{VHOLDL}, V_{VOGL}

(7) Inter-horizontal register transfer clock waveform

HHGφ1, HHGφ2

tr   tf1

V_{HHG1H}, V_{HHG2H}

90%

90%

tf2

10%

V_{HHG1M}, V_{HHG2M}

90%

10%

10%

V_{HHG1L}, V_{HHG2L}
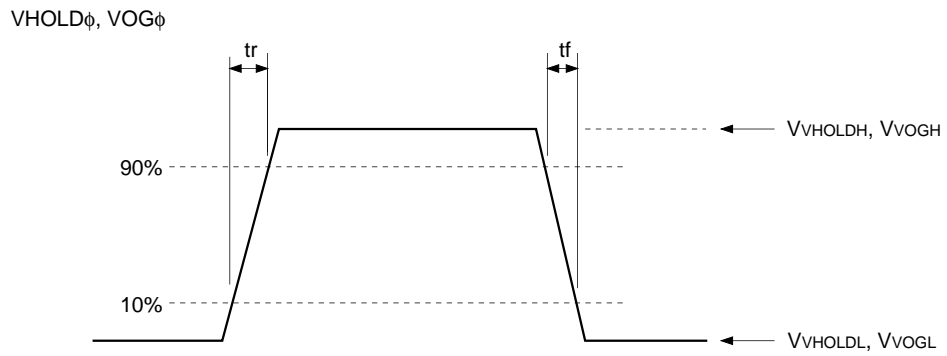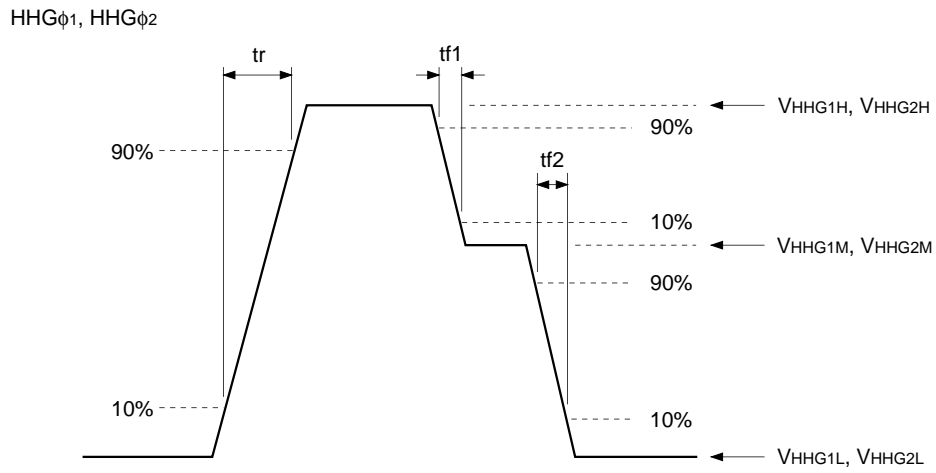
Clock Switching Characteristics

Item	Symbol	twh Min.	twh Typ.	twh Max.	twl Min.	twl Typ.	twl Max.	tr Min.	tr Typ.	tr Max.	tf, tf1, tf2 Min.	tf, tf1, tf2 Typ.	tf, tf1, tf2 Max.	Unit	Remarks
Readout clock	VT	2.3	2.5						0.4			0.1		µs	During readout
Vertical transfer clock	Vφ1, Vφ2, Vφ3										15		400	ns	*1
Horizontal transfer clock — During imaging	Hφ1	18	23		21	26			10	17.5		10	17.5	ns	*2
Horizontal transfer clock — During imaging	Hφ2	21	26		18	23			10	15		10	15	ns	*2
Horizontal transfer clock — During parallel-serial conversion	Hφ1								0.01			0.01		µs	
Horizontal transfer clock — During parallel-serial conversion	Hφ2								0.01			0.01		µs	
Reset gate clock	φRG	11	14			49			2			2		ns	
Substrate clock	φSUB	1.4	1.6							0.4			0.4	µs	During drain charge
Vertical final stage accumulation/ transfer clock	VHOLDφ								20			20		ns	
Vertical final stage accumulation/ transfer clock	VOGφ								20			20		ns	
Inter-horizontal register transfer clock	HHGφ1								20			20		ns	
Inter-horizontal register transfer clock	HHGφ2								20			20		ns	

*1 When vertical transfer clock driver CXD1268M is used.

*2 $tf \geq tr - 2ns$, and the cross-point voltage (V_{CR}) for the Hφ1 rising side of the Hφ1 and Hφ2 waveforms must be at least 2.5V.

Item	Symbol	two Min.	two Typ.	two Max.	Unit	Remarks
Horizontal transfer clock	Hφ1, Hφ2	20	24		ns	*3

*3 The overlap period for twh and twl of horizontal transfer clocks Hφ1 and Hφ2 is two.

**Image Sensor Characteristics** (Ta = 25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
Sensitivity	S	230	300		mV	1	
Saturation signal	Vsat	375			mV	2	Ta = 60°C
Smear	Sm		0.003	0.007	%	3	
Video signal shading	SH			25	%	4	Zone 0
Dark signal	Vdt			2	mV	5	Ta = 60°C
Dark signal shading	ΔVdt			1	mV	6	Ta = 60°C
Lag	Lag			0.5	%	7	
Uniformity between output channels	ΔV			3	%	8	

Note) All the characteristic data of this image sensor was yielded when the sensor was operated in the 1/50s interlaced mode.
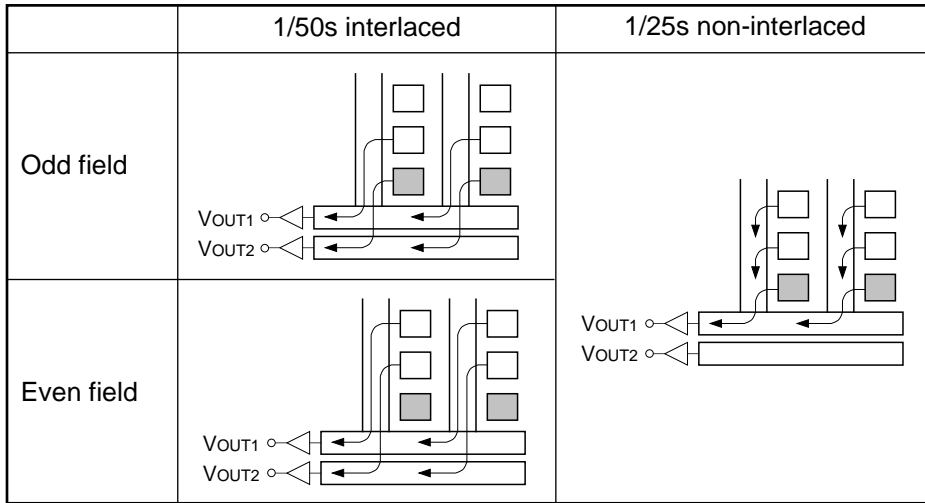
Zone Definition of Video Signal Shading
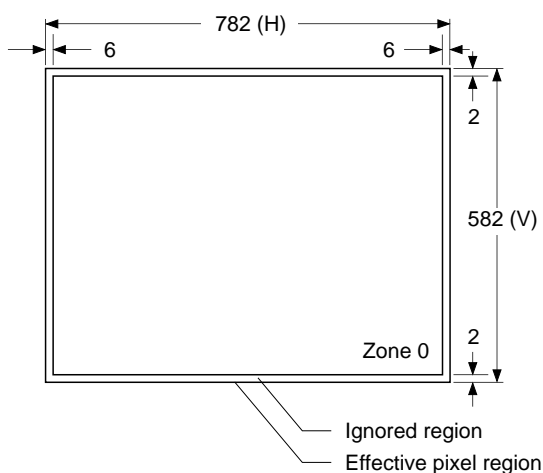
Measurement System
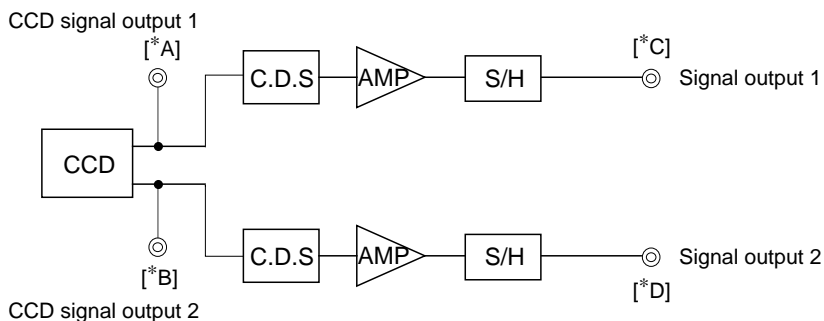
Note) Adjust the amplifier gain so that the gain between [*A] and [*C], and between [*B] and [*D] equals 1.

◎ **Readout modes**

The output methods for the two readout modes indicated below are now described.

	1/50s interlaced	1/25s non-interlaced
Odd field		
Even field		

1. 1/50s interlaced

   In this mode, the signals are output in a 1/50s period using the two output pins (V_{OUT1}, V_{OUT2}).

   The signals from two adjacent horizontal lines are simultaneously output from the respective output pins.

   The lines output from the output pins are changed over with each field. The V_{OUT1} signal after it has passed through the CDS and other external circuits or the signal produced by adding the V_{OUT1} and V_{OUT2} signals accommodate interlaced scanning.

2. 1/25s non-interlaced

   In this mode, the signals are output in a 1/25s period using only one output pin (V_{OUT1}).

   Unlike the 1/50s interlaced mode described above, the external circuit can be simplified. The imaging characteristics also differ from those of the other modes.

Image Sensor Characteristics Measurement Method

◎ **Measurement conditions**

1) In the following measurements, the substrate voltage is set to the value indicated on the device, and the device drive conditions are at the typical values of the bias and clock voltage conditions.

2) In the following measurements, spot blemishes are excluded and, unless otherwise specified, the optical black level (OB) is used as the reference for the signal output and the value measured at point [*A] in the measurement system is used.

3) In the following measurements, this image sensor is operated in 1/50s interlaced mode.

◎ **Definition of standard imaging conditions**

1) Standard imaging condition Ⅰ:
   Use a pattern box (luminance 706cd/m^2, color temperature of 3200K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.00mm) as an IR cut filter and image at F8. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

2) Standard imaging condition Ⅱ:
   Image a light source (color temperature of 3200K) with a uniformity of brightness within 2% at all angles. Use a testing standard lens with CM500S (t = 1.00mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

1. Sensitivity
   Set to standard imaging condition Ⅰ. After selecting the electronic shutter mode with a shutter speed of 1/250s, measure the signal output (Vs) at the center of the screen and substitute the value into the following formula.

   $$S = Vs \times \frac{250}{50} \text{ [mV]}$$

2. Saturation signal
   Set to standard imaging condition Ⅱ. After adjusting the luminous intensity to 10 times the intensity with average value of signal output, 120mV, measure the minimum value of the signal output.

3. Smear
   Set to standard imaging condition Ⅱ. With the lens diaphragm at F5.6 to F8, adjust the luminous intensity to 500 times the intensity with average value of signal output, 120mV. When the readout clock is stopped and the charge drain is executed by the electronic shutter at the respective H blankings, measure the maximum value VSm [mV] of the signal output and substitute the value into the following formula.

   $$Sm = \frac{VSm}{120} \times \frac{1}{500} \times \frac{1}{10} \times 100 \text{ [%] (1/10V method conversion value)}$$

4. Video signal shading
   Set to standard imaging condition Ⅱ. With the lens diaphragm at F5.6 to F8, adjust the luminous intensity so that the average value of the signal output is 120mV. Then measure the maximum (Vmax [mV]) and minimum (Vmin [mV]) values of the signal output and substitute the values into the following formula.

   $$SH = (Vmax - Vmin)/120 \times 100 \text{ [%]}$$

5. Dark signal
   Measure the average value of the signal output (Vdt [mV]) with the device ambient temperature 60°C and the device in the light-obstructed state, using the horizontal idle transfer level as a reference.

6. Dark signal shading

   After measuring 5, measure the maximum (Vdmax [mV]) and minimum (Vdmin [mV]) values of the dark signal output and substitute the values into the following formula.

   ΔVdt = Vdmax – Vdmin [mV]

7. Lag

   Adjust the signal output value generated by strobe light to 120mV. After setting the strobe light so that it strobes with the following timing, measure the residual signal (Vlag). Substitute the value into the following formula.

   Lag = (Vlag/120) $\times$ 100 [%]

FLD

SG

Strobe light timing

Light

Output

Signal output 120mV

Vlag (lag)
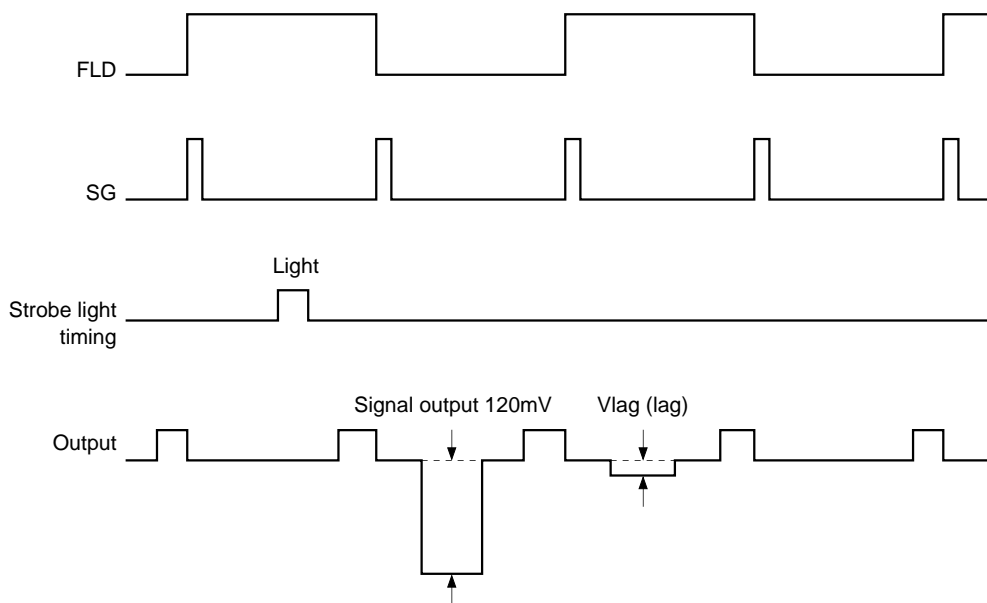
8. Uniformity between output channels

   Set to standard imaging condition I. Measure the signals at signal output 1 (V1) and at signal output 2 (V2), and substitute the values into the following formula.

   $$\Delta V = \frac{|\,V2 - V1\,|}{V1} \times 100\ [\%]$$

Drive Circuit

Spectral Sensitivity Characteristics

(includes lens characteristics, excludes light source characteristics)

Wave Length [nm]
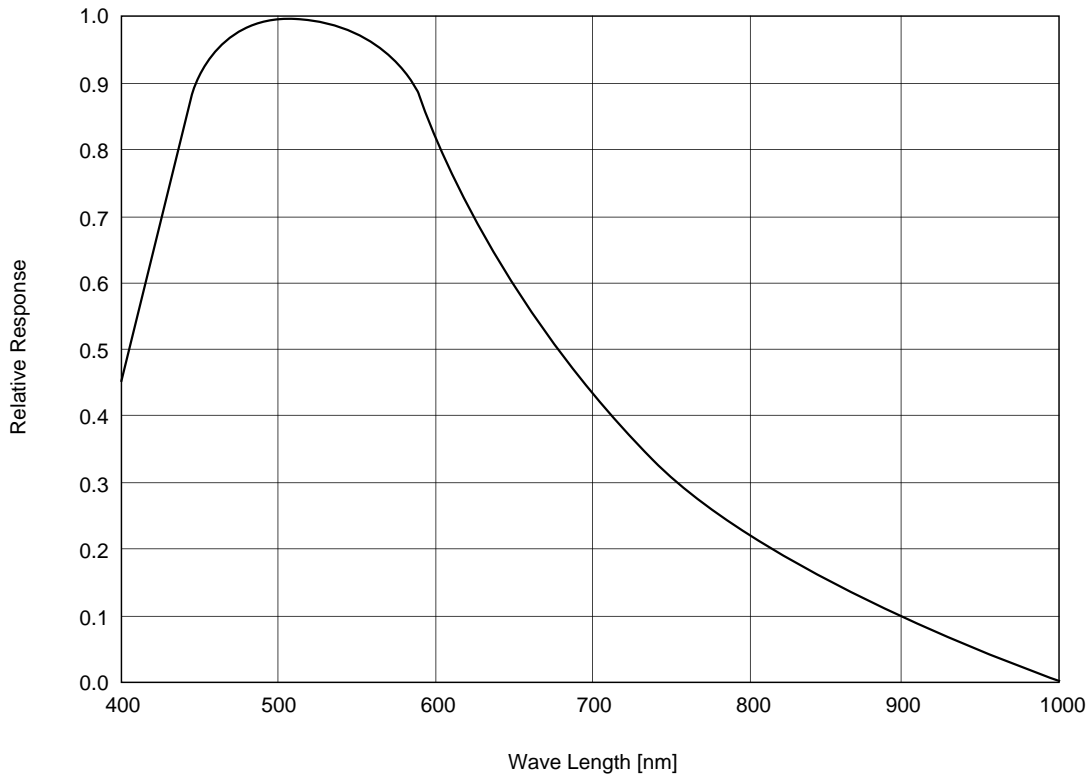
Sensor Readout Clock Timing Chart   1/50s interlaced mode

Unit: μs
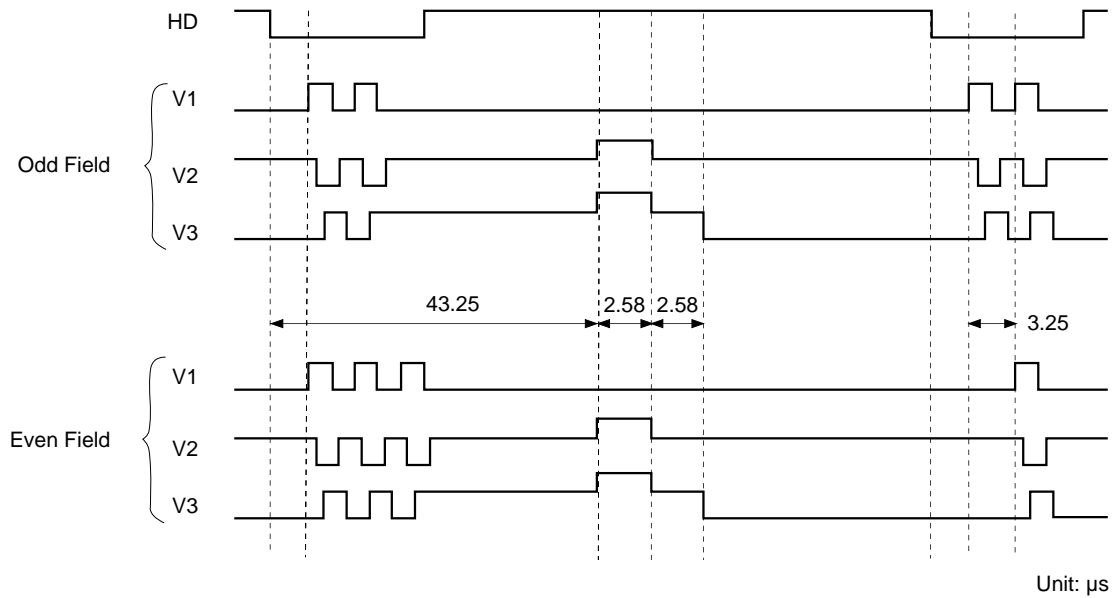
Drive Timing Chart (Vertical Sync)   1/50s interlaced mode

FLD

VD

BLK

HD

V1

V2

V3

CCD OUT1

CCD OUT2

SG
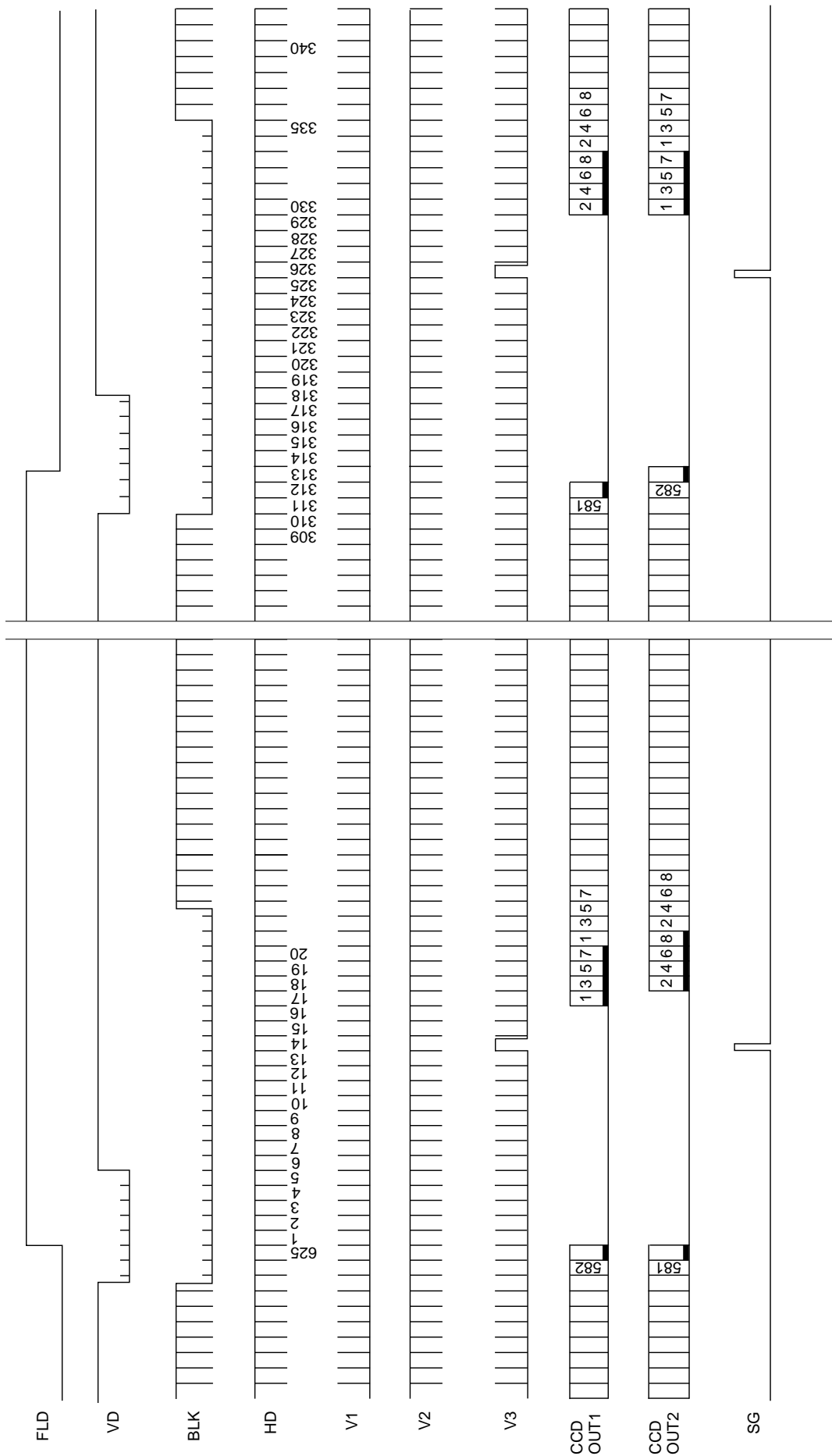
Drive Timing Chart (Horizontal Sync)   1/50s interlaced mode

HD

BLK

CLK

V1

V2

V3

VOG

VHOLD

HHG1

HHG2

H1

H2

RG

SHP

SHD

SUB
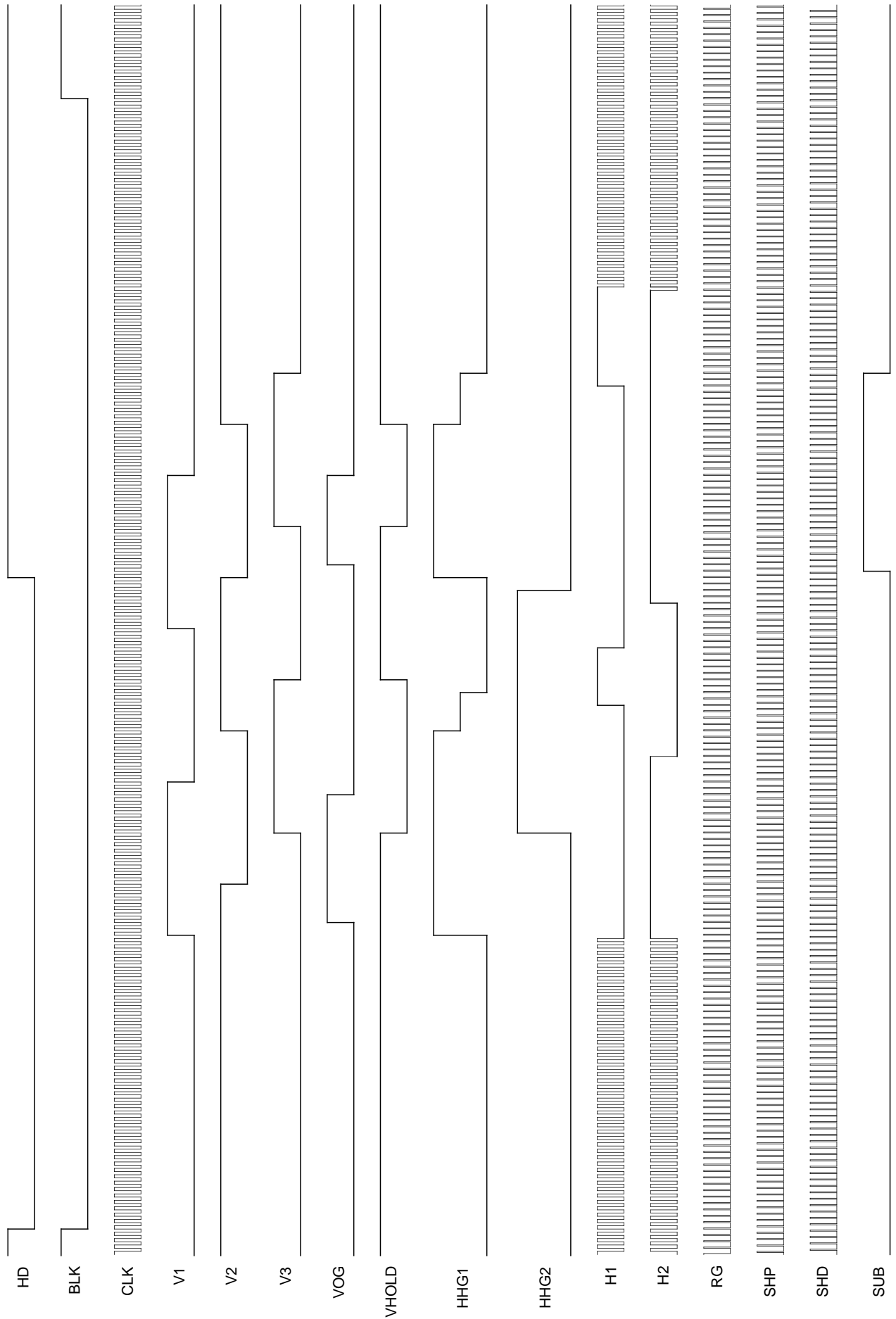
Notes on Handling

1) Static charge prevention
   CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.
   a) Either handle bare handed or use non-chargeable gloves, clothes or material. Also use conductive shoes.
   b) When handling directly use an earth band.
   c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
   d) Ionized air is recommended for discharge when handling CCD image sensor.
   e) For the shipment of mounted substrates, use boxes treated for the prevention of static charges.

2) Soldering
   a) Make sure the package temperature does not exceed 80°C.
   b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a ground 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
   c) To dismount an imaging sensor, do not use a solder suction equipment. When using an electric desoldering tool, use a thermal controller of the zero cross On/Off type and connect it to ground.

3) Dust and dirt protection
   Image sensors are packed and delivered by taking care of protecting its glass plates from harmful dust and dirt. Clean glass plates with the following operation as required, and use them.
   a) Operate in clean environments (around class 1000 is appropriate).
   b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)
   c) Clean with a cotton bud and ethyl alcohol if the grease stained. Be careful not to scratch the glass.
   d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
   e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Do not expose to strong light (sun rays) for long periods. For continuous using under cruel condition exceeding the normal using condition, consult our company.

5) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensors are precise optical equipment that should not be subject to too much mechanical shocks.

Package Outline Unit: mm

22pin DIP (600mil)

1. "**A**" is the center of the effective image area.

2. The two points "**B**" of the package are the horizontal reference. The point "**B'**" of the package is the vertical reference.

3. The bottom "**C**" of the package is the height reference.

4. The center of the effective image area, relative to "**B**" and "**B'**" is (H, V) = (9.0, 7.55) ± 0.15mm.

5. The rotation angle of the effective image area relative to H and V is ± 1°.

6. The height from the bottom "**C**" to the effective image area is 1.41 ± 0.15mm.

7. The tilt of the effective image area relative to the bottom "**C**" is less than 60µm.

8. The thickness of the cover glass is 0.75mm, and the refractive index is 1.5.

9. The notches on the bottom must not be used for reference of fixing.

PACKAGE STRUCTURE

PACKAGE MATERIAL	Cer-DIP
LEAD TREATMENT	TIN PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	2.6g