Integrated Device Technology, Inc.

CMOS PARALLEL-SERIAL FIFO 2,048 x 9 and 4,096 x 9

IDT72103
IDT72104

FEATURES:

- 35ns parallel port access time, 45ns cycle time
- 50MHz serial input/output frequency
- Serial-to-parallel, parallel-to-serial, serial-to-serial, and parallel-to-parallel operations
- Expandable in both depth and width with no external components
- Flexishift™ — Sets programmable serial word width from 4 bits to any width with no external components
- Multiple flags: Full, Almost-Full (Full-1/8),Full-Minus-One, Empty, Almost-Empty (Empty + 1/8), Empty-Plus-One, and Half-Full
- Asynchronous and simultaneous read or write operations
- Dual-Port, zero fall-through time architecture
- Retransmit capability in single-device mode
- Packaged in 44-pin PLCC
- Industrial temperature range (–40°C to +85°C)

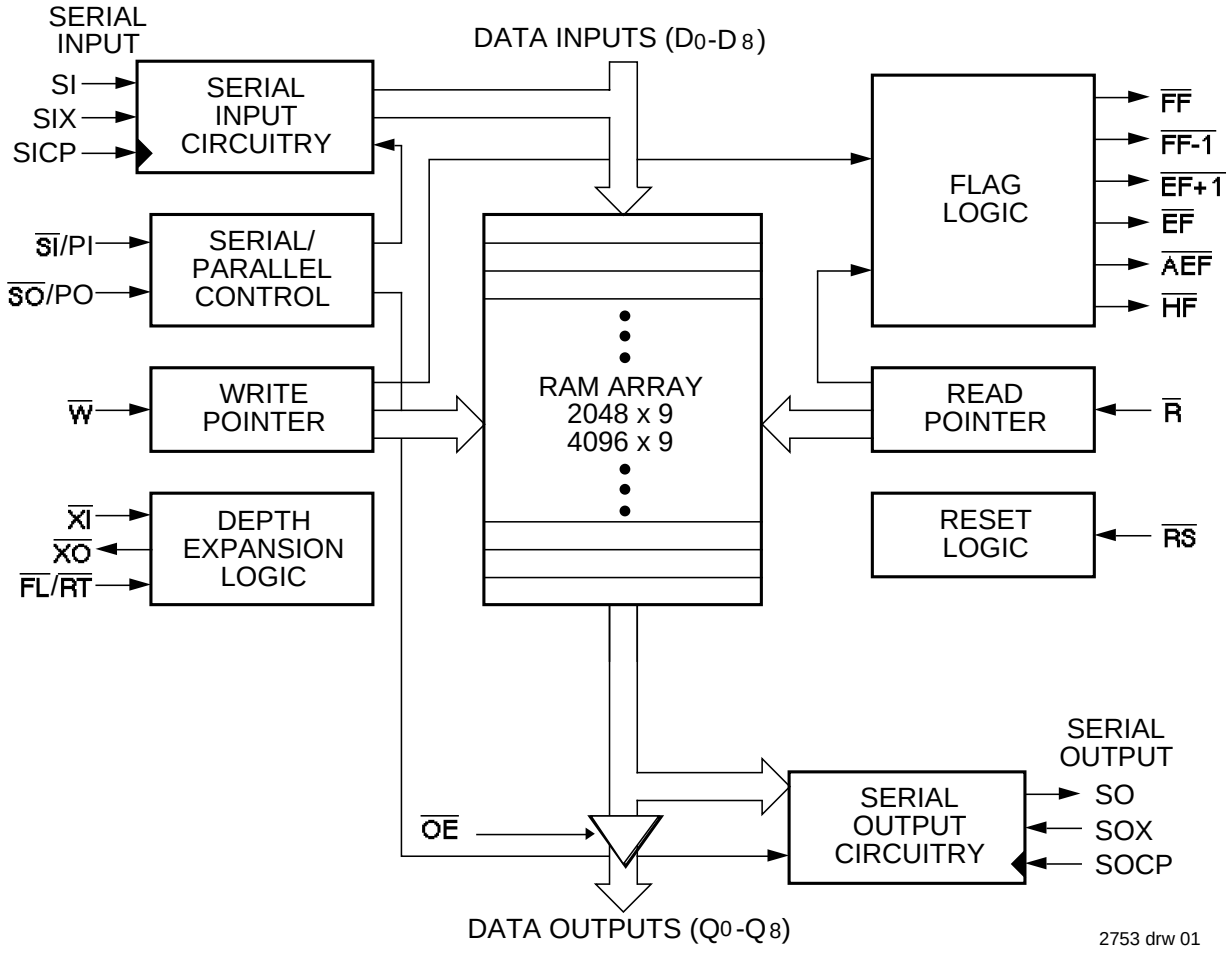
APPLICATIONS:

- High-speed data acquisition systems
- Local area network (LAN) buffer
- High-speed modem data buffer
- Remote telemetry data buffer
- FAX raster video data buffer
- Laser printer engine data buffer
- High-speed parallel bus-to-bus communications
- Magnetic media controllers
- Serial link buffer

DESCRIPTION:

The IDT72103/72104 are high-speed Parallel-Serial FIFOs to be used with high-performance systems for functions such as serial communications, laser printer engine control and local area networks.

FUNCTIONAL BLOCK DIAGRAM



2753 drw 01

DESCRIPTION (Continued)

A serial input, a serial output and two 9-bit parallel ports make four modes of data transfer possible: serial-to-parallel, parallel-to-serial, serial-to-serial, and parallel-to-parallel. These devices are expandable in both depth and width for all of these operational configurations.

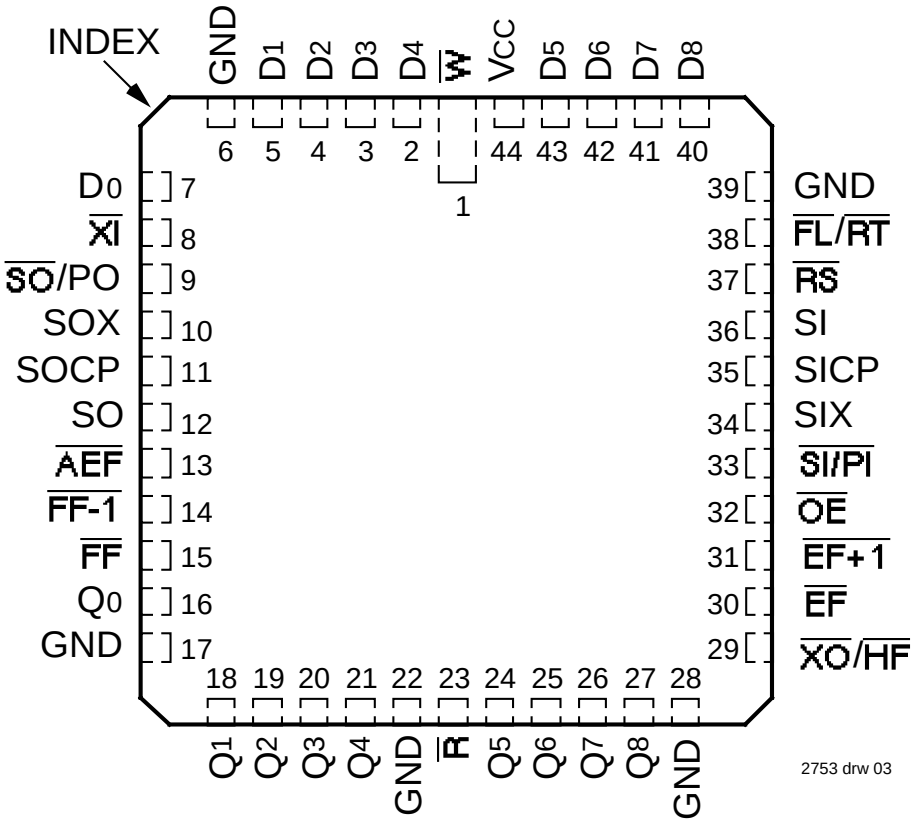
These FIFOs may be configured to handle serial word widths of four or greater using IDT's unique Flexishift feature. Flexishift allows serial width and depth expansion without external components. For example, you may configure a 4K x 24 FIFO using three IDT72104s in a serial width expansion configuration.

Seven flags are provided to signal memory status of the FIFO. The flags are $\overline{FF}$ (Full), $\overline{AF}$ (7/8 full), $\overline{FF-1}$ (Full-minus-one), $\overline{EF}$ (Empty), $\overline{AE}$ (1/8 full), $\overline{EF+1}$ (Empty-plus-one), and $\overline{HF}$ (Half-full).

Read ($\overline{R}$) and Write ($\overline{W}$) control pins are provided for asynchronous and simultaneous operations. An Output Enable ($\overline{OE}$) control pin is available on the parallel output port for high-impedance control. The depth expansion control pins $\overline{XO}$ and $\overline{XI}$ are provided to allow cascading for deeper FIFOs.

The IDT72103/72104 are manufactured using IDT's CMOS technology.

PIN CONFIGURATIONS



PLCC (J44-1, order code: J)
TOP VIEW

PIN DESCRIPTION

Symbol	Name	I/O	Description
D_0-D_8	Data Inputs Serial Input Word Width Select	I/O	In a parallel input configuration – data inputs for 9-bit wide data. In a serial input configuration – one of the nine output pins is used to select the serial input word width.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set low, internal READ and WRITE pointers are set to the first location of the RAM array. $\overline{EF}$, $\overline{EF+1}$, $\overline{AEF}$ are all LOW after a reset, while $\overline{FF}$, $\overline{FF-1}$, $\overline{HF}$ are HIGH after a reset.
$\overline{W}$	Write	I	A parallel word write cycle is initiated on the falling edge of $\overline{W}$ if the $\overline{FF}$ is high. When the FIFO is full, $\overline{FF}$ will go low inhibiting further write operations to prevent data overflow. In a serial input configuration, data bits are clocked into the input shift register and the write pointer does not advance until a full parallel word is assembled. One of the pins, D_i, is connected to $\overline{W}$ and advances the write pointer every i-th serial input clock.
$\overline{R}$	Read	I	A read cycle is initiated on the falling edge of $\overline{R}$ if the $\overline{EF}$ is HIGH. After all the data from the FIFO has been read $\overline{EF}$ will go LOW inhibiting further read operations. In a serial output configuration, a data word is read from memory into the output shift register. One of the pins, Q_j, is connected to $\overline{R}$ and advances the read pointer every j-th serial output clock.
$\overline{FL}/\overline{RT}$	First Load/ Retransmit	I	This is a dual-purpose pin. In multiple-device mode, $\overline{FL}/\overline{RT}$ is grounded to indicate the first device loaded. In single-device mode, $\overline{FL}/\overline{RT}$ acts as the retransmit input. Single-device mode is initiated by grounding the $\overline{XI}$ pin.
$\overline{XI}$	Expansion In	I	In single-device mode, $\overline{XI}$ is grounded. In depth expansion or daisy chain mode, $\overline{XI}$ is connected to the $\overline{XO}$ pin of the previous device.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is LOW, both parallel and serial outputs are enabled. When $\overline{OE}$ is HIGH, the parallel output buffers are placed in a high-impedance state.
Q_0-Q_8	Data Outputs/Serial Output Word Width Select	O	In a parallel output configuration - data outputs for 9-bit wide data. In a serial output configuration - one of nine output pins used to select the serial output word width.
$\overline{FF}$	Full Flag	O	$\overline{FF}$ is asserted LOW when the FIFO is full and further write operations are inhibited. When the $\overline{FF}$ is HIGH, the FIFO is not full and data can be written into the FIFO.
$\overline{FF-1}$	Full-1 Flag	O	$\overline{FF-1}$ goes LOW when the FIFO memory array is one word away from being full. It will remain LOW when every memory location is filled.
$\overline{XO}/\overline{HF}$	Expansion Out/ Half-Full Flag	O	$\overline{HF}$ is LOW when the FIFO is more than half-full in the single device or width expansion modes. The $\overline{HF}$ will remain LOW until the difference between the write and read pointers is less than or equal to one-half of the FIFO memory. In depth expansion mode, a pulse is written from $\overline{XO}$ to $\overline{XI}$ of the next device when the last location in the FIFO is filled. Another pulse is sent from $\overline{XO}$ to $\overline{XI}$ of the next device when the last FIFO location is read.
$\overline{AEF}$	Almost-Empty/ Almost-Full Flag	O	When $\overline{AEF}$ is LOW, the FIFO is empty to 1/8 full or 7/8 full to completely full. If $\overline{AEF}$ is HIGH, then the FIFO is greater than 1/8 full, but less than 7/8 full.
$\overline{EF+1}$	Empty+1 Flag	O	$\overline{EF+1}$ is LOW when there is zero or one word in the FIFO memory array.
$\overline{EF}$	Empty Flag	O	$\overline{EF}$ goes LOW when the FIFO is empty and further read operations are inhibited. $\overline{FF}$ is HIGH when the FIFO is not empty and data reads are permitted.
SI	Serial Input Expansion	I	Data input for serial data.
SO	Serial Output Expansion	O	Data output for serial data.
SICP	Serial Input Clock	I	This pin is the serial input clock. On the rising edge of the SICP signal, new serial data bits are read into the serial input shift register.
SOCP	Serial Output Clock	I	This pin is the serial output clock. On the rising edge of the SOCP signal, new serial data bits are read from the serial output shift register.
SIX	Serial Input Expansion	I	SIX controls the serial input expansion for word widths greater than 9 bits. In a serial input configuration, the SIX pin of the least significant device is tied HIGH. The SIX pin of all other devices is connected to the D_8 pin of the previous device. In parallel input configurations or serial input configurations of 9 bits or less, SIX is tied HIGH.
SOX	Serial Output Expansion	I	SOX controls the serial output expansion for word widths greater than 9 bits. In a serial output configuration, the SOX pin of the least significant device is tied HIGH. The SOX pin of all other devices is connected to the Q_8 pin of the previous device. In parallel output configurations or serial output configurations of 9 bits or less, SOX is tied HIGH.
$\overline{SI}$/PI	Serial/Parallel Input	I	When this pin is HIGH, the FIFO is in a parallel input configuration and accepts input data through D_0-D_8. When $\overline{SI}$/PI is LOW, the FIFO is in a serial input configuration and data is input through SI.
$\overline{SO}$/PO	Serial/Parallel Output	I	When this pin is HIGH, the FIFO is in a parallel output configuration and sends output data through Q_0-Q_8. When $\overline{SO}$/PO is LOW the FIFO is in a serial output configuration and data is input through SO.
GND	Ground		Five ground pins for the PLCC.
V_{CC}	Power		One + 5V power pin.

2753 tbl 04

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	–50 to +50	mA

2753 tbl 01

NOTE:
1.Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	—	—	V
V_{IL}(1)	Input Low Voltage	—	—	0.8	V
T_A	Operating Temperature Industrial	-40	—	85	°C

2753 tbl 03

NOTE:
1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Industrial: V_{CC} = 5.0V ± 10%, T_A = -40°C to +85°C)

Symbol	Parameter	IDT72103 IDT72104 Industrial t_A = 35, 50ns			
		Min.	Typ.	Max.	Unit
I_{LI}(1)	Input Leakage Current (Any Input)	–1	—	1	µA
I_{LO}(2)	Output Leakage Current	–10	—	10	µA
V_{OH}	Output Logic "1" Voltage, I_{OUT} = –2mA(4)	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage, I_{OUT} = 8mA(5)	—	—	0.4	V
I_{CC1}(3)	Active Power Supply Current	—	90	140	mA
I_{CC2}(3,6)	Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}/\overline{RT}$ = V_{IH}) (SOCP = SICP = V_{IL})	—	8	12	mA
I_{CC3}(3,6)	Power Down Current	—	—	2	mA

2753 tbl 06

NOTES:
1. Measurements with 0.4 ≤ V_{IN} ≤ V_{CC}.
2. $\overline{R}$ ≥ V_{IH}, SOCP ≤ V_{IL}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
3. Tested with outputs open (I_{OUT} = 0).
4. For SO, I_{OUT} = –8mA.
5. For SO, I_{OUT} =16mA.
6. SOCP = SICP ≤ 0.2V; other Inputs = V_{CC} - 0.2V.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

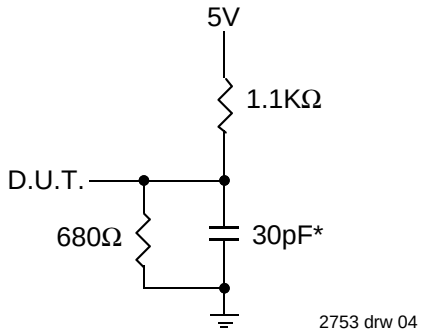
2753 tbl 02

NOTE:
1. This parameter is sampled and not 100% tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2753 tbl 07



or equivalent circuit

Figure 1. Ouput Load

*Including jig and scope capacitances

AC ELECTRICAL CHARACTERISTICS

(Industrial: V_{CC} = 5.0V ± 10%, T_A = -40°C to +85°C)

Symbol	Parameter	Industrial IDT72103L35 IDT72104L35 Min.	Industrial IDT72103L35 IDT72104L35 Max.	Industrial IDT72103L50 IDT72104L50 Min.	Industrial IDT72103L50 IDT72104L50 Max.	Unit	Timing Figure
f_S	Parallel Shift Frequency	—	22.2	—	15	MHz	—
f_{SOCP}	Serial-Out Shift Frequency	—	50	—	40	MHz	—
f_{SICP}	Serial-In Shift Frequency	—	50	—	40	MHz	—
PARALLEL-OUTPUT MODE TIMINGS							
t_A	Access Time	—	35	—	50	ns	4
t_{RR}	Read Recovery Time	10	—	15	—	ns	4
t_{RPW}	Read Pulse Width	35	—	50	—	ns	4
t_{RC}	Read Cycle Time	45	—	65	—	ns	4
t_{WLZ}	Write Pulse LOW to Data Bus at Low-Z[1]	5	—	15	—	ns	15
t_{RLZ}	Read Pulse LOW to Data Bus at Low-Z[1]	5	—	10	—	ns	4
t_{RHZ}	Read Pulse HIGH to Data Bus at High-Z[1]	—	20	—	30	ns	4
t_{DV}	Data Valid from Read Pulse HIGH	5	—	5	—	ns	4
PARALLEL-INPUT MODE TIMINGS							
t_{DS}	Data Set-up Time	18	—	20	—	ns	3
t_{DH}	Data Hold Time	0	—	0	—	ns	3
t_{WC}	Write Cycle Time	45	—	50	—	ns	3
t_{WPW}	Write Pulse Width	35	—	40	—	ns	3
t_{WR}	Write Recovery Time	10	—	10	—	ns	3
RESET TIMINGS							
t_{RSC}	Reset Cycle Time	45	—	50	—	ns	2,18
t_{RS}	Reset Pulse Width	35	—	40	—	ns	2,18
t_{RSS}	Reset Set-up Time	35	—	40	—	ns	2,18
t_{RSR}	Reset Recovery Time	10	—	10	—	ns	2,17,18
RESET TO FLAG TIMINGS							
t_{RSF1}	Reset to $\overline{EF}$, $\overline{AEF}$, and $\overline{EF+1}$ LOW	—	45	—	65	ns	2
t_{RSF2}	Reset to $\overline{HF}$, $\overline{FF}$, and $\overline{FF-1}$ LOW	—	45	—	65	ns	2
RESET TO OUTPUT TIMINGS – SERIAL MODE ONLY							
t_{RSQL}	Reset Going LOW to Q_{0-8} LOW	20	—	20	—	ns	18
t_{RSQH}	Reset Going HIGH to Q_{0-8} HIGH	20	—	20	—	ns	18
t_{RSDL}	Reset Going LOW to D_{0-8} LOW	20	—	20	—	ns	17
RETRANSMIT TIMINGS							
t_{RTC}	Retransmit Cycle Time	45	—	50	—	ns	5
t_{RT}	Retransmit Pulse Width	35	—	40	—	ns	5
t_{RTS}	Retransmit Set-up Time	35	—	40	—	ns	5
t_{RTR}	Retransmit Recovery Time	10	—	10	—	ns	5
t_{RTF}	Retransmit to Flags	—	35	—	50	ns	5
PARALLEL MODE FLAG TIMINGS							
t_{REF}	Read LOW to $\overline{EF}$ LOW	—	30	—	45	ns	6
t_{RFF}	Read HIGH to $\overline{FF}$ HIGH	—	30	—	45	ns	7
t_{RF}	Read HIGH to Transitioning $\overline{HF}$, $\overline{AEF}$ and $\overline{FF-1}$	—	45	—	65	ns	8,9,10
t_{RE}	Read LOW to $\overline{EF+1}$ LOW	—	45	—	65	ns	11
t_{RPE}	Read Pulse Width after $\overline{EF}$ HIGH	35	—	40	—	ns	15
t_{WEF}	Write HIGH to $\overline{EF}$ HIGH	—	30	—	45	ns	6
t_{WFF}	Write LOW to $\overline{FF}$ LOW	—	30	—	45	ns	7
t_{WF}	Write LOW to Transitioning $\overline{HF}$, $\overline{AEF}$ and $\overline{FF-1}$	—	45	—	65	ns	8,9,10
t_{WE}	Write HIGH to $\overline{EF+1}$ HIGH	—	45	—	65	ns	11
t_{WPF}	Write Pulse Width after $\overline{FF}$ HIGH	35	—	40	—	ns	16

NOTE:
1. Values guaranteed by design, not tested.

2753 tbl 08

AC ELECTRICAL CHARACTERISTICS

(Industrial: V_{CC} = 5.0V ± 10%, T_A = -40°C to +85°C)

Symbol	Parameter	Industrial IDT72103L35 IDT72104L35 Min.	Industrial IDT72103L35 IDT72104L35 Max.	Industrial IDT72103L50 IDT72104L50 Min.	Industrial IDT72103L50 IDT72104L50 Max.	Unit	Timing Figure
DEPTH EXPANSION MODE TIMINGS							
t_{XOL}	Read/Write to $\overline{XO}$ LOW	—	35	—	50	ns	13
t_{XOH}	Read/Write to $\overline{XO}$ HIGH	—	35	—	50	ns	13
t_{XI}	$\overline{XI}$ Pulse Width	35	—	50	—	ns	14
t_{XIR}	$\overline{XI}$ Recovery Time	10	—	10	—	ns	14
t_{XIS}	$\overline{XI}$ Set-up Time	15	—	15	—	ns	14
SERIAL-INPUT MODE TIMINGS							
t_{S2}	Serial Data In Set-up Time to SICP Rising Edge	12	—	15	—	ns	19
t_{H2}	Serial Data In Hold Time to SICP Rising Edge	0	—	0	—	ns	19
t_{S3}	SIX Set-up Time to SICP Rising Edge	5	—	5	—	ns	19
t_{S4}	$\overline{W}$ Set-up Time to SICP Rising Edge	5	—	5	—	ns	19
t_{H4}	$\overline{W}$ Hold Time to SICP Rising Edge	7	—	7	—	ns	19
t_{SICW}	Serial In Clock Width High/Low	8	—	10	—	ns	19
t_{S5}	SI/PI Set-up Time to SICP Rising Edge	35	—	50	—	ns	19
SERIAL-OUTPUT MODE TIMINGS							
t_{S6}	SO/PO Set-up Time to SOCP Rising Edge	35	—	50	—	ns	20
t_{S7}	SOX Set-up Time to SOCP Rising Edge	5	—	5	—	ns	20
t_{S8}	$\overline{R}$ Set-up Time to SOCP Rising Edge	5	—	5	—	ns	20
t_{H8}	$\overline{R}$ Hold Time to SOCP Rising Edge	7	—	7	—	ns	20
t_{SOCW}	Serial Out Clock Width HIGH/LOW	8	—	10	—	ns	20
SERIAL MODE RECOVERY TIMINGS							
t_{REFSO}	Recovery Time SOCP after $\overline{EF}$ Goes HIGH	35	—	80	—	ns	22
t_{RFFSI}	Recovery Time SICP after $\overline{FF}$ Goes HIGH	15	—	15	—	ns	23
SERIAL MODE FLAG TIMINGS							
t_{SOCEF}	SOCP Rising Edge (Bit 0- Last Word) to $\overline{EF}$ LOW	—	20	—	25	ns	22
t_{SOCFF}	SOCP Rising Edge (Bit 0- First Word) to $\overline{FF}$ HIGH	—	30	—	40	ns	24
t_{SOCF}	SOCP Rising Edge to $\overline{FF-1}$, $\overline{HF}$, $\overline{AEF}$ HIGH	—	30	—	40	ns	24,26
t_{SOCF}	SOCP Rising Edge to $\overline{AEF}$, $\overline{EF}$, $\overline{EF+1}$ LOW	—	30	—	40	ns	22,26
t_{SICEF}	SICP Rising Edge (Last Bit-First Word) to $\overline{EF}$ HIGH	—	45	—	65	ns	21
t_{SICFF}	SICP Rising Edge (Bit 1-Last Word) to $\overline{FF}$ LOW	—	30	—	40	ns	23
t_{SICF}	SICP Rising Edge to $\overline{EF+1}$, $\overline{AEF}$ HIGH	—	45	—	65	ns	21,25
t_{SICF}	SICP Rising Edge to $\overline{FF-1}$, $\overline{HF}$, $\overline{AEF}$ HIGH	—	45	—	65	ns	23,25
SERIAL-INPUT MODE TIMINGS							
t_{PD1}	SICP Rising Edge to D[1]	5	17	5	20	ns	17,19
SERIAL-OUTPUT MODE TIMINGS							
t_{PD2}	SOCP Rising Edge to Q[1]	5	17	5	20	ns	20
t_{SOHZ}	SOCP Rising Edge to SO at High-Z[1]	5	16	5	16	ns	20
t_{SOLZ}	SOCP Rising Edge to SO at Low-Z[1]	5	22	5	22	ns	20
t_{SOPD}	SOCP Rising Edge to Valid Data on SO	—	18	—	18	ns	20
OUTPUT ENABLE/DISABLE TIMINGS							
t_{OEHZ}	Output Enable to High-Z (Disable)[1]	—	16	—	16	ns	12
t_{OELZ}	Output Enable to Low-Z (Enable)[1]	5	—	5	—	ns	12
t_{AOE}	Output Enable to Data Valid (Q_{0-8})	—	20	—	22	ns	12

NOTE:

1. Values guaranteed by design, not tested.

2753 tbl 09

GENERAL SIGNAL DESCRIPTION

INPUTS:

Data Inputs (D_0-D_8)

The parallel-in mode is selected by connecting the $\overline{SI}$/PI pin to V_{CC}. D_0-D_8 are the data input lines.

The serial-input mode is selected by grounding the $\overline{SI}$/PI pin. The D_0-D_8 lines are control output pins used to program the serial word width.

Reset ($\overline{RS}$)

Reset is accomplished whenever the $\overline{RS}$ input is taken to a low state. Both internal read and write pointers are set to the first location during reset. A reset is required after power up before a write operation can take place. Both Read ($\overline{R}$) and Write ($\overline{W}$) inputs must be HIGH during reset.

Write ($\overline{W}$)

A write cycle is initiated on the falling edge of $\overline{W}$ provided the Full Flag ($\overline{FF}$) is not asserted. Data set-up and hold times must be met with respect to the rising edge of $\overline{W}$. Data is stored in the RAM array sequentially and independently of any on going read operation.

When the FIFO is full, the $\overline{FF}$ will go LOW inhibiting further write operations to prevent data overflow. After a valid read operation is completed, the $\overline{FF}$ will go HIGH after t_{RFF} allowing a valid write to begin.

Read ($\overline{R}$)

A read cycle is initiated on the falling edge of $\overline{R}$, provided the $\overline{EF}$ is not set. Data is accessed on a first-in/first out basis independent of any on going write operations. After $\overline{R}$ goes HIGH, the Data Outputs (Q_0-Q_8) go to a high-impedance condition until the next read operation. When all the data has been read from the FIFO, the $\overline{EF}$ will go LOW, and Q_0-Q_8 will go to a high-impedance state inhibiting further read operations. After the completion of a valid write operation, the $\overline{EF}$ will go HIGH after t_{WEF} allowing a valid read to begin.

First Load/Retransmit ($\overline{FL}$/$\overline{RT}$)

In the depth-expansion mode, the $\overline{FL}$/$\overline{RT}$ pin is grounded to indicate that it is the first device loaded. In the single-device mode, the $\overline{FL}$/$\overline{RT}$ pin acts as the retransmit input. The single-device mode is initiated by grounding the Expansion-In ($\overline{XI}$) pin.

The IDT72103/72104 can be made to retransmit data when the $\overline{RT}$ input is pulsed LOW. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. During retransmit, $\overline{R}$ and $\overline{W}$ must be set HIGH and the $\overline{FF}$ will be affected depending on the relative locations of the read and write pointers. This feature is useful when less than 2,048/4,096 writes are performed between resets. The retransmit feature is not available in the depth expansion mode.

Expansion In ($\overline{XI}$)

The $\overline{XI}$ pin is grounded to indicate an operation in the the single-device mode. In the depth expansion or daisy-chain mode, the $\overline{XI}$ pin is connected to the $\overline{XO}$ pin of the previous device.

Output Enable ($\overline{OE}$)

When $\overline{OE}$ is HIGH, the parallel output buffers are tristated. When $\overline{OE}$ is LOW, both parallel and serial outputs are enabled.

Serial Input (SI)

Serial data is read into the serial input register via the SI pin. In both depth and serial width expansion modes, the serial-input signals of the different FIFOs in the expansion array are connected together.

Serial Input Clock (SICP)

Serial data is read into the serial input register on the rising edge of the SICP signal. In both depth and serial width expansion modes, the SICP signals of the different FIFOs in the expansion array are connected together.

Serial Output Clock (SOCP)

New serial data bits are read from the serial output register on the rising edge of the SOCP signal. In both depth and serial width expansion modes, the SOCP signals of the different FIFOs in the expansion array are connected together.

Serial Input Expansion (SIX)

The SIX pin is tied HIGH for single-device serial or parallel input operation. In a serial input configuration, the SIX pin of the least significant device is tied HIGH. The SIX pin of all other devices is connected to the D_8 pin of the previous device.

Serial Output Expansion (SOX)

The SOX pin is tied HIGH for single-device serial or parallel output operation. In a serial output configuration, the SOX pin of the least significant device is tied HIGH. The SOX pin of all other devices is connected to the Q_8 pin of the previous device.

Serial/Parallel Input ($\overline{SI}$/PI)

The $\overline{SI}$/PI pin programs whether the IDT72103/72104 accepts parallel or serial data as input. When this pin is LOW, the FIFO expects serial data and the D_0-D_8 pins become output pins used to program the write signal and the serial input word width. For instance, connecting D_8 to $\overline{W}$ will program a serial word width of 9 bits; connecting D_7 to $\overline{W}$ will program a serial word width of 8 bits and so on.

Serial/Parallel Output ($\overline{SO}$/PO)

The $\overline{SO}$/PO pin programs whether the IDT72103/72104 outputs parallel or serial data. When this pin is LOW, the FIFO expects serial data and the Q_0-Q_8 pins output signals used to program the read signal and the serial output word width.

OUTPUTS:

Data Outputs (Q_0–Q_8)

Data outputs for 9-bit wide data. These output lines are in a high-impedance condition whenever $\overline{R}$ is in a high state. The serial output mode is selected by grounding the $\overline{SO}$/PO pin. The Q_0-Q_8 lines are control pins used to program the serial word width.

Serial Output (SO)

Serial data is output on the SO pin. In both depth and serial width expansion modes the serial output signals of the different FIFOs in the expansion array are connected together. Following reset, SO is tristated until the first rising edge of the Serial Out Clock (SOCP) signal. Data is clocked out least significant bit first. In the serial width expansion mode, SO is tristated again after the ninth bit is output.

Full Flag ($\overline{FF}$)

$\overline{FF}$ is asserted LOW when the FIFO is full. When the FIFO is full, the internal write pointer will not be incremented by any additional write pulses.

Full Flag — Serial In Mode

When the FIFO is loaded serially, the Serial In Clock (SICP) asserts the $\overline{FF}$. On the second rising edge of the SICP for the last word in the FIFO, the $\overline{FF}$ will assert LOW, and it will remain asserted until the next read operation. Note that when the $\overline{FF}$ is asserted, the last SICP for that word will have to be stretched as shown in Figure 23.

Full Flag — Parallel–In Mode

When the FIFO is in the Parallel-In mode, the falling edge of $\overline{W}$ asserts the $\overline{FF}$ (LOW). The $\overline{FF}$ is then de-asserted (HIGH) by subsequent read operations - either serial or parallel.

Full–Minus — One Flag ($\overline{FF–1}$)

The $\overline{FF–1}$ flag is asserted low when the FIFO is one word away from being full. It will remain asserted when the FIFO is full.

Expansion Out/Half–Full Flag ($\overline{XO}$/$\overline{HF}$)

In the single-device mode, the $\overline{XO}$/$\overline{HF}$ pin operates as a $\overline{HF}$ pin when the $\overline{XI}$ pin is grounded. After half of the memory is filled, the $\overline{HF}$ will be set to LOW at the falling edge of the next write operation. It will remain set until the difference between the write pointer and read pointer is less than or equal to one-half of the FIFO total memory. The $\overline{HF}$ is then reset by the rising edge of the read operation.

In the multiple-device mode, the $\overline{XI}$ pin is connected to the $\overline{XO}$ pin of the previous device. The $\overline{XO}$ pin signals a pulse to the next device when the previous device reaches the best location of memory in the daisy chain configuration.

Almost–Empty or Almost–Full Flag ($\overline{AEF}$)

The $\overline{AEF}$ asserts LOW if there are 0-255 or 1,793-2,048 bytes in the IDT72103, 2,048 x 9 FIFO. The $\overline{AEF}$ asserts LOW if there are 0-511 or 3,585-4,096 bytes in the IDT72104, 4,096 x 9 FIFO.

Empty–Plus–One Flag ($\overline{EF+1}$)

In the parallel-output mode, the $\overline{EF+1}$ flag is asserted LOW when there is one word or less in the FIFO. It will remain LOW when the FIFO is empty.

In the serial-output mode, the $\overline{EF+1}$ flag operates as an $\overline{EF+2}$ flag. It goes LOW when the second to the last word is read from the RAM array and is ready to be shifted out.

Empty Flag ($\overline{EF}$) — Parallel–Out Mode

When the FIFO is in the parallel out mode and there is only one word in the FIFO, the falling edge of the $\overline{R}$ line will cause the $\overline{EF}$ line to be asserted LOW. This is shown in Figure 6. The $\overline{EF}$ is then de-asserted HIGH by either the rising edge of $\overline{W}$ or the rising edge of SICP, as shown in Figure 6.

Empty Flag — Serial–Out Mode

The use of the $\overline{EF}$ is important for proper serial-out operation when the FIFO is almost empty. The $\overline{EF}$ flag is asserted LOW after the first bit of the last word is shifted out. This is shown in Figure 22.

TABLE 1 — STATUS FLAGS

Number of Words in FIFO IDT72103	Number of Words in FIFO IDT72104	$\overline{FF}$	$\overline{FF-1}$	$\overline{AEF}$	$\overline{HF}$	$\overline{EF+1}$ (1)	$\overline{EF}$
0	0	H	H	L	H	L	L
1	1	H	H	L	H	L	H
2-255	2-511	H	H	L	H	H	H
256-1,024	512-2,048	H	H	H	H	H	H
1,025-1,792	2,049-3,584	H	H	H	L	H	H
1,793-2,046	3,585-4,094	H	H	L	L	H	H
2,047	4,095	H	L	L	L	H	H
2,048	4,096	L	L	L	L	H	H

NOTE: 2753 tbl 10

1. $\overline{EF+1}$ acts as $\overline{EF+2}$ in the serial out mode.

PARALLEL TIMINGS:

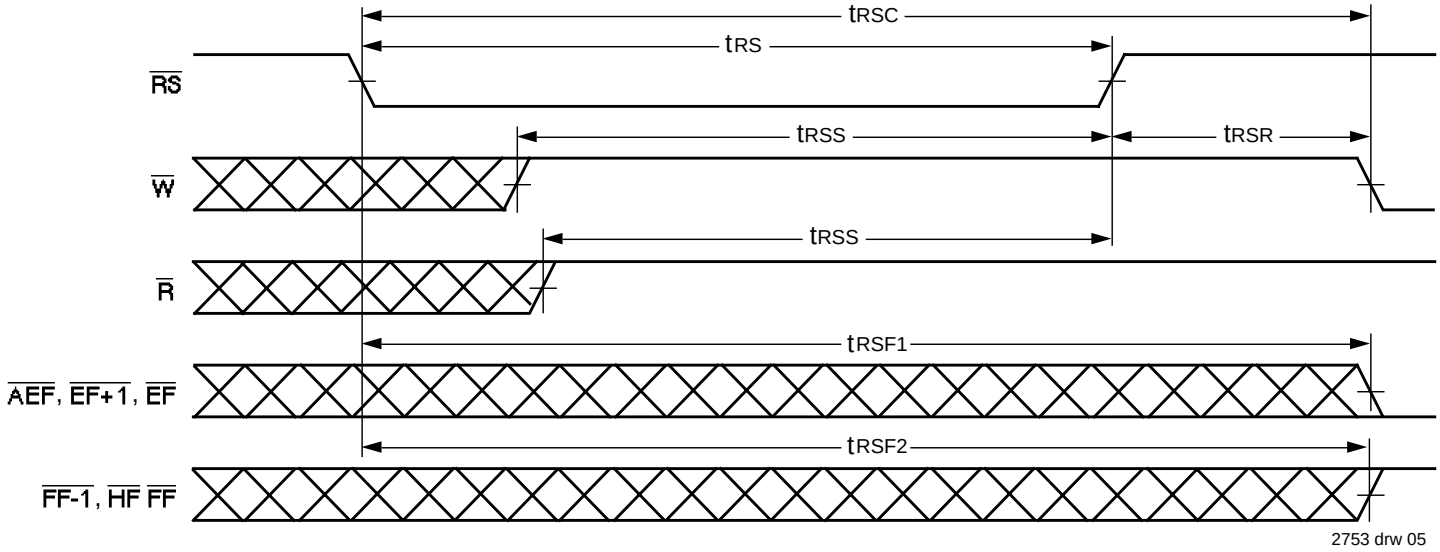


Figure 2. Reset

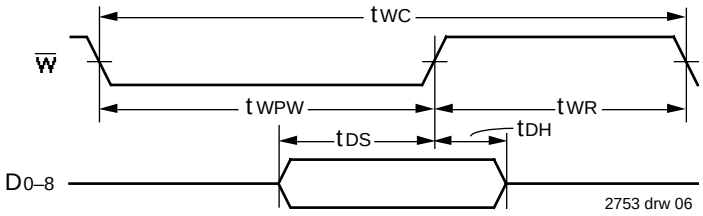


Figure 3. Write Operation in Parallel Data In Mode

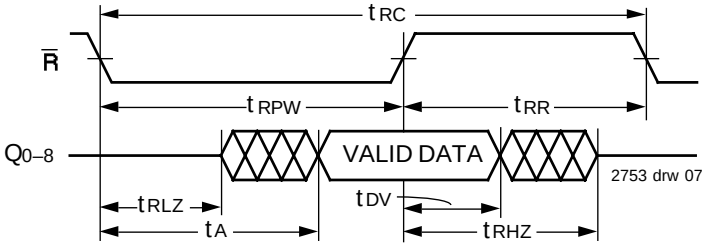


Figure 4. Read Operation in Parallel Data Out Mode

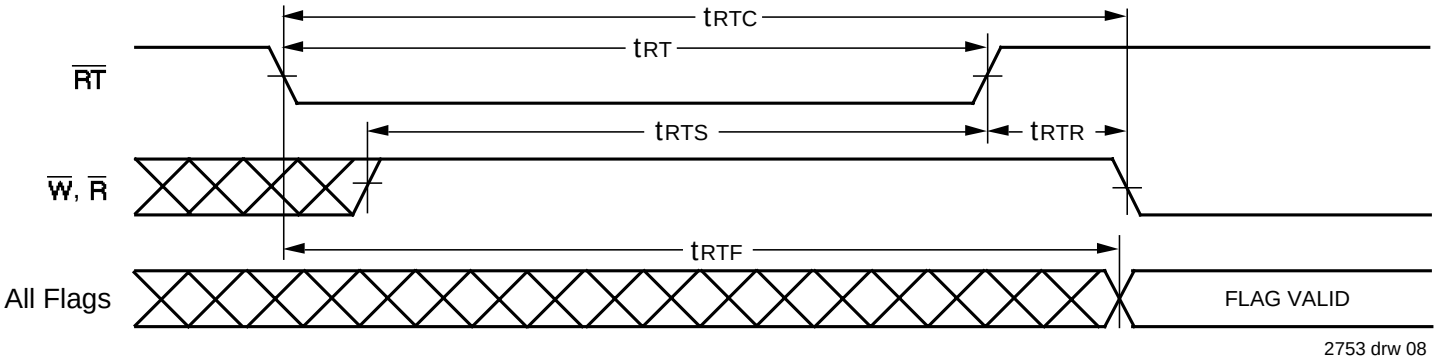
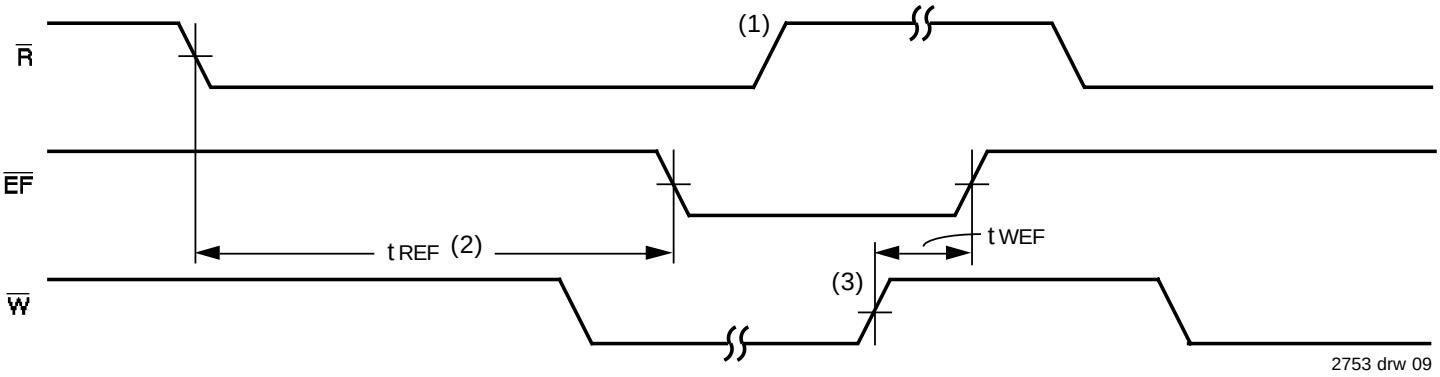
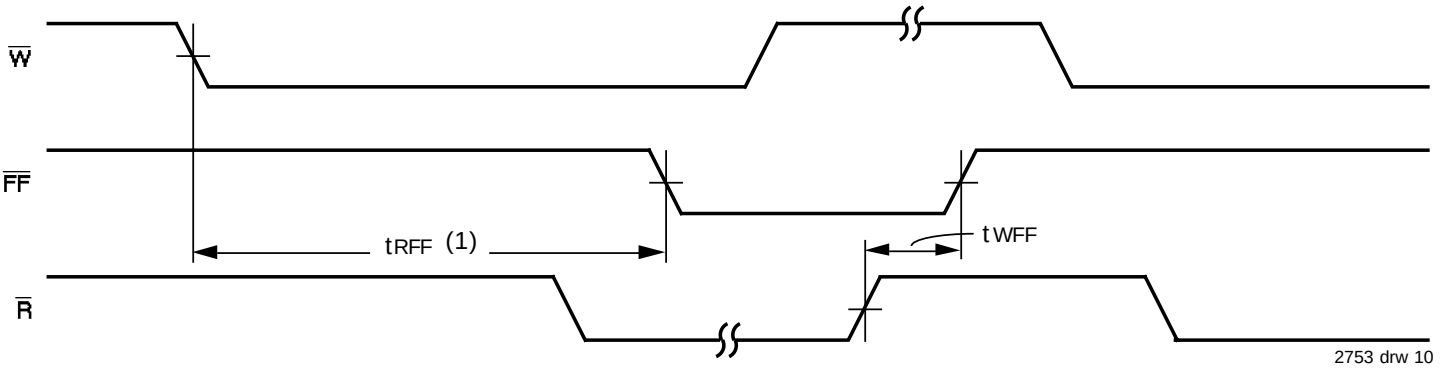


Figure 5. Retransmit



NOTES:
1. Data is valid on this edge.
2. The Empty Flag is asserted by R in the Parallel-Out mode and is specified by tREF. The EF flag is deasserted by the rising edge of W.
3. First rising edge of Write after EF is set.

Figure 6. Empty Flag Timings in Parallel Out Mode



NOTE:
1. For the assertion time, tWFF is used when data is written in the Parallel mode. The FF is de-asserted by the rising edge of R.

Figure 7. Full Flag Timings in Parallel-In Mode

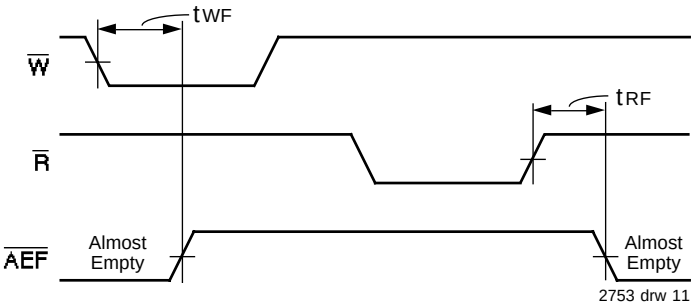


Figure 8. Almost-Empty Flag Region

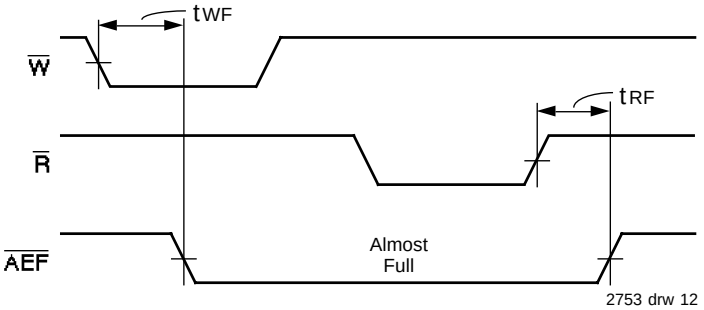


Figure 9. Almost-Full Flag Region

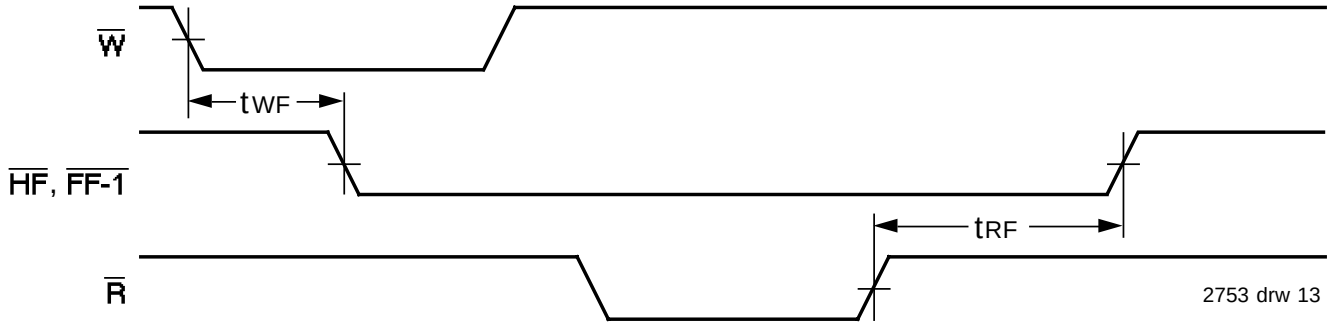


Figure 10. Half-Full and Full-minus-1 Flag Timings

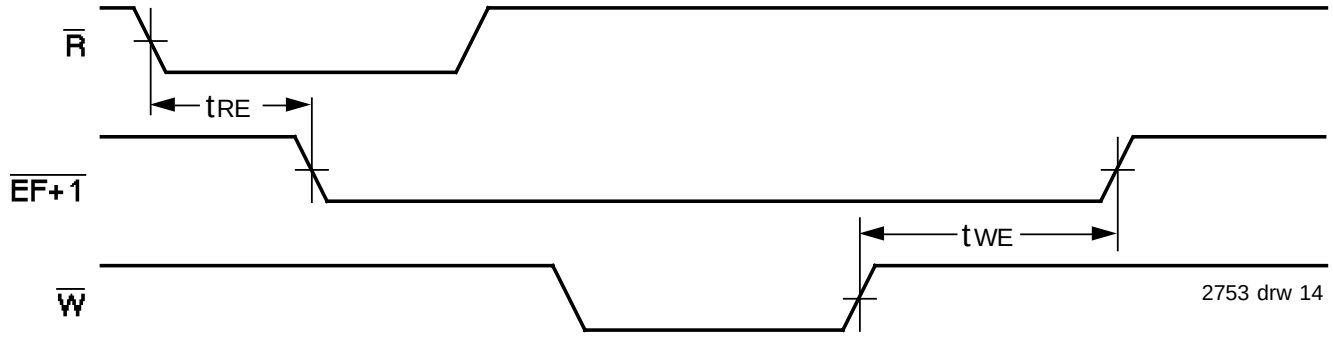


Figure 11. Empty+1 Flag Timings

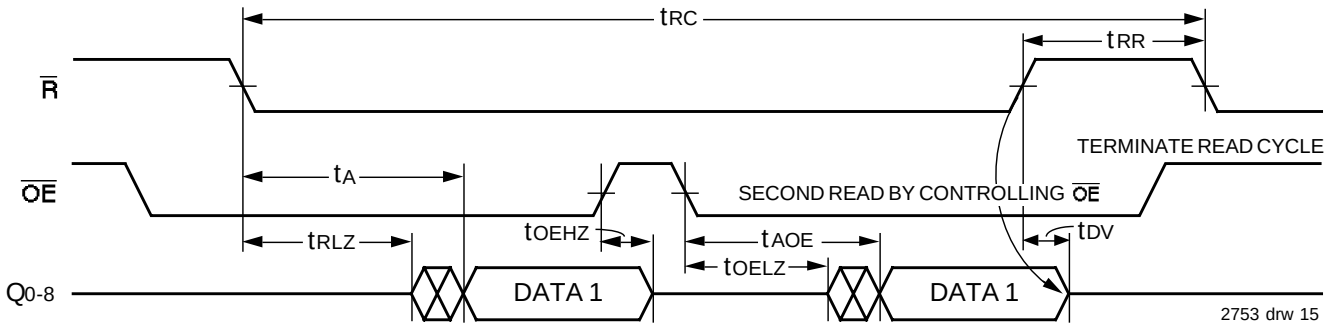


Figure 12. Output Enable Timings

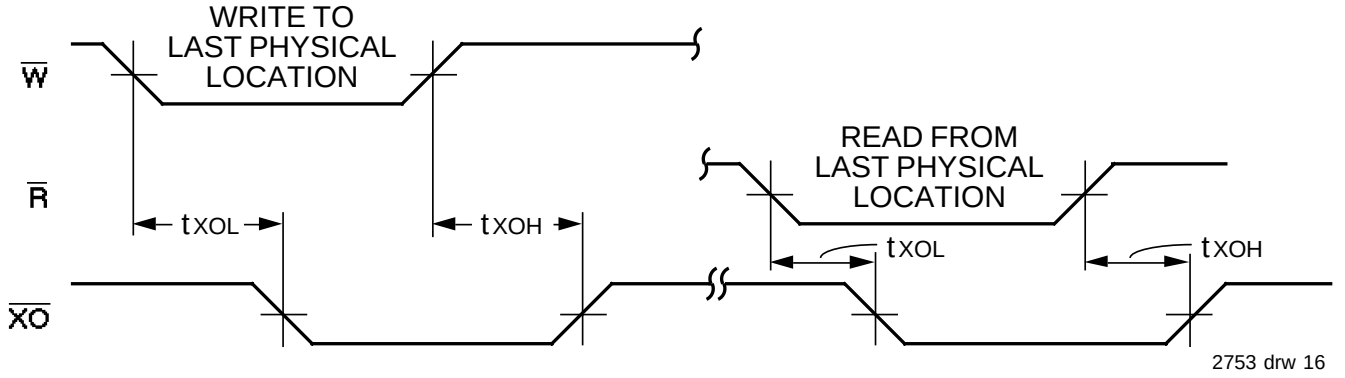


Figure 13. Expansion-Out

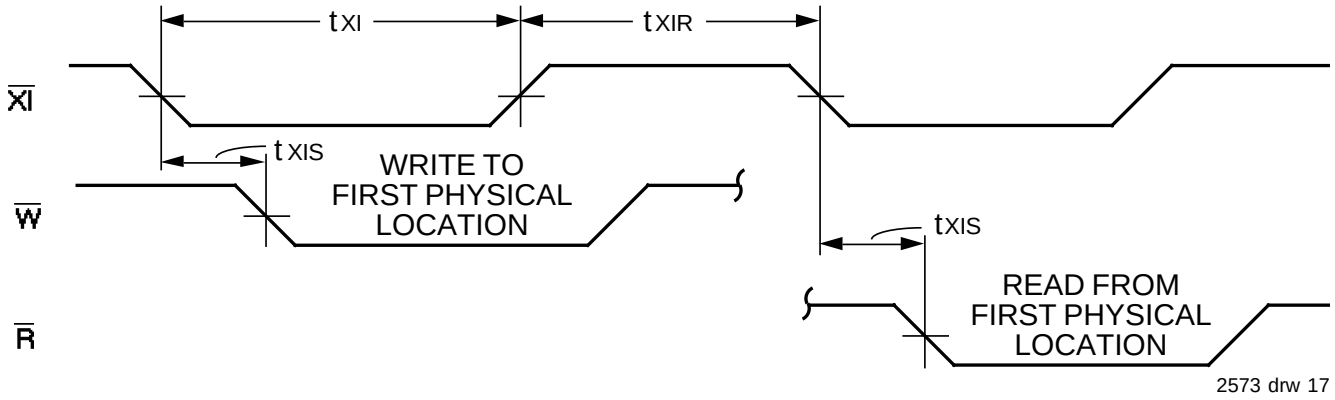


Figure 14. Expansion-In

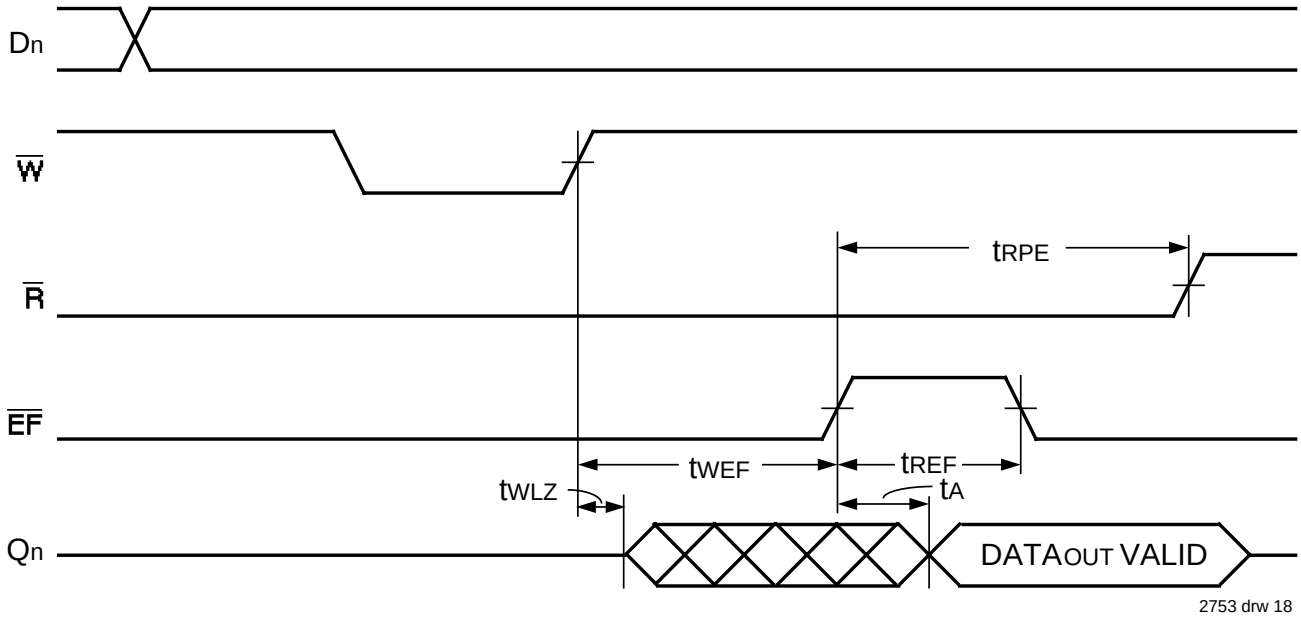


Figure 15. Read Data Flow-Through Mode

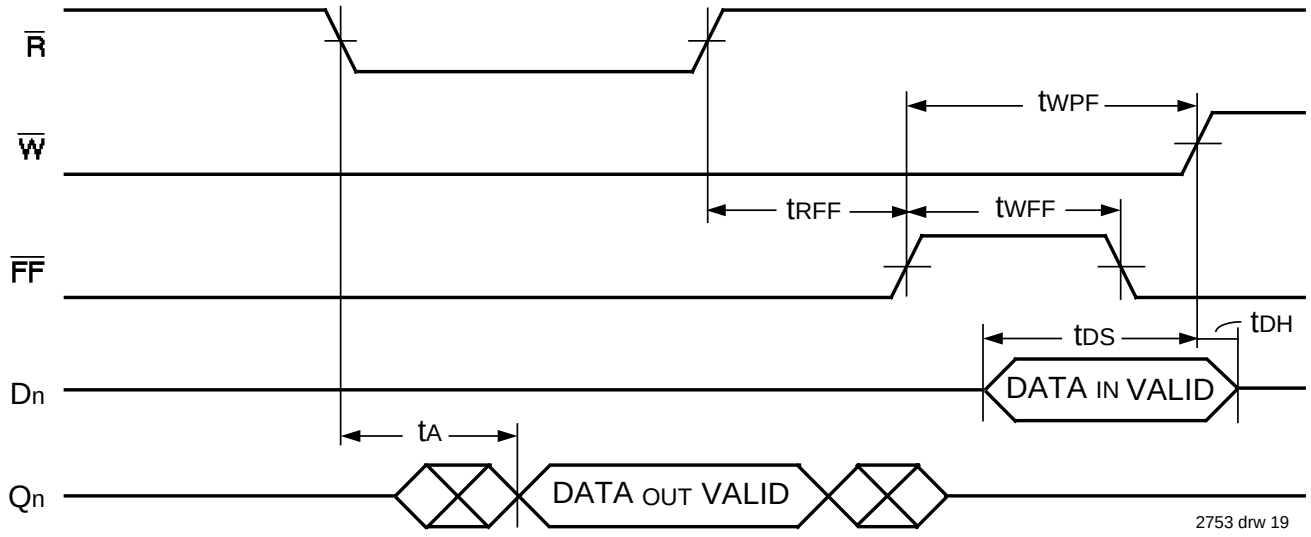
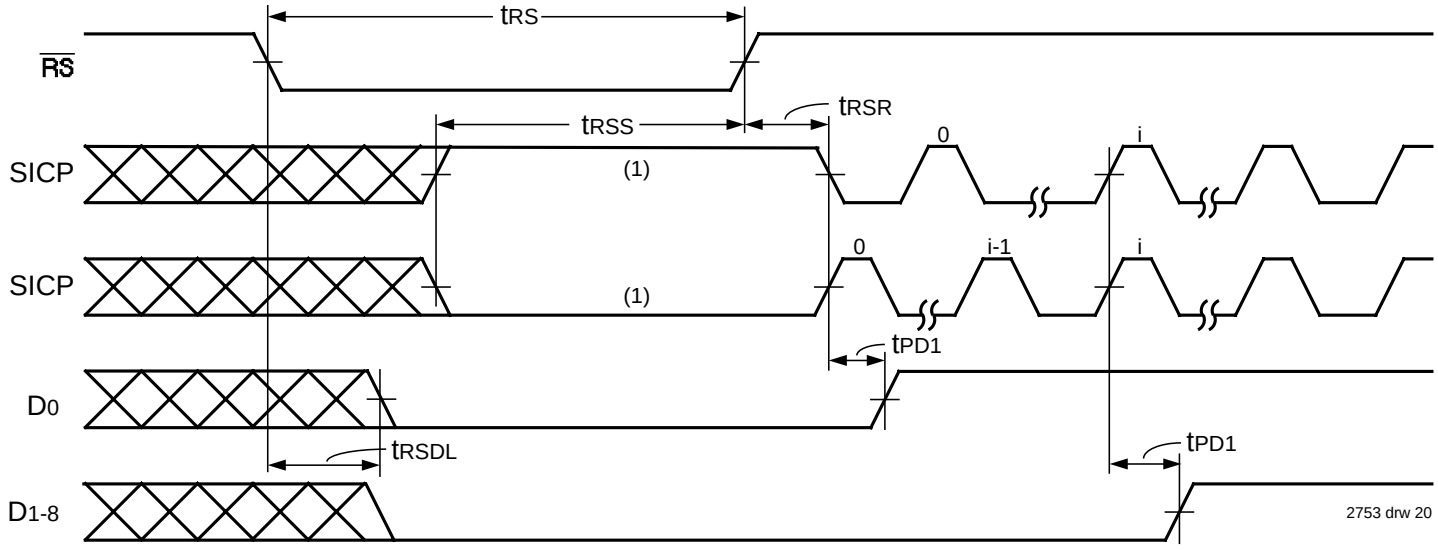


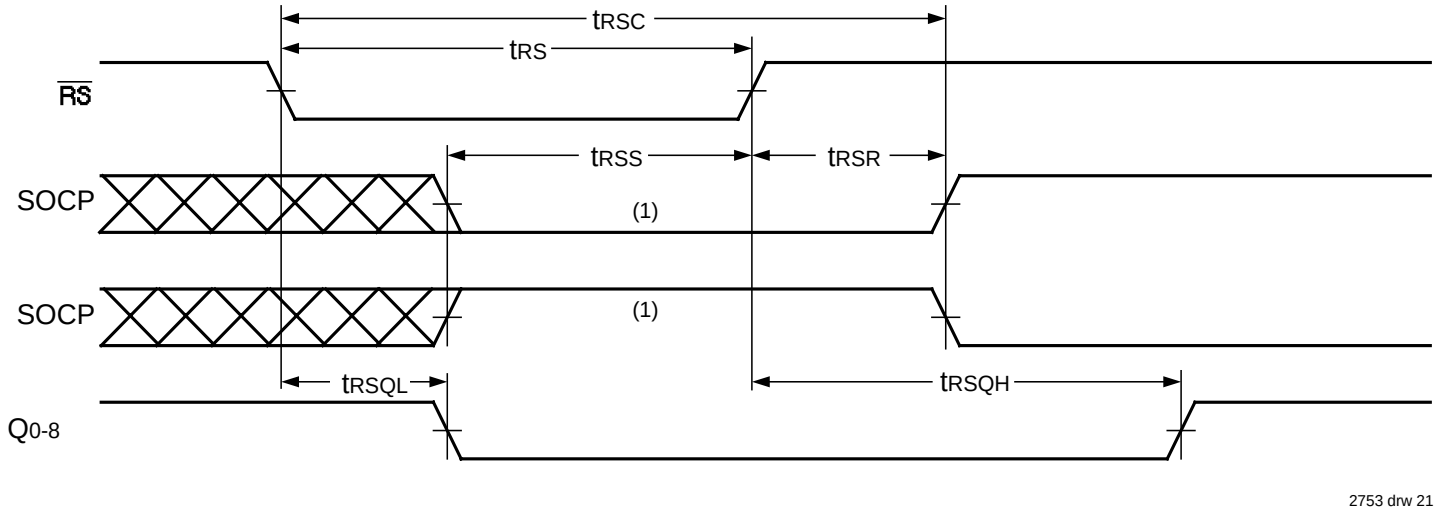
Figure 16. Write Data Flow-Through Mode

SERIAL TIMINGS:



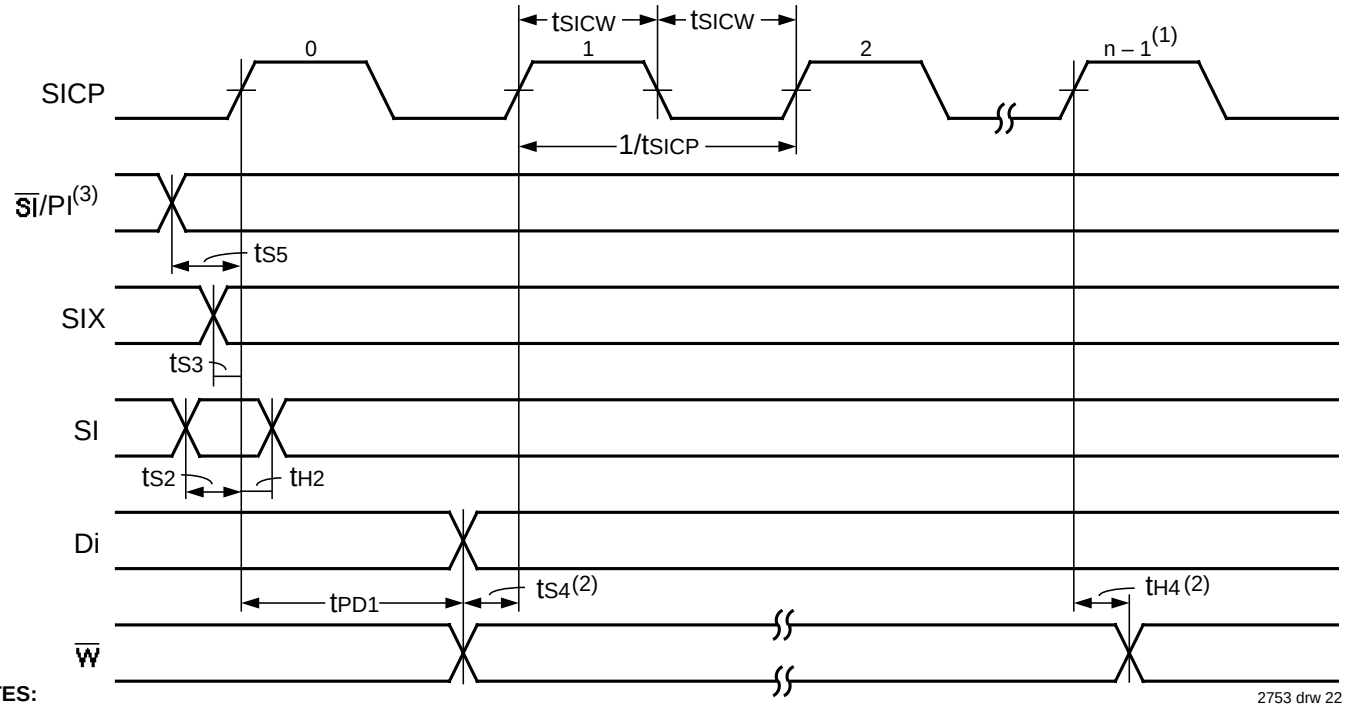
NOTE:
1. SICP should be in the steady LOW or HIGH during t_{RSS}. The first LOW-HIGH (or HIGH-LOW) transition can begin after t_{RSR}.

Figure 17. Reset Timings for Serial-In Mode



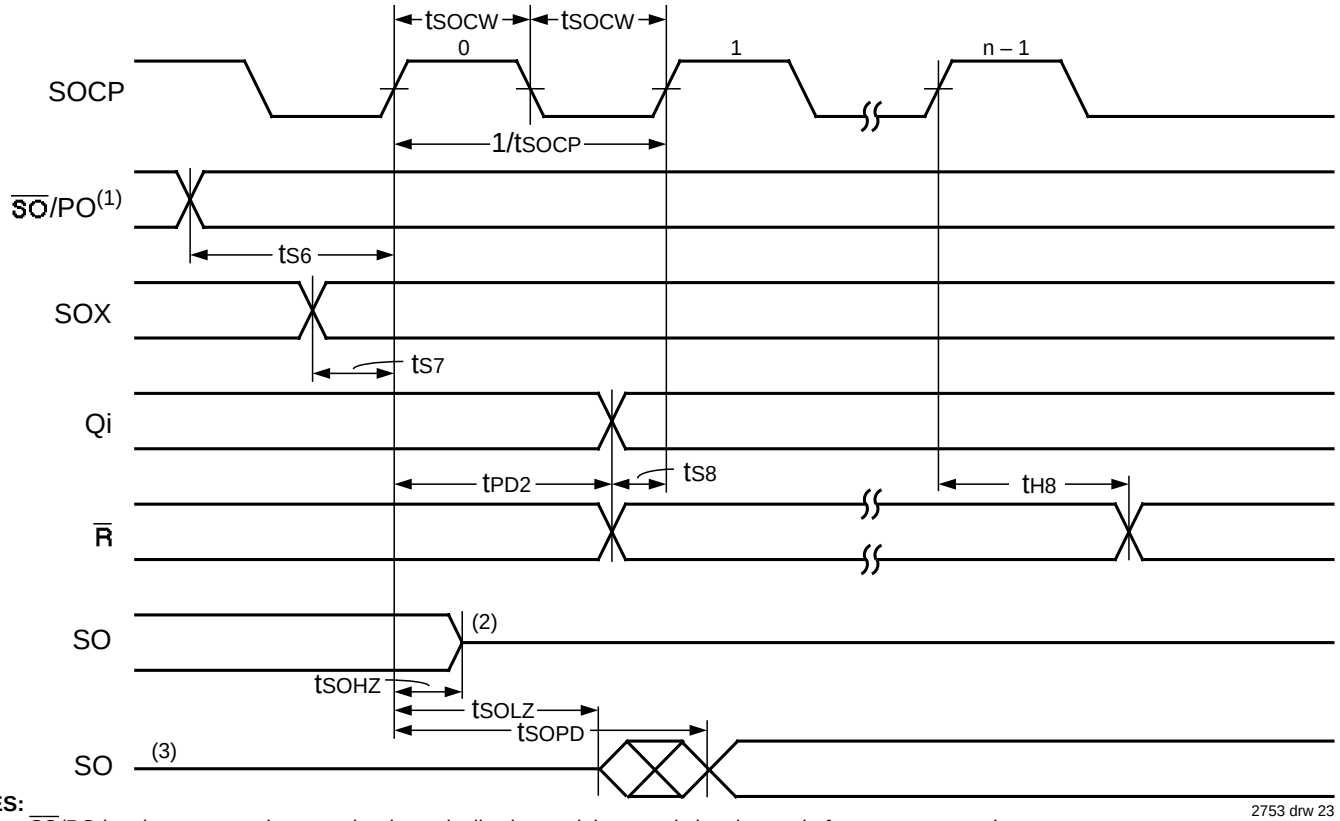
NOTE:
1. SOCP should be in the steady LOW or HIGH during t_{RSS}. The first LOW-HIGH (or HIGH-LOW) transition can begin after t_{RSR}.

Figure 18. Reset Timings for Serial-Out Mode



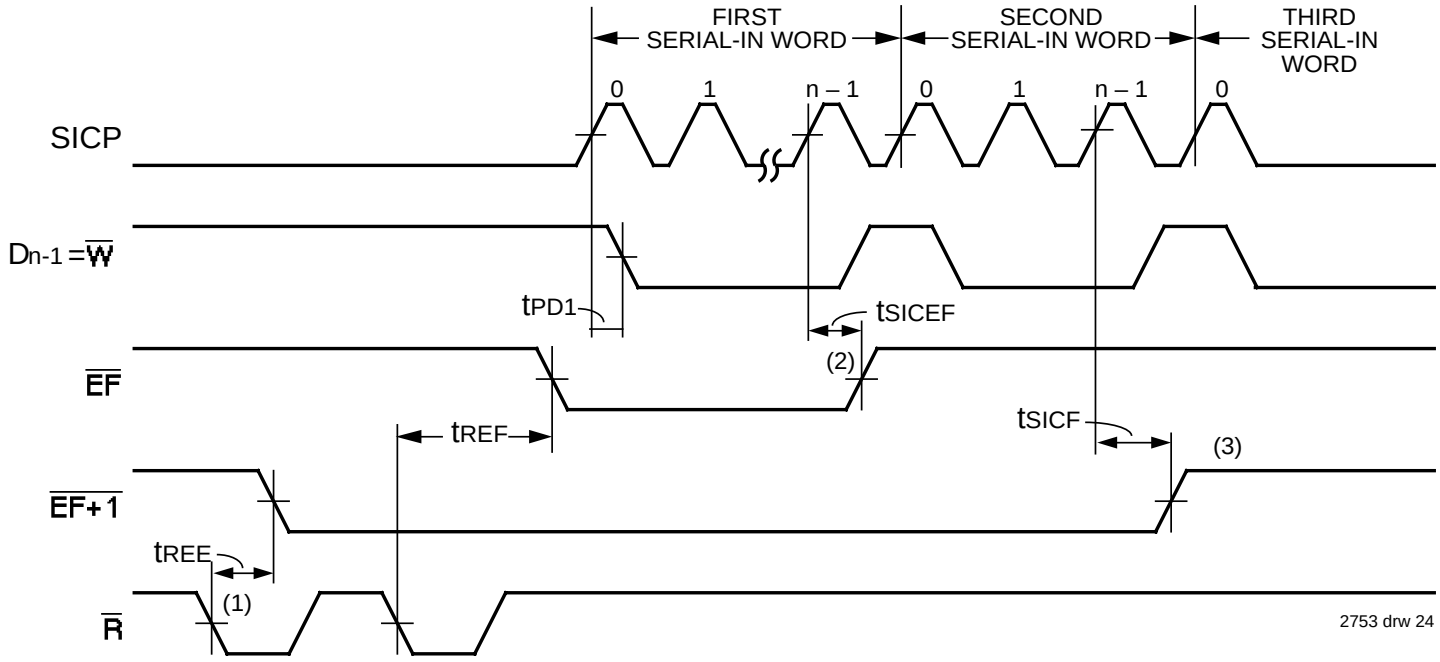
NOTES:
1. For the stand alone mode, n ≥ 4 and the input bits are numbered 0 to n-1.
2. For the recommended interconnections, Di is to be directly tied to $\overline{W}$ and the t_{S4} and t_{H4} requirements will be satisfied. For users that modify $\overline{W}$ externally, t_{S4} and t_{H4} requirements have to be met.
3. After $\overline{SI}$/PI has been set up, it cannot be dynamically changed; it can only be changed after a reset operation.

Figure 19. Write Operation In Serial-In Mode



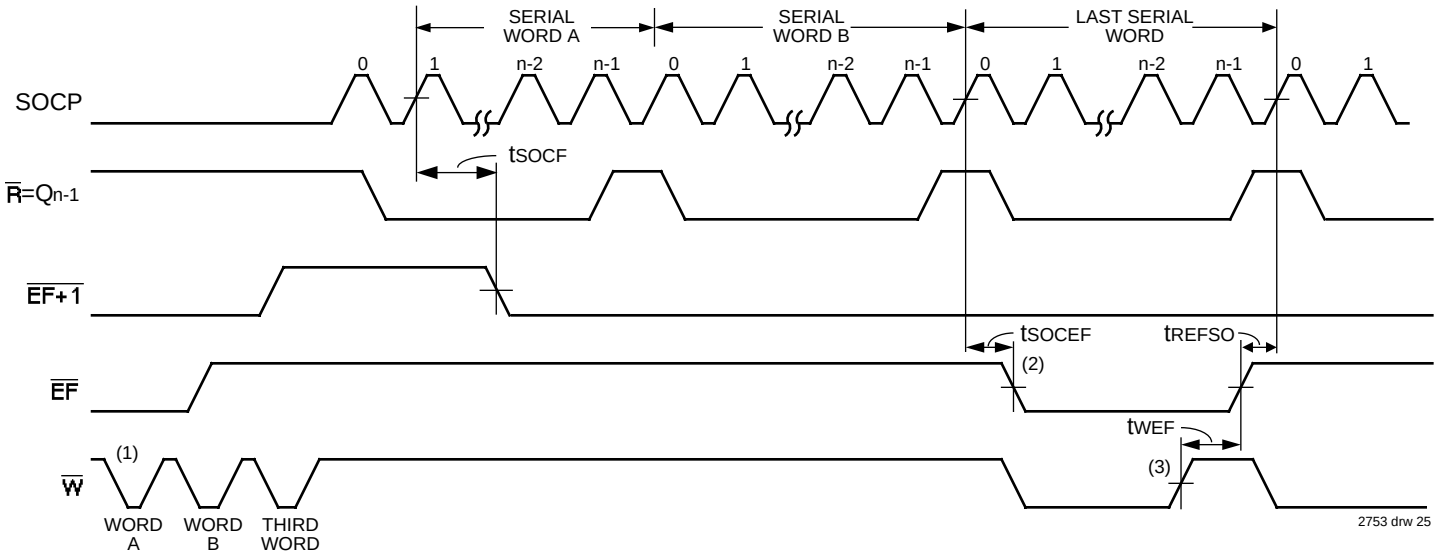
NOTES:
1. After $\overline{SO}$/PO has been set up, it cannot be dynamically changed; it can only be changed after a reset operation.
2. For single device: Read out the last bit after $\overline{EF}$ is asserted.
   For Serial Width Expansion mode: Read out the last bit of the current memory location from the active device.
3. For single device: The operation starts after Reset.
   For Serial Width Expansion mode: Read the first bit of the current memory location from the active device.

Figure 20. Read Operation In Serial-Out Mode



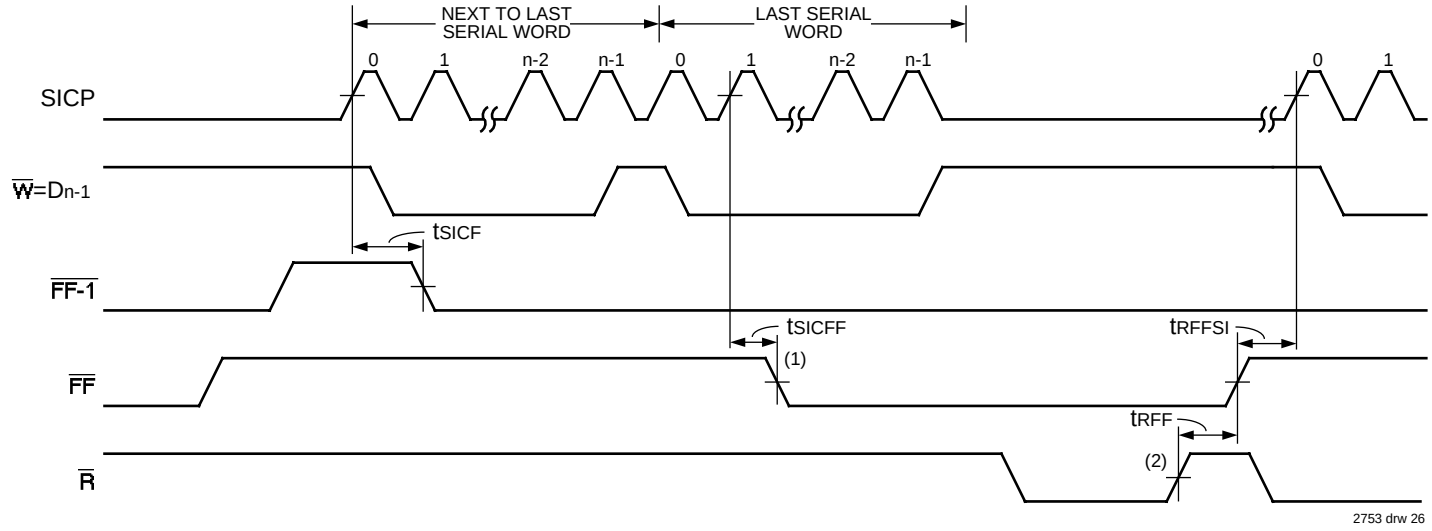
NOTES:
1. Parallel Read shown for reference only. Can also use serial output mode.
2. The Empty Flag is de-asserted after the N–1 rising edge of SICP of the first serial-in word. In the Serial-Out mode, a new read operation can begin t_{REFSO} after $\overline{EF}$ goes HIGH. In the Parallel-Out mode, a new read operation can occur immedately after $\overline{FF}$ goes HIGH.
3. The $\overline{EF+1}$ Flag is de-asserted after the N–1 rising edge of SICP of the second serial-in word.

Figure 21. Empty Flag and Empty+1 Flag De-assertion in the Serial-In Mode



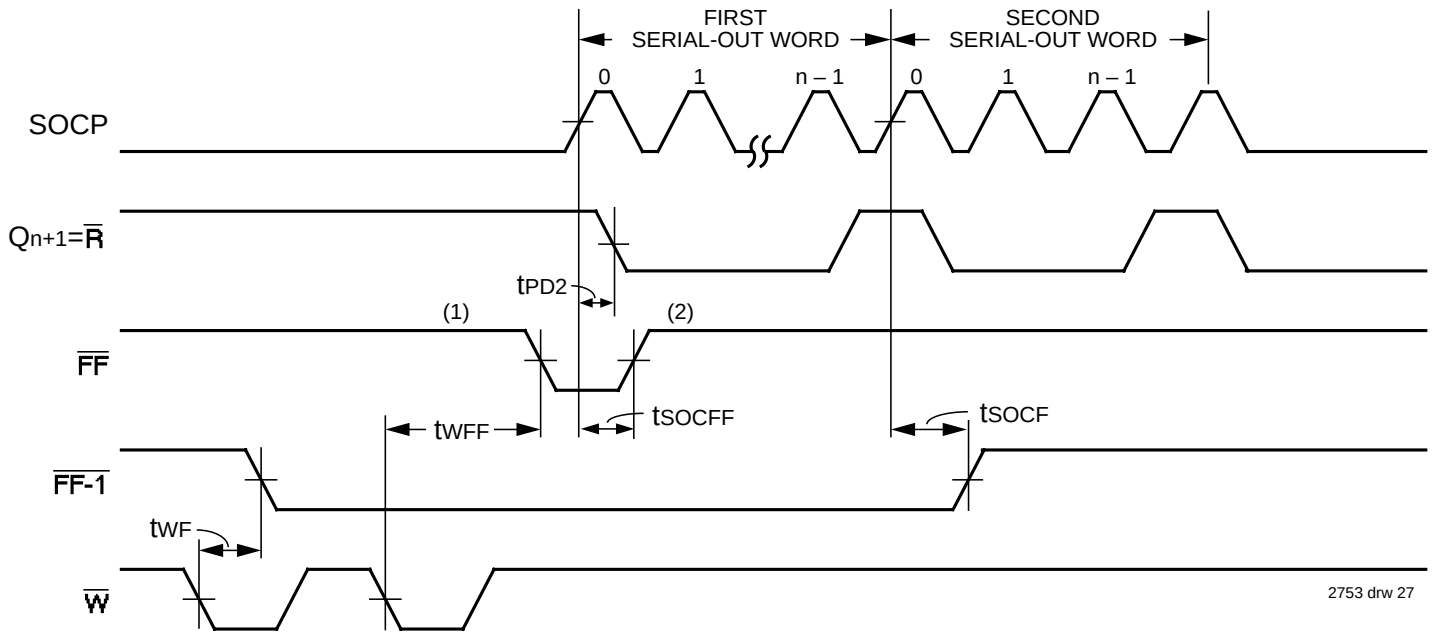
NOTES:
1. Parallel write shown for reference only. Can also use serial input mode.
2. The Empty Flag ($\overline{EF}$) is asserted in Serial-Out mode by using the t_{SOCEF} parameter. This parameter is measured in the worst case condition from the rising edge of the SOCP used to clock data bit 0. Whenever $\overline{EF}$ goes LOW, there is only one word to be shifted out. In the Parallel-In mode, the $\overline{EF}$ flag is de-asserted by the rising edge of W. In the Serial-In mode, the $\overline{EF}$ flag is de-asserted by the rising edge of $\overline{W}$.
3. First Write rising edge after $\overline{EF}$ is set.
4. Once $\overline{EF}$ has gone LOW and the last bit of the final word has been shifted out, SOCP should not be clocked until $\overline{EF}$ goes HIGH.

Figure 22. Empty Flag and Empty+1 Flag Assertion in the Serial-Out Mode (FIFO Being Emptied)



NOTES:
1. The Full Flag is asserted in the Serial-In mode by using the t_{SICFF} parameter. This parameter is measured in the worst case condition from the rising edge of SICP following a (t_{PD1}+t_{WFF}) delay from the first SICP rising edge of the last word.
2. First Read rising edge after $\overline{FF}$ is set.
3. After $\overline{FF}$ goes LOW and the last bit of the final word has been clocked in, SICP should not be clocked until $\overline{FF}$ goes HIGH.

Figure 23. Full Flag and Full-1 Flag Assertlon in the Serial-In Mode (FIFO Being Filled)



NOTES:
1. The FIFO is full and a new read sequence is started.
2. On the first rising edge of SOCP, the $\overline{FF}$ is de-asserted. In the Serial-In mode, a new write operation can begin following t_{RFFS1} after $\overline{FF}$, goes HIGH. In the Parallel-In mode, a new write operation can occur immediately after $\overline{FF}$ goes HIGH.
3. The $\overline{FF\text{-}1}$ flag is de-asserted after the first SOCP of the second serial word.

Figure 24. Full Flag and Full-1 Flag De-assertion in the Serial-Out Mode

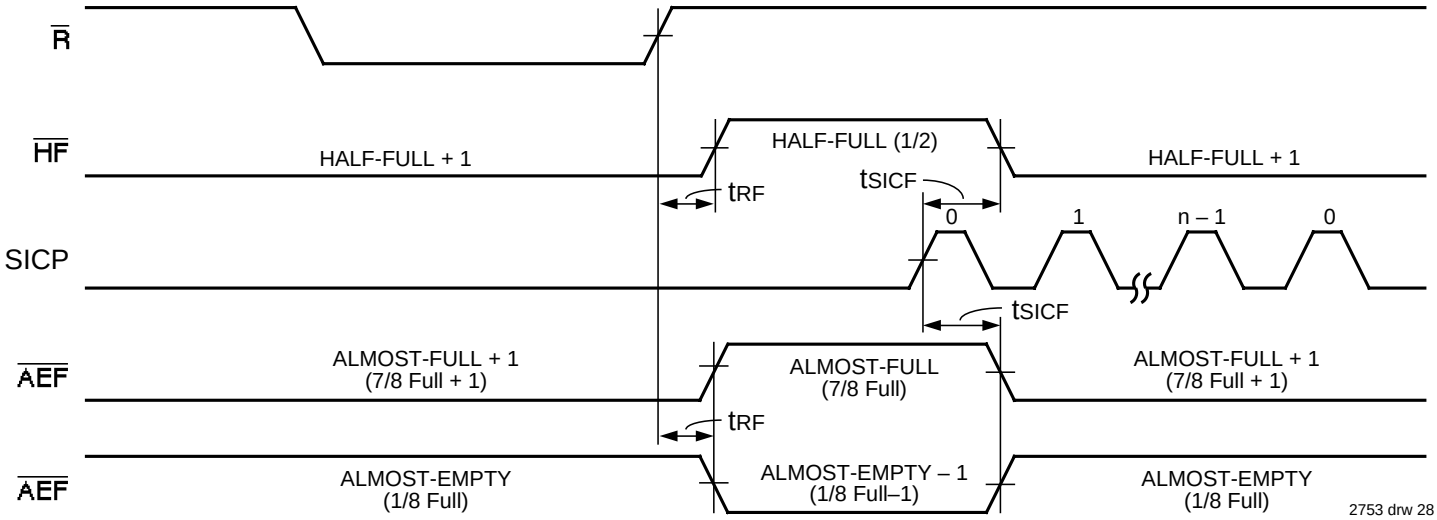


Figure 25. Half-Full, Almost-Full and Almost-Empty Timings for Serial-In Mode

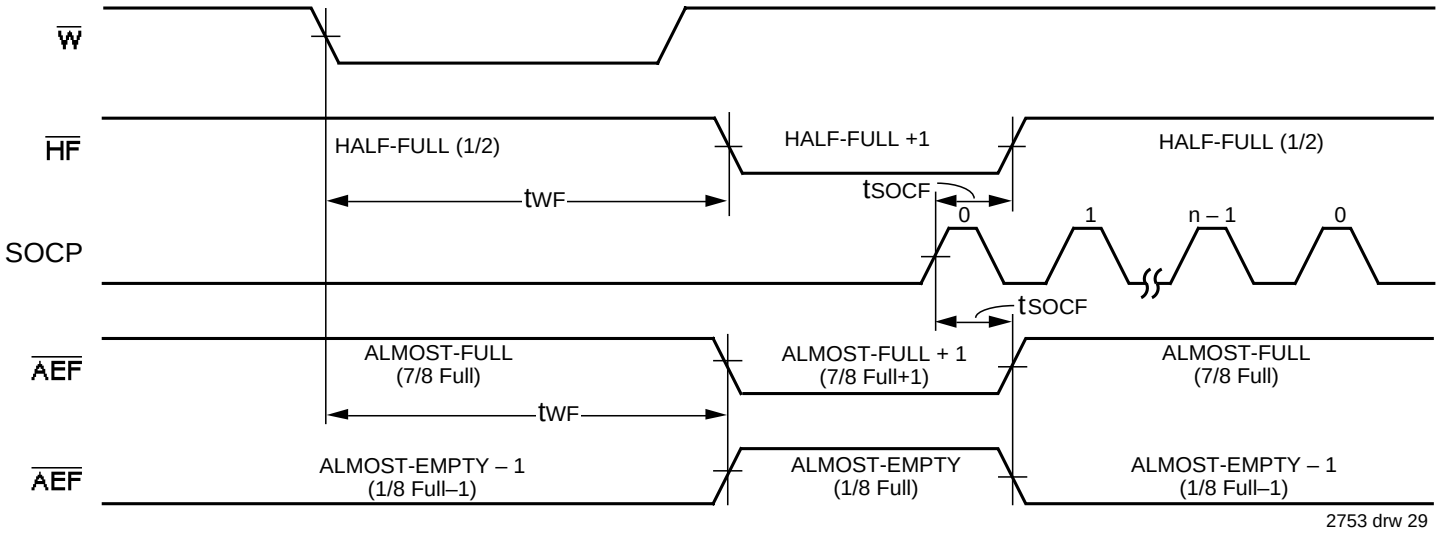


Figure 26. Half-Full, Almost-Full and Almost-Empty Timings for Serial-Out Mode

OPERATING DESCRIPTION

PARALLEL OPERATING MODES:

Parallel Data Input

By setting $\overline{SI}$/PI HIGH, data is written into the FIFO in parallel through the D0-D8 input data lines.

Parallel Data Output

By setting $\overline{SO}$/PO HIGH, the parallel-out mode is chosen. In the parallel-out mode, as shown in Figure 4, data is available tA after the falling edge of $\overline{R}$ and the output bus Q goes into high-impedance after $\overline{R}$ goes HIGH.

Alternately, the user can access the FIFO by keeping $\overline{R}$ LOW and enabling data on the bus by asserting $\overline{OE}$. When $\overline{R}$ is LOW, the $\overline{OE}$ is HIGH and the output bus is tri-stated. When $\overline{R}$ is HIGH, the output bus is disabled irrespective of $\overline{OE}$. The enable and disable timings for $\overline{OE}$ are shown in Figure 12.

Single Device Mode

A single IDT172103/72104 may be used when application requirements are for 2,048/4,096 words or less. The IDT72103/72104 is in the Single Device Configuration when the Expansion In ($\overline{XI}$) control input is grounded (See Figure 27). In this mode, the $\overline{HF/XO}$ is used as a Half-Full flag.

Wldth Expanslon Mode

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags can be detected from any one of the connected devices. Figure 28 demonstrates an 18-bit word width by using two IDT72103/72104s. Any word width can be attained by adding additional IDT72103/72104s.

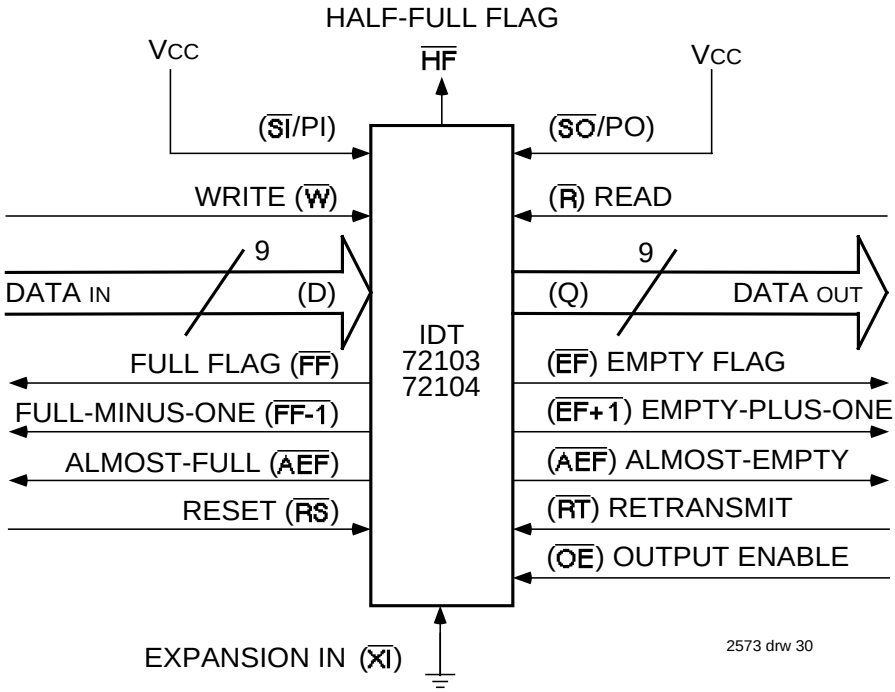


Figure 27. Block Diagram of Single 2,048 x 9 and 4,096 x 9 FIFO in Parallel Mode

INPUT CONFIGURATION TABLE

Pin	Parallel Input	Serial Input			
			Width Expansion		
		Single Device	Least Significant Device	All Other Devices	Most Significant Device
$\overline{SI}$/PI	HIGH	LOW	LOW	LOW	LOW
SI	HIGH or LOW	Input Data	Input Data	Input Data	Input Data
SICP	HIGH or LOW	Input Clock	Input Clock	Input Clock	Input Clock
SIX	HIGH	HIGH	HIGH	D_8 of next least significant device	D_8 of next least significant device
$\overline{W}$	Write Control	D_i	D_i of most significant device	D_i of most significant device	D_i of most significant device
D_0-D_8	Input Data	No connect except D_i	No connect except D_8	No connect except D_8	No connect except D_i
D_i[1]	—	$\overline{W}$	—	—	$\overline{W}$ of all devices
D_8	—	—	SIX of next most significant device	SIX of next most significant device	—

2753 tbl 11

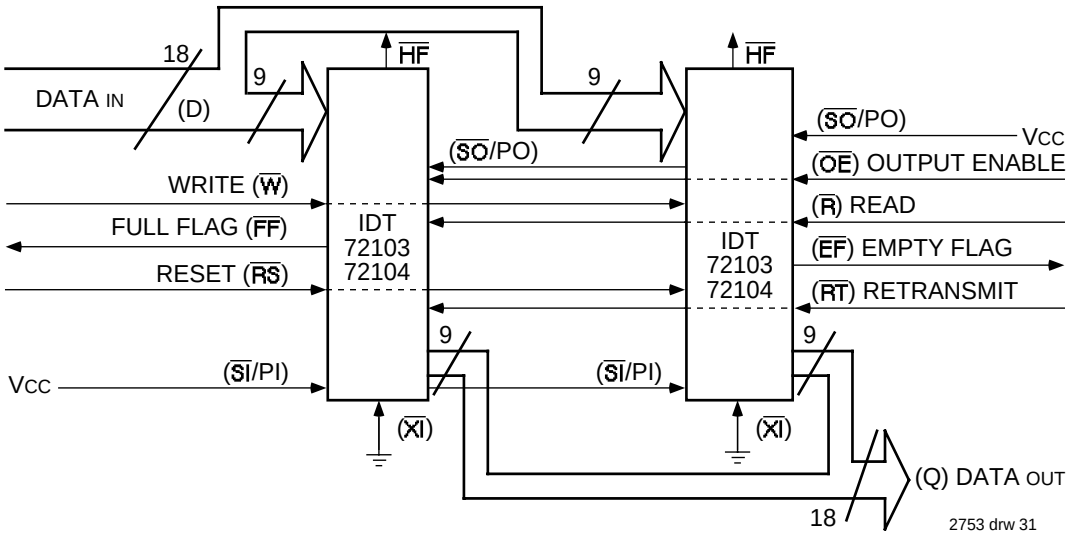
NOTE:
1. D_i refers to the most significant bit of the serial word. If multiple devices are width cascaded. D_i is the most significant bit from the most significant device.

OUTPUT CONFIGURATION TABLE

Pin	Parallel Output	Serial Output			
			Width Expansion		
		Single Device	Least Significant Device	All Other Devices	Most Significant Device
$\overline{SO}$/PO	HIGH	LOW	LOW	LOW	LOW
SO	—	Output Data	Output Data	Output Data	Output Data
SOCP	HIGH or LOW	Output Clock	Output Clock	Output Clock	Output Clock
SOX	HIGH	HIGH	HIGH	Q_8 of next least significant device	Q_8 of next least significant device
$\overline{R}$	Read Control	Q_i	Q_i of most significant device	Q_i of most significant device	Q_i of most significant device
Q_0-Q_8	Output Data	No connect except D_i	No connect except Q_8	No connect except Q_8	No connect except Q_i
Q_i[1]	—	$\overline{R}$	—	—	$\overline{R}$ of all devices
Q_8	—	—	SOX of next most significant device	SOX of next most significant device	—

2753 tbl 12

NOTE:
1. Q_i refers to the most significant bit of the serial word. If multiple devices are width cascaded. Q_i isthe most significant bit from the most significant device.



NOTE:
1. Flag detection is accomplished by monitoring all the flag signals of either (any) device used in the width expansion configuration. Do not connect any flag signals together.

Figure 28. Block Diagram of 2,048 x 18 and 4,096 x 18 FIFO Memory Used in Width Expansion in Parallel Mode

TRUTH TABLES
TABLE 2: RESET AND RETRANSMIT — SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION IN PARALLEL MODE

Mode	Inputs[2]			Internal Status[1]		Outputs		
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{AEF}$, $\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment[1]	Increment[1]	X	X	X

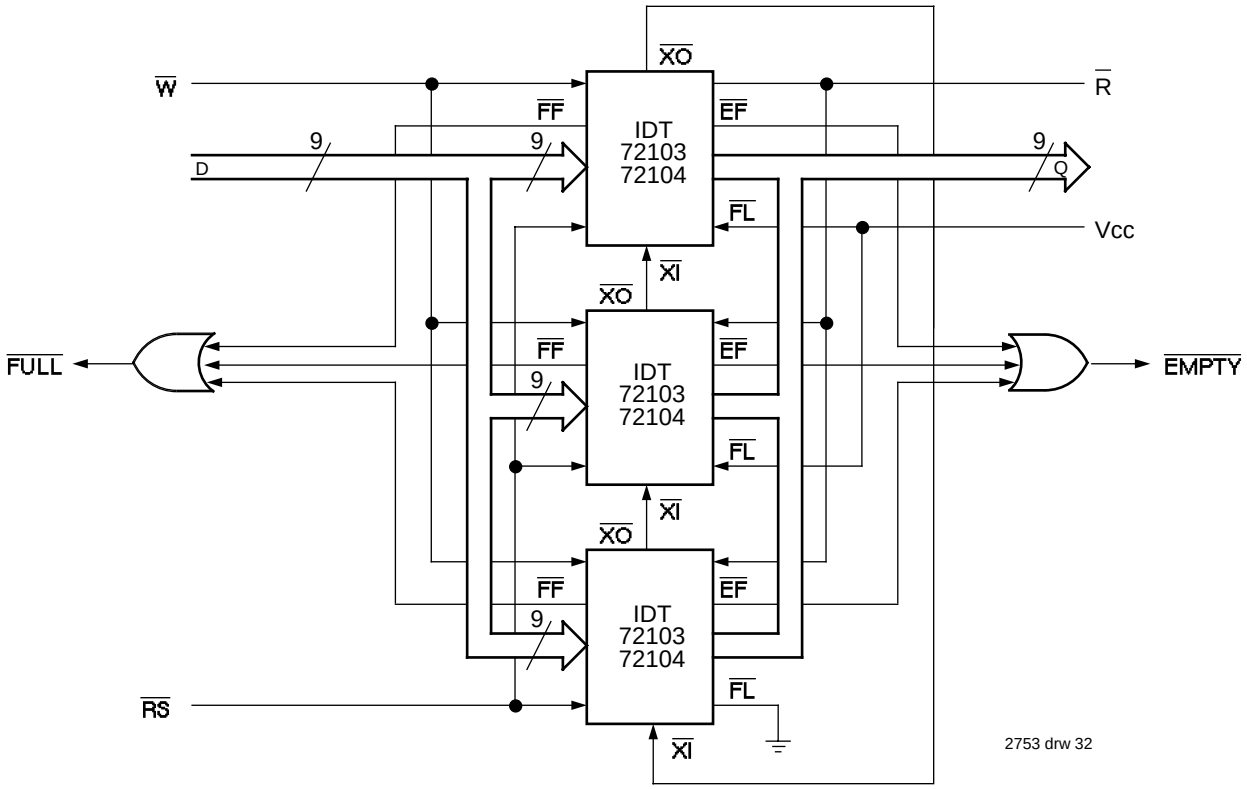
2753 tbl 13

NOTES:
1. Pointer will increment if appropriate flag is HIGH.
2. $\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input.

DEPTH EXPANSION (DAISY CHAIN) MODE

The IDT72103/72104 can be easily adapted to applications where the requirements are for greater than 2,048/4,096 words. Figure 29 demonstrates Depth Expansion using three IDT72103/72104s. Any memory depth can be attained by adding additional IDT72103/72104s. The IDT72103/72104 operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designated by grounding the First Load ($\overline{FL}$) control input pin.
2. All other devices must have the $\overline{FL}$ pin in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. See Figure 29.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the OR-ing of all EFs and OR-ing of all FFs (i.e., all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). See Figure 29.
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion mode.

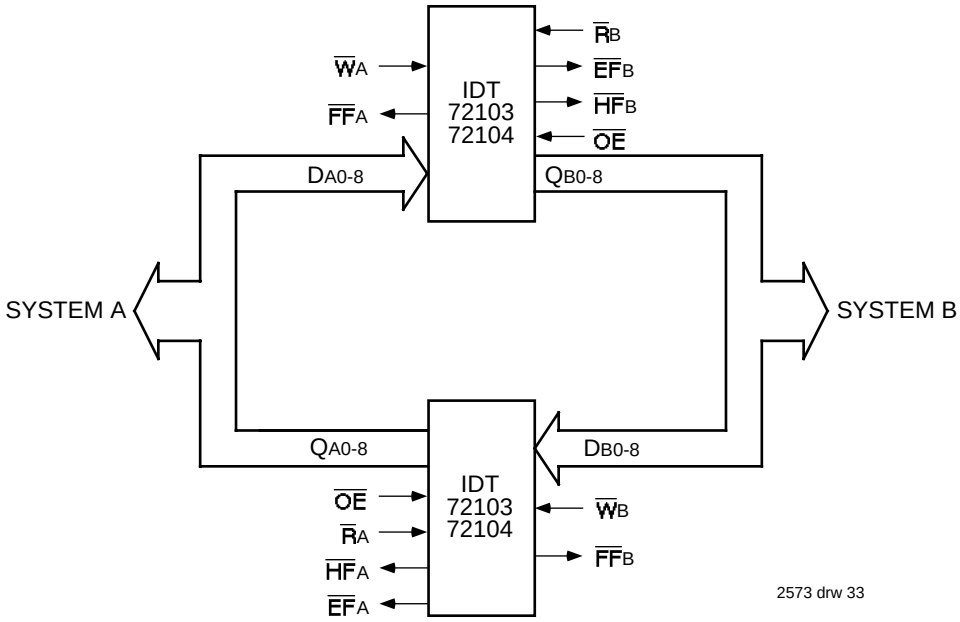


NOTE:
1. $\overline{SI}$/PI and $\overline{SO}$/PO pins are tied to Vcc.

Figure 29. Block Diagram of 6,144 x 9 and 12,288 x 9-FIFO Memory, Depth Expansion in Parallel Mode

BIDIRECTIONAL MODE

Applications requiring data buffering between two systems (each system capable of Read and Write operations) can be achieved by pairing IDT72103/72104 as shown in Figure 30. Both Depth Expansion and Width Expansion may be used in this mode.

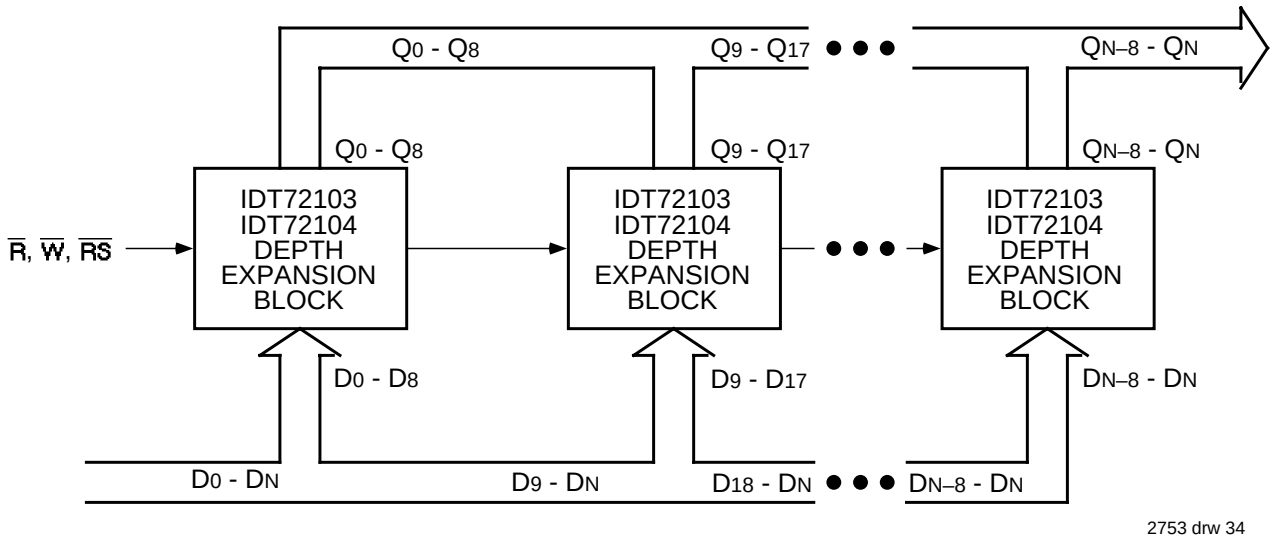


NOTE:
1. SI/PI and SO/PO pins are tied to VCC.

Figure 30. Bidirectional FIFO Mode

COMPOUND EXPANSION MODE

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays (see Figure 31).



NOTES:
1. SI/PI and SO/PO pins are tied to VCC.
2. For depth expansion block see DEPTH EXPANSION Section and Figure 29.
3. For Flag Detection see WIDTH EXPANSION SECTION and Figure 28.

Figure 31. Compound FIFO Expansion

TABLE 3: RESET AND FIRST LOAD TRUTH TABLE — DEPTH EXPANSION/COMPOUND EXPANSION MODE

Mode	Inputs (2)			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset-First Device	0	0	(1)	Location Zero	Location Zero	0	1
Retransmit all Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTES:
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device.
2. $\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Ouput, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input.

2753 tbl 14

SERIAL OPERATING MODES:

Serial Data Input

The Serial Input mode is selected by grounding the $\overline{SI}$/PI line. The D_{0-8} lines are then outputs which are used to program the width of the serial word. They are taps off a digital delay line which are meant for connection to the $\overline{W}$ input. For instance, connecting D_6 to $\overline{W}$ will program a serial word width of 7 bits, connecting D_7 to $\overline{W}$ will program a serial word width of 8 bits and so on.

By programming the serial word width, an economy of clock cycles is achieved. As an example, if the word width is 6 bits, then on every 6th clock cycle the serial data register is written in parallel into the FIFO RAM array. Thus, the possible clock cycles for an extra 3 bits of width in the RAM array are not required.

The SIX signal is used for Serial-In Expansion. When the serial word width is 9 or less, the SIX input must be tied HIGH. When more than 9 bits of serial word width is required, more than one device is required. The SIX input of the least significant device must be tied HIGH. The D_8 pin of the least significant device must be tied to SIX of the next significant device. In other words, the SIX input of the most significant and intermediate devices must always be connected to the D_8 of the next least significant device.

Figure 32 shows the relationship of the SIX, SICP and D_{0-8} lines. In the stand alone case (Figure 32), on the first LOW-to-HIGH of SICP, the D_{1-8} lines go LOW and the D_0 line remains HIGH. On the next SICP clock edge, the D_1 goes HIGH, then D_2 and so on. This continues until the D line, which is connected to $\overline{W}$, goes HIGH. On the next clock cycle, after $\overline{W}$ is HIGH, all of the D lines go LOW again and a new serial word input starts.

In the cascaded case, the first LOW-to-HIGH SICP clock edge for a serial word will cause all timed outputs (D) to go LOW except for D_0 of the least significant device. The D outputs of the least significant device will go high on consecutive clock cycles until D_8. When D_8 goes HIGH, the SIX of the next device goes HIGH. On the next cycle after the SIX input is brought HIGH, the D0 goes HIGH; then on the next cycle D_1 and so on. A D_i output from the most significant device is issued to create the $\overline{W}$ for all cascaded devices.

The minimum serial word width is 4 bits and the maximum is virtually unlimited.

When in the Serial mode, the Least Significant Bit of a serial stream is shifted in first. If the FIFO output is in the Parallel mode, the first serial bit will come out on Q_0. The second bit shifted in is on Q_1 and so on.

In the Serial Cascade mode, the serial input (SI) pins must be connected together. Each of the devices then receives serial information together and uses the SIX and D_{0-8} lines to determine whether to store it or not.

The example shown in Figure 34 shows the interconnections for a serializing FIFO that transfers data to the internal RAM in 16-bit quantities (i.e. every 16 SICP cycles). This corresponds to incrementing the write pointer every 16 SICP cycles.

Once $\overline{W}$ goes HIGH With the last serial bit in, SICP should not be clocked again until $\overline{FF}$ goes HIGH.

SINGLE DEVICE SERIAL INPUT CONFIGURATION

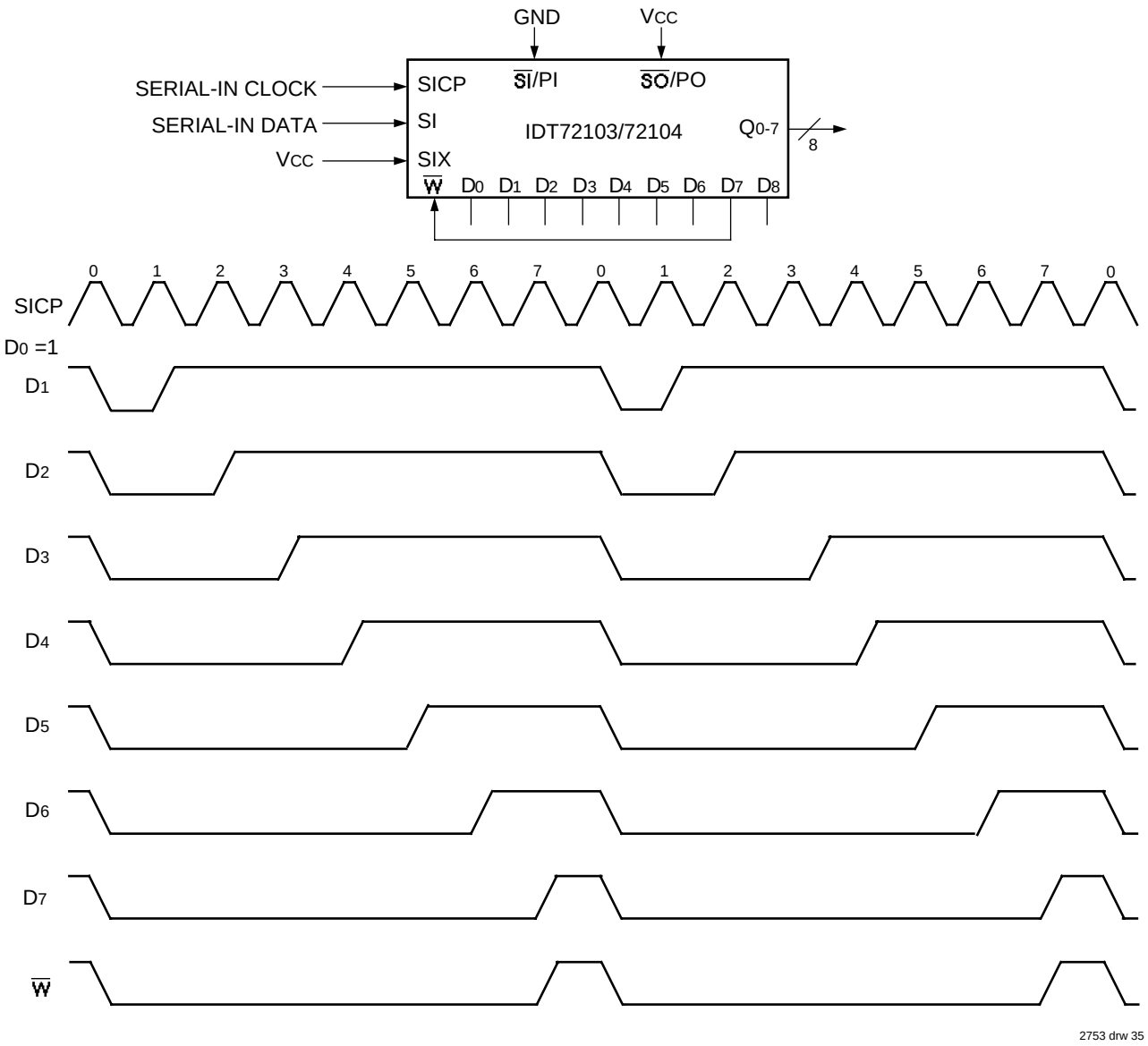


Figure 32. Serial-In Mode Where 8-Bit Parallel Output Data is Read

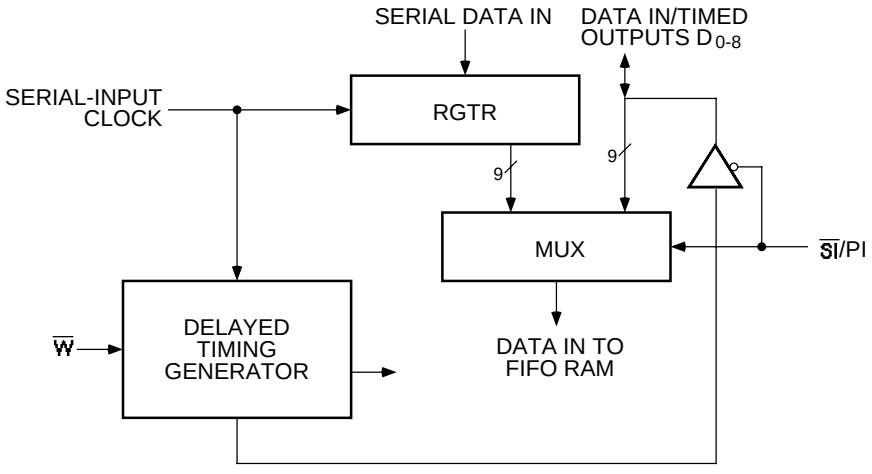


Figure 33. Serial-Input Circuitry

SERIAL INPUT WIDTH EXPANSION

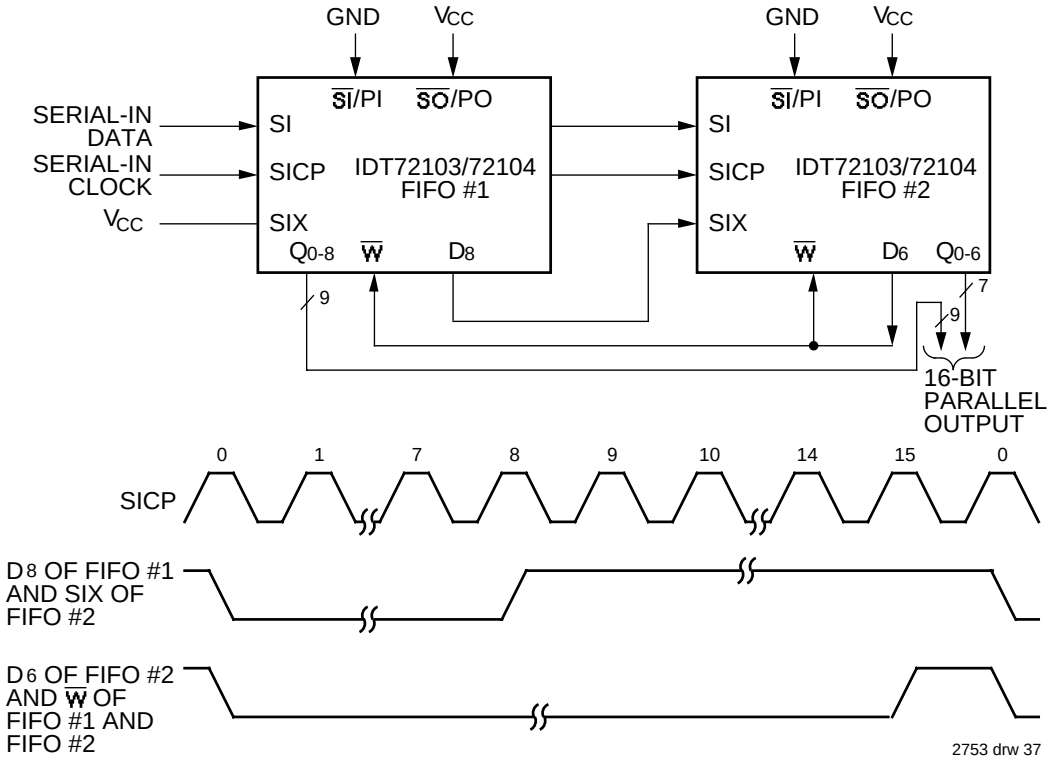
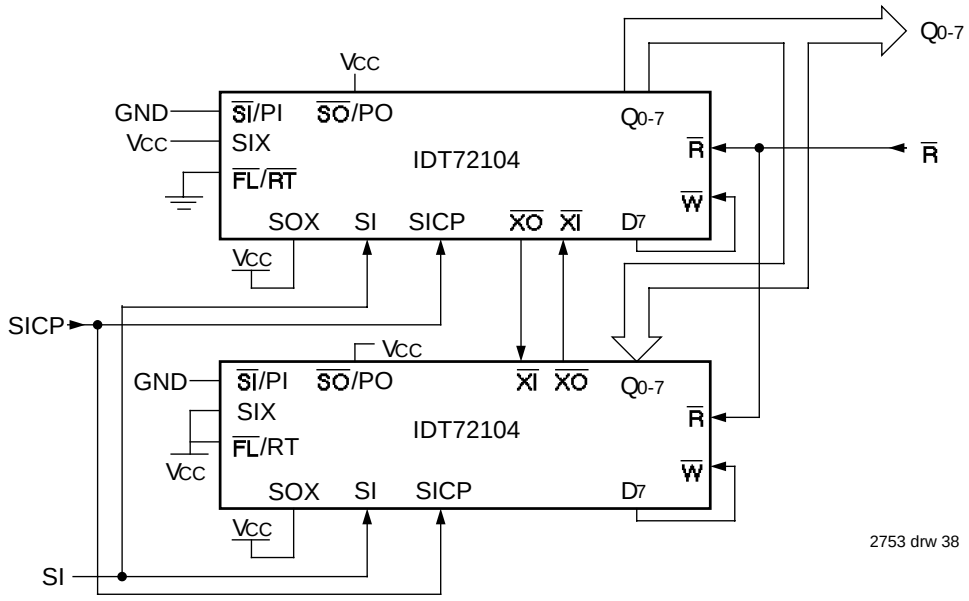


Figure 34. Serial-In Configuration for Serial-In to Parallel-Out Data of 16 bits

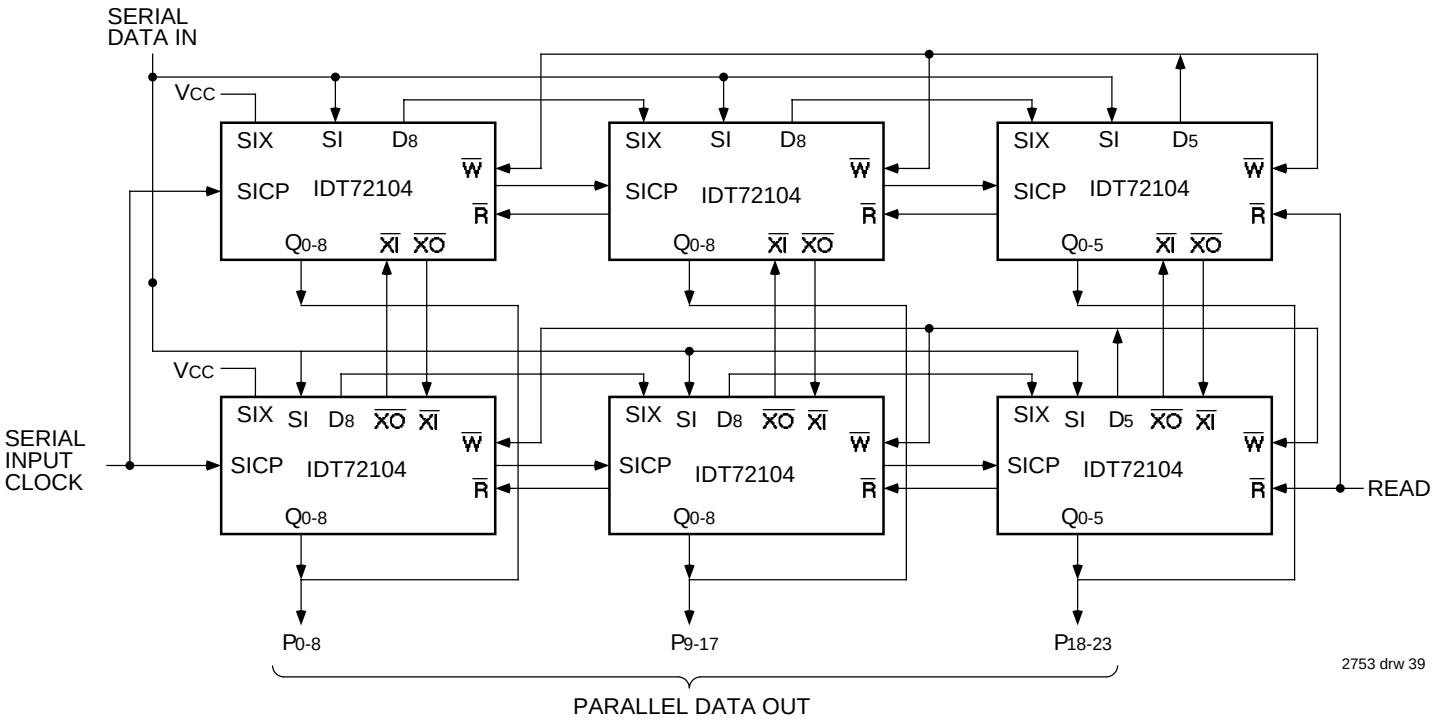
SERIAL INPUT WITH DEPTH EXPANSION



NOTE:
1. All SI/PI pins are tied to GND and SO/PO pins are tied to VCC. OE is tied LOW. For FF and EF connections see Figure 29.

Figure 35. An 8,192 x 8 Serial-In, Parallel-Out FIFO

SERIAL INPUT WITH WIDTH AND DEPTH EXPANSION



NOTE:
1. All $\overline{SI}$/PI pins are tied to GND. $\overline{SO}$/PO pins are tied to VCC. For $\overline{FL}/\overline{RT}$, $\overline{FF}$ and $\overline{EF}$ connections see Figure 29.

Figure 36. An 8,192 x 24 Serial-In, Parallel-Out FIFO Using Six IDT72104s

SERIAL DATA OUTPUT

The Serial Output mode is selected by setting the $\overline{SO}$/PO line LOW. When in the Serial-Out mode, one of the Q_{1-8} lines should be used to control the $\overline{R}$ signal. In the Serial-Out mode, the Q_{0-8} are taps off a digital delay line. By selecting one of these taps and connecting it to $\overline{R}$, the width of the serial word to be read and shifted is programmed. For instance, if the Q_5 line is connected to the $\overline{R}$ input, on every sixth clock cycle a new word is read from the FIFO RAM array and begins to be shifted out. The serial word is shifted out Least Significant Bit first. If the input mode of the FIFO is parallel, the information that was written into the D_0 bit will come out as the first bit of the serial word. The second bit of the serial stream will be the D_1 bit and so on.

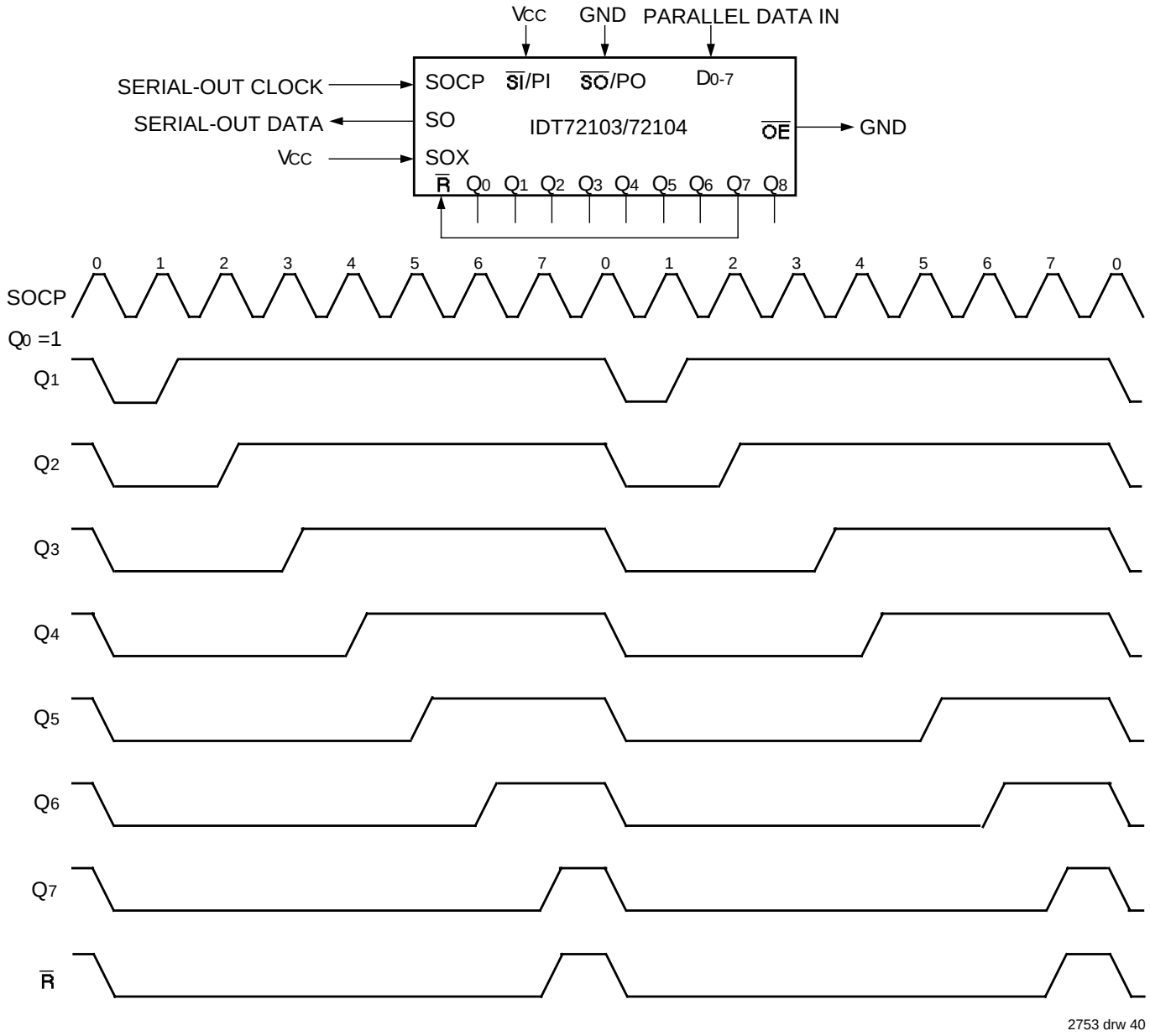
In the stand alone case, the SOX line is tied HIGH and not used. On the first LOW-to-HIGH of the SOCP clock, all of the Q outputs except for Q_0 go LOW and a new serial word is started. On the next clock cycle, Q_1 will go HIGH, Q_2 on the next clock cycle and so on, as shown in Figure 37. This continues until the Q line, which is connected to R, goes HIGH at which point all of the Q lines go LOW on the next clock and a new word is started.

In the cascaded case, word width of more than 9 bits can be achieved by using more than one device. By tying the SOX line of the least significant device HIGH and the SOX of the subsequent devices to Q_8 of the previous device, a cascaded serial word is achieved. On the first LOW-to-HIGH clock edge of SOCP, all the Q lines go low except for Q_0. Just as in the stand alone case, on each consecutive clock cycle, each Q line goes HIGH in the order of least to most significant. When Q_8 (which is connected to the SOX input of the next device) goes HIGH, the D_0 of that device goes HIGH, thus cascading from one device to the next. The Q line of the most significant device, which programs the serial word width, is connected to all R inputs.

The Serial Data Output (SO) of each device in the serial word must be tied together. Since the SO pin is tri-stated, only the device which is currently shifting out is enabled and driving the 1-bit bus.

Figure 39 shows an example of the interconnections for a 16-bit serialized FIFO.

Once $\overline{R}$ goes HIGH with the last serial bit out, SOCP should not be clocked again until EF goes HIGH.



NOTE:
1. Input data is loaded in 8-bit quantities and read out serially.

Figure 37. Serial-Out Configuration

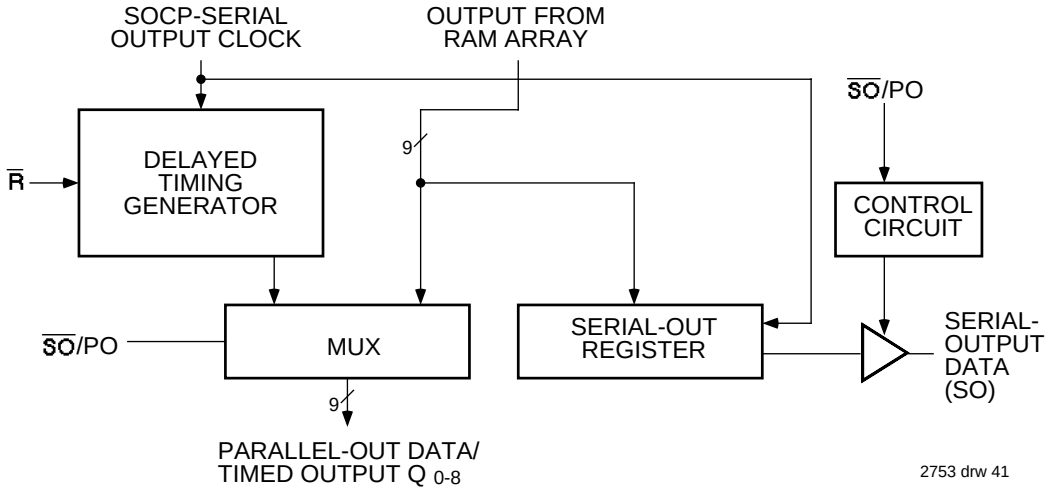
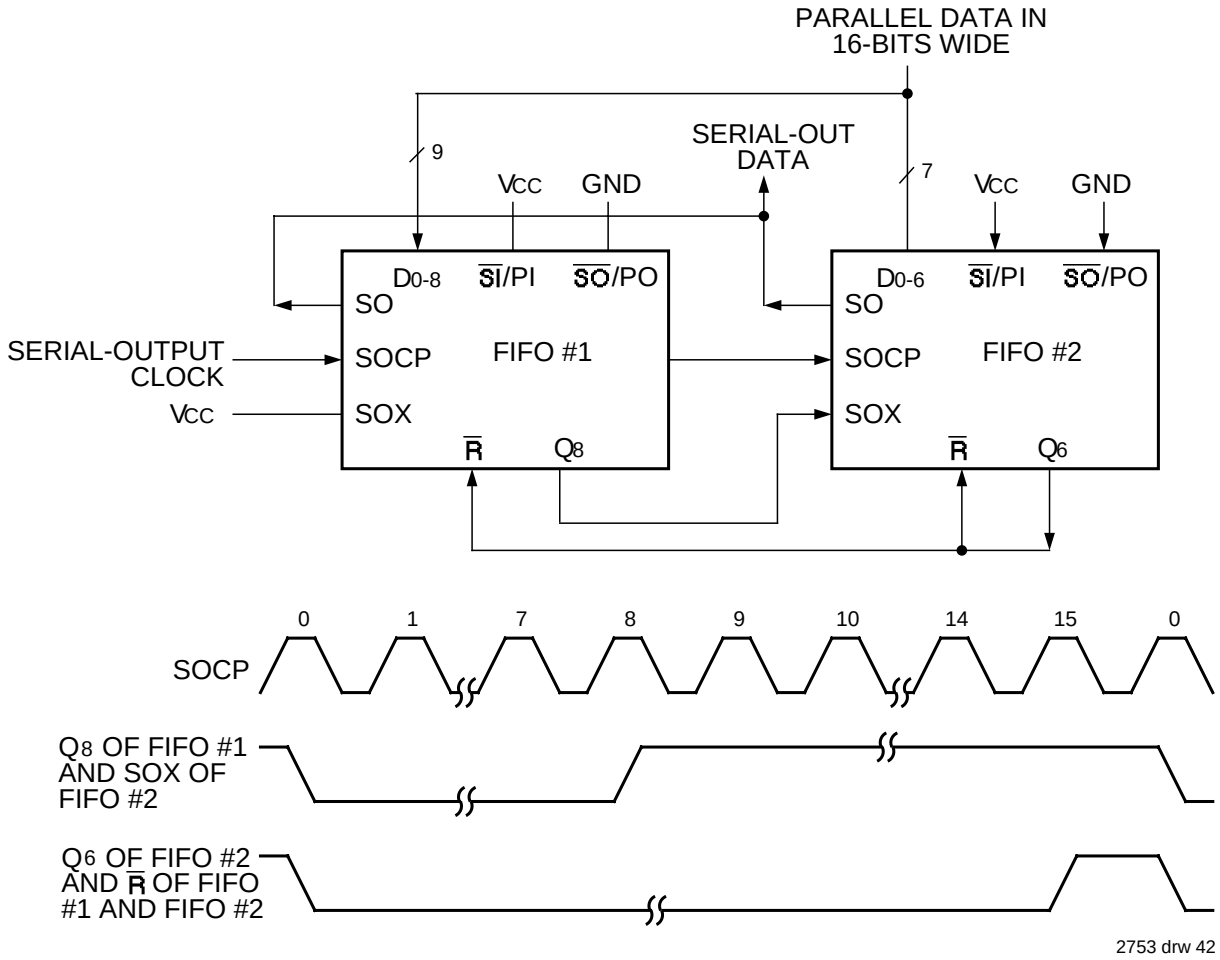


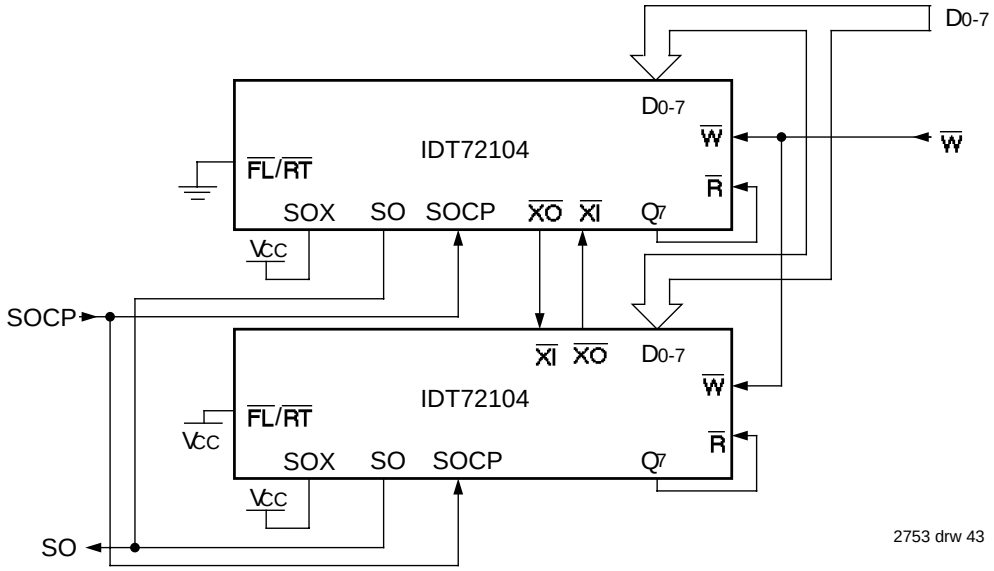
Figure 38. Serial-Output Circuitry



NOTE:
1. The parallel Data In is tied to D_{0-8} of FIFO #1 and D_{0-6} of FIFO #2.

Figure 39. Serial-Output for 16-Bit Parallel Data In

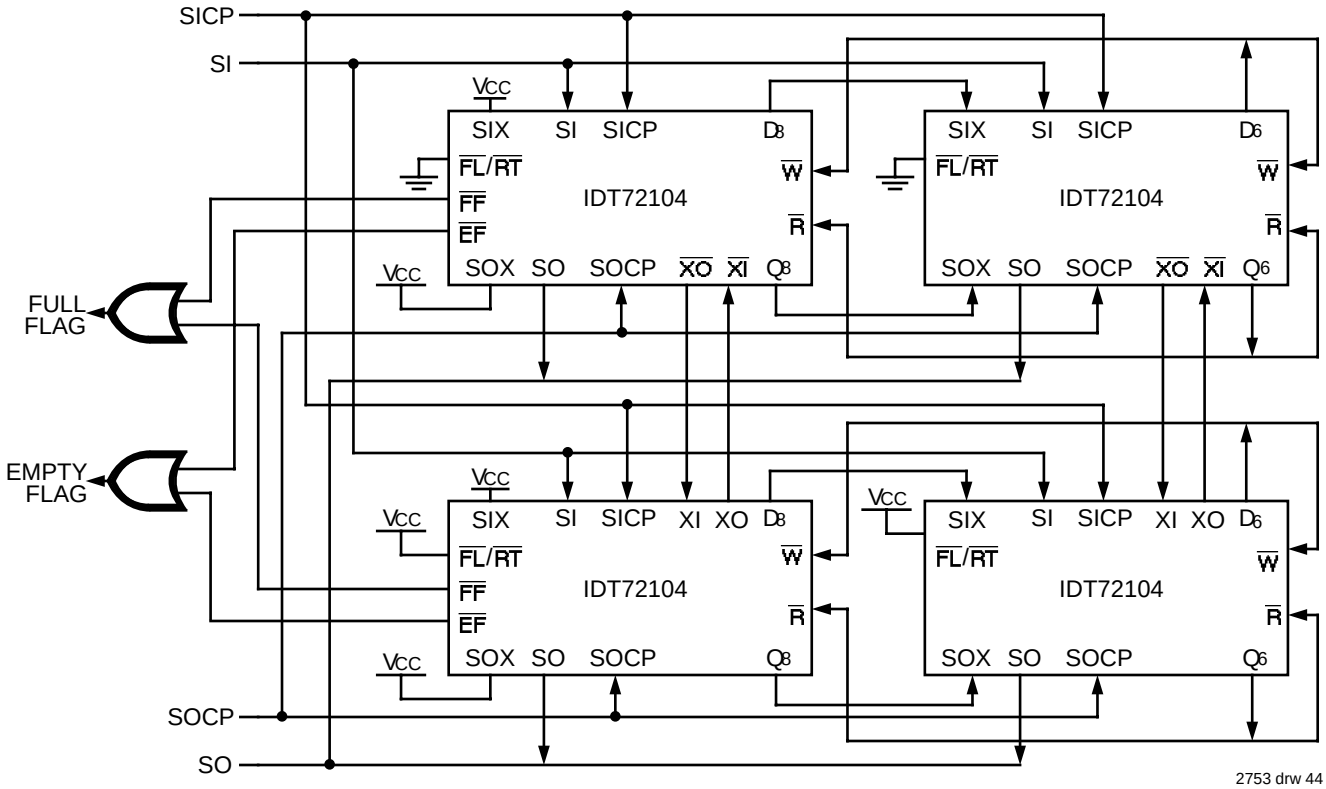
SERIAL OUTPUT WITH DEPTH EXPANSION



NOTE:
1. All SI/PI pins are tied to VCC and SO/PO pins are tied to GND. OE is tied LOW. For FF and EF connections see Figure 17.

Figure 40. An 8,192 x 8 Parallel-In Serial-Out FIFO

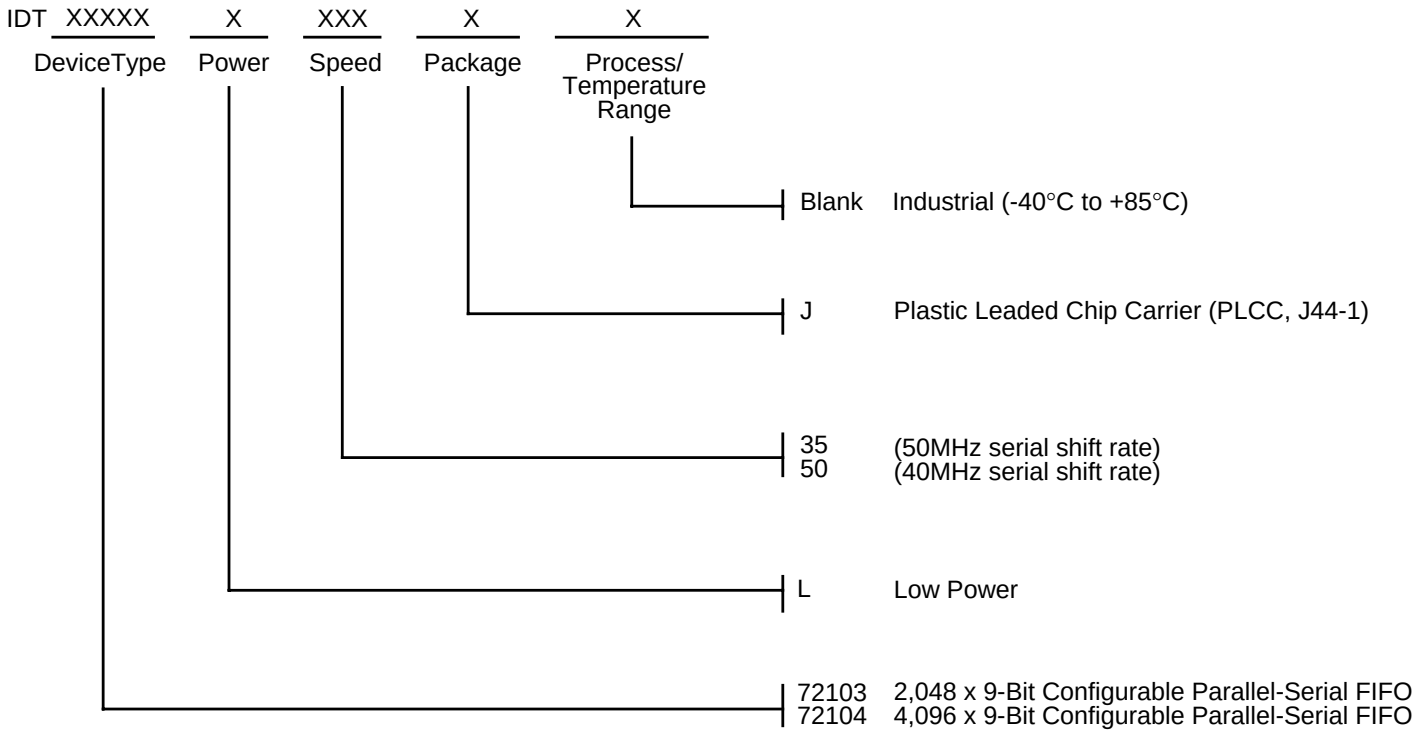
SERIAL IN AND SERIAL OUT WITH WIDTH AND DEPTH EXPANSION



NOTE:
1. All RS pins are connected together. All OE pins are connected LOW. All SI/PI and SO/PO pins are grounded.

Figure 41. 131,072 x 1 Serial-In Serial-Out FIFO

ORDERING INFORMATION



2753 drw 45