2.5V QUADMUX DDR FLOW-CONTROL DEVICE WITH MUX/DEMUX/BROADCAST FUNCTIONS
8,192 x 40 x 4
16,384 x 40 x 4
32,768 x 40 x 4

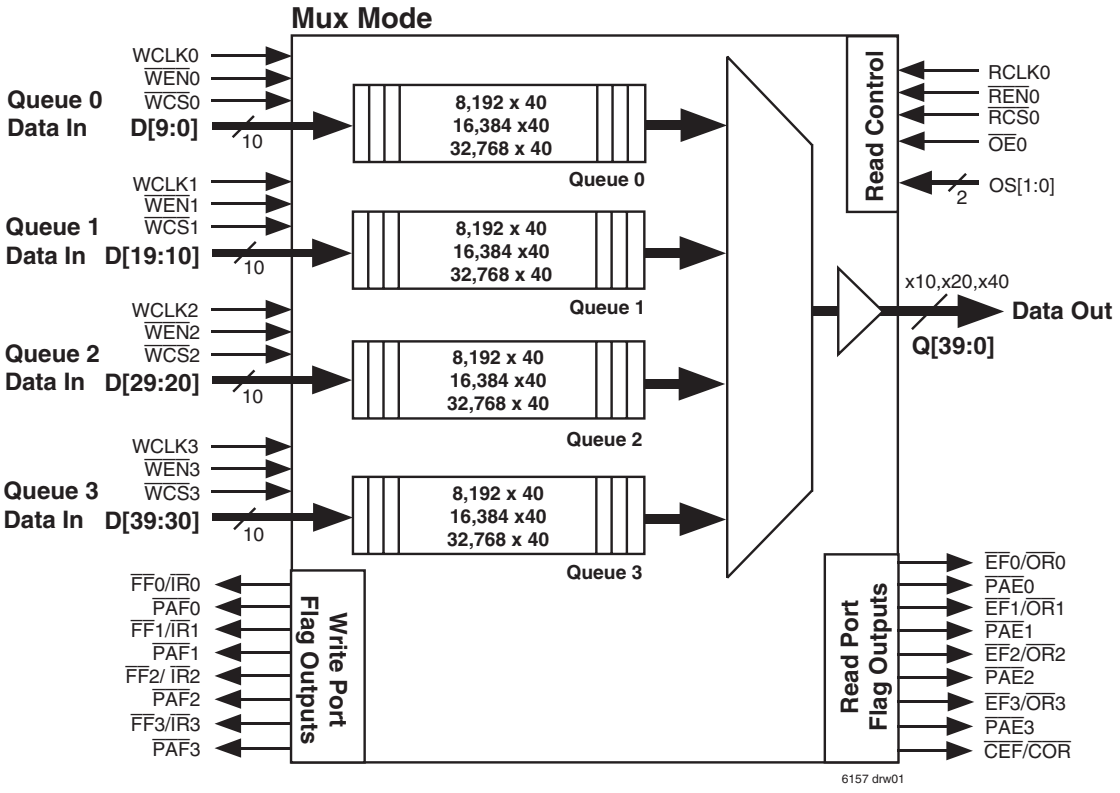
PRELIMINARY

IDT72T55248
IDT72T55258
IDT72T55268

FEATURES

- **Choose from among the following memory organizations:**
  IDT72T55248 - 8,192 words, 40-bits/word maximum, 4 Sequential Queues total
  IDT72T55258 - 16,384 words, 40-bits/word maximum, 4 Sequential Queues total
  IDT72T55268 - 32,768 words, 40-bits/word maximum, 4 Sequential Queues total
- **User Selectable Mux / Demux / Broadcast Write Modes**
- **Mux Mode offers 4:1 architecture**
  - *Five discrete clock domains, four write clocks and one read clock*
  - *Four separate write ports, writes data to four independent Queues*
  - *One single read port, capable of reading from any four Queues*
  - *Selectable single or double data rate (SDR/DDR) on read and write ports*
  - *10-bit wide write ports in single data rate, doubles internally in double data rate*
  - *40-bit wide read port, doubles internally in double data rate, selectable between the four independent Queues*
  - *Bus Matching on the Read Port x10/x20/x40 (SDR/DDR)*
  - *Fully independent status flags for every Queue*
  - *Composite Empty/Output Ready Flag monitors currently selected Queue*
  - *Dedicated partial reset for every Queue*
- **Demux Mode offers 1:4 architecture**
  - *Five discrete clock domains, one write clock and four read clocks*
  - *Four separate read ports, read data from four independent Queues*
  - *One single write port, capable of writing to any four Queues*
  - *Selectable single or double data rate on read and write ports*
  - *10-bit wide read ports in single data rate, doubles internally in double data rate*
  - *40-bit wide write port, doubles internally in double data rate, selectable between the four independent Queues*
  - *Bus Matching on the Write Port x10/x20/x40 (SDR/DDR)*
  - *Fully independent status flags for every Queue*
  - *Composite Full/Input Ready Flag monitors currently selected Queue*
  - *Dedicated partial reset for every Queue*
- **Broadcast Write Mode offers, 1:4 architecture (with simultaneous writes to all Queues)**
  - *Five discrete clock domains, one write clock and four read clocks*
  - *Four separate read ports, read data from four independent Queues*
  - *One single write port, writes to all four independent Queues simultaneously*
  - *10-bit wide read ports in single data rate, doubles internally in double data rate*
  - *40-bit wide write port, doubles internally in double data rate*
  - *Selectable single or double data rate on read and write ports*
  - *Bus-Matching on the write port x10/x20/x40 (SDR/DDR)*

FUNCTIONAL BLOCK DIAGRAMS

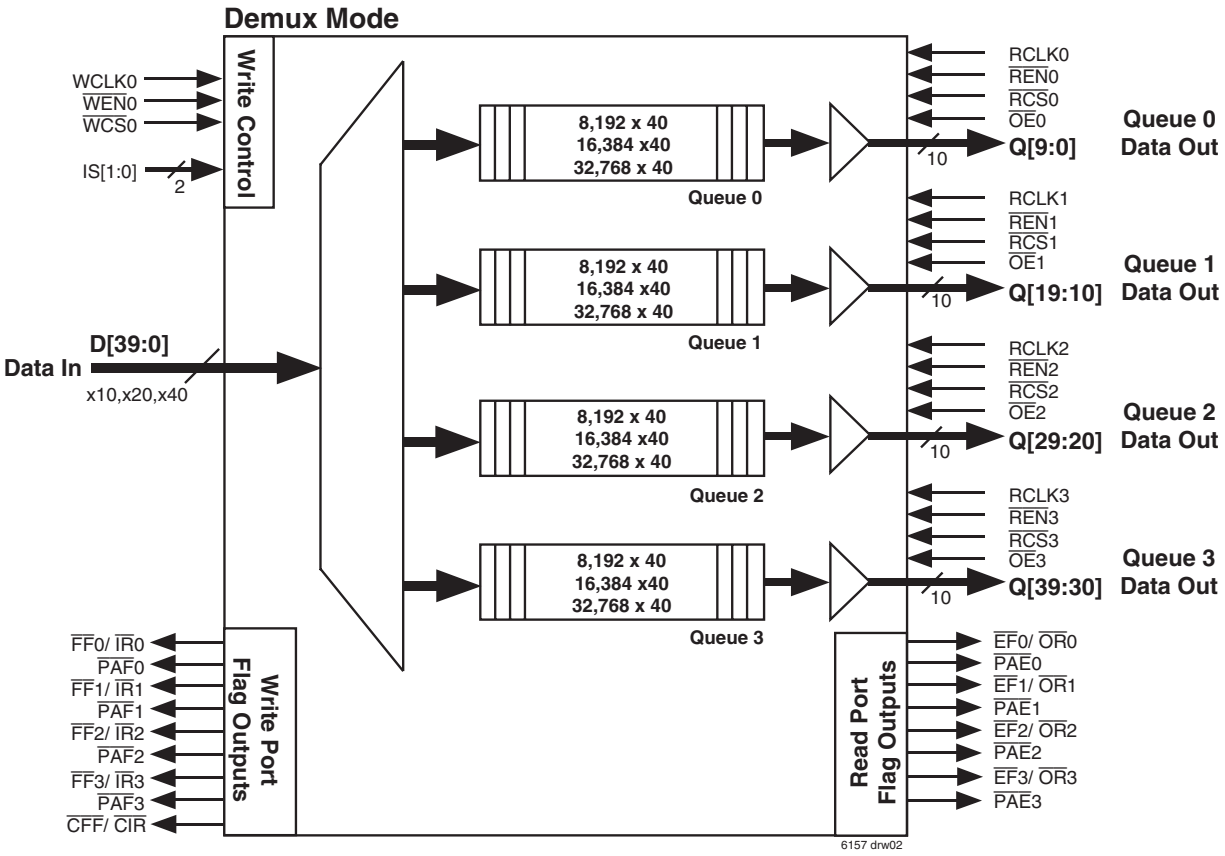


(See next page for Demux and Broadcast modes)

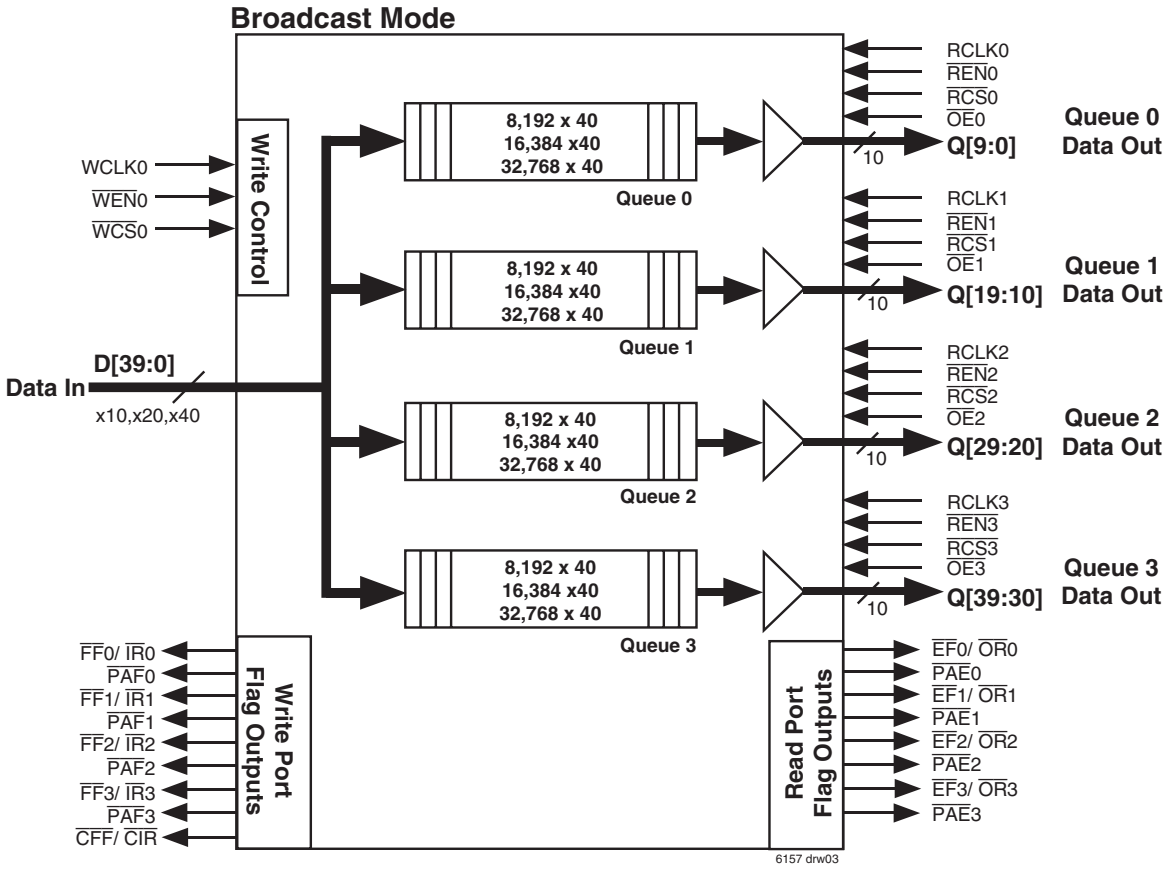
FEATURES (CONTINUED)

- *Fully independent status flags for every Queue*
- *Composite Full/Input Ready Flag monitors currently selected Queue*
- *Dedicated partial reset for every Queue*
- Up to 200MHz operating frequency, 8Gbps (SDR) and 16Gbps (DDR)
- User selectable Single Data Rate (SDR) or Double Data Rate (DDR) modes on both the write port(s) and read port(s)
- All I/O are LVTTL/ HSTL/ eHSTL user selectable
- 3.3V tolerant inputs in LVTTL mode
- ERCLK and $\overline{\text{EREN}}$ Echo outputs on all read ports
- Write Chip Select $\overline{\text{WCS}}$ input for each write port
- Read Chip Select $\overline{\text{RCS}}$ input for each read port
- User Selectable IDT Standard mode (using $\overline{\text{EF}}$ and $\overline{\text{FF}}$ flags) or FWFT mode (using $\overline{\text{IR}}$ and $\overline{\text{OR}}$ flags)
- Composite Full/ Input Ready Flag in Demux and Broadcast mode
- Composite Empty/ Output Ready flag in Mux mode
- Independent Programmable Almost Empty and Almost Full flags per Queue
- Dedicated Serial Port for flag programming
- Dedicated Partial Reset for each individual Queue
- Power Down pin minimizes power consumption
- 2.5V Supply Voltage
- Available in a 324-pin Plastic Ball Grid Array (PBGA) 19mm x 19mm, 1mm Pitch
- IEEE 1149.1 compliant JTAG port provides boundary scan function, or flag programming
- Low Power, High Performance CMOS technology
- Industrial temperature range (-40°C to +85°C)

FUNCTIONAL BLOCK DIAGRAMS (CONTINUED)



FUNCTIONAL BLOCK DIAGRAMS (CONTINUED)



DESCRIPTION

The IDT72T55248/72T55258/72T55268 QuadMux flow-control devices are ideal for many applications where data stream convergence and parallel buffering of multiple data paths are required. These applications may include communication and networking systems such as terabit routers, quality of service (QOS) and packet prioritization routing systems, data bandwidth aggregation, data acquisition systems, WCDMA baseband systems, and medical equipments. The QuadMux replaces traditional methods of muxing multiple data paths at different data rates, in essence reducing external glue logic. The QuadMux offers three modes of operation, Mux, Demux and Broadcast. Regardless of the mode of operation there are four internal Sequential Queues built using IDT FIFO technology and five discrete clock domains. All four Queues have the same density, and the read and write ports can operate independently in Single Data Rate (SDR) or Double Data Rate (DDR). See Figure 1, *QuadMux Block Diagram* or an outline of the functional blocks within the device.

The QuadMux device is capable of up to 200MHz operation of all five clock inputs, all clocks being totally independent of each other. Along with this high speed of operation the input and output ports are independently selectable between Single Data Rate, SDR mode, and Double Data Rate, DDR mode. If Double Data Rate mode is selected data can be written into or read out of a Queue on every rising and falling edge of the respective clock. For example, if the write clock is running at 200MHz and the write port(s) is/are setup for DDR mode, a data input pin has a bandwidth of 400Mbps. So for a 40-bit wide bus a total bandwidth of 16Gbps can be achieved.

In Mux mode operation a 4:1 architecture is setup, (four input ports to one output port). Here there are four internal Sequential Queues each with a dedicated write port. Data can be written into each of the dedicated write ports totally independent of any other port, each port has its own write clock input and control enables. There is a single read port that can access any one of the four Queues. Data is read out of a specific Queue based on the address present on the output select pins. Only one Queue can be selected and read from at a time. All input ports are 10 bits wide and the output port has a selectable Bus Matching x10, x20 or x40 bus widths. A full set of flag outputs per Queue are available in this mode providing the user with continuous status of each individual Queue levels.

In Demux mode operation a 1:4 architecture is setup, (one input port to four output ports). Here there is a single write port that can write data into any one of four internal Queues. Data is written into a specific Queue based on the address present on the input select pins. Only one Queue can be selected and written into at a time. There are four dedicated read ports, one port for each Queue. Data can be read out of the four Queues through the read port totally independent of any other port. Each port has its own read clock input and control enables. The input port has a selectable Bus Matching x10, x20 or x40 bus width and all the output ports are 10-bits. A full set of flag outputs per Queue are available in this mode providing the user with continuous status of each individual Queue levels.

In the Broadcast Write mode the architecture is similar to the Demux mode, 1:4 (one input port to four output ports). However, there is no Queue select operation in Broadcast mode. Instead data written into the write port is written to all four internal Queues simultaneously. Again there are four independent read ports, one port per Queue. In Broadcast mode write operations to all Queues will be prevented when any one or more of the four Queues are full or being partially reset. A full set of flag outputs is available in this mode providing the user with continuous status of each individual Queue levels.

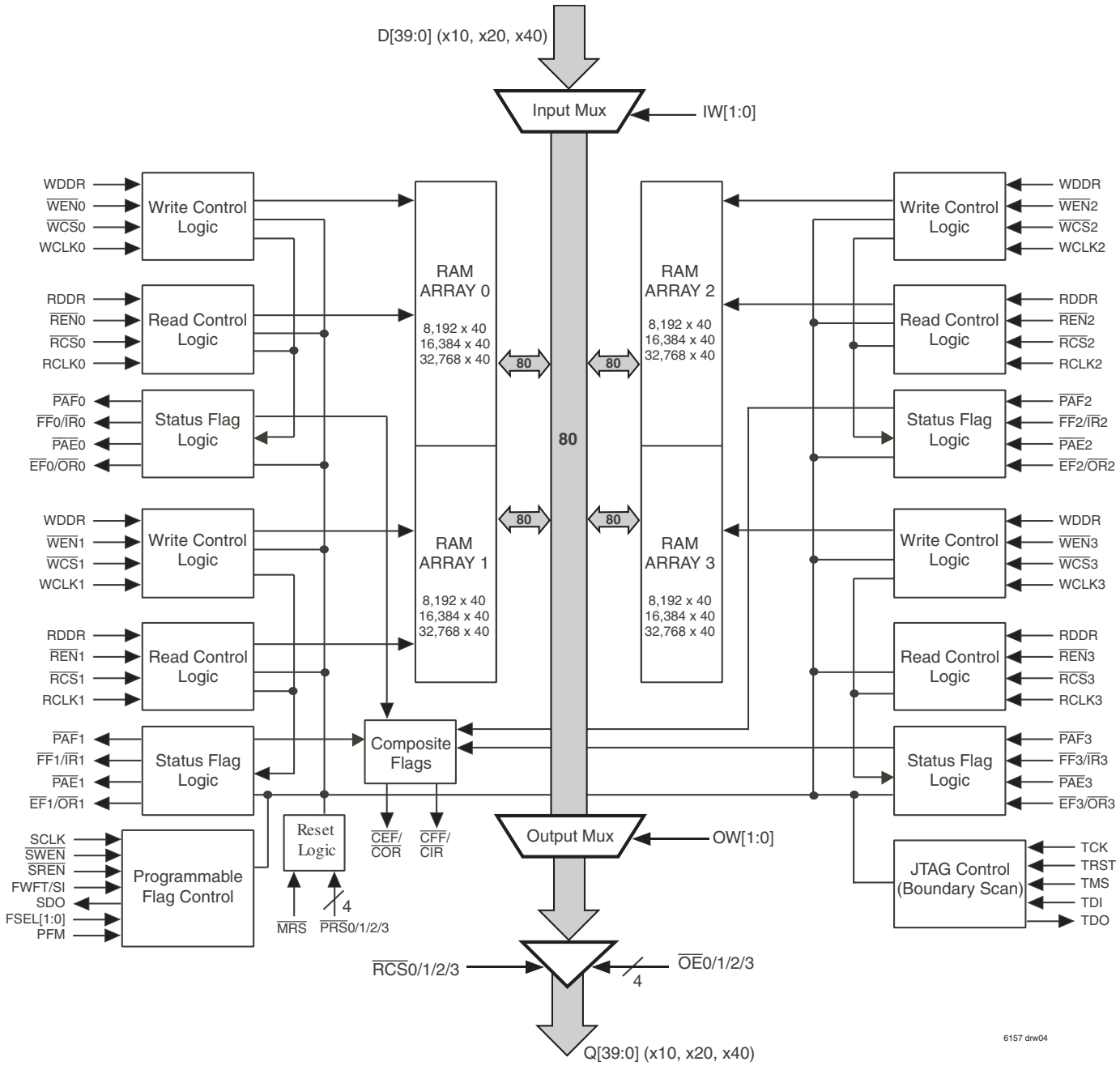
As is typical with most IDT Queues, two types of data timing modes are available, IDT Standard mode and First Word Fall Through (FWFT) mode. This affects the device's operation and also the flag outputs. The device provides four flag outputs, for each internal Queue. The device also provides composite flags that represent the full and empty status of the currently selected Queue.

All read ports provide the user with a dedicated Echo Read Enable, $\overline{EREN}$ and an Echo Read Clock, ERCLK output. These outputs aid in high-speed applications where synchronization of the input clock and data of a receiving device is critical. Otherwise known as "Source Synchronous clocking" the echo outputs provide tighter synchronization of the data transmitted from the Queue to the read clock interfacing the Queue outputs.

A master reset input is provided and all setup and configuration pins are latched with respect to a Master Reset. A Partial Reset is provided for each internal Queue. When a Partial Reset is performed on a Queue the read and write pointers of that Queue only are reset to the first memory location. The flag offset values, timing modes, and initial configurations are retained.

The QuadMux device has the capability of operating its I/Os at either 2.5V LVTTL, 1.5V HSTL or 1.8V eHSTL levels. A Voltage Reference, V_{REF} input is provided for HSTL and eHSTL interfaces. The type of I/O is selected by the IOSEL pin. There are certain inputs that are CMOS based and must be tied to either V_{CC} or GND. The core supply voltage of the device, V_{CC} is always 2.5V, however the output pins have a separate supply, V_{DDQ} which can be 2.5V, 1.8V or 1.5V. The device also offers significant power savings, achieved through the use of the Power Down input, $\overline{PD}$ in HSTL/eHSTL mode.

A JTAG test port is provided on the QuadMux device. The Boundary Scan is fully compliant with IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture. The JTAG port can also be used to program the flag offsets.

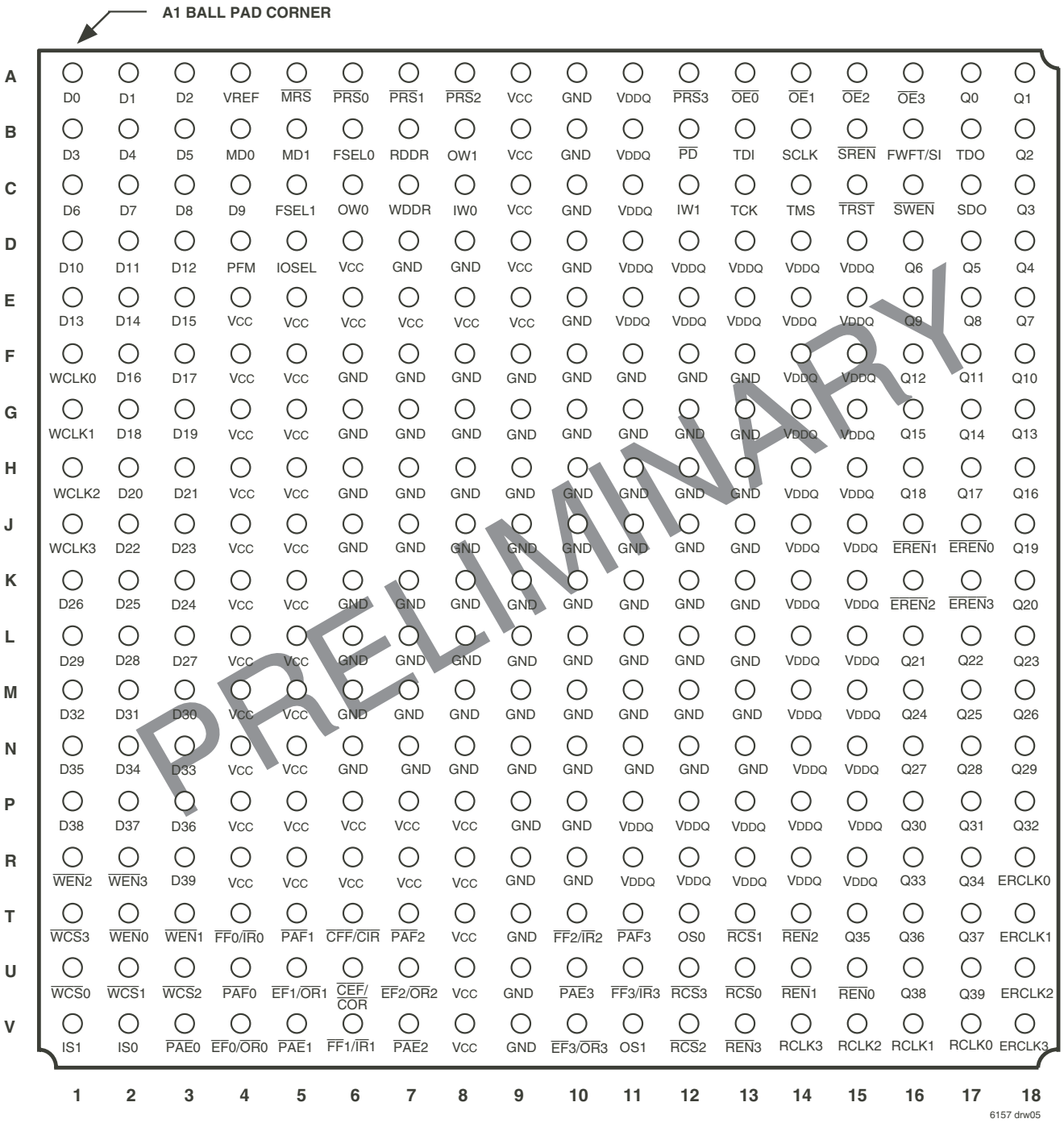


NOTES:

1. This block diagram only shows the architecture for Queue 0. There are a total of four Queues inside this device all with the identical architecture.
2. *Denotes dedicated signal for each internal Queue inside the device.

Figure 1. QuadMux Block Diagram

PIN CONFIGURATION



PBGA (BB324-1, order code: BB)
TOP VIEW

PIN DESCRIPTIONS

Symbol & Pin No.	Name	I/O TYPE	Description
$\overline{CEF}/\overline{COR}$ (U6)	Composite Empty/ Composite Output Ready Flag	HSTL-LVTTL OUTPUT(2)	If Mux mode is selected this flag will represent the exact status of the current Queue being read without the user having to observe the empty flag corresponding to the current Queue. If Demux or Broadcast mode is selected this output is not used and can be left floating.
$\overline{CFF}/\overline{CIR}$ (T6)	Composite Full/ Composite Input Ready flag	HSTL-LVTTL OUTPUT(2)	If Mux mode is selected this output is not used and can be left floating. If Demux mode is selected this flag will represent the exact status of the current Queue being written without the user having to observe the full flag corresponding to the current Queue. If Broadcast mode is selected this flag goes active when any one of the four Queues goes full and inactive when all four Queues are not full.
D[39:0] (See Pin No. table for details)	Data Input Bus	HSTL-LVTTL INPUT	These are the data inputs for the device. Data is written into the part using the respective write port clock(s) and enable(s). If Demux or Broadcast mode is selected this is a single data input bus providing Bus-Matching of x10, x20 or x40 bits. If Mux mode is selected these inputs become four separate busses to the four separate Queues. D[9:0] is Queue[0], D[19:10] is Queue[1], D[29:20] is Queue[2], D[39:30] is Queue[3]. Any unused inputs should be tied to GND. Note the inputs are 3.3V tolerant in LVTTL mode.
$\overline{EF}$0/1/2/3/- $\overline{OR}$0/1/2/3 (See Pin No. table for details)	Empty Flags 0/1/2/3 or Output Ready Flags 0/1/2/3	HSTL-LVTTL OUTPUT(2)	This is the Empty Flag (Standard IDT mode) or Output Ready Flag (FWFT mode) corresponding to each of the four Queues on the read port. $\overline{EF}$ indicates whether or not the Queue is empty. $\overline{OR}$ indicates whether or not there is valid data available at the outputs. These flags always represent the status of the corresponding Queue at all times in every mode.
ERCLK0 (R18)	Echo Read Clock 0	HSTL-LVTTL OUTPUT(2)	If Mux mode is selected this is the only echo clock output available for the read port. If Demux or Broadcast mode is selected this is the echo read clock output for Queue 0. Echo read clock always follows RCLK0 with an associated delay.
ERCLK1/2/3 (ERCLK1-T18 ERCLK2-U18 ERCLK3-V18)	Echo Read Clock 1/2/3	HSTL-LVTTL OUTPUT(2)	If Mux mode is selected these clock outputs are inactive and can be left floating. If Demux or Broadcast mode is selected these are the echo read clock outputs for Queues 1, 2, and 3 respectively. ERCLK1, ERCLK2 and ERCLK3 always follow RCLK1, RCLK2 and RCLK3 respectively.
$\overline{EREN}$0 (J17)	Echo Read Enable 0	HSTL-LVTTL OUTPUT(2)	If Mux mode is selected this is the echo read enable output for the read port. If Demux or Broadcast mode is selected this is the echo read enable input for Queue 0. Echo Read Enable is synchronous to the RCLK input and is active when a read operation has occurred and a new word has been placed onto the data output bus.
$\overline{EREN}$1/2/3 ($\overline{EREN}$1-J16 $\overline{EREN}$2-K16 $\overline{EREN}$3-K17)	Echo Read Enable 1/2/3	HSTL-LVTTL OUTPUT(2)	If Mux mode is selected these outputs are inactive and can be left floating. If Demux or Broadcast mode is selected these are the echo read enable outputs for Queues 1, 2 and 3 respectively. Echo Read Enable is synchronous to the RCLK input and is active when a read operation has occurred and a new word has been placed onto the data output bus.
$\overline{FF}$0/1/2/3- $\overline{IR}$0/1/2/3 (See Pin table)	Full Flags 0/1/2/3 or Input Ready Flags 0/1/2/3	HSTL-LVTTL OUTPUT(2)	This is the Full Flag (Standard IDT mode) or Input Ready Flag (FWFT mode) corresponding to each of the four Queues on the write port. $\overline{FF}$ indicates whether or not the Queue is full. $\overline{IR}$ indicates whether or not there is valid space for writing data onto the Queue.
FSEL [1:0] (FSEL1-C5 FSEL0-B6)	Flag Select	HSTL-LVTTL INPUT	During master reset, the FSEL pins are used to select one of four default $\overline{PAE}$ and $\overline{PAF}$ offsets. All four internal Queues are programmed to the same $\overline{PAE}/\overline{PAF}$ offset value. Values are: 00 = 7; 01 = 63; 10 = 127; 11 = 1023
FWFT/SI (B16)	First Word Fall Through/ Serial Input	HSTL-LVTTL INPUT	During master reset, FWFT is HIGH then the First Word Fall Through mode is selected. If FWFT is LOW the IDT Standard mode is selected. After master reset this pin is used for the serial data input for the programming of the $\overline{PAE}$ and $\overline{PAF}$ flags offset registers.
IOSEL (D5)	I/O Select	CMOS(1) INPUT	This input determines whether the inputs will operate in LVTTL or HSTL/eHSTL mode. If IOSEL pin is HIGH, then all inputs and outputs that are designated "LVTTL or HSTL" in this section will be set to LVTTL format. If IOSEL is LOW then HSTL/eHSTL format is selected. This signal must be tied to either V_{CC} or GND for proper operation.
IS[1:0] (IS1-V1 IS0-V2)	Input Select	HSTL-LVTTL INPUT	If Mux or Broadcast mode is selected these inputs are not used and should be tied to GND. If Demux mode is selected these inputs select one of the four Queues to be written into on the write port. The address on the input select pins is setup with respect to the rising edge of WCLK0.

PIN DESCRIPTIONS (CONTINUED)

Symbol & Pin No.	Name	I/O TYPE	Description
IW[1:0] (IW1-C12 IW0-C8)	Input Width	CMOS[1] INPUT	In Demux or Broadcast, these pins are used during master reset to select the input bus size for the device. The values are: 00 = x10; 01 = x20; 10 = x40. 11 = Restricted. In Mux mode these pins must be tied to GND.
MD[1:0] (MD1-B5 MD0-B4)	Mode Pin	CMOS[1] INPUT	This mode selection pin used during Master Reset to select the mode of the Queue. The values are: 00 = Demux; 10 = Mux; 01 = Broadcast Write; 11 = Restricted.
$\overline{MRS}$ (A5)	Master Reset	HSTL-LVTTL INPUT	This input provides a full device reset. All set-up pins are sampled based on a master reset operation. Read and write pointers will be reset to the first location memory. All flag offsets are cleared and reset to default values determined by FSEL[1:0].
$\overline{OE}$0 (A13)	Output Enable 0	HSTL-LVTTL INPUT	If Mux mode is selected this is the Output Enable for the read port. All data output pins will be placed into High Impedance if this pin is HIGH. If Demux or Broadcast mode is selected this is the output enable pin for Queue 0. All data output pins of Queue 0 will be placed into High Impedance if this pin is HIGH. This input is asynchronous.
$\overline{OE}$1-(A14) $\overline{OE}$2-(A15) $\overline{OE}$3-(A16)	Output Enable 1/2/3	HSTL-LVTTL INPUT	If Mux mode is selected these inputs are ignored and can be tied HIGH. If Demux or Broadcast mode is selected these are the output enable pins Queues 1, 2 and 3 respectively. All data outputs on Queue 1, Queue 2 and Queue 3 will be in High-Impedance if the respective output enable pin is High. These inputs are asynchronous.
OS[1:0] (OS1-V11 OS0-T12)	Output Select	HSTL-LVTTL INPUT	If Mux mode is selected these inputs select one of the four Queues to be read from on the read port. The address on the output select pins is setup with respect to the rising edge of RCLK0. If Demux or Broadcast mode is selected these inputs are not used and should be tied to GND.
OW[1:0] (OW1-B8 OW0-C6)	Output Width	HSTL-LVTTL INPUT	If Mux mode is selected, this pin is used during master reset to select the output word width bus size for the device. The values are: 00 = x10; 01 = x20; 10 = x40; 11 = Restricted. If Demux or Broadcast mode is selected the output word width will be x10. These pins are not used and must be tied to GND.
$\overline{PAE}$0-(V3) $\overline{PAE}$1-(V5) $\overline{PAE}$2-(V7) $\overline{PAE}$3-(U10)	Programmable Almost Empty Flag 0/1/2/3	HSTL-LVTTL OUTPUT[2]	This is the programmable almost empty flag that can be used to pre-indicate the empty boundary of each Queue. The $\overline{PAE}$ flags can be set to one of four default offsets determined by the state of FSEL0 and FSEL1 during master reset. The $\overline{PAE}$ offset values can also be written and read from serially by either the JTAG port or the serial programming pins (SCLK, FWFT/SI, SDO, $\overline{SWEN}$, $\overline{SREN}$). This flag can operate in synchronous or asynchronous mode depending on the state of the PFM pin during master reset.
$\overline{PAF}$0-(U4) $\overline{PAF}$1-(T5) $\overline{PAF}$2-(T7) $\overline{PAF}$3-(T11)	Programmable Almost Full Flag 0/1/2/3	HSTL-LVTTL OUTPUT[2]	This is the programmable almost full flag that can be used to pre-indicate the full boundary of each Queue. The $\overline{PAF}$ flags can be set to one of four default offsets determined by the state of FSEL0 and FSEL1 during master reset. The $\overline{PAF}$ offset values can also be written and read from serially by either the JTAG port or the serial programming pins (SCLK, FWFT/SI, SDO, $\overline{SWEN}$, $\overline{SREN}$). This flag can operate in synchronous or asynchronous mode depending on the state of the PFM pin during master reset.
$\overline{PD}$ (B12)	Power Down	HSTL-LVTTL INPUT	This input provides considerable power saving in HSTL/eHSTL mode. If this pin is low, the input level translators for all the data input pins, clocks and non-essential control pins are turned off. When $\overline{PD}$ is brought high, power-up sequence timing will have to be followed to before the inputs will be recognized. It is essential that the user respect these conditions when powering down the part and powering up the part, so as to not produce runt pulses or glitches on the clocks if the clocks are free running. $\overline{PD}$ does not provide any power consumption savings when the inputs are configured for LVTTL
PFM (D4)	Programmable Flag Mode	CMOS[1] INPUT	During master reset, a HIGH on PFM selects synchronous $\overline{PAE}$/$\overline{PAF}$ flag timing, a Low during master reset selects asynchronous $\overline{PAE}$/$\overline{PAF}$ flag timing. This pin controls all $\overline{PAE}$/$\overline{PAF}$ flag outputs.
$\overline{PRS}$0-(A6) $\overline{PRS}$1-(A7) $\overline{PRS}$2-(A8) $\overline{PRS}$3-(A12)	Partial Reset 0/1/2/3	HSTL-LVTTL	These are the partial reset inputs for each internal Queue. The read, write, flag pointers, and output registers will all be set to zero when partial reset is activated. During partial reset, the existing mode (IDT or FWFT), input/output bus width and rate mode, and the programmable flag settings are all retained.

PIN DESCRIPTIONS (CONTINUED)

Symbol & Pin No.	Name	I/O TYPE	Description
Q[39:0] See Pin No. table for details)	Data Output Bus	HSTL-LVTTL OUTPUT(2)	These are the data outputs for the device. Data is read from the part using the respective read port clock(s) and enable(s). If Mux mode is selected this is a single data output bus providing Bus-Matching of x10, x20 or x40 bits. If Demux or Broadcast mode is selected these outputs become four separate busses from the four separate Queues. Q[9:0] is Queue[0], Q[19:10] is Queue[1], Q[29:20] is Queue[2], Q[39:30] is Queue[3]. Any unused outputs should be left floating. Note, that the outputs are NOT 3.3V tolerant.
RCLK0 (V17)	Read Clock 0	HSTL-LVTTL INPUT	If Mux mode is selected this is the clock input for the read port. All read port operations will be synchronous to this clock input. If Demux or Broadcast mode is selected this is the read clock input for Queue 0. All read port operations on Queue 0 will be synchronous to this clock input.
RCLK1-(V16) RCLK2-(V15) RCLK3-(V14)	Read Clock 1/2/3	HSTL-LVTTL INPUT	If Mux mode is selected these clock inputs are ignored and if unused can be tied to GND. If Demux or Broadcast mode is selected these are the read clock inputs for Queues 1, 2, and 3 respectively. All read port operations on Queue 1, Queue 2 and Queue 3 will be synchronous to clock inputs RCLK1, RCLK2 and RCLK3 respectively.
$\overline{RCS}$0 (U13)	Read Chip Select 0	HSTL-LVTTL INPUT	If Mux mode is selected this is the read chip select input for the read port. All read operations will occur synchronous to the RCLK0 input provided that $\overline{REN}$0 and $\overline{RCS}$0 are LOW. If Demux or Broadcast mode is selected this is the read chip select input for Queue 0. All read operations on Queue 0 will occur synchronous to the RCLK0 input provided that $\overline{REN}$0 and $\overline{RCS}$0 are LOW.
$\overline{RCS}$1-(T13) $\overline{RCS}$2-(V12) $\overline{RCS}$3-(U12)	Read Chip Select 1/2/3	HSTL-LVTTL INPUT	If Mux mode is selected these inputs are ignored and can be tied HIGH. If Demux or Broadcast mode is selected these are the read chip select inputs for Queues 1, 2 and 3 respectively. All read operations on Queue 1, Queue 2 and Queue 3 will occur synchronous to the RCLK1, 2 and 3 input respectively, provided that the corresponding read enable and read chip select inputs are LOW.
RDDR (B7)	Read Port DDR	CMOS(1) INPUT	During master reset, this pin selects the output port to operate in DDR or SDR format. If RDDR is HIGH, then a word is read on the rising and falling edge of the appropriate RCLK0, 1, 2 and 3 input. If RDDR is LOW, then a word is read only on the rising edge of the appropriate RCLK0, 1, 2 and 3 inputs.
$\overline{REN}$0 (U15)	Read Enable 0	HSTL-LVTTL INPUT	If Mux mode is selected this is the read enable input for the read port. All read operations will occur synchronous to the RCLK0 clock input provided that $\overline{REN}$0 and $\overline{RCS}$0 are LOW. If Demux or Broadcast mode is selected this is the read enable input for Queue 0. All read operations on Queue 0 will occur synchronous to the RCLK0 input provided that $\overline{REN}$0 and $\overline{RCS}$0 are LOW.
$\overline{REN}$1-(U14) $\overline{REN}$2-(T14) $\overline{REN}$3-(V13)	Read Enable 1/2/3	HSTL-LVTTL INPUT	If Mux mode is selected these inputs are ignored and can be tied HIGH. If Demux or Broadcast mode is selected these are the read enable inputs for Queues 1, 2 and 3 respectively. All read operations on Queue 1, Queue 2 and Queue 3 will occur synchronous to the RCLK0, 1, 2 and 3 inputs respectively, provided that the corresponding read enable and read chip select inputs are LOW.
SCLK (B14)	Serial Clock	HSTL-LVTTL INPUT	Serial clock for writing and reading the $\overline{PAE}$ and $\overline{PAF}$ offset registers. On the rising edge of each SCLK, when $\overline{SWEN}$ is LOW, one bit of data is shifted from the FWFT/SI pin into the $\overline{PAE}$ and $\overline{PAF}$ offset registers. On the rising edge of each SCLK, when $\overline{SREN}$ is LOW, one bit of data is shifted out of the $\overline{PAE}$ and $\overline{PAF}$ offset registers. The reading of the $\overline{PAE}$ and $\overline{PAF}$ offset registers are non-destructive. If programming of the $\overline{PAE}$/$\overline{PAF}$ offset registers is done via the JTAG port, this input must be tied to Vcc.
SDO (C17)	Serial Data Output	LVTTL OUTPUT(2)	This output is used to read data from the programmable flag offset registers. It is used in conjunction with the $\overline{SREN}$ and SCLK signals.
$\overline{SREN}$ (B15)	Serial Read Enable	HSTL-LVTTL INPUT	When $\overline{SREN}$ is brought LOW before the rising edge of SCLK, the contents of the $\overline{PAE}$ and $\overline{PAF}$ offset registers are copied to a serial shift register. While $\overline{SREN}$ is maintained LOW, on each rising edge of SCLK, one bit of data is shifted out of this serial shift register through the SDO output pin. If programming of the $\overline{PAE}$/$\overline{PAF}$ offset registers is done via the JTAG port, this input must be tied to Vcc.
$\overline{SWEN}$ (C16)	Serial Write Enable	HSTL-LVTTL INPUT	On each rising edge of SCLK when $\overline{SWEN}$ is LOW, data from the FWFT/SI pin is serially loaded into the $\overline{PAE}$ and $\overline{PAF}$ registers. If programming of the $\overline{PAE}$/$\overline{PAF}$ offset registers is done via the JTAG port, this input must be tied to Vcc. On each clock, data is shifted into and through the actual $\overline{PAE}$ and $\overline{PAF}$ registers, so the value of the registers is changed on each clock

PIN DESCRIPTIONS (CONTINUED)

Symbol & Pin No.	Name	I/O TYPE	Description
TCK[3] (C13)	JTAG Clock	HSTL-LVTTL INPUT	Clock input for JTAG function. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to TCK. Data from TMS and TDI are sampled on the rising edge of TCK and output TDO change on the falling edge of TCK. If the JTAG function is not used this signal needs to be tied to GND.
TDI[3] (B13)	JTAG Test Data Input	HSTL-LVTTL INPUT	One of four terminals required by IEEE Standard 1149.1-1990. During the JTAG boundary scan operation, test data is serially loaded via the TDI on the rising edge of TCK to either the Instruction Register, ID Register, Bypass Register or Boundary Scan chain. An internal pull-up resistor forces TDI HIGH if left unconnected.
TDO[3] (B17)	JTAG Test Data Output	HSTL-LVTTL OUTPUT	One of four terminals required by IEEE Standard 1149.1-1990. During the JTAG boundary scan operation, test data is scanned to the TDO output on the falling edge of TCK from either the Instruction Register, ID Register, Bypass Register and Boundary Scan chain. This output is high impedance except when shifting, while in SHIFT-DR and SHIFT-IR controller states.
TMS[3] (C14)	JTAG Mode Select	HSTL-LVTTL INPUT	TMS is a serial input pin. One of four terminals required by IEEE Standard 1149.1-1990. TMS directs the device through its TAP controller states sampled on the rising edge of TCK. An internal pull-up resistor forces TMS HIGH if left unconnected.
$\overline{TRST}$[3] (C15)	JTAG Reset	HSTL-LVTTL INPUT	$\overline{TRST}$ is an asynchronous reset pin for the JTAG controller. The JTAG TAP controller is automatically reset upon power-up. If the TAP controller is not properly reset then the Queue outputs will always be in high-impedance. If the JTAG function is used but the user does not want to use $\overline{TRST}$, then $\overline{TRST}$ can be tied with $\overline{MRS}$ to ensure proper Queue operation. If the JTAG function is not used then this signal needs to be tied to GND. An internal pull-up resistor forces $\overline{TRST}$ HIGH if left unconnected.
WCLK0 (F1)	Write Clock 0	HSTL-LVTTL INPUT	If Mux mode is selected this is the clock input for Queue 0. All write port operations to Queue 0 will be synchronous to this clock input. If Demux or Broadcast mode is selected this is the clock input for the write port. All write port operations will be synchronous to this clock input. Sampled on the rising edge of WCLK and independent of WDDR.
WCLK1-(G1) WCLK2-(H1) WCLK3-(J1)	Write Clock 1/2/3	HSTL-LVTTL INPUT	If Mux mode is selected these are the clock inputs for Queues 1, 2, and 3 respectively. All write port operations on Queue1, Queue 2 and Queue 3 will be synchronous to clock inputs WCLK1, WCLK2 and WCLK3 respectively. If Demux or Broadcast mode is selected these clock inputs are ignored and can be tied to GND.
$\overline{WCS}$0 (U1)	Write Chip Select 0	HSTL-LVTTL INPUT	If Mux mode is selected this is the write chip select input for Queue 0. All write operations on Queue 0 will occur synchronous to the WCLK0 input provided that $\overline{WEN}$0 and $\overline{WCS}$0 are LOW. If Demux or Broadcast mode is selected this is the write chip select input for the write port. All write operations will occur synchronous to the WCLK0 input provided that $\overline{WEN}$0 and $\overline{WCS}$0 are LOW. Sampled on the rising edge of WCLK and independent of WDDR.
$\overline{WCS}$1-(U2) $\overline{WCS}$2-(U3) $\overline{WCS}$3-(T1)	Write Chip Select 1, 2, 3	HSTL-LVTTL INPUT	If Mux mode is selected these are the write chip select inputs for Queues 1, 2 and 3 respectively. All write operations on Queue 1, Queue 2 and Queue 3 will occur synchronous to the WCLK1, 2 and 3 respectively, provided that the corresponding write enable and write chip select inputs are LOW. Sampled on the rising edge of WCLK and independent of WDDR. If Demux or Broadcast mode is selected these inputs are ignored and can be tied HIGH.
WDDR (C7)	Write Port DDR	CMOS[1] INPUT	During master reset, this pin selects the input port to operate in DDR or SDR format. If WDDR is HIGH, then a word is written on the rising and falling edge of the appropriate WCLK0, 1, 2 and 3 input. If WDDR is LOW, then a word is written only on the rising edge of the appropriate WCLK1, 1, 2 and 3 inputs.
$\overline{WEN}$0 (T2)	Write Enable 0	HSTL-LVTTL INPUT	If Mux mode is selected this is the write enable input for Queue 0. All write operations on Queue 0 will occur synchronous to the WCLK0 input provided that $\overline{WEN}$0 and $\overline{WCS}$0 are LOW. If Demux or Broadcast mode is selected this is the write enable input for the write port. All write operations will occur synchronous to the WCLK0 clock input provided that $\overline{WEN}$0 and $\overline{WCS}$0 are LOW.
$\overline{WEN}$1-(T3) $\overline{WEN}$2-(R1) $\overline{WEN}$3-(R2)	Write Enable 1/2/3	LVTTL	If Mux mode is selected these are the write enable inputs for Queues 1, 2 and 3 respectively. All write operations on Queue 1, Queue 2 and Queue 3 will occur synchronous to the WCLK1, 2 and 3 inputs respectively, provided that the corresponding write enable and write chip select inputs are LOW. If Demux or Broadcast mode is selected these inputs are ignored and can be tied HIGH.

PIN DESCRIPTIONS (CONTINUED)

Symbol & Pin No.	Name	I/O TYPE	Description
V_{CC} (See Pin table)	+2.5V Supply	Power	These are V_{CC} core power supply pins and must all be connected to a +2.5V supply rail.
V_{DDQ} (See Pin table)	Output Rail Voltage	Power	This pin should be tied to the desired voltage rail for providing to the output drivers. Nominally 1.5V or 1.8V for HSTL, 2.5V for LVTTL.
GND (See Pin table)	Ground Pin	Ground	These ground pins are for the core device and must be connected to the GND rail.
Vref (A4)	Reference voltage	Analog	This is a Voltage Reference input and must be connected to a voltage level determined in the Voltage Recommended DC Operating Conditions section. This provides the reference voltage when using HSTL class inputs. If HSTL class inputs are not being used, this pin must be connected to GND.

NOTES:
1. All CMOS pins should remain unchanged. CMOS format means that the pin is intended to be tied directly to V_{CC} or GND and these particular pins are not tested for V_{IH} or V_{IL}.
2. All unused outputs may be left floating.
3. These pins are for the JTAG port. Please refer to pages 35-38, Figure 4-6 for JTAG information.

PIN NUMBER TABLE

Symbol	Name	I/O TYPE	Pin Number
D[39:0]	Data Input Bus	HSTL-LVTTL INPUT	D39-R3, D(38-36)-P(1-3), D(35-33)-N(1-3), D(32-30)-M(1-3), D(29-27)-L(1-3), D(26-24)-K(1-3), D(23,22)-J(3,2), D(21,20)-H(3,2), D(19,18)-G(3,2), D(17,16)-F(3,2), D(15-13)-E(3-1), D(12-10)-D(3-1), D(9-6)-C(4-1), D(5-3)-B(3-1), D(2-0)-A(3-1)
EF0/1/2/3-OR0/1/2/3	Empty Flags0-3 or Output Ready Flags 0-3	HSTL-LVTTL OUTPUT[2]	$\overline{EF}$0/$\overline{OR}$0-V4, $\overline{EF}$1/$\overline{OR}$1-U5, $\overline{EF}$2/$\overline{OR}$2-U7, $\overline{EF}$3/$\overline{OR}$3-V10
FF0/1/2/3-IR0/1/2/3	Full Flags0-3 or Input Ready Flags 0-3	HSTL-LVTTL OUTPUT[2]	$\overline{FF}$0/$\overline{IR}$0-T4, $\overline{FF}$1/$\overline{IR}$1-V6, $\overline{FF}$2/$\overline{IR}$2-T10, $\overline{FF}$3/$\overline{IR}$3-U11
Q[39:0]	Data Output Bus	HSTL-LVTTL OUTPUT[2]	Q(39,38)-U(17,16), Q(37-35)-T(17-15), Q(34,33)-R(17,16), Q(32-30)-P(18-16), Q(29-27)-N(18-16), Q(26-24)-M(18-16), Q(23-21)-L(18-16), Q20-K18, Q19-J18, Q(18-16)-H(16-18), Q(15-13)-G(16-18), Q(12-10)-F(16-18), Q(9-7)-E(16-18), Q(6-4)-D(16-18), Q3-C18, Q2-B18, Q(1-0)-A(18-17)
V_{CC}	+2.5V Supply	Power	A9, B9, C9, D(6,9), E(4-9), F(4,5), G(4,5), H(4,5), J(4,5), K(4,5), L(4,5), M(4,5), N(4,5), P(4-8), R(4-8), T8, U8, V8
V_{DDQ}	O/P Rail Voltage	Power	A11, B11, C11, D(11-15), E(11-15), F(14,15), G(14,15), H(14,15), J(14,15), K(14,15), L(14,15), M(14,15), N(14,15), P(11-15), R(11-15)
GND	Ground Pin	Ground	A10, B10, C10, D(7,8,10), E10, F(6-13), G(6-13), H(6-13), J(6-13), K(6-13), L(6-13), M(6-13), N(6-13), P(9,10), R(9,10), T9, U9, V9

QUADMUX I/O USAGE SUMMARY

SET-UP, CONFIGURATION & RESET PINS

Regardless of the mode of operation, (Mux, Demux or Broadcast), the following inputs must always be used. These inputs must be set-up with respect to master reset as they are latched during master reset.

WDDR – Write Port DDR/SDR selection
RDDR – Read Port DDR/SDR selection
MD[1:0] – Mode Selection
OW[1:0] – Output width
IW[1:0] – Input Width
FSEL[1:0] – Flag offset default values
IOSEL – I/O Level Selection
PFM – Programmable Flag Mode
FWFT/SI – First word Fall Through or Standard IDT mode flag timing selection

SERIAL PORT

The following pins are used for writing and reading the Programmable Flag Offsets values:

SCLK – Serial Clock
$\overline{SWEN}$ – Serial Write Enable
$\overline{SREN}$ – Serial Read Enable
FWFT/SI – Serial Data In
SDO – Serial Data Out

MUX MODE

The following inputs/ outputs should be used when Mux mode is selected by the user:

INPUTS:
WCLK0, WCLK1, WCLK2, WCLK3 – Four write port clocks
$\overline{WEN}$0, $\overline{WEN}$1, $\overline{WEN}$2, $\overline{WEN}$3 – Four write port enables
$\overline{WCS}$0, $\overline{WCS}$1, $\overline{WCS}$2, $\overline{WCS}$3 – Four write port chip selects
OS[1:0] - Output Select
RCLK0 – Read port clock
$\overline{REN}$0 – Read port enable
$\overline{RCS}$0 – Read port chip select
$\overline{OE}$0 – Read port output enable

OUTPUTS:
ERCLK0 – Read port echo read clock
$\overline{EREN}$0 – Read port echo read enable
$\overline{EF}$0/$\overline{OR}$0, $\overline{EF}$1/$\overline{OR}$1, $\overline{EF}$2/$\overline{OR}$2, $\overline{EF}$3/$\overline{OR}$3 – Four read port empty/output ready flags
$\overline{PAE}$0, $\overline{PAE}$1, $\overline{PAE}$2, $\overline{PAE}$3 – Four read port programmable almost empty flags
$\overline{PAF}$0, $\overline{PAF}$1, $\overline{PAF}$2, $\overline{PAF}$3 – Four write port programmable almost full flags
$\overline{FF}$0/$\overline{IR}$0, $\overline{FF}$1/$\overline{IR}$1, $\overline{FF}$2/$\overline{IR}$2, $\overline{FF}$3/$\overline{IR}$3 – Four write port full/ input ready flags
$\overline{CEF}$/$\overline{COR}$ – Composite empty/output ready flag on read port

DEMUX OR BROADCAST MODE

The following inputs/outputs should be used when Demux or Broadcast Write mode is selected by the user:

INPUTS:
IS[1:0] - Input Select, Demux mode only, not used in broadcast mode.
WCLK0 – Write port clock
$\overline{WEN}$0 – Write port enable
$\overline{WCS}$0 – Write port chip select
RCLK0, RCLK1, RCLK2, RCLK3 – Four read port clocks
$\overline{REN}$0, $\overline{REN}$1, $\overline{REN}$2, $\overline{REN}$3 – Four read port enables
$\overline{RCS}$0, $\overline{RCS}$1, $\overline{RCS}$2, $\overline{RCS}$3 – Four read port chip selects
$\overline{OE}$0, $\overline{OE}$1, $\overline{OE}$2, $\overline{OE}$3 – Four read port output enables

OUTPUTS:
ERCLK0, ERCLK1, ERCLK2, ERCLK3 – Four read port echo read clock outputs
$\overline{EREN}$0, $\overline{EREN}$1, $\overline{EREN}$2, $\overline{EREN}$3 – Four read port echo read enable outputs
$\overline{EF}$0/$\overline{OR}$0, $\overline{EF}$1/$\overline{OR}$1, $\overline{EF}$2/$\overline{OR}$2, $\overline{EF}$3/$\overline{OR}$3 – Four read port empty/output ready flags
$\overline{FF}$0/$\overline{IR}$0, $\overline{FF}$1/$\overline{IR}$1, $\overline{FF}$2/$\overline{IR}$2, $\overline{FF}$3/$\overline{IR}$3 – Four write port full/input ready flags
$\overline{PAF}$0, $\overline{PAF}$1, $\overline{PAF}$2, $\overline{PAF}$3 – Four write port programmable almost full flags
$\overline{PAE}$0, $\overline{PAE}$1, $\overline{PAE}$2, $\overline{PAE}$3 – Four read port programmable almost empty flags
$\overline{CFF}$/$\overline{CIR}$ – Composite full/ input ready flag on write port

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Com'l & Ind'l	Unit
V_{TERM}	Terminal Voltage with respect to GND	–0.5 to +3.6(2)	V
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	–? to +?	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Compliant with JEDEC JESD8-5. V_{CC} terminal only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}(2,3)	Input Capacitance	V_{IN} = 0V	10(3)	pF
C_{OUT}(1,2)	Output Capacitance	V_{OUT} = 0V	10	pF

NOTES:

1. With output deselected, ($\overline{OE} \geq V_{IH}$).
2. Characterized values, not currently tested.
3. C_{IN} for Vref is 20pF.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		2.375	2.5	2.625	V
V_{DDQ}	Output Supply Voltage	—LVTTL	2.375	2.5	2.625	V
		— eHSTL	1.7	1.8	1.9	V
		— HSTL(2)	1.4	1.5	1.6	V
V_{REF}	Voltage Reference Input	— eHSTL	0.8	0.9	1.0	V
		— HSTL(2)	0.68	0.75	0.9	V
GND	Supply Voltage		0	0	0	V
V_{IH}	Input High Voltage	—LVTTL	1.7	—	3.45	V
		— eHSTL	V_{REF}+0.1	—	V_{DDQ}+0.3	V
		— HSTL(2)	V_{REF}+0.1	—	V_{DDQ}+0.3	V
V_{IL}	Input Low Voltage	—LVTTL	—	—	0.7	V
		— eHSTL	V_{REF}-0.3	—	V_{REF}-0.1	V
		— HSTL(2)	V_{REF}-0.3	—	V_{REF}-0.1	V
T_A	Operating Temperature Commercial		0	—	+70	°C
T_A	Operating Temperature Industrial		-40	—	+85	°C

NOTES:

1. V_{REF} is only required for HSTL or eHSTL inputs. V_{REF} should be tied LOW for LVTTL operation.
2. Compliant with JEDEC JESD8-6.

DC ELECTRICAL CHARACTERISTICS

(Industrial: V_{CC} = 2.5V ± 0.125V, T_A = -40°C to +85°C)

Symbol	Parameter		Min.	Max.	Unit
I_{LI}	Input Leakage Current		–10	+10	µA
I_{LO}	Output Leakage Current		–10	+10	µA
V_{OH}[7]	Output Logic "1" Voltage,	I_{OH} = –8 mA @LVTTL	V_{DDQ}-0.4	—	V
		I_{OH} = –8 mA @eHSTL	V_{DDQ}-0.4	—	V
		I_{OH} = –8 mA @HSTL	V_{DDQ}-0.4	—	V
V_{OL}	Output Logic "0" Voltage,	I_{OL} = 8 mA @LVTTL	—	0.4	V
		I_{OL} = 8 mA @eHSTL	—	0.4	V
		I_{OL} = 8 mA @HSTL	—	0.4	V
I_{CC1}[1,2,3]	Active V_{CC} Current	--LVTTL	—	239	mA
	(See Note 8 and 9 for test conditions)	-- eHSTL	—	336	mA
		-- HSTL	—	332	mA
I_{CC3}[1,2,3]	Standby V_{CC} Current (Mux mode)	--LVTTL	—	112	mA
	(See Note 10 and 11 for test conditions)	-- eHSTL	—	188	mA
		-- HSTL	—	186	mA
I_{CC5}[1,2,3]	Power Down V_{CC} Current (Mux mode)	--LVTTL	—	9	mA
	(See Note 12 and 13 for test conditions)	-- eHSTL	—	26	mA
		-- HSTL	—	24	mA

NOTES:

1. Both WCLK and RCLK toggling at 20MHz.
2. Data inputs toggling at 10MHz.
3. Typical I_{CC1} calculation: for LVTTL I/O I_{CC1} (mA) = 10 x fS, fS = WCLK frequency = RCLK frequency (in MHz)
   for HSTL or eHSTL I/O I_{CC1} (mA) = 72+ (10 x fS), fS = WCLK frequency = RCLK frequency (in MHz)
4. Typical I_{DDQ} calculation: With Data Outputs in High-Impedance: I_{DDQ} (mA) = 0.78 x fs
   With Data Outputs in Low-Impedance: I_{DDQ} (mA) = C_L x V_{DDQ} x fS x N /2000
   fs = WCLK frequency = RCLK frequency (in MHz), V_{DDQ} = 2.5V for LVTTL; 1.5V for HSTL; 1.8V for eHSTL
   t_A = 25°C, C_L = capacitive load (pf), N = Number of bits switching
5. Total Power consumed: PT = [(V_{CC} x I_{CC}) + (V_{DDQ} x I_{DDQ})]. I_{OH} = -8mA for all voltage levels.
6. $I_{OH} \geq$ 8mA, $I_{OL} \geq$ -8mA.
7. Outputs are not 3.3V tolerant.
8. V_{CC} = 2.5V, WCLK0-3 = RCLK0 = 20MHz, $\overline{WEN}$0-3 = $\overline{REN}$0 = LOW, $\overline{WCS}$0-3 = $\overline{RCS}$0 = LOW, $\overline{OE}$ = LOW, $\overline{PD}$ = HIGH.
9. V_{CC} = 2.5V, WCLK0 = RCLK0-3 = 20MHz, $\overline{WEN}$0 = $\overline{REN}$0-3 = LOW, $\overline{WCS}$0 = $\overline{RCS}$0-3 = LOW, $\overline{OE}$0-3 = LOW, $\overline{PD}$ = HIGH.
10. V_{CC} = 2.5V, WCLK0-3 = RCLK0 = 20MHz, $\overline{WEN}$0-3 = $\overline{REN}$0 = HIGH, $\overline{WCS}$0-3 = $\overline{RCS}$0 = HIGH, $\overline{OE}$ = LOW, $\overline{PD}$ = HIGH.
11. V_{CC} = 2.5V, WCLK0 = RCLK0-3 = 20MHz, $\overline{WEN}$0 = $\overline{REN}$0-3 = HIGH, $\overline{WCS}$0 = $\overline{RCS}$0-3 = HIGH, $\overline{OE}$0-3 = LOW, $\overline{PD}$ = HIGH.
12. V_{CC} = 2.5V, WCLK0-3 = RCLK0 = 20MHz, $\overline{WEN}$0-3 = $\overline{REN}$0 = HIGH, $\overline{WCS}$0-3 = $\overline{RCS}$0 = HIGH, $\overline{OE}$ = LOW, $\overline{PD}$ = LOW.
13. V_{CC} = 2.5V, WCLK0 = RCLK0-3 = 20MHz, $\overline{WEN}$0 = $\overline{REN}$0-3 = HIGH, $\overline{WCS}$0 = $\overline{RCS}$0-3 = HIGH, $\overline{OE}$0-3 = LOW, $\overline{PD}$ = LOW.

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 2.5V ± 0.15V, T_A = 0°C to +70°C;Industrial: V_{CC} = 2.5V ± 0.15V, T_A = -40°C to +85°C; JEDEC JESD8-A compliant)

Symbol	Parameter	Commercial & Industrial IDT72T55248L5 IDT72T55258L5 IDT72T55268L5		Commercial & Industrial IDT72T55248L6-7 IDT72T55258L6-7 IDT72T55268L6-7		Unit
		Min.	Max.	Min.	Max.	
f_S	Clock Cycle Frequency (WCLK & RCLK)	—	200	—	150	MHz
t_A	Data Access Time	0.6	3.6	0.6	3.8	ns
t_{CLK}	Clock Cycle Time	5	—	6.7	—	ns
t_{CLKH}	Clock High Time	2.3	—	2.8	—	ns
t_{CLKL}	Clock Low Time	2.3	—	2.8	—	ns
t_{DS}	Data Setup Time	1.5	—	2.0	—	ns
t_{DH}	Data Hold Time	0.5	—	0.5	—	ns
t_{ENS}	Enable Setup Time	1.5	—	2.0	—	ns
t_{ENH}	Enable Hold Time	0.5	—	0.5	—	ns
f_C	Clock Cycle Frequency (SCLK)	—	10	—	10	MHz
t_{ASO}	Serial Output Data Access Time	—	20	—	20	ns
t_{SCLK}	Serial Clock Cycle	100	—	100	—	ns
t_{SCKH}	Serial Clock High	45	—	45	—	ns
t_{SCKL}	Serial Clock Low	45	—	45	—	ns
t_{SDS}	Serial Data In Setup	15	—	15	—	ns
t_{SDH}	Serial Data In Hold	5	—	5	—	ns
t_{SENS}	Serial Enable Setup	5	—	5	—	ns
t_{SENH}	Serial Enable Hold	5	—	5	—	ns
t_{RS}	Reset Pulse Width	200	—	200	—	ns
t_{RSS}	Reset Setup Time	15	—	15	—	ns
t_{RSR}	Reset Recovery Time	10	—	10	—	ns
t_{RSF}	Reset to Flag and Output Time	—	12	—	15	ns
t_{OLZ} ($\overline{OE}$ - Q_n)[2]	Output Enable to Output in Low-Impedance	0.6	3.6	0.8	3.8	ns
t_{OHZ}[2]	Output Enable to Output in High-Impedance	0.6	3.6	0.8	3.8	ns
t_{OE}	Output Enable to Data Output Valid	0.6	3.6	0.8	3.8	ns
t_{WFF}	Write Clock to $\overline{FF}$ or $\overline{IR}$	—	3.6	—	3.8	ns
t_{REF}	Read Clock to $\overline{EF}$ or $\overline{OR}$	—	3.6	—	3.8	ns
t_{CEF}	Read Clock to Composite $\overline{EF}$ or $\overline{OR}$	—	3.6	—	3.8	ns
t_{CFF}	Write Clock to Composite $\overline{FF}$ or $\overline{IR}$	—	3.6	—	3.8	ns
t_{PAFS}	Write Clock to Synchronous Programmable Almost-Full Flag	—	3.6	—	3.8	ns
t_{PAES}	Read Clock to Synchronous Programmable Almost-Empty Flag	—	3.6	—	3.8	ns
t_{PAFA}	Write Clock to Asynchronous Programmable Almost-Full Flag	—	10	—	12	ns
t_{PAEA}	Read Clock to Asynchronous Programmable Almost-Empty Flag	—	10	—	12	ns
t_{ERCLK}	RCLK to Echo RCLK Output	—	4.0	—	4.3	ns
t_{CLKEN}	RCLK to Echo $\overline{REN}$ Output	—	3.6	—	3.8	ns
t_D	Time Between Data Switching and ERCLK edge	0.4	—	0.5	—	ns
t_{RCSLZ}	RCLK to Active from High-Impedance	—	3.6	—	3.8	ns
t_{RCSHZ}	RCLK to High-Impedance	—	3.6	—	3.8	ns
t_{SKEW1}[3]	SKEW time between RCLK and WCLK for $\overline{EF}$/$\overline{OR}$ and $\overline{FF}$/$\overline{IR}$	4	—	5	—	ns
t_{SKEW2}	SKEW time between RCLK and WCLK for $\overline{EF}$/$\overline{OR}$ and $\overline{FF}$/$\overline{IR}$ in DDR mode	5	—	7	—	ns
t_{SKEW3}	SKEW time between RCLK and WCLK for $\overline{PAE}$ and $\overline{PAF}$	5	—	7	—	ns

NOTES:
1. Values guaranteed by design, not currently tested.
2. This applies to both DDR and SDR modes of operation.

HSTL
1.5V AC TEST CONDITIONS

Input Pulse Levels	0.25 to 1.25V
Input Rise/Fall Times	0.4ns
Input Timing Reference Levels	0.75
Output Reference Levels	$V_{DDQ}/2$

NOTE:
1. V_{DDQ} = 1.5V.

AC TEST LOADS

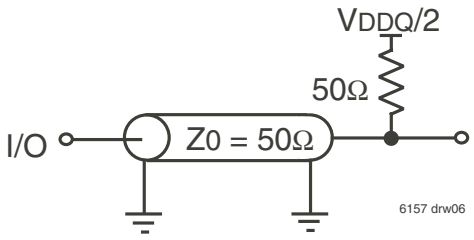


Figure 2a. AC Test Load

EXTENDED HSTL
1.8V AC TEST CONDITIONS

Input Pulse Levels	0.4 to 1.4V
Input Rise/Fall Times	0.4ns
Input Timing Reference Levels	0.9
Output Reference Levels	$V_{DDQ}/2$

NOTE:
1. V_{DDQ} = 1.8V.

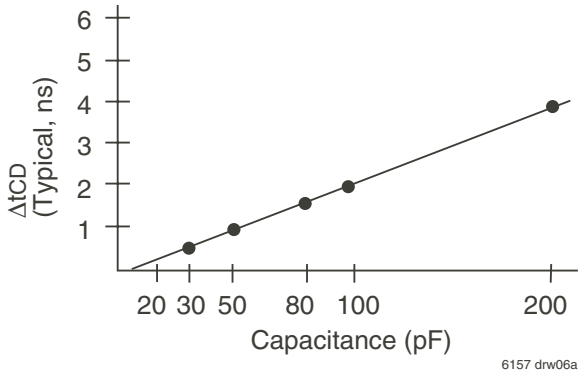


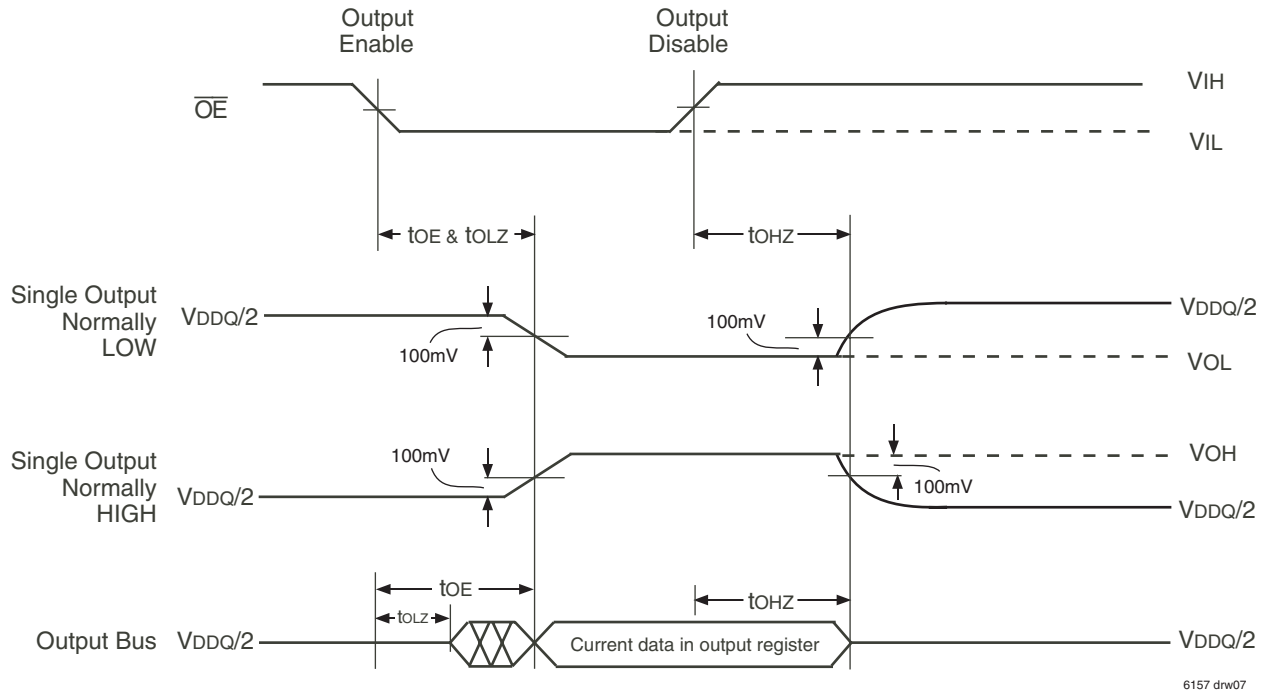
Figure 2b. Lumped Capacitive Load, Typical Derating

LVTTL
2.5V AC TEST CONDITIONS

Input Pulse Levels	GND to 2.5V
Input Rise/Fall Times	1ns
Input Timing Reference Levels	$V_{CC}/2$
Output Reference Levels	$V_{DDQ}/2$

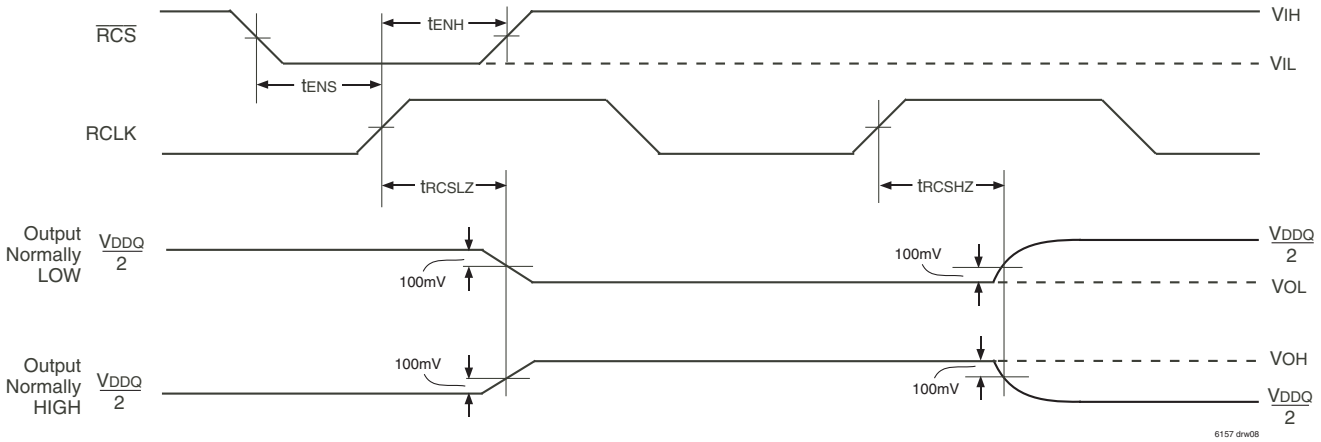
NOTE:
1. For LVTTL, V_{CC} = V_{DDQ} = 2.5V.

OUTPUT ENABLE & DISABLE TIMING



NOTES:
1. $\overline{REN}$ is HIGH.
2. $\overline{RCS}$ is LOW.

READ CHIP SELECT ENABLE & DISABLE TIMING



NOTES:
1. $\overline{REN}$ is HIGH.
2. $\overline{OE}$ is LOW.

FUNCTIONAL DESCRIPTION

MASTER RESET & DEVICE CONFIGURATION - $\overline{MRS}$

During Master Reset the device operation is determined, this includes the following:

1. Mux, Demux or Broadcast mode
2. IDT Standard or First Word Fall Through (FWFT) flag timing mode
3. Single or Double Data Rates on both the Write and Read ports
4. Programmable flag mode, synchronous or asynchronous timing
5. Write and read port bus widths, x10, x20 or x40
6. Default offsets for the programmable flags, 7, 63, 127 or 1023
7. LVTTL or HSTL I/O level selection
8. Input and output Queue selection

The state of the configuration inputs during a master reset will determine which of the above modes are selected. A Master Reset comprises of pulsing the $\overline{MRS}$ input ping from high to low for a period of time (t_{RS}) with the configuration inputs held in their respective states. Table 1 summarizes the configuration modes available doing master reset. The are described as follows:

TABLE 1 — DEVICE CONFIGURATION

PINS	VALUES	CONFIGURATION
MD[1:0]	00	Demux
	10	Mux
	01	Broadcast Write
	11	Restricted
FWFT/SI	0	IDT Standard
	1	FWFT
WDDR	0	Single Data Rate write port
	1	Double Data Rate write port
RDDR	0	Single Data Rate read port
	1	Double Data Rate read port
PFM	0	Asynchronous operation of $\overline{PAE}$ and $\overline{PAF}$ outputs
	1	Synchronous operation of $\overline{PAE}$ and $\overline{PAF}$ outputs
IW[1:0]	00	Write port is 10 bits wide
	01	Write port is 20 bits wide
	10	Write port is 40 bits wide
	11	Restricted
OW[1:0]	00	Read port is 10 bits wide
	01	Read port is 20 bits wide
	10	Read port is 40 bits wide
	11	Restricted
FSEL[1:0]	00	Programmable flag offset registers value = 7
	01	Programmable flag offset registers value = 63
	10	Programmable flag offset registers value = 127
	11	Programmable flag offset registers value = 1023
IOSEL	0	All applicable I/Os (except CMOS) are LVTTL
	1	All applicable I/Os (except CMOS) are HSTL/eHSTL
IS[1:0]		Mux/Broadcast Mode — Demux Mode
	00	not used — Queue0
	01	not used — Queue1
	10	not used — Queue2
	11	not used — Queue3
OS[1:0]		Mux Mode — Demux/Broadcast Mode
	00	Queue0 — not used
	01	Queue1 — not used
	10	Queue2 — not used
	11	Queue3 — not used

Mux/Demux/Broadcast. This mode is selected using the MD[1:0] inputs. If during master reset, MD1 is HIGH and MD0 is LOW then Mux mode is selected. If MD1 and MD2 are LOW then Demux is selected. If MD1 is LOW and MD0 is HIGH then Broadcast mode is selected.

IDT Standard or FWFT Mode. The two available flag timing modes are selected using the FWFT/SI input. If FWFT/SI is LOW during Master Reset then IDT Standard mode is selected, if it is high then FWFT mode is selected.

Single Data Rate (SDR) or Double Data Rate (DDR). The input/output data rates are port selectable. This is a versatile feature that allows the user to select either SDR or DDR on the write port(s) and/or read(s) port using the WDDR and/or RDDR inputs. If WDDR is LOW during master reset then the write port(s) will function in SDR mode, if it is high then the write port will be DDR mode. If RDDR is LOW during master reset then the read port(s) will function in SDR mode, if it is high then the read port will be DDR mode. Note that WDDR will select the data rate mode for the single write port in Demux and Broadcast mode and all four write ports in Mux mode. Likewise, RDDR will select the data rate mode for the single read port in Mux mode and all four read ports in Demux and Broadcast mode.

Programmable Almost Empty/Full Flags. These flags can operate in either synchronous or asynchronous timing mode. If the programmable flag input, PFM is HIGH during master reset then all programmable flags will operate in a synchronous manner, meaning the $\overline{PAE}$ flags are double buffered and updated based on the rising edge of its respective read clocks. The $\overline{PAF}$ flags are also double buffered and updated based on the rising edge of its respective write clocks. If it is LOW then all programmable flags will operate in an asynchronous manner, meaning the $\overline{PAE}$ and $\overline{PAF}$ flags are not double buffered and will update through the internal counter after a nominal delay.

Selectable Bus Width. The bus width can be selected on the write port in Demux and Broadcast mode and on the read port in Mux mode. In Demux and Broadcast mode the write port width is selected using the IW[1:0] inputs. If IW0 and IW1 are LOW then the write port will be 10 bits wide, if IW0 is LOW and IW1 is HIGH then the write port will be 20 bits wide, if IW0 is HIGH and IW1 is LOW then the write port will be 40 bits wide. Note, in Demux and Broadcast mode all read ports are 10 bits wide. In Mux mode the read port width is selected using the OW[1:0] inputs. If OW0 and 0W1 are LOW then the read port will be 10 bits wide, if OW0 is LOW and OW1 are HIGH then the read port will be 20 bits wide, if OW0 is HIGH and OW1 are LOW then the read port will be 40 bits wide. Note, in Mux mode all write ports are 10 bits wide.

Programmable Flag Offset Values. These offset values can be user programmed or they can be set to one of four default values during a master reset. For default programming, the state of the FSEL[1:0] inputs during master

TABLE 2 — DEFAULT PROGRAMMABLE FLAG OFFSETS

IDT72T55248
IDT72T55258
IDT72T55268

FSEL1	FSEL0	Offsets n,m
0	0	7
0	1	63
1	0	127
1	1	1,023

NOTES:
1. In default programming, the offset value selected applies to all internal Queues.
2. To program different offset values for each Queue, serial programming must be used.

reset will determine the value. Table 1 lists the four offset values and how to select them. For programming the offset values to a specific number, use the serial programming signals (SCLK, $\overline{SWEN}$, $\overline{SREN}$, FWFT/SI) to load the value into the offset register. You may also use the JTAG port on this device to load the offset value. Keep in mind that you must disable the serial programming signals if you plan to use the JTAG port for loading the offset values. To disable the serial programming signals, tie SCLK, $\overline{SWEN}$, $\overline{SREN}$, and SI to V_{CC}. A thorough explanation of the serial and JTAG programming of the flag offset values is provided in the next section.

I/O Level Selection. The I/Os can be selected for either 2.5V LVTTL levels or 1.5V HSTL / 1.8V eHSTL levels. The state of the IOSEL input will determine which I/O level will be selected. If IOSEL is HIGH then the applicable I/Os will be 1.5V HSTL or 1.8V eHSTL, depending on the voltage level applied to V_{DDQ} and V_{REF}. For HSTL, V_{DDQ} and V_{REF} = 0.75V and for eHSTL V_{DDQ} and V_{REF} = 0.9V. If IOSEL is LOW then the applicable I/Os will be 2.5V LVTTL V_{REF} = 0. As noted in the Pin Description section, IOSEL is a CMOS input and must be tied to either V_{CC} or GND for proper operation.

Input and Output Selection. During master reset, the value of IS[1:0] and OS[1:0] will be held constant and indicates which internal Queue the read and write port will select for initial operation. Data will be written to or read from this internal Queue on the first valid write and read operation after master reset.

SERIAL WRITING AND READING OF OFFSET REGISTERS

These offset registers can be loaded with a default value or they can be user programmed with another value. One of four default values are detected based on the state of the FSEL[1:0] inputs, discussed in the Functional Description section earlier. User programming of the offset values can be performed by either the dedicated serial programming port or the JTAG port. The dedicated serial port can be used to load or read the contents of the offset registers. The offset registers are programmed and read sequentially and behave similar to a shift register.

The serial read and write operations are performed by the dedicated SCLK, FWFT/SI, $\overline{SWEN}$, $\overline{SREN}$, and SDO pins. The total number of bits per device is listed in Figure? *Programmable Flag Offset Programming Sequence*. These bits account for all four $\overline{PAE}$/$\overline{PAF}$ offset registers in the device. To write to the offset registers, set the serial write enable signal active (LOW), and on each rising edge of SCLK one bit from the FWFT/SI pin is serially shifted into the flag offset register chain. Once the complete number of bits has been programmed into all four registers, the programming sequence is complete. The programming sequence is listed in Figure ? To read values from the offsets registers, set the serial read enable active (LOW). Then on each rising edge of SCLK, one bit is shifted out to the serial data output. The serial read enable must be kept LOW throughout the entire read operation. To stop reading the offset register, disable the serial read enable (HIGH). There is serial read enable to SCLK time for reading the offset registers, as the offset register data for each Queue is temporarily stored in a scan chain. When data has been completely read out of the offset registers, any additional read operations to the offset register will result in zeros as the output data.

Reading and writing of the offset registers can also be accomplished using the JTAG port. To write to the offset registers using JTAG, set the instructional register to the offset write command (Hex Value = 0x0008). The JTAG port will load data into each of the offset registers in a similar fashion as the serial programming described above. To read the values from the offset registers, set the instructional register to the offset read command (Hex Value = 0x0007). The

TDI*	TCK*	$\overline{SWEN}$	$\overline{SREN}$	SCLK	IDT72T55258 IDT72T55268 IDT72T55278 IW/OW = x40	IW/OW = x20	IW/OW = x10
0008	↑	0	1	↑	Serial write into register: 104 bits for the IDT72T55248 112 bits for the IDT72T55258 120 bits for the IDT72T55268 1 bit for each rising SCLK edge starting with empty offset (LSB) ending with full offset (MSB)	Serial write into register: 112 bits for the IDT72T55248 120 bits for the IDT72T55258 128 bits for the IDT72T55268 1 bit for each rising SCLK edge starting with empty offset (LSB) ending with full offset (MSB)	Serial write into register: 120 bits for the IDT72T55248 128 bits for the IDT72T55258 136 bits for the IDT72T55268 1 bit for each rising SCLK edge starting with empty offset (LSB) ending with full offset (MSB)
0007	↑	1	0	↑	Serial read from registers: 104 bits for the IDT72T55248 112 bits for the IDT72T55258 120 bits for the IDT72T55268 1 bit for each rising SCLK edge starting with empty offset (LSB) ending with full offset (MSB)	Serial read from registers: 112 bits for the IDT72T55248 120 bits for the IDT72T55258 128 bits for the IDT72T55268 1 bit for each rising SCLK edge starting with empty offset (LSB) ending with full offset (MSB)	Serial read from registers: 120 bits for the IDT72T55248 128 bits for the IDT72T55258 136 bits for the IDT72T55268 1 bit for each rising SCLK edge starting with empty offset (LSB) ending with full offset (MSB)
Don't care except 0008 & 0007	X	1	1	X	No Operation	No Operation	No Operation

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NOTES:

***** Programming done using the JTAG port.

1. The programming methods apply to both IDT Standard mode and FWFT mode.
2. Parallel programming is not featured in this device.
3. The number of bits includes programming to all four dedicated $\overline{PAE}$/$\overline{PAF}$ offset registers.

Figure 3. Programmable Flag Offset Programming Methods

TDO of the JTAG port will output data in a similar fashion as the serial programming described above.

The number of bits required to load the offset registers is dependent on the size of the device selected. Each offset register requires different total number of bits depending on input and output bus width configuration. This total must be programmed into the device in order for all the flags to be programmed correctly. To change values of one or more offset register, all of the registers must be reprogrammed serially again. See Figure? *Offset Registers Serial Bit Sequence*.

TIMING MODES: IDT STANDARD vs FIRST WORD FALL THROUGH (FWFT) MODE

The IDT72T55248/72T55258/72T55268 support two different timing modes of operation: IDT Standard mode or First Word Fall Through (FWFT) mode. The selection of which mode will operate is determined during master reset, by the state of the FWFT input.

During master reset, if the FWFT pin is LOW, then IDT Standard mode will be selected. This mode uses the Empty Flag ($\overline{EF}$) to indicate whether or not there are any words present in the Queue. It also uses the Full Flag ($\overline{FF}$) to indicate whether or not the Queue has any free space for writing. In IDT Standard mode, every word read from the Queue, including the first, must be requested using the Read Enable ($\overline{REN}$) and RCLK.

If the FWFT pin is HIGH during master reset, then FWFT mode will be selected. This mode uses Output Ready ($\overline{OR}$) to indicate whether or not there is valid data at the data outputs. It also uses Input Ready ($\overline{IR}$) to indicate whether or not the Queue has any free space for writing. In the FWFT mode, the first word written to an empty Queue goes directly to output bus after three RCLK rising edges, applying $\overline{RCS}$ = LOW is not necessary. However, subsequent words must be accessed using the ($\overline{RCS}$) and RCLK. Various signals, in both inputs and outputs operate differently depending on which timing mode is in effect. The timing mode selected affects all internal Queues equally.

IDT STANDARD MODE

In this mode, the status flags $\overline{FF}$, $\overline{PAF}$, $\overline{PAE}$, and $\overline{EF}$ operate in the manner outlined in Table 3. To write data into the Queue, Write Enable ($\overline{WEN}$) and $\overline{WCS}$ must be LOW. Data presented to the DATA IN lines will be clocked into the Queue on subsequent transitions of the Write Clock (WCLK). After the first write is performed, the Empty Flag ($\overline{EF}$) will go HIGH after three clock latency. Subsequent writes will continue to fill up the Queue. The Programmable Almost-Empty flag ($\overline{PAE}$) will go HIGH after n + 1 words have been loaded into the Queue, where n is the empty offset value. The default setting for these values are listed in Table ?. This parameter is also user programmable as described in the serial writing and reading of offset registers section.

Continuing to write data into the Queue without performing read operations will cause the Programmable Almost-Full flag ($\overline{PAF}$) to go LOW. Again, if no reads are performed, the $\overline{PAF}$ will go LOW after (8,192-m) writes for the IDT72T55248, (16,384-m) writes for the IDT72T55258, and (32,768-m) writes for the IDT72T55268. This is assuming the I/O bus width is configured to x40. If the I/O is x20, then $\overline{PAF}$ will go LOW after (16,384-m) writes for the IDT72T55248, (32,768-m) writes for the IDT72T55258, and (65,536-m) writes for the IDT72T55268. If the I/O is x10, then $\overline{PAF}$ will go LOW after (32,768-m) writes for the IDT72T55248, (65,536-m) writes for the IDT72T55258, and (131,072-m) writes for the IDT72T55268. The offset "m" is the full offset value. The default setting for these values are listed in Table 3. This parameter is also user programmable. See the section on serial writing and reading of offset registers for details.

When the Queue is full, the Full Flag ($\overline{FF}$) will go LOW, inhibiting further write operations. If no reads are performed after a reset, $\overline{FF}$ will go LOW after D writes to the Queue. If the I/O bus width is configured to x40, then D = 8,192 writes for the IDT72T55248, 16,384 writes for the IDT72T55258, and 32,768 writes for the IDT72T55268. If the I/O is x20, then D = 16,384 writes for the IDT72T55248, 32,768 writes for the IDT72T55258, and 65,536 writes for the IDT72T55268. If the I/O is x10, then D = 32,768 writes for the IDT72T55248, 65,536 writes for the IDT72T55258, and 131,072 writes for the IDT72T55268.

	IDT72T55248 IW/OW = x40	IDT72T55248 IW/OW = x20 or IDT72T55258 IW/OW = x40	IDT72T55248 IW/OW = x20 or IDT72T55258 IW/OW = x20 or IDT72T55268 IW/OW = x40	IDT72T55258 IW/OW = x10 or IDT72T55268 IW/OW = x20	IDT72T55268 IW/OW = x10	Offset Register
Serial Bits	1 - 13	1 - 14	1 - 15	1 - 16	1 - 17	$\overline{PAE}$3
	14 - 26	15 - 28	16 - 30	17 - 32	18 - 34	$\overline{PAF}$3
	27 - 39	29 - 42	31 - 45	33 - 48	35 - 51	$\overline{PAE}$2
	40 - 52	43 - 56	46 - 60	49 - 64	52 - 68	$\overline{PAF}$2
	53 - 65	57 - 70	61 - 75	65 - 80	69 - 85	$\overline{PAE}$1
	66 - 78	71 - 84	76 - 90	81 - 96	86 - 102	$\overline{PAF}$1
	79 - 91	85 - 98	91 - 105	97 - 112	103 - 119	$\overline{PAE}$0
	92 - 104	99 - 112	106 - 120	113 - 128	120 - 136	$\overline{PAF}$0

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Figure 4. Offset Registers Serial Bit Sequence

If the Queue is full, the first read operation will cause $\overline{FF}$ to go HIGH after two WCLKS. Subsequent read operations will cause $\overline{PAF}$ to go HIGH at the conditions described in Table ?. If further read operations occur, without write operations, $\overline{PAE}$ will go LOW when there are n words in the Queue, where n is the empty offset value. Continuing read operations will cause the Queue to become empty. Then the last word has been read from the Queue, the $\overline{EF}$ will go LOW inhibiting further read operations. $\overline{REN}$ is ignored when the Queue is empty.

When configured in IDT Standard mode, the $\overline{EF}$ and $\overline{FF}$ outputs are double register-buffered outputs. IDT Standard mode is available when the device is configured in both Single Data Rate and Double Data Rate mode. Relevant timing diagrams for IDT Standard mode can be found in Figures 14, 15, 16.

FIRST WORD FALL THROUGH MODE (FWFT)

In this mode, the status flags $\overline{OR}$, $\overline{IR}$, $\overline{PAE}$, and $\overline{PAF}$ operate in the manner outlined in Table 4. To write data into to the Queue, $\overline{WCS}$ must be LOW. Data presented to the DATA IN lines will be clocked into the Queue on subsequent transitions of WCLK. After the first write is performed, the Output Ready ($\overline{OR}$) flag will go LOWafter 3rd rising edge of RCLK. Subsequent writes will continue to fill up the Queue. $\overline{PAE}$ will go HIGH after n + 2 words have been loaded into the Queue, where n is the empty offset value. The default setting for these values are listed in Table 4. This parameter is also user programmable as described in the serial writing and reading of offset registers section.

Continuing to write data into the Queue without performing read operations will cause the Programmable Almost-Full flag ($\overline{PAF}$) to go LOW. Again, if no reads are performed, the $\overline{PAF}$ will go LOW after (8,193-m) writes for the IDT72T55248, (16,385-m) writes for the IDT72T55258, and (32,769-m) writes for the IDT72T55268. This is assuming the I/O bus width is configured to x40. If the I/O is x20, then $\overline{PAF}$ will go LOW after (16,385-m) writes for the IDT72T55248, (32,769-m) writes for the IDT72T55258, and (65,537-m) writes for the IDT72T55268. If the I/O is x10, then $\overline{PAF}$ will go LOW after (32,769-m) writes for the IDT72T55248, (65,537-m) writes for the IDT72T55258, and (131,073-m) writes for the IDT72T55268. The offset "m" is the full offset value. The default setting for these values are listed in Table ?. This parameter is also user programmable. See the section on serial writing and reading of offset registers for details.

When the Queue is full, the Input Ready ($\overline{IR}$) will go LOW, inhibiting further write operations. If no reads are performed after a reset, $\overline{IR}$ will go LOW after D writes to the Queue. If the I/O bus width is configured to x40, then D = 8,193 writes for the IDT72T55248, 16,385 writes for the IDT72T55258, and 32,769 writes for the IDT72T55268. If the I/O is x20, then D = 16,385 writes for the IDT72T55248, 32,769 writes for the IDT72T55258, and 65,537 writes for the IDT72T55268. If the I/O is x10, then D = 32,769 writes for the IDT72T55248, 65,537 writes for the IDT72T55258, and 131,073 writes for the IDT72T55268.

If the Queue is full, the first read operation will cause $\overline{IR}$ to go HIGH after two WCLKs after RCLK. Subsequent read operations will cause $\overline{PAF}$ to go HIGH at the conditions described in Table ? If further read operations occur, without write operations, $\overline{PAE}$ will go LOW when there are n words in the Queue, where n is the empty offset value. Continuing read operations will cause the Queue to become empty. Then the last word has been read from the Queue, the $\overline{OR}$ will go HIGH inhibiting further read operations. $\overline{RCS}$ is ignored when the Queue is empty.

When configured in FWFT mode, the $\overline{OR}$ flag output is triple register-buffered and the $\overline{IR}$ flag output is double register-buffered. Relevant timing diagrams for FWFT mode can be found in Figures 17, 18, 19.

TABLE 3 — STATUS FLAGS FOR IDT STANDARD MODE

OW = x40	IDT72T55248	IDT72T55258	IDT72T55268						
OW = x20		IDT72T55248	IDT72T55258	IDT72T55268					
OW = x10			IDT72T55248	IDT72T55258	IDT72T55268	$\overline{FF}$	$\overline{PAF}$	$\overline{PAE}$	$\overline{EF}$
Number of Words in Queue	0	0	0	0	0	H	H	L	L
	1 to n[1]	1 to n[1]	1 to n[1]	1 to n[1]	1 to n[1]	H	H	L	H
	(n+1) to (8,192 - m)	(n+1) to (16,384 - m)	(n+1) to (32,768 - m)	(n+1) to (65,536 - m)	(n+1) to (131,072 - m)	H	L	H	H
	8,192	16,384	32,768	65,536	131,072	L	L	H	H

NOTE:
1. n, m = 7 if FSEL[1:0] = 00, n, m = 63 if FSEL[1:0] = 01, n, m = 127 if FSEL[1:0] = 10, n, m = 1023 if FSEL[1:0] = 11.

TABLE 4 — STATUS FLAGS FOR FWFT MODE

OW = x40	IDT72T55248	IDT72T55258	IDT72T55268						
OW = x20		IDT72T55248	IDT72T55258	IDT72T55268					
OW = x10			IDT72T55248	IDT72T55258	IDT72T55268	$\overline{FF}$	$\overline{PAF}$	$\overline{PAE}$	$\overline{EF}$
Number of Words in Queue	0	0	0	0	0	H	H	L	L
	1 to n+1[1]	1 to n+1[1]	1 to n+1[1]	1 to n+1[1]	1 to n+1[1]	H	H	L	H
	(n+2) to (8,193 - m)	(n+2) to (16,385 - m)	(n+2) to (32,769 - m)	(n+2) to (65,537 - m)	(n+2) to (131,073 - m)	H	L	H	H
	8,193	16,385	32,769	65,537	131,073	L	L	H	H

NOTE:
1. n, m = 7 if FSEL[1:0] = 00, n, m = 63 if FSEL[1:0] = 01, n, m = 127 if FSEL[1:0] = 10, n, m = 1023 if FSEL[1:0] = 11.

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HSTL/LVTTL I/O

The inputs and outputs of this device can be configured for either LVTTL or HSTL/eHSTL operation. If the IOSEL pin is HIGH during master reset, then all applicable LVTTL or HSTL signals will be configured for HSTL/eHSTL operating voltage levels. To select between HSTL or eHSTL V_{REF} must be driven to 0.75V or 0.9V respectively. Typically a logic HIGH in HSTL would be V_{REF} ±300mV and a logic LOW would be V_{REF} ±300mV. If the IOSEL pin is LOW during master reset, then all applicable LVTTL or HSTL signals will be configured for LVTTL operating voltage levels. In this configuration V_{REF} must be set to the static core voltage of 2.5V. Table ? illustrates which pins are and are not associated with this feature. Note that all "Static Pins" must be tied to V_{CC} or GND. These pins are CMOS only and are purely device configuration pins. Note the IOSEL pin should be tied HIGH or LOW and cannot toggle before and after master reset.

BUS MATCHING

The write and read port has bus-matching capability such that the input and output bus can be either 10 bits, 20 bits or 40 bits wide, depending on which operating mode the device is configured to. The bus width of both the input and output port is determined during master reset using the input and output width setup pins (IW[1:0], OW[1:0]). The selected port width is applied to all four Queue ports, such that all four Queues will be configured for either x10, x20 or x40 bus widths. When writing or reading data from a Queue the number of memory locations available to be written or read will depend on the bus width selected and the density of the device.

If the write/read port is 10 bits wide, this provides the user with a Queue depth of 32,768 x 10 for the IDT72T55248, 65,536 x 10 for the IDT72T55258, or 131,072 x 10 for the IDT72T55268. If the write/read port is 20 bits wide, this provides the user with a Queue depth of 16,384 x 20 for the IDT72T55248, 32,768 x 20 for the IDT72T55258, or 65,536 x 20 for the IDT72T55268. If the write/read port is 40 bits wide, this provides the user with a Queue depth of 8,192 x 40 for the IDT72T55248, 16,384 x 40 for the IDT72T55258, or 32,768 x 40 for the IDT72T55268. The Queue depths will always have a fixed density of 327,680 bits for the IDT72T55248, 655,360 bits for the IDT72T55258 and 1,310,072 bits for the IDT72T55268 regardless of bus-width configuration on the write/read port.

When the device is operating in double data rate, the word is twice as large as in single data rate since one word written or read on both the rising and falling edge of clock. Therefore in DDR, the Queue depths will be half of what it is mentioned above. For instance, if the write/read port is 10 bits wide, the depth of each Queue is 16,384 x 10 for the IDT72T55248, 32,768 x 10 for the IDT72T55258, or 65,536 x 10 for the IDT72T55268.

See Figure 5, *Bus-Matching Byte Arrangement* for more information.

TABLE 5 — I/O VOLTAGE LEVEL CONFIGURATION

LVTTL/HSTL/eHSTL					STATIC CMOS SIGNALS
Write Port	**Read Port**	**JTAG**	**Control Pins**	**Serial Port**	**Static Pins**
D[39:0]	$\overline{CEF}$/$\overline{COR}$	TCK	FSEL[1:0]	SCLK	IOSEL
WCLK0/1/2/3	$\overline{EF}$0/1/2/3	$\overline{TRST}$	IS[1:0]	$\overline{SREN}$	IW[1:0]
$\overline{WEN}$0/1/2/3	$\overline{OR}$0/1/2/3	TMS	OS[1:0]	$\overline{SWEN}$	MD[1:0]
$\overline{FF}$0/1/2/3	ERCLK0/1/2/3	TDI	$\overline{PD}$	FWFT/SI	OW[1:0]
$\overline{WCS}$0/1/2/3	$\overline{OE}$0/1/2/3	TDO	$\overline{MRS}$	SDO	PFM
$\overline{CFF}$/$\overline{CIR}$	$\overline{PAE}$0/1/2/3		$\overline{PRS}$0/1/2/3		RDDR
$\overline{PAF}$0/1/2/3	Q[39:0]		FWFT/SI		WDDR
	RCLK0/1/2/3				
	$\overline{RCS}$0/1/2/3				
	$\overline{REN}$0/1/2/3				
	$\overline{EREN}$[3:0]				

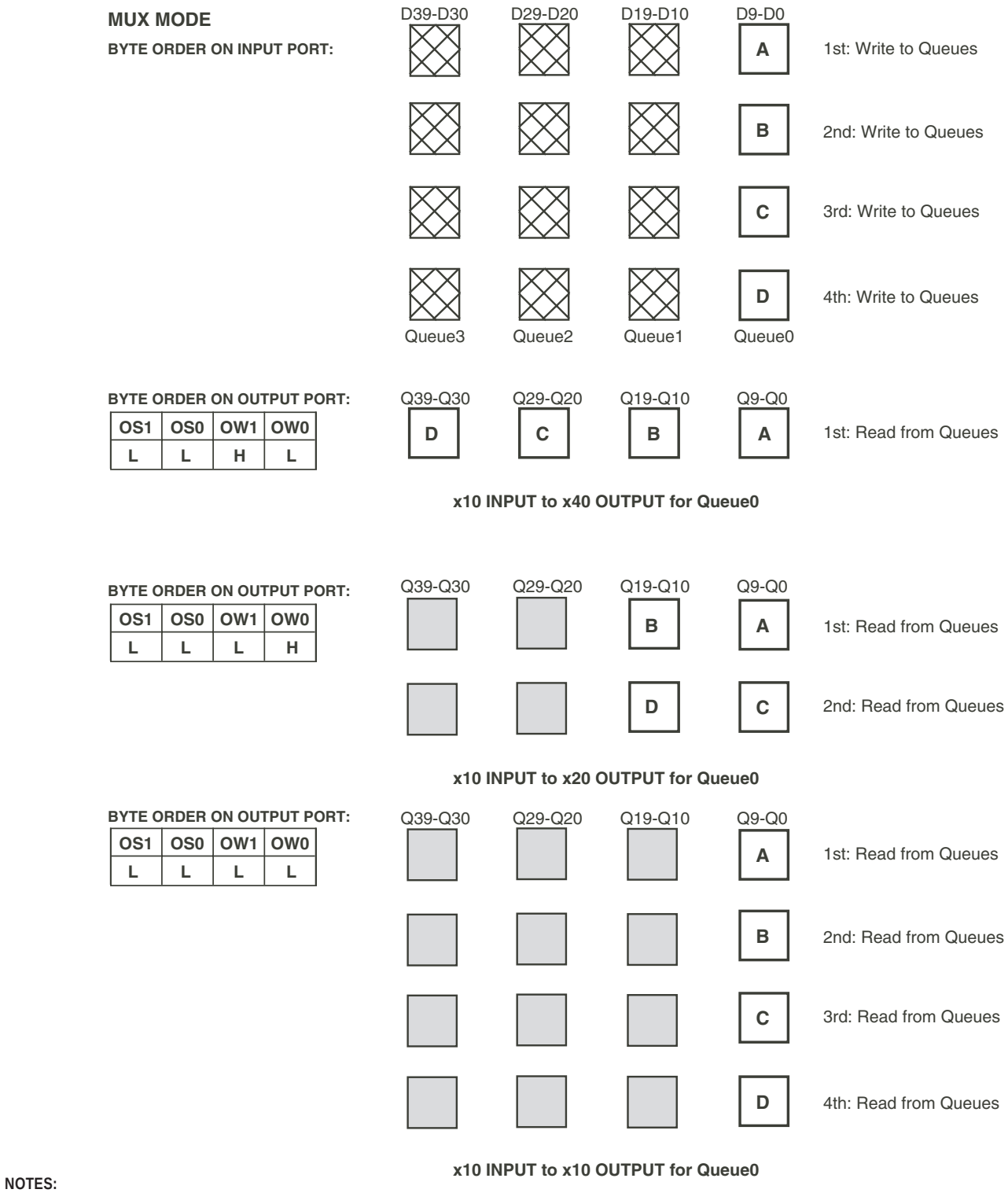


Figure 5. Bus-Matching Byte Arrangement (Mux Mode)

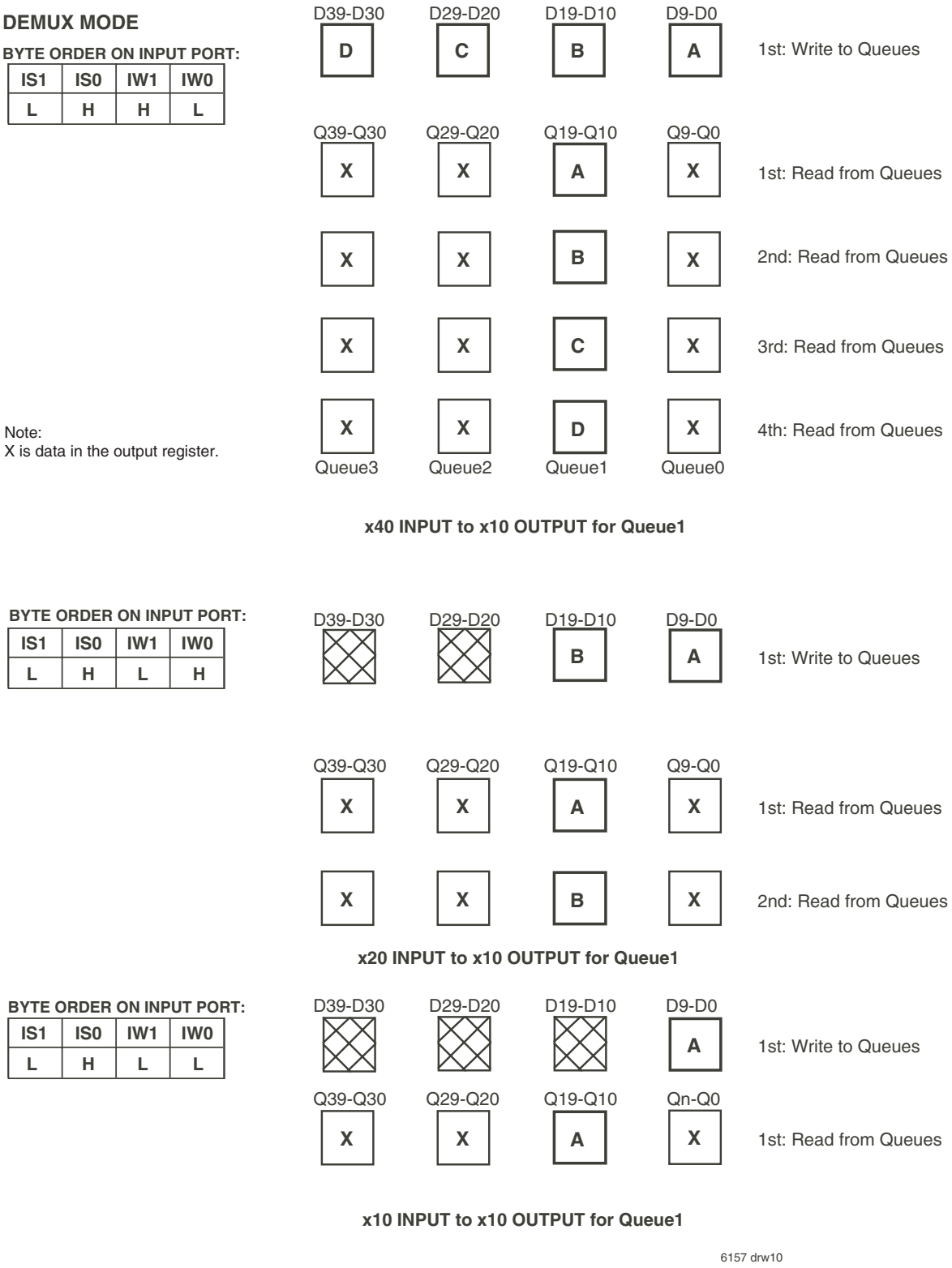


Figure 5. Bus-Matching Byte Arrangement (Demux Mode) (Continued)

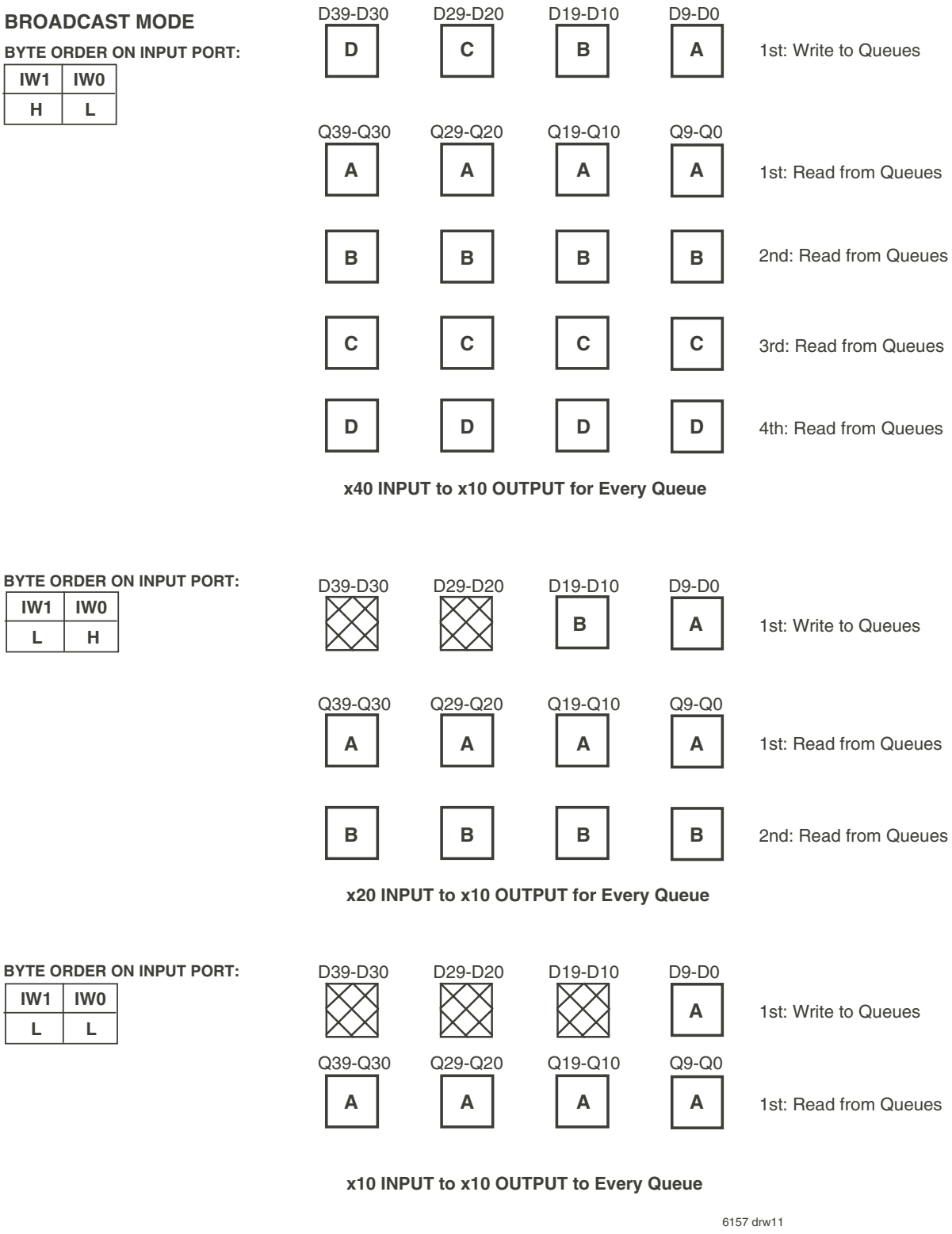


Figure 5. Bus-Matching Byte Arrangement (Broadcast Mode) (Continued)

SELECTABLE MODES

The device is capable of operating in three different modes, Mux, Demux, and Broadcast Write. Each of these three modes can be selected based on the MD[1:0] bits. These bits should be tied directly to VCC or GND as they are latched in during master reset. The state of the MD pins for each mode is summarized in Table 1 – Device Configuration.

Each mode has access to four dedicated Queues internally, with each Queue having densities of 327,680 bits for the IDT72T55248, 655,360 bits for the IDT72T55258 and 1,310,072 bits for the IDT72T55268. The density of each Queue is fixed and cannot be programmed. Also, the density does not change when the device is operating in single or double data rate, or when the device is utilizing the bus-matching feature.

The QuadMux flow-control device accommodates for all of the timing issues associated with converging multiple data rates onto one path. Such issues include clock skew, race conditions, and meeting setup and hold times. These issues are difficult to address when performing mux operations from external logic or within an FPGA, especially at higher frequencies. The complexity of the design makes it difficult to implement within an FPGA, where speed degradations occur as the circuit becomes more complicated.

MUX MODE

In Mux mode the device is configured as shown in the Mux mode block diagram on page 1. The device in this mode consists of four separate Queues: Queue 0, Queue 1, Queue 2 and Queue 3. The four Queues all have the same common read port, and the read control selecting which Queue to read from. The Mux mode can be used in applications where multiple incoming data rates from different data paths are being buffered to one common data rate and data bus.

WRITE PORT OPERATION

In Mux mode there are four independent write port controls for each individual Queue. Data can be written to any of the four Queues using its corresponding write clock, write enable, and write chip select. A data word will be written on the rising (and falling in DDR) edge of write clock provided $\overline{WEN}$ and write chip select are active. Note in double data rate the setup and hold times of the write enables and write chip selects are sampled with respect to the rising edge of its respective write clock only. The falling edge of WCLK does not sample the write enable and write chip select.

In FWFT mode the first word written to any Queue will automatically be placed onto the output bus of that respective Queue when selected on the read port via the OS[1:0] pins. There is a two cycle input pipeline and a two cycle output pipeline. It will take two cycles or three rising edges of the WCLK to move data from the write port to the queue and two cycles or those rising edges of RCLK to move data from the queue to the data outlines. This is regardless of the state of the corresponding read enable and read chip select, provided that the selected Queue was empty. This is not true in IDT Standard mode, where the first word written to a selected Queue must be accessed by setting $\overline{REN}$ and $\overline{RCS}$ are LOW on the rising edge of RCLK.

READ PORT OPERATION

In Mux mode the output select pins (OS[1:0]) determine which one of the four Queues the output bus will read data from. The output select pins are sampled on the rising edge of every RCLK, and may change on every clock edge. Thus there is no latency switching from one Queue to another. Note that in Mux mode only the RCLK0 is active, all other output read clocks are not used. The same applies to the read enable ($\overline{REN}$0) and read chip select ($\overline{RCS}$0). Data will be read on the rising (and falling in DDR) edge of read clock provided read enable and read chip select are active (LOW). When selecting a Queue for read operations the new word read from that Queue will be available immediately on the next clock edge after the new Queue is selected. For example, if OS[1:0] is set to 01 (Queue1) on RCLK edge 0, then on RCLK edge 1 (next read clock edge) data can be read from Queue1 if $\overline{REN}$0 and $\overline{RCS}$0 are enabled.

In FWFT mode, the first word written to a selected Queue will automatically be placed onto the output bus of that respective Queue regardless of the state of the corresponding read enable, provided that the selected Queue was empty and its corresponding output ready flag was inactive. This occurs due to the nature of the FWFT flag timing. There is a two cycle input pipeline and a two cycle output pipeline. It will take two cycles or three rising edges of the WCLK to move data from the write port to the queue and two cycles or those rising edges of RCLK to move data from the queue to the data outlines. Subsequent writes to the Queue that is not empty will not fall through to the output bus. Note in FWFT mode, during a Queue selection the next word available in the Queue will automatically fall through to the output bus regardless of the read enable and read chip select.

In IDT Standard mode, every word including the first word must be accessed by the read enable and read chip select. Unlike FWFT mode, during a Queue selection the next word available in the Queue will not automatically fall through to the output bus. The previous word that was read out of the read port will remain on the output bus if the $\overline{REN}$ and $\overline{RCS}$ select are HIGH.

DEMUX MODE

In Demux mode the device is configured as shown in the Demux mode block diagram on page 2. The device in this mode consists of four separate Queues: Queue 0, Queue 1, Queue 2 and Queue 3. The four Queues all have the same common write port, and the read control selecting which Queue to read from. The Demux mode can be used in applications where a single incoming data rate is being buffered to multiple outgoing data rates.

WRITE PORT OPERATION

In Demux mode the input select pins (IS[1:0]) determine which one of the four Queues the input bus will write data into. The input select pins are sampled on the rising edge of every WCLK, and may change on every clock edge. Thus there is no latency switching from one Queue to another. Note that in Demux mode only the WCLK0 is active, all other input write clocks are not used. The same applies to the write enable ($\overline{WEN}$0) and write chip select ($\overline{WCS}$0). Data will be written on the rising (and falling in DDR) edge of write clock provided $\overline{WEN}$ and $\overline{WCS}$ are active on the rising edge of the WCLK. Note in double data rate the setup and hold times of the $\overline{WEN}$ and $\overline{WCS}$ selects are sampled with respect to the rising edge of the write clock only. The falling edge of WCLK does not sample the write enable and write chip select. When selecting a Queue for write operations the next word can be written to that Queue immediately on the next clock edge after the new Queue is selected. For example, if IS[1:0] is set to 01 (Queue1) on WCLK edge 0, then on WCLK edge 1 (next read clock edge) data can be written to Queue1 if $\overline{WEN}$0 and $\overline{WCS}$0 are enabled.

In FWFT mode the first word written to a selected Queue will automatically be placed onto the output bus regardless of the state of the corresponding read enable, provided that the selected Queue was empty and its corresponding output ready flag was inactive. There is a two cycle input pipeline and a two cycle output pipeline. It will take two cycles or three rising edges of the WCLK to move data from the write port to the queue and two cycles or those rising edges of RCLK to move data from the queue to the data outlines. This occurs due to the nature of the FWFT flag timing. Subsequent writes to the Queue that is not empty will not fall through to the output bus. In IDT Standard mode, every word including the first word must be accessed by the read enable and read chip select.

READ PORT OPERATION

In Demux mode there are four independent read port controls for each individual Queue. Data can be read from any of the four Queues using its

corresponding read clock, read enable, and read chip select. A data word will be read on the rising (and falling in DDR) edge of read clock provided read enable and read chip select are active. There are also four individual output enables that will take the output bus to high-impedance. Note that data will be read from memory regardless of the state of the output enable $\overline{OE}$[3:0] pins. As explained above, in FWFT mode the first word written to each Queue will automatically be placed onto the output bus regardless of the of the state of the corresponding read enable. There is a two cycle input pipeline and a two cycle output pipeline. It will take two cycles or three rising edges of the WCLK to move data from the write port to the queue and two cycles or those rising edges of RCLK to move data from the queue to the data outlines.

BROADCAST WRITE MODE

In Broadcast Write mode the device is configured as shown in the Broadcast Write mode block diagram on page 2. The device in this mode consists of four separate Queues: Queue 0, Queue 1, Queue 2 and Queue 3. The four Queues all have one common write port which will write data into all four Queues simultaneously when a write operation is initiated, there is no write selection to write data into a specific Queue. The Broadcast Write mode can be used in applications where a single incoming data bus needs to be sent to multiple data paths simultaneously.

WRITE PORT OPERATION

In Broadcast Write mode there are no input or output select pins to select the individual Queues separately. The write port will write data into all four Queues simultaneously. Note that in Broadcast mode only the WCLK0 is active, all other input clocks are not used. The same applies to the write enable ($\overline{WEN}$0) and write chip select ($\overline{WCS}$0). Data will be written on the rising (and falling in DDR) edge of write clock provided write enable and write chip select are active (LOW) on the rising edge of write clock. Write operations are prohibited if any of the four Queues are being partially reset or any of their full flag status full ($\overline{FF}$ = LOW).

In FWFT mode, the first word written to a selected Queue will automatically be placed onto the output bus of that respective Queue regardless of the state of the corresponding read enable, provided that the selected Queue was empty and its corresponding output ready flag was inactive. There is a two cycle input pipeline and a two cycle output pipeline. It will take two cycles or three rising edges of the WCLK to move data from the write port to the queue and two cycles or those rising edges of RCLK to move data from the queue to the data outlines. This occurs due to the nature of the FWFT flag timing. Subsequent writes to the Queue that is not empty will not fall through to the output bus. In IDT Standard mode, every word including the first word must be accessed by the read enable and read chip select.

READ PORT OPERATION

In Broadcast Write mode there are four independent read port controls for each individual Queue. Data can be read from any of the four Queues using its corresponding read clock, read enable, and read chip select. A data word will be read on the rising (and falling in DDR) edge of read clock provided read enable and read chip select are active. There are also four individual output enables that will take the output bus to high-impedance. Note that data will be read from memory regardless of the state of the output enable $\overline{OE}$[3:0] pins.

SIGNAL DESCRIPTIONS

INPUTS:

DATA INPUT BUS (D[39:0])

The data input bus can be 40, 20, or 10 bits wide in Demux and Broadcast mode. D[39:0] are data inputs for the 40-bit wide data bus, D[19:0] are data inputs for 20-bit wide data bus, and D[9:0] are data inputs for the 10-bit wide data bus. In Mux mode the input bus will be 10 bits wide for each of the four internal Queues. D[9:0] are dedicated to Queue 0, D[19:10] are dedicated to Queue 1, D[29:20] are dedicated to Queue 2, and D[39:30] are dedicated to Queue 3. Data can be written into each of the four Queues on every WCLK cycle. There is a two cycle input pipeline and a two cycle output pipeline. It will take two cycles or three rising edges of the WCLK to move data from the write port to the queue and two cycles or those rising edges of RCLK to move data from the queue to the data outlines.

MASTER RESET ($\overline{MRS}$)

There is a single master reset available for all internal Queues in this device. A master reset is accomplished whenever the $\overline{MRS}$ input is taken to a LOW state. This operation sets the internal read and write pointers of all Queues to the first location in memory. The programmable almost empty flag will go LOW and the almost full flags will go HIGH.

If FWFT/SI signal is LOW during master reset then IDT Standard mode is selected. This mode utilizes the empty and full status flags from the $\overline{EF}$/$\overline{OR}$ and $\overline{FF}$/$\overline{IR}$ dual-purpose pin. During master reset, all empty flags will be set to LOW and all full flags will be set to HIGH.

If FWFT/SI signal is HIGH during master reset, then the First Word Fall Through mode is selected. This mode utilizes the input read and output ready status flags from the $\overline{EF}$/$\overline{OR}$ and $\overline{FF}$/$\overline{IR}$ dual-purpose pin. During master reset, all input ready flags will be set to LOW and all output ready flags will be set to HIGH.

All device configuration pins such as MD[1:0], OW[1:0], IW[1:0], IS[1:0], OS[1:0], WDDR, RDDR, IOSEL, PFM, FSEL[1:0] and FWFT/SI needs to be defined before the master reset cycle. During a master reset the output register is initialized to all zeros. If the output enable(s) are LOW during master reset, then the output bus will be LOW. If the output enable(s) are HIGH during master reset, then the output bus will be in High-impedance. $\overline{RCS}$ has no affect on the data outputs during master reset. If the output width OW[1:0] is configured to x10 or x20, then the unused outputs will be in high-impedance. A master reset is required after power up before a write operation to any Queue can take place. Master reset is an asynchronous signal and thus the read and write clocks can be free-running or idle during master reset. See Figure 10, *Master Reset Timing*, for the associated timing diagram.

PARTIAL RESET ($\overline{PRS}$0/1/2/3)

A partial reset is a means by which the user can reset both the read and write pointers of each individual Queue inside the device without changing the Queue's configuration. There are four dedicated partial reset signals that each correspond to an individual Queue. There are restrictions as to when partial reset can be performed that apply to each operating modes.

In Mux mode, partial reset may not be performed on the two Queues involved during Queue selection on the read port. For instance, if OS[1:0] is switching from 00 to 01 then $\overline{PRS}$0 and $\overline{PRS}$1 may not be enabled from the first rising RCLK edge with OS[1:0]=01 until three more rising RCLK edges have been received. In other words, partial reset may not be performed for a minimum of three RCLK cycles from the time a new Queue is selected. Also, if Queue0 or Queue1 are partially reset before the switch, the appropriate $\overline{PRS}$ signal must return HIGH at least t_{RSR} (reset recovery time) before the first RCLK edge with OS[1:0]=01. Any Queues not involved in the selection can be partially reset.

In Demux mode, partial reset may not be performed on the two Queues involved during Queue selection on the write port. For instance, if IS[1:0] is switching from 11 to 10 then $\overline{PRS}$3 and $\overline{PRS}$2 may not be enabled from the first rising WCLK edge with OS[1:0]=01 until three more rising WCLK edges have been received. In other words, partial reset may not be performed for a minimum of three WCLK cycles from the time a new Queue is selected. Also, if Queue0 or Queue1 are partially reset before the switch, the appropriate $\overline{PRS}$ signal must be HIGH at least t_{RSR} (reset recovery time) before the first WCLK edge with IS[1:0]=10. Any Queues not involved in the selection can be partially reset.

In Broadcast mode, partial reset may not be performed during write operations. The write enable and write chip select must be HIGH with respect to the rising edge of WCLK0 for a minimum of t_{RSS} before partial reset can be performed. If the device is operating in DDR mode, partial reset of any Queue must be initiated after the falling edge of WCLK0 to ensure data from the falling edge are written into all four Queues in memory. This maintains the data integrity of all four Queues in the device.

See Figures 11, 12, 13, *Partial Reset Timing*, for the associated timing diagram.

FIRST WORD FALL THROUGH/SERIAL IN (FWFT/SI)

This is a dual purpose pin. During Master Reset, the state of the FWFT/SI input determines whether the device will operate in IDT Standard mode or First Word Fall Through (FWFT) mode.

If FWFT/SI is LOW before the falling edge of master reset, then IDT Standard mode will be selected. This mode uses the Empty Flag ($\overline{EF}$) to indicate whether or not there are any words present in the Queues memory. It also uses the Full Flag function ($\overline{FF}$) to indicate whether or not the Queues memory has any free space for writing. In IDT Standard mode, every word read from the Queues, including the first, must be requested using the Read Enable ($\overline{REN}$), Read Chip Select ($\overline{RCS}$) and RCLK.

If FWFT/SI is HIGH before the falling edge of master reset, then FWFT mode will be selected. This mode uses Output Ready ($\overline{OR}$) to indicate whether or not there is valid data at the data outputs (Qn). It also uses Input Ready ($\overline{IR}$) to indicate whether or not the Queues have any free space for writing. In the FWFT mode, the first word written to an empty Queue goes directly to Qn after three RCLK rising edges, provided that the first RCLK meets t_{SKEW} parameters. There will be a one RCLK cycle delay if t_{SKEW} is not met. $\overline{REN}$ and $\overline{RCS}$ do not need to be enabled. Subsequent words must be accessed using the $\overline{REN}$, $\overline{RCS}$, and RCLK. $\overline{RCS}$ must be LOW or the outputs will be in a High-state.

The state of the FWFT/SI input must be kept at the present state for the minimum of the reset recovery time (t_{RSR}) after master reset. After this time, the FWFT/SI acts as a serial input for loading $\overline{PAE}$ and $\overline{PAF}$ offsets into the programmable offset registers. The serial input is used in conjunction with SCLK, $\overline{SWEN}$, $\overline{SREN}$, and SDO to access the offset registers. Serial programming using the FWFT/SI pin functions the same way in both IDT Standard and FWFT modes.

WRITE CLOCK (WCLK0/1/2/3)

There are a possible total of four write clocks available in this device depending on the mode selected, each corresponding to the individual Queues in memory. A write cycle is initiated on the rising and/or falling edge of the WCLK input. If the write double data rate (WDDR) mode pin is tied HIGH during master reset, data will be written on both the rising and falling edge of WCLK0/1/2/3, provided that $\overline{WEN}$0/1/2/3 and $\overline{WCS}$0/1/2/3 are enabled. If WDDR is tied LOW, data will be written only on the rising edge of WCLK0/1/2/3 provided that $\overline{WEN}$0/1/2/3 and $\overline{WCS}$0/1/2/3 are enabled. The four write clocks are completely independent of one another.

Data setup and hold times must be met with respect to the LOW-to-HIGH (and HIGH-to-LOW in DDR) transition of the write clock(s). It is permissible to stop the write clock(s). Note that while the write clocks are idle, the $\overline{FF}$/$\overline{IR}$0/1/2/3 and $\overline{PAF}$0/1/2/3 flags will not be updated unless it is operating in asynchronous timing mode (PFM=00). The write clocks can either be independent or coincident of one another.

In Demux and Broadcast Write mode, only the WCLK0 input is available. All other write clocks inputs should be tied to GND.

WRITE ENABLE ($\overline{WEN}$0/1/2/3)

There are a possible total of four write enables available in this device depending on the mode selected, one for each individual Queues in memory. When the write enable input is LOW on the rising edge of WCLK in single data rate, data is loaded on the rising edge of every WCLK cycle, provided the device is not full and the write chip select ($\overline{WCS}$) is enabled. The setup and hold times are referenced with respect to the rising edge of WCLK only. When the write enable input is LOW on the rising edge of WCLK in double data rate, data is loaded into the selected Queue on the rising and falling edge of every WCLK cycle, provided the device is not full and the write chip select ($\overline{WCS}$) is enabled. In this mode, the data setup and hold times are referenced with respect to the rising and falling edge of WCLK. Note that $\overline{WEN}$ and $\overline{WCS}$ are sampled only on the rising edge of WCLK in either data rate modes.

Data is stored in the Queues sequentially and independently of any ongoing read operation. When the write enable(s) and write chip select(s) are HIGH, no new data is written into the corresponding Queue on each WCLK cycle. The four write enables operate independent of one another.

In Demux and Broadcast mode, only the $\overline{WEN}$0 input is available. All other write enables should be tied to VCC.

WRITE CHIP SELECT ($\overline{WCS}$0/1/2/3)

There are a possible total of four write chip selects available in this device depending on the mode selected, one for each individual Queues in memory. The write chip selects disables all Write Port inputs for each individual Queue if it is held HIGH. To perform normal write operations for each individual Queue, the write chip select must be enabled, held LOW. The four write chip selects are completely independent of one another.

When the write chip select is LOW on the rising edge of WCLK in single data rate, data is loaded on the rising edge of every WCLK cycle, provided the device is not full and the write enable ($\overline{WEN}$) of the corresponding Queue is LOW. When the write chip select is LOW on the rising edge of WCLK in double data rate, data is loaded into the selected Queue on the rising and falling edge of every WCLK cycle, provided the device is not full and the write enable ($\overline{WEN}$) of the corresponding Queue is LOW.

When the write chip select is HIGH on the rising edge of WCLK in single data rate, the write port is disabled and no words are written on the rising edge of WCLK into the Queue, even if $\overline{WEN}$ is LOW. If the write chip select is HIGH on the rising edge of WCLK in double data rate, the write port is also disabled and no words are written on the rising and falling edge of WCLK into the Queue, even if $\overline{WEN}$ is LOW. Note that $\overline{WCS}$ is sampled on the rising edge of WCLK only in either data rate modes.

In Demux and Broadcast mode, only the $\overline{WCS}$0 input is available. All other write chip selects should be tied to VCC.

WRITE DOUBLE DATA RATE (WDDR)

When the write double data rate (WDDR) pin is HIGH prior to master reset, the write port will be set to double data rate mode. In this mode, all write operations are based on the rising and falling edge of the write clocks, provided that write enables and write chip selects are LOW for the rising clock edges. In double data rate the write enable signals are sampled with respect to the rising edge of write clock only, and a word will be written on both the rising and falling edge of write clock regardless of whether or not the write enables are active on the falling edge of write clock.

When WDDR is LOW, the write port will be set to single data rate mode. In this mode, all write operations are based on only the rising edge of the write clocks, provided that write enables and write chip selects are LOW during the rising edge of write clock. This pin should be tied HIGH or LOW and cannot toggle before or after master reset.

READ CLOCK (RCLK0/1/2/3)

There are a possible total of four read clocks available in this device depending on the mode selected, each corresponding to the individual Queues in memory. A read cycle is initiated on the rising and/or falling edge of the RCLK input. If the read double data rate (RDDR) mode pin is tied HIGH, data will be read on both the rising and falling edge of RCLK0/1/2/3, provided that $\overline{REN}$0/1/2/3 and $\overline{RCS}$0/1/2/3 are enabled. If RDDR is tied LOW, data will be read only on the rising edge of RCLK0/1/2/3 provided that $\overline{REN}$0/1/2/3 and $\overline{RCS}$0/1/2/3 are enabled. The four read clocks are completely independent of one another.

There is an associated data access time (tA) for the data to be read out of the Queues. It is permissible to stop the read clocks. Note that while the read clocks are idle, the $\overline{EF}$/$\overline{OR}$0/1/2/3 and $\overline{PAE}$0/1/2/3 flags will not be updated unless it is operating in asynchronous timing mode (PFM=0). The write and read clocks can either be independent or coincident.

In Mux mode, only the RCLK0 input is available. All other read clock inputs should be tied to GND.

READ ENABLE ($\overline{REN}$0/1/2/3)

There are a possible total of four read enables available in this device depending on the mode selected, one for each individual Queue in memory. When the read enable input is LOW on the rising edge of RCLK in single data rate, data will be read on the rising edge of every RCLK cycle, provided the device is not empty and the read chip select ($\overline{RCS}$) is enabled. The associated data access time (tA) is referenced with respect to the rising edge of RCLK. When the read enable input is LOW on the rising edge of RCLK in double data rate, will be read on the rising and falling edge of every RCLK cycle, provided the device is not empty and $\overline{RCS}$ is enabled. In this mode, the data access times are referenced with respect to the rising and falling edges of RCLK. Note that $\overline{REN}$ is sampled only on the rising edge of RCLK in either data rate modes.

Data is stored in the Queues sequentially and independently of any ongoing write operation. When the read enable(s) and read chip select(s) are HIGH, no new data is read on each RCLK cycle. The four read enables operate independent of one another.

To prevent reading from an empty Queue in the IDT Standard mode, the empty flag of each Queue will go LOW with respect to RCLK, when the total number of words in the Queue has been read out, thus inhibiting further read operations. Upon the completion of a valid write cycle, the empty flag will go HIGH with respect to RCLK two cycles later, thus allowing another read to occur, providing tSKEW of WCLK to RCLK is met.

In Mux mode, only the $\overline{REN}$0 input is available. All other read enables should be tied to VCC.

READ CHIP SELECT ($\overline{RCS}$0/1/2/3)

There are a possible total of four read chip selects available in this device, each corresponding to the individual Queue in memory. The read chip select inputs provides synchronous control of the read port for each individual Queue. When the read chip select is held LOW, the next rising edge of the correspond-

ing RCLK will enable the output bus. When the read chip select goes HIGH, the next rising edge of RCLK will send the output bus into high-impedance and prevent that RCLK from initiating a read, regardless of the state of $\overline{REN}$. During a master or partial Reset the read chip select input has no effect on the output bus, output enable ($\overline{OE}$[3:0]) is the only input that provides high-impedance control of the output bus. If output enable is LOW, the data outputs will be active regardless of read chip select until the first rising edge of RCLK after a reset is complete. Afterwards if read chip select is HIGH the data outputs will go to high-impedance. The four read chip selects are completely independent of one another.

The read chip select inputs do not affect the updating of the flags. For example, when the first word is written to any/all empty Queues, the empty flag(s) will still go from LOW to HIGH based on a rising edge of the RCLK(s), regardless of the state of the read chip select inputs. Also, when operating the Queue in FWFT mode the first word written to any/all empty Queues will still be clocked through to the output bus on the third rising edge of RCLK(s), regardless of the state of read chip select inputs, assuming that the t_{SKEW} parameter is met. For this reason the user should pay extra attention to the read chip selects when a data word is written to any/all empty Queues in FWFT mode. If the read chip select inputs are HIGH when an empty Queue is written into, the first word will fall through to the output register but will not be available on the outputs because they are in high-impedance. The user must enable the read chip selects on the next rising edge of RCLK to access this first word.

In Mux mode, only the $\overline{RCS}$0 input is available. All other read chip select inputs should be tied to V_{CC}.

READ DOUBLE DATA RATE (RDDR)

When the read double data rate (RDDR) pin tied HIGH, the read port will be set to double data rate mode, sampled during master reset. In this mode, all read operations are based on the rising and falling edge of the read clocks, provided that read enables and read chip selects are LOW. In double data rate mode, the read enable signals are sampled with respect to the rising edge of read clock only, and a word will be read from both the rising and falling edge of read clock regardless of whether or not read enable and read chip select are active on the falling edge of read clock.

When RDDR is tied LOW at master reset, the read port will be set to single data rate mode. In this mode, all read operations are based on only the rising edge of the read clocks, provided that read enables and read chip selects are LOW during the rising edge of read clock. This pin should be tied HIGH or LOW and cannot toggle before and after master reset.

OUTPUT ENABLE ($\overline{OE}$0/1/2/3)

There are a possible total of four asynchronous output enables available in this device, each corresponding to the individual Queues in memory. When the output enable inputs are LOW, the output bus of each individual Queue become active and drives the data currently in the output register. When the output enable inputs ($\overline{OE}$[3:0]) are HIGH, the output bus of each individual Queue goes into high-impedance. During master or partial Reset the output enable is the only input that can place the output data bus into high-impedance. During reset the read chip select input has no effect on the output data bus. The four output enable inputs are completely independent of one another.

In Mux mode, only the $\overline{OE}$0 input is available. All other output enable inputs should be tied to GND.

I/O SELECT (IOSEL)

The inputs and outputs of this device can be configured for either LVTTL or HSTL/eHSTL operation. If the IOSEL pin is HIGH during master reset, then all applicable LVTTL or HSTL signals will be configured for HSTL/eHSTL operating voltage levels. To select between HSTL or eHSTL VREF must be driven to 0.75V or 0.9V respectively.

If the IOSEL pin is LOW during master reset, then all applicable LVTTL or HSTL signals will be configured for LVTTL operating voltage levels. In this configuration VREF should be set to the static core voltage of 2.5V.

This pin should be tied HIGH or LOW and cannot toggle before or after master reset. Please refer to table ? for a list of applicable LVTTL/HSTL/eHSTL signals.

POWER DOWN ($\overline{PD}$)

This device has a power down feature intended for reducing power consumption for HSTL/eHSTL configured inputs when the device is idle for a long period of time. By entering the power down state certain inputs can be disabled, thereby significantly reducing the power consumption of the part. All $\overline{WEN}$ and $\overline{REN}$ signals must be disabled for a minimum of four WCLK and RCLK cycles before activating the power down signal. The power down signal is asynchronous and needs to be held LOW throughout the desired power down time. During power down, the following conditions for the inputs/outputs signals are:

- All data in Queue(s) are retained.
- All data inputs become inactive.
- All write and read pointers maintain their last value before power down.
- All enables, chip selects, and clock input pins become inactive.
- All data outputs become inactive and enter high-impedance state.
- All flag outputs will maintain their current states before power down.
- All programmable flag offsets maintain their values.
- All echo clocks and enables will become inactive and enter high-impedance state.
- The serial programming and JTAG port will become inactive and enter high-impedance state.
- All setup and configuration CMOS static inputs are not affected, as these pins are tied to a known value and do not toggle during operation.

All internal counters, registers, and flags will remain unchanged and maintain their current state prior to power down. Clock inputs can be continuous and free-running during power down, but will have no affect on the part. However, it is recommended that the clock inputs be low when the power down is active. To exit power down state and resume normal operations, disable the power down signal by bringing it HIGH. There must be a minimum of 1µs waiting period before read and write operations can resume. The device will continue from where it had stopped, no form of reset is required after exiting power down state. The power down feature does not provide any power savings when the inputs are configured for LVTTL operation. However, it will reduce the current for I/Os that are not tied directly to V_{CC} or GND. See Figure ?, for the associated timing diagram.

SERIAL CLOCK (SCLK)

The serial clock is used to load data and read data from in the programmable offset registers. Data from the serial input signal (FWFT/SI) can be loaded into the offset registers on the rising edge of SCLK provided that the serial write enable ($\overline{SWEN}$) signal is LOW. Data can be read from the offset registers via the serial data output (SDO) signal on the rising edge of SCLK provided that $\overline{SREN}$ is LOW. The serial clock can operate at a maximum frequency of 10MHz. The read operation is non-destructive. However, the write operation will change the flag offsets on each SCLK rising edge as data shifts into the registers.

SERIAL WRITE ENABLE ($\overline{SWEN}$)

The serial write enable input is an enable used for serial programming of the programmable offset registers. It is used in conjunction with the serial input

(FWFT/SI) and serial clock (SCLK) when programming the offset registers. When the serial write enable is LOW, data at the serial input is loaded into the offset register, one bit for each LOW-to-HIGH transition of SCLK. When serial write enable is HIGH, the offset registers retain the previous settings and no offsets are loaded. Serial write enable functions the same way in both IDT Standard and FWFT modes.

SERIAL READ ENABLE ($\overline{SREN}$)

The serial read enable input is an enable used for reading the value of the programmable offset registers. It is used in conjunction with the serial data output (SDO) and serial clock (SCLK) when reading the offset registers. When the serial read enable is LOW, data at the serial data output can be read from the offset register, one bit for each LOW-to-HIGH transition of SCLK. When serial read enable is HIGH, the reading of the offset registers will stop. Whenever serial read enable ($\overline{SREN}$) is activated values in the offset registers are read starting from the first location in the offset registers. The $\overline{SREN}$ HIGH to LOW transition copies the values in the offset registers directly into a serial scan out register. $\overline{SREN}$ must be kept LOW in order to read the entire contents of the offset register. If at any point $\overline{SREN}$ is toggled HIGH to LOW, another copy function from the offset register to the serial scan out register will occur. Serial read enable functions the same way in both IDT Standard and FWFT modes.

OUTPUTS:

DATA OUTPUT BUS (Q[39:0])

The data output bus can be 40, 20, or 10 bits wide in Mux mode. Q[39:0] are data outputs for the 40-bit wide data bus, Q[19:0] are data outputs for 20-bit wide data bus, and Q[9:0] are data outputs for the 10-bit wide data bus. In Demux and Broadcast mode the output bus will be 10 bits wide for each of the four internal Queues. Q[9:0] are dedicated to Queue 0, Q[19:10] are dedicated to Queue 1, Q[29:20] are dedicated to Queue 2, and Q[39:30] are dedicated to Queue 3. In FWFT mode, when switching from one Queue to another, the data of the newly selected Queue will always be present on the output bus two cycles after the next RCLK cycle after OS[1:0] is selected providing $\overline{RCS}$ is LOW regardless of whether or not $\overline{REN}$ is active. Thus each of the four Queues can be accessed on every RCLK cycle.

EMPTY/OUTPUT READY FLAG ($\overline{EF}$/$\overline{OR}$0/1/2/3)

There are four empty/output ready flags available in this device, each corresponding to the individual Queues in memory. This is a dual-purpose pin that is determined based on the state of the FWFT/SI pin during master reset for selecting one of the two timing modes of this device. In the IDT Standard mode, the empty flags are selected. When an individual Queue is empty, its empty flag will go LOW, inhibiting further read operations from that Queue. When the empty flag is HIGH, the individual Queue is not empty and valid read operations can be applied. See Figures 24, 25, Read Cycle, Empty Flag and First Word Latency Timing (IDT Standard Mode), for the relevant timing information. Also see Table 3 "Status Flags for IDT Standard Mode" for the truth table of the empty flags.

In FWFT mode, the output ready flags are selected. Output ready flags ($\overline{OR}$) go LOW at the same time that the first word written to an empty Queue appears on the outputs, which is a minimum of three read clock cycles provided the RCLK and WCLK meets the t_{SKEW} parameter. $\overline{OR}$ stays LOW after the RCLK LOW-to-HIGH transitions that shifts the last word from the Queue to the outputs. $\overline{OR}$ goes HIGH when an enabled read operation is performed to an empty queue. The previous data stays at the outputs, indicating the last word was read. Further data reads are inhibited until a new word is on the bus when $\overline{OR}$ goes LOW again. See Figures 21, 22, 23, *Read Timing (FWFT Mode*), for the relevant timing information. Also see Table 4 "Status Flags for FWFT Mode" for the truth table of the empty flags.

The empty/output ready flags are synchronous and updated on the rising edge of RCLK. In IDT Standard mode, the flags are double register-buffered outputs. In FWFT mode, the flags are triple register-buffered outputs. The four empty flags operate independent of one another and always indicate the respective Queue's status.

COMPOSITE EMPTY/OUTPUT READY FLAG ($\overline{CEF}$/$\overline{COR}$)

This status pin is used to determine the empty state of the current Queue selected. The composite empty/output ready flag represents the state of the Queue selected on the read port, such that the user does not have to monitor each individual Queues' empty/output ready flags. The composite empty/output ready flag is only available in Mux mode, since the output select bits (OS[1:0]) are used to select any one of the four Queues to read from.

The timing of the composite empty/output ready flag differs in IDT Standard and FWFT modes. In IDT Standard mode, when switching from one Queue to another, the composite empty flag will update to the status of the newly selected Queue one RCLK cycle after the rising edge of RCLK that made the new Queue selection. In FWFT mode, the composite output ready flag will update to the status of the newly selected Queue on two clock cycles after the rising edge of RCLK that made the new Queue selection. See Figures 26, 27 for the associated timing diagram. See Table 3 and 4 "Status Flags for IDT Standard and FWFT Mode " for the truth table of the composite empty flag.

FULL/INPUT READY FLAG ($\overline{FF}$/$\overline{IR}$0/1/2/3)

There are four full/input ready flags available in this device, each corresponding to the individual Queues in memory. This is a dual-purpose pin that is determined based on the state of the FWFT/SI pin during master reset for selecting the two timing modes of this device. In the IDT Standard mode, the full flags are selected. When an individual Queue is full, its full flags will go LOW after the rising edge of WCLK that wrote the last word, thus inhibiting further write operations to the Queue. When the full flag is HIGH, the individual Queue is not full and valid write operations can be applied. See Figures 14, 15, 16, Write Cycle, Full Flag and First Word Latency Timing (IDT Standard Mode), for the associated timing diagram. Also see Table 3 "Status Flags for IDT Standard Mode" for the truth table of the full flags.

In FWFT mode, the input ready flags are selected. Input ready flags go LOW when there is adequate memory space in the Queues for writing in data. The input ready flags go HIGH after the rising edge of WCLK that wrote the last word, when there are no free spaces available for writing in data. See Figures 17, 18, 19, *Write Timing (FWFT Mode*), for the associated timing information. Also see Table 4 "Status Flags for FWFT Mode" for the truth table of the full flags. The input ready status not only measures the depth of the Queues memory, but also counts the presence of a word in the output register. Thus, in FWFT mode, the total number of writes necessary to make $\overline{IR}$ HIGH is one greater than needed to set $\overline{FF}$ = LOW in IDT Standard mode.

In Broadcast mode, when any one of the four full flags becomes asserted, all write operations to every Queue will be disabled. This maintains data integrity throughout all four Queues for comparison. In all other modes, the full flag will only disable write operations to its corresponding Queue.

$\overline{FF}$/$\overline{IR}$ is synchronous and updated on the rising edge of WCLK. $\overline{FF}$/$\overline{IR}$ are double register-buffered outputs. The four full flags operate independent of one another, except in Broadcast mode.

To prevent data overflow in the IDT Standard mode, the full flag of each Queue will go LOW with respect to WCLK, when the maximum number of words has been written into the Queue, thus inhibiting further write operations. Upon the

completion of a valid read cycle, the full flag will go HIGH with respect to WCLK two cycles later, thus allowing another write to occur, provided tSKEW has been met.

To prevent data overflow in the FWFT mode, the input ready flag of each Queue will go HIGH with respect to WCLK, when the maximum number of words has been written into the Queue, thus inhibiting further write operations. Upon the completion of a valid read cycle, the input ready flag will go LOW with respect to WCLK two cycles later, thus allowing another write to occur, provided tSKEW has been met.

COMPOSITE FULL/INPUT READY FLAG ($\overline{CFF}/\overline{CIR}$)

This status pin is used to determine the full state of the current Queue selected. The composite full/input ready flag represents the state of the Queue selected on the write port, such that the user does not have to monitor each individual Queues' full/input ready flags. The composite full/input ready flag is only available in both Demux and Broadcast modes. When switching from one Queue to another, the composite full/input ready flag will update to the status of the newly selected Queue one WCLK cycle after the rising edge of WCLK that made the new Queue selection, regardless of which timing mode the device is operating in. See Figure ? for the relevant associated timing diagram. See Table ? and ? "Status Flags for IDT Standard and FWFT Mode " for the truth table of the composite full flag

PROGRAMMABLE ALMOST EMPTY FLAG ($\overline{PAE}$0/1/2/3)

There are four programmable almost empty flags available in this device, each corresponding to the individual Queues in memory. The programmable almost empty flag is an additional status flag that notifies the user when the Queue is near empty. The user may utilize this feature as an early indicator as to when the Queue will become empty. In IDT Standard mode, $\overline{PAE}$ will go LOW when there are n words or less in the Queue. In FWFT mode, the $\overline{PAE}$ will go LOW when there are n-1 words or less in the Queue. The offset "n" is the empty offset value. The default setting for this value is stated in Table ?. Since there are four internal Queues hence four $\overline{PAE}$ offset values, n0, n1, n2, and n3.

There are two timing modes available for the $\overline{PAE}$ flags, selectable by the state of the Programmable Flag Mode (PFM) pin during master reset. If PFM is tied HIGH, then synchronous timing mode is selected. If PFM is tied LOW, then asynchronous timing mode is selected. In synchronous $\overline{PAE}$ configuration, the $\overline{PAE}$ flag is updated on the rising edge of RCLK. In asynchronous $\overline{PAE}$ configuration, the $\overline{PAE}$ flag is asserted LOW on the LOW-to-HIGH transitions of the Read Clock (RCLK). $\overline{PAE}$ is reset to HIGH on the LOW-to-HIGH transitions of the Write Clock (WCLK). See Figure ? and ?, Synchronous and Asynchronous Programmable Almost-Empty Flag Timing (IDT Standard and FWFT mode), for the relevant timing information.

The four programmable almost empty flags operate independent of one another.

PROGRAMMABLE ALMOST FULL FLAG ($\overline{PAF}$0/1/2/3)

There are four programmable almost full flags available in this device, each corresponding to the individual Queues in memory. The programmable almost full flag is an additional status flag that notifies the user when the Queue is nearly full. The user may utilize this feature as an early indicator as to when the Queue will not be able to accept any more data and thus prevent data from being dropped. In IDT Standard mode, if no reads are performed after master reset, $\overline{PAF}$ will go LOW after (D-m) (D meaning the density of the particular device) words are written to the Queue. In FWFT mode, $\overline{PAF}$ will go LOW after (D+1-m) words are written to the Queue. The offset "m" is the full offset value. The default setting for this value is stated in Table 2. Since there are four internal Queues hence four $\overline{PAF}$ offset values, m0, m1, m2, and m3.

There are two timing modes available for the $\overline{PAF}$ flags, selectable by the state of the Programmable Flag Mode (PFM) pin during master reset. If PFM is tied HIGH, then synchronous timing mode is selected. If PFM is tied LOW, then asynchronous timing mode is selected. In synchronous $\overline{PAF}$ configuration, the $\overline{PAF}$ flag is updated on the rising edge of WCLK. In asynchronous $\overline{PAF}$ configuration, the $\overline{PAF}$ flag is asserted LOW on the LOW-to-HIGH transitions of the Write Clock (WCLK). $\overline{PAF}$ is reset to HIGH on the LOW-to-HIGH transitions of the Read Clock (RCLK). See Figures 35 and 37, Synchronous and Asynchronous Programmable Almost-Full Flag Timing (IDT Standard and FWFT mode), for the relevant timing information.

The four programmable almost full flags operate independent of one another.

TABLE 6 — TSKEW MEASUREMENT

Data Port Configuration	Status Flags	TSKEW Measurement	Datasheet Parameter
DDR Input to DDR Output	$\overline{EF}/\overline{OR}$	Negative Edge WCLK to Positive Edge RCLK	tSKEW2
	$\overline{FF}/\overline{IR}$	Negative Edge RCLK to Positive Edge WCLK	tSKEW2
	$\overline{PAE}$	Negative Edge WCLK to Positive Edge RCLK	tSKEW3
	$\overline{PAF}$	Negative Edge RCLK to Positive Edge WCLK	tSKEW3
DDR Input to SDR Output	$\overline{EF}/\overline{OR}$	Negative Edge WCLK to Positive Edge RCLK	tSKEW2
	$\overline{FF}/\overline{IR}$	Positive Edge RCLK to Positive Edge WCLK	tSKEW1
	$\overline{PAE}$	Negative Edge WCLK to Positive Edge RCLK	tSKEW3
	$\overline{PAF}$	Positive Edge RCLK to Positive Edge WCLK	tSKEW3
SDR Input to DDR Output	$\overline{EF}/\overline{OR}$	Positive Edge WCLK to Positive Edge RCLK	tSKEW1
	$\overline{FF}/\overline{IR}$	Negative Edge RCLK to Positive Edge WCLK	tSKEW2
	$\overline{PAE}$	Positive Edge WCLK to Positive Edge RCLK	tSKEW3
	$\overline{PAF}$	Negative Edge RCLK to Positive Edge WCLK	tSKEW3
SDR Input to SDR Output	$\overline{EF}/\overline{OR}$	Positive Edge WCLK to Positive Edge RCLK	tSKEW1
	$\overline{FF}/\overline{IR}$	Positive Edge RCLK to Positive Edge WCLK	tSKEW1
	$\overline{PAE}$	Positive Edge WCLK to Positive Edge RCLK	tSKEW3
	$\overline{PAF}$	Positive Edge RCLK to Positive Edge WCLK	tSKEW3

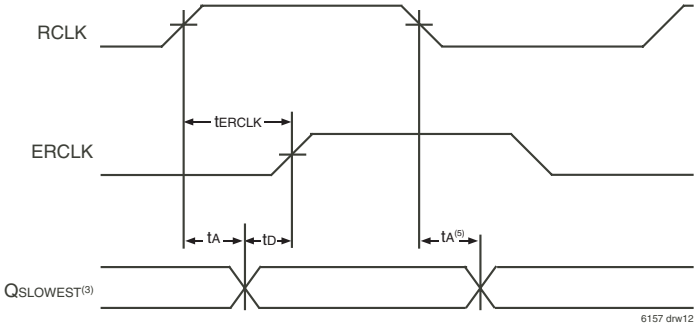
ECHO READ CLOCK (ERCLK0/1/2/3)

There are four echo read clock outputs available in this device, each corresponding to their respective input read clocks in the Queue. The echo read clock is a free-running clock output, that will always follow the RCLK input regardless of the read enables and read chip selects. The ERCLK output follows the RCLK input with an associated delay. This delay provides the user with a more effective read clock source when reading data from the output bus. This is especially helpful at high speeds when variables within the device may cause changes in the data access times. These variations in access time may be caused by ambient temperature, supply voltage, or device characteristics.

Any variations effecting the data access time will also have a corresponding effect on the echo read clock output produced by the device, therefore the echo read clock output level transitions should always be at the same position in time relative to the data outputs. Note, that echo read clock is guaranteed by design to be slower than the slowest data outputs. Refer to Figure 6, *Echo Read Clock and Data Output Relationship*, Figure 27, *Echo Read Clock and Read Enable Operation in Double Data Rate Mode* and Figure 28, *Echo RCLK and Echo $\overline{REN}$ Operation* for timing information. The four echo read clock outputs operate independent of one another and are direct copies of their respective RCLK inputs.

ECHO READ ENABLE ($\overline{EREN}$0/1/2/3)

There are four echo read enable outputs available in this device, each corresponding to the individual Queues in memory. The echo read enable output is provided to be used in conjunction with the echo read clock and provides the device receiving data from the Queue with a more effective scheme for reading the Queues' data. The echo read enable output is controlled by internal logic that becomes active for the read clock cycle that a new word is read out of the Queue. That is, a rising edge of read clock will cause echo read enable to go LOW, if both read enable and read chip select are active and the Queue is not empty. In other words, every cycle puts data on the output bus and drives $\overline{EREN}$ output to the LOW.



NOTES:
1. $\overline{REN}$ is LOW. $\overline{OE}$ is LOW.
2. $t_{ERCLK} > t_A$, guaranteed by design.
3. Qslowest is the data output with the slowest access time, t_A.
4. Time, t_D is greater than zero, guaranteed by design.
5. DDR mode clocks data on rising and falling edge of RCLK.

Figure 6. Echo Read Clock and Data Output Relationship

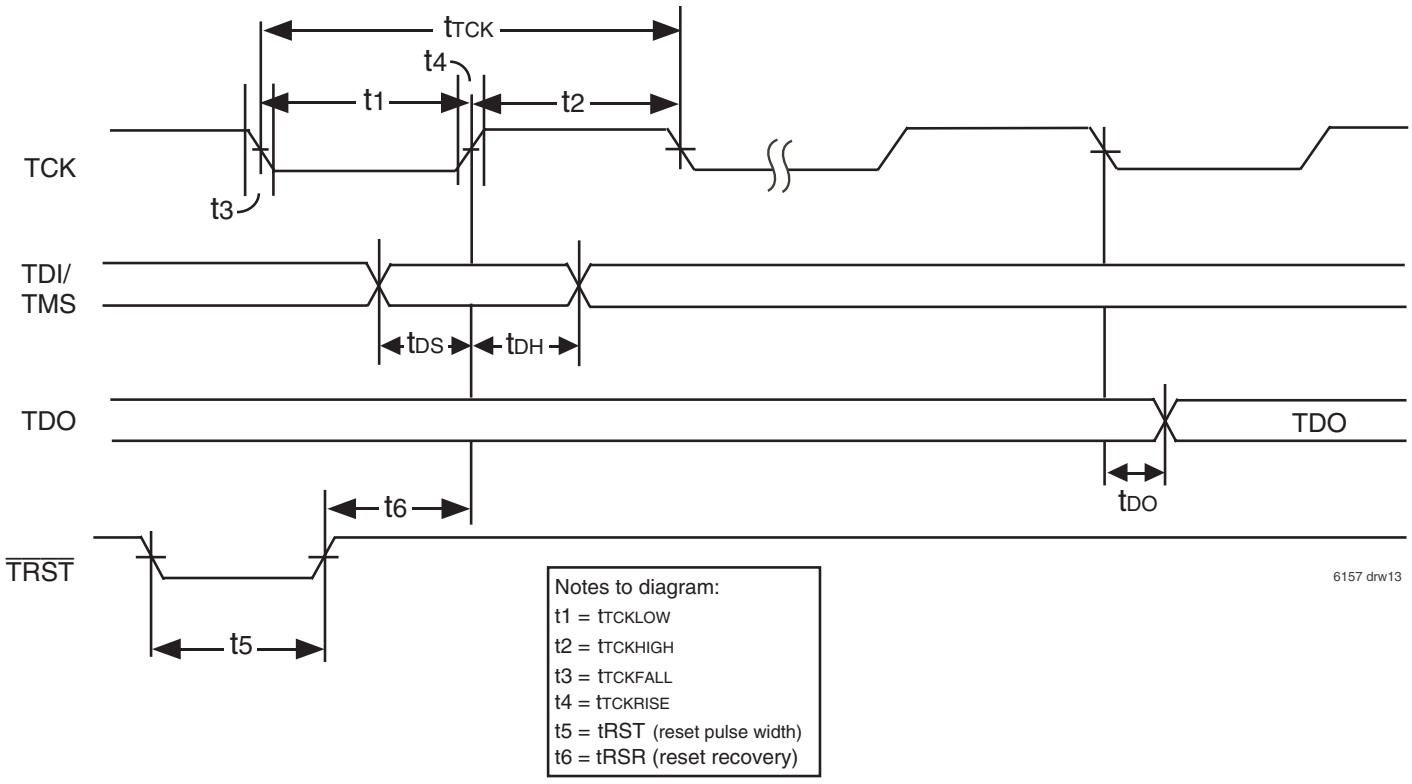


Figure 7. Standard JTAG Timing

SYSTEM INTERFACE PARAMETERS

Parameter	Symbol	Test Conditions	IDT72T55248 IDT72T55258 IDT72T55268		
			Min.	Max.	Units
Data Output	t_{DO}[1]		-	20	ns
Data Output Hold	t_{DOH}[1]		0	-	ns
Data Input	t_{DS}	trise=3ns	10	-	ns
	t_{DH}	tfall=3ns	10	-	

NOTE:
1. 50pf loading on external output signals.

JTAG AC ELECTRICAL CHARACTERISTICS

(Vcc = 3.3V ± 5%; Tambient (Industrial) = 0°C to +85°C)

Parameter	Symbol	Test Conditions			
			Min.	Max.	Units
JTAG Clock Input Period	tTCK	-	100	-	ns
JTAG Clock HIGH	tTCKHIGH	-	40	-	ns
JTAG Clock Low	tTCKLOW	-	40	-	ns
JTAG Clock Rise Time	tTCKRISE	-	-	5[1]	ns
JTAG Clock Fall Time	tTCKFALL	-	-	5[1]	ns
JTAG Reset	tRST	-	50	-	ns
JTAG Reset Recovery	tRSR	-	50	-	ns

NOTE:
1. Guaranteed by design.

JTAG TIMING SPECIFICATIONS (IEEE 1149.1 COMPLIANT)

The JTAG test port in this device is fully compliant with the IEEE Standard Test Access Port (IEEE 1149.1) specifications. Five additional pins (TDI, TDO, TMS, TCK and $\overline{TRST}$) are provided to support the JTAG boundary scan interface. Note that IDT provides appropriate Boundary Scan Description Language program files for these devices.

The Standard JTAG interface consists of seven basic elements:

- *Test Access Port (TAP)*
- *TAP controller*
- *Instruction Register (IR)*
- *Data Register Port (DR)*
- *Bypass Register (BYR)*
- *ID Code Register*
- *Flag Programming*

The following sections provide a brief description of each element. For a complete description refer to the IEEE Standard Test Access Port Specification (IEEE Std. 1149.1-1990).

The Figure below shows the standard Boundary-Scan Architecture

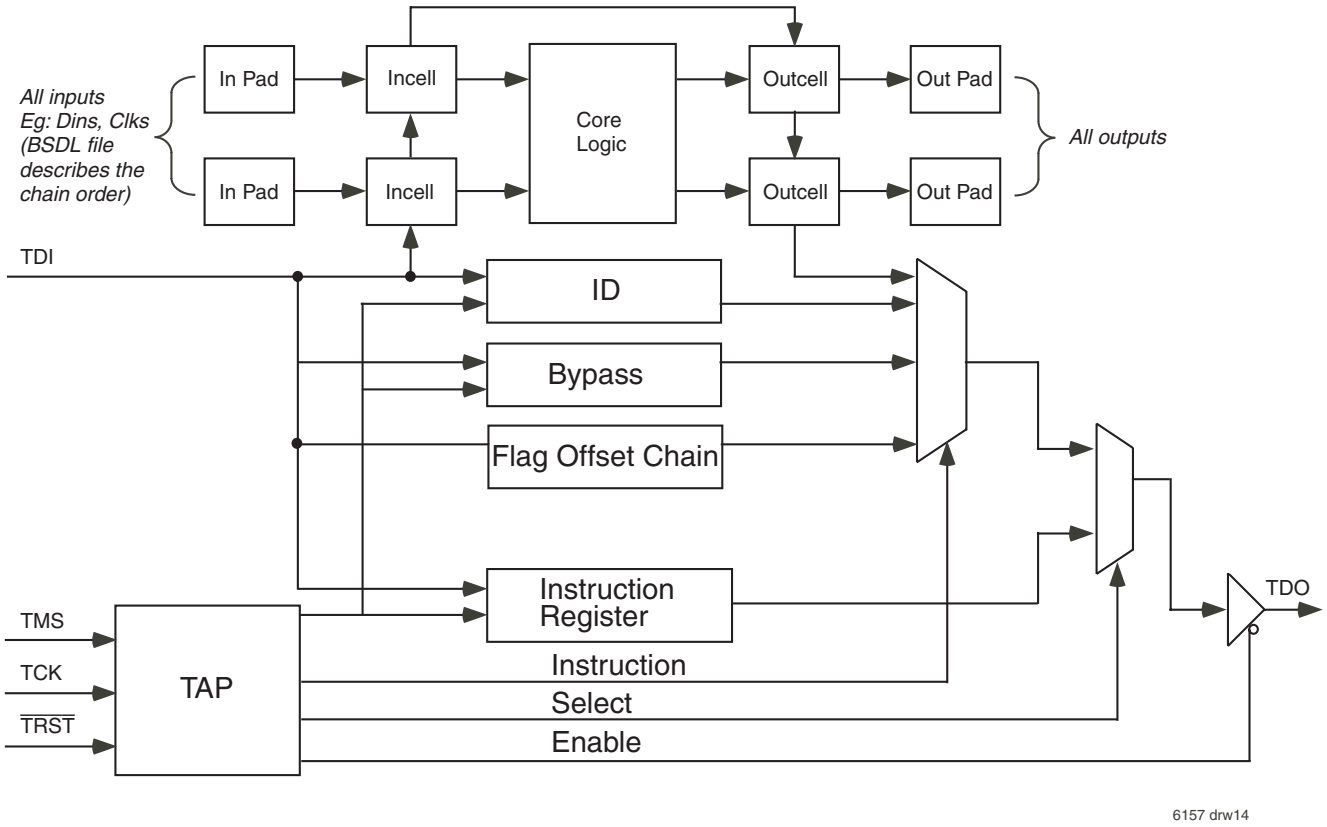


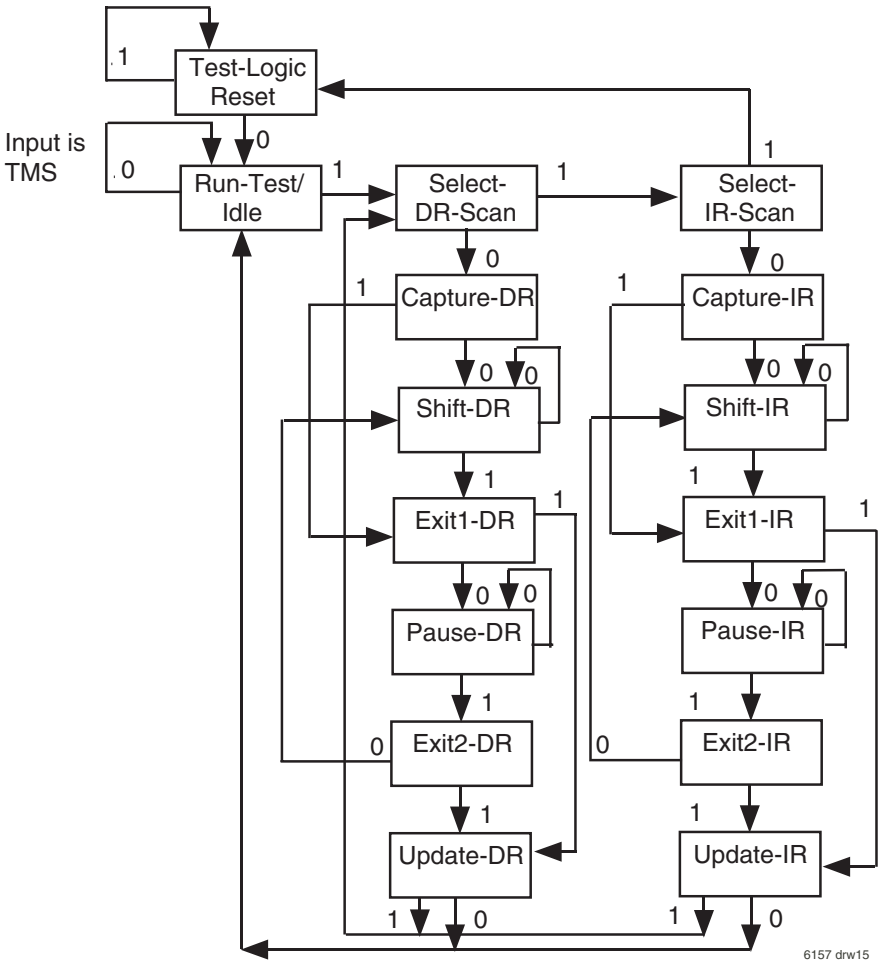
Figure 8. JTAG Architecture

TEST ACCESS PORT (TAP)

The TAP interface is a general-purpose port that provides access to the internal JTAG state machine. It consists of four input ports (TCLK, TMS, TDI, $\overline{TRST}$) and one output port (TDO).

THE TAP CONTROLLER

The TAP controller is a synchronous finite state machine that responds to TMS and TCLK signals to generate clock and control signals to the Instruction and Data Registers for capture and updating of data passed through the TDI serial input.



NOTES:
1. Five consecutive 1's at TMS will reset the TAP.
2. TAP controller resets automatically upon power-up.

Figure 9. TAP Controller State Diagram

Refer to the IEEE Standard Test Access Port Specification (IEEE Std. 1149.1) for the full state diagram

All state transitions within the TAP controller occur at the rising edge of the TCLK pulse. The TMS signal level (0 or 1) determines the state progression that occurs on each TCLK rising edge. The TAP controller takes precedence over the Queue operation and must be reset after power up of the device. See $\overline{TRST}$ description for more details on TAP controller reset.

Test-Logic-Reset All test logic is disabled in this controller state enabling the normal operation of the IC. The TAP controller state machine is designed in such a way that, no matter what the initial state of the controller is, the Test-Logic-Reset state can be entered by holding TMS at high and pulsing TCK five times. This is the reason why the Test Reset ($\overline{TRST}$) pin is optional.

Run-Test-Idle In this controller state, the test logic in the IC is active only if certain instructions are present. For example, if an instruction activates the self test, then it will be executed when the controller enters this state. The test logic in the IC is idle otherwise.

Select-DR-Scan This is a controller state where the decision to enter the Data Path or the Select-IR-Scan state is made.

Select-IR-Scan This is a controller state where the decision to enter the Instruction Path is made. The Controller can return to the Test-Logic-Reset state other wise.

Capture-IR In this controller state, the shift register bank in the Instruction Register parallel loads a pattern of fixed values on the rising edge of TCK. The last two significant bits are always required to be “01”.

Shift-IR In this controller state, the instruction register gets connected between TDI and TDO, and the captured pattern gets shifted on each rising edge of TCK. The instruction available on the TDI pin is also shifted in to the instruction register. TDO changes on the falling edge of TCK.

Exit1-IR This is a controller state where a decision to enter either the Pause-IR state or Update-IR state is made.

Pause-IR This state is provided in order to allow the shifting of instruction register to be temporarily halted.

Exit2-DR This is a controller state where a decision to enter either the Shift-IR state or Update-IR state is made.

Update-IR In this controller state, the instruction in the instruction register scan chain is latched in to the register of the Instruction Register on every falling edge of TCK. This instruction also becomes the current instruction once it is latched.

Capture-DR In this controller state, the data is parallel loaded in to the data registers selected by the current instruction on the rising edge of TCK.

Shift-DR, Exit1-DR, Pause-DR, Exit2-DR and Update-DR These controller states are similar to the Shift-IR, Exit1-IR, Pause-IR, Exit2-IR and Update-IR states in the Instruction path.

THE INSTRUCTION REGISTER

The instruction register (IR) is eight bits long and tells the device what instruction is to be executed. Information contained in the instruction includes the mode of operation (either normal mode, in which the device performs its normal logic function, or test mode, in which the normal logic function is inhibited or altered), the test operation to be performed, which of the four data registers is to be selected for inclusion in the scan path during data-register scans, and the source of data to be captured into the selected data register during Capture-DR.

TEST DATA REGISTER

The Test Data register contains three test data registers: the Bypass, the Boundary Scan register and Device ID register.

These registers are connected in parallel between a common serial input and a common serial data output.

The following sections provide a brief description of each element. For a complete description, refer to the IEEE Standard Test Access Port Specification (IEEE Std. 1149.1-1990).

TEST BYPASS REGISTER

The register is used to allow test data to flow through the device from TDI to TDO. It contains a single stage shift register for a minimum length in the serial path. When the bypass register is selected by an instruction, the shift register stage is set to a logic zero on the rising edge of TCLK when the TAP controller is in the Capture-DR state.

The operation of the bypass register should not have any effect on the operation of the device in response to the BYPASS instruction.

THE BOUNDARY-SCAN REGISTER

The boundary-scan register (BSR) is 48 bits long. It contains one boundary-scan cell (BSC) for each normal-function input pin and one BSC for each normal-function I/O pin (one single cell for both input data and output data). The BSR is used 1) to store test data that is to be applied externally to the device output pins, and/or 2) to capture data that appears internally at the outputs of the normal on-chip logic and/or externally at the device input pins.

THE DEVICE IDENTIFICATION REGISTER

The Device Identification Register is a Read Only 32-bit register used to specify the manufacturer, part number and version of the device to be determined through the TAP in response to the IDCODE instruction.

IDT JEDEC ID number is 0xB3. This translates to 0x33 when the parity is dropped in the 11-bit Manufacturer ID field.

For the IDT72T55248/72T55258/72T55268, the Part Number field contains the following values:

Device	Part# Field
IDT72T55248	04C9 (hex)
IDT72T55258	04CA (hex)
IDT72T55268	04CB (hex)

31(MSB) 28	27 12	11 1	0(LSB)
Version (4 bits) 0000	Part Number (16-bit)	Manufacturer ID (11-bit) 0033 (hex)	1

IDT72T55248/258/268 JTAG Device Identification Register

JTAG INSTRUCTION REGISTER

The Instruction register allows an instruction to be serially input into the device when the TAP controller is in the Shift-IR state. The instruction is decoded to perform the following:

- Select test data registers that may operate while the instruction is current. The other test data registers should not interfere with chip operation and the selected data register.
- Define the serial test data register path that is used to shift data between TDI and TDO during data register scanning.

The Instruction Register is a 4 bit field (i.e. IR3, IR2, IR1, IR0) to decode 16 different possible instructions. Instructions are decoded as follows.

Hex Value	Instruction	Function
0000	EXTEST	Test external pins
0001	SAMPLE/PRELOAD	Select boundary scan register
0002	IDCODE	Selects chip identification register
0003	CLAMP	Fix the output chains to scan chain values
0004	HIGH-IMPEDANCE	Puts all outputs in high-impedance state
0007	OFFSET READ	Read $\overline{PAE}$/$\overline{PAF}$ offset register values
0008	OFFSET WRITE	Write $\overline{PAE}$/$\overline{PAF}$ offset register values
000F	BYPASS	Select bypass register
	Private	Several combinations are private (for IDT internal use). Do not use codes other than those identified above.

JTAG INSTRUCTION REGISTER DECODING

The following sections provide a brief description of each instruction. For a complete description refer to the IEEE Standard Test Access Port Specification (IEEE Std. 1149.1-1990).

EXTEST

The required EXTEST instruction places the device into an external boundary-test mode and selects the boundary-scan register to be connected between TDI and TDO. During this instruction, the boundary-scan register is accessed to drive test data off-chip via the boundary outputs and receive test data off-chip via the boundary inputs. As such, the EXTEST instruction is the workhorse of IEEE. Std 1149.1, providing for probe-less testing of solder-joint opens/shorts and of logic cluster function.

SAMPLE/PRELOAD

The required SAMPLE/PRELOAD instruction allows the device to remain in a normal functional mode and selects the boundary-scan register to be connected between TDI and TDO. During this instruction, the boundary-scan register can be accessed via a data scan operation, to take a sample of the functional data entering and leaving the device. This instruction is also used to preload test data into the boundary-scan register before loading an EXTEST instruction.

IDCODE

The optional IDCODE instruction allows the device to remain in its functional mode and selects the optional device identification register to be connected between TDI and TDO. The device identification register is a 32-bit shift register containing information regarding the device manufacturer, device type, and version code. Accessing the device identification register does not interfere with the operation of the device. Also, access to the device identification register should be immediately available, via a TAP data-scan operation, after power-up of the device or after the TAP has been reset using the optional $\overline{TRST}$ pin or by otherwise moving to the Test-Logic-Reset state.

CLAMP

The optional CLAMP instruction sets the outputs of an device to logic levels determined by the contents of the boundary-scan register and selects the one-bit bypass register to be connected between TDI and TDO. Before loading this instruction, the contents of the boundary-scan register can be preset with the SAMPLE/PRELOAD instruction. During this instruction, data can be shifted through the bypass register from TDI to TDO without affecting the condition of the outputs.

HIGH-IMPEDANCE

The optional High-Impedance instruction sets all outputs (including two-state as well as three-state types) of an device to a disabled (high-impedance) state and selects the one-bit bypass register to be connected between TDI and TDO. During this instruction, data can be shifted through the bypass register from TDI to TDO without affecting the condition of the device outputs.

OFFSET READ

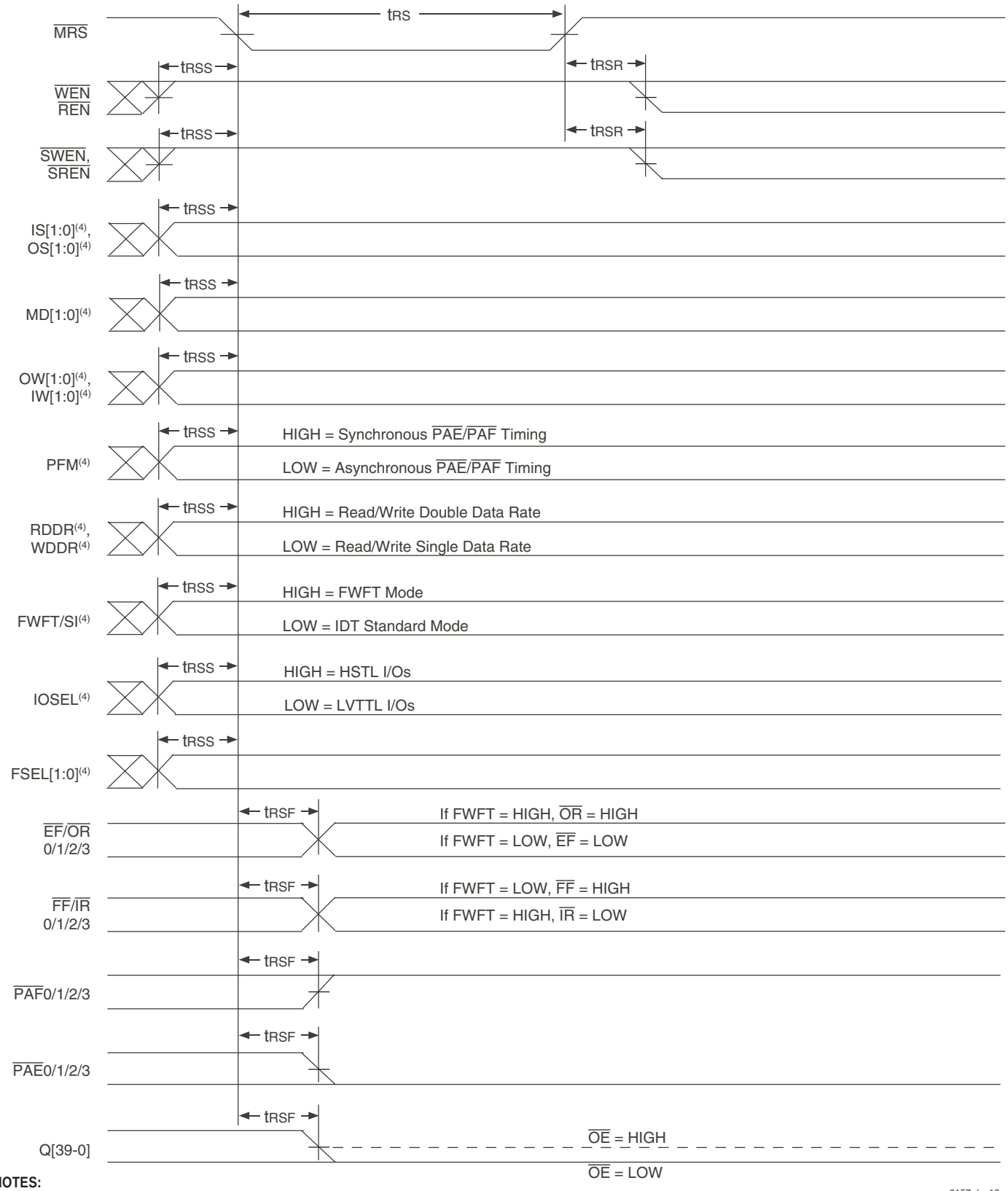
This instruction is an alternative to serial reading the offset registers for the $\overline{PAE}/\overline{PAF}$ flags. When reading the offset registers through this instruction, the dedicated serial programming signals must be disabled.

OFFSET WRITE

This instruction is an alternative to serial programming the offset registers for the $\overline{PAE}/\overline{PAF}$ flags. When writing the offset registers through this instruction, the dedicated serial programming signals must be disabled.

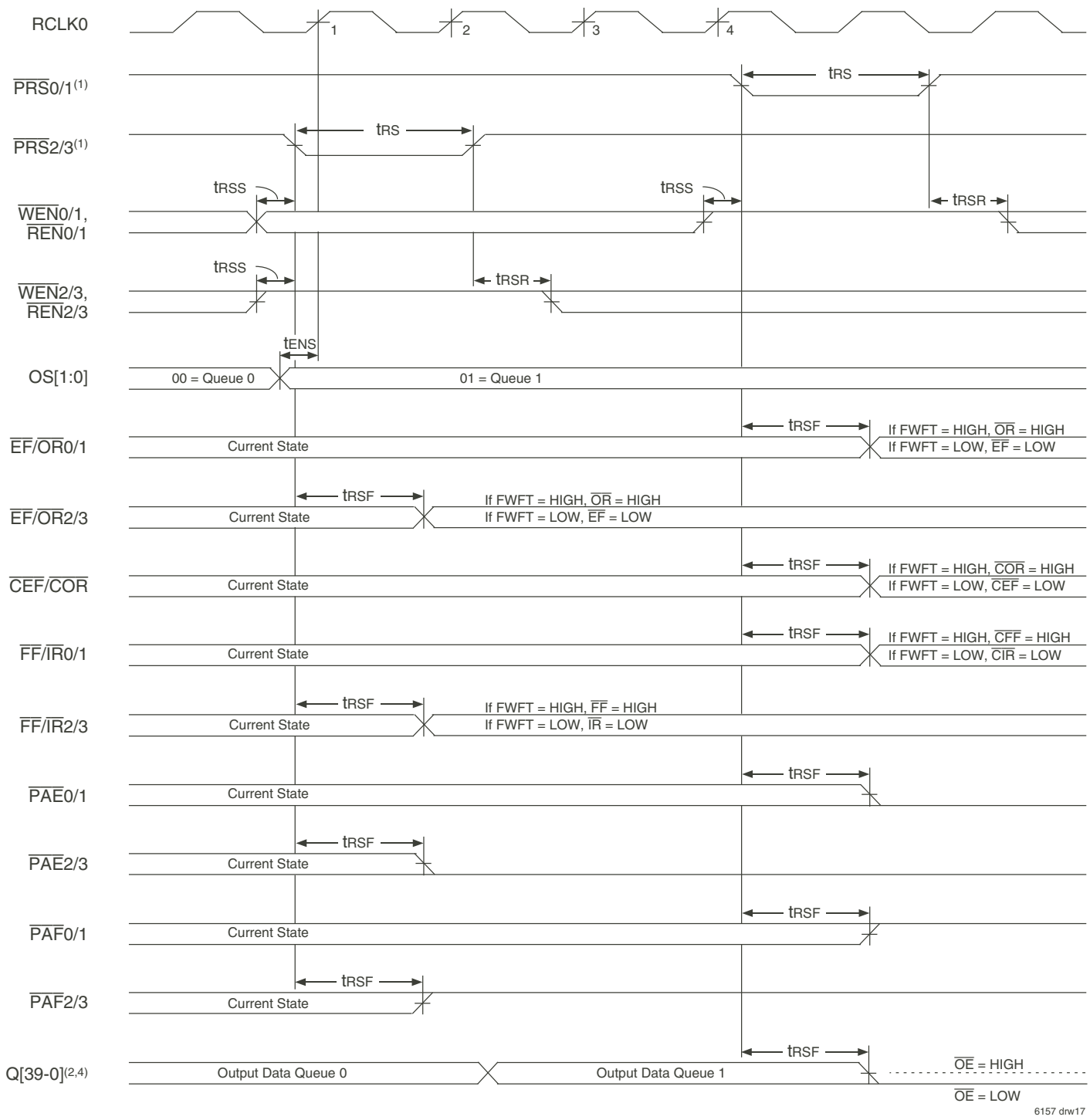
BYPASS

The required BYPASS instruction allows the device to remain in a normal functional mode and selects the one-bit bypass register to be connected between TDI and TDO. The BYPASS instruction allows serial data to be transferred through the IC from TDI to TDO without affecting the operation of the device.



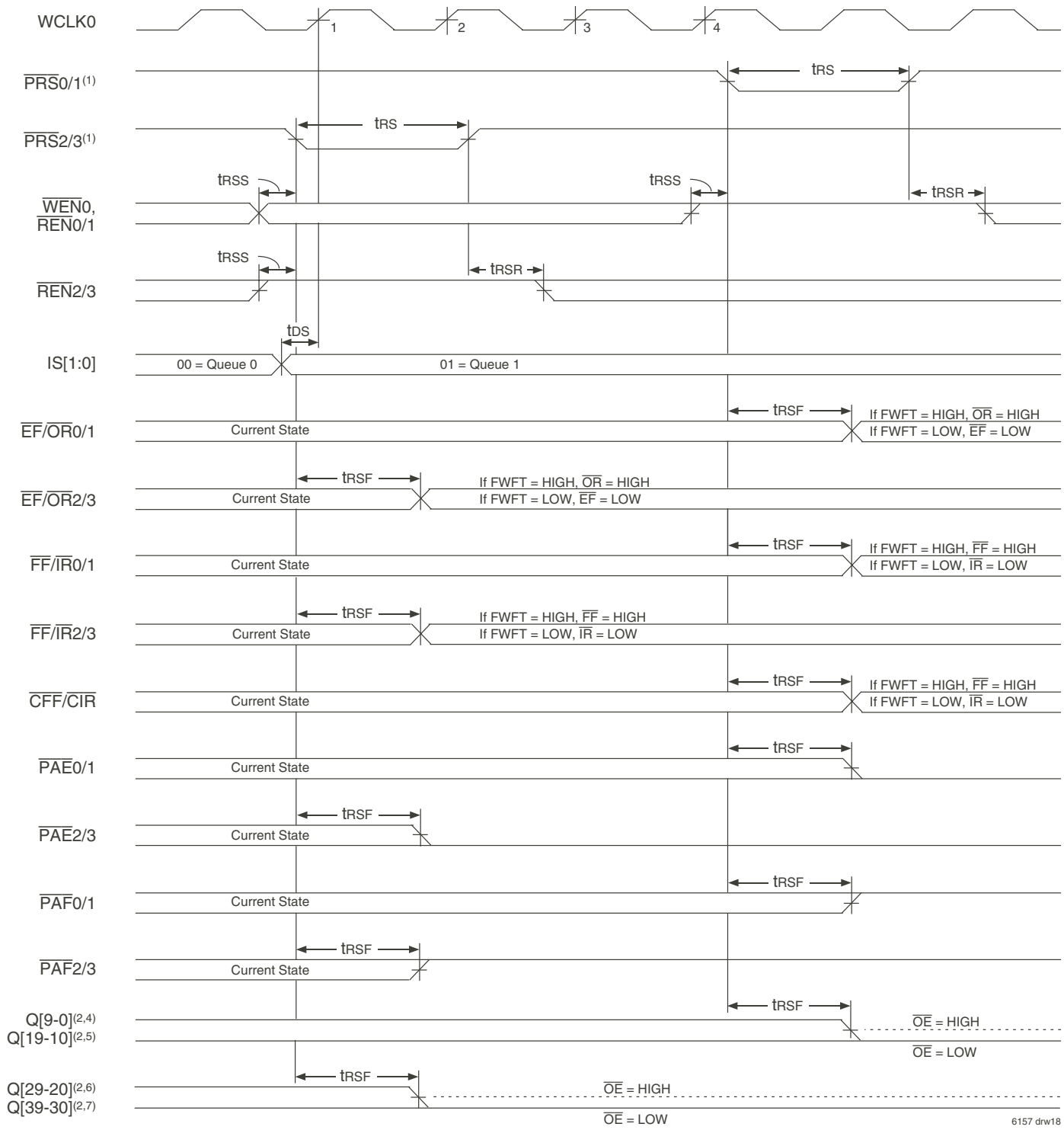
NOTES:
1. $\overline{OE}$ can be toggled during this period.
2. $\overline{PRS}$ should be HIGH during a $\overline{MRS}$.
3. RCLK(s), WCLK(s) and SCLK(s) can be free running or idle.
4. The state of these pins are latched when the master reset pulse is LOW.
5. JTAG clock should not toggle during master reset.
6. $\overline{RCS}$ and $\overline{WCS}$ can be HIGH or LOW until the first rising edge of RCLK after master reset is complete.
7. $\overline{EREN}$ wave form is identical to $\overline{REN}$, ERCLK wave form is identical to RCLK.

Figure 10 . Master Reset



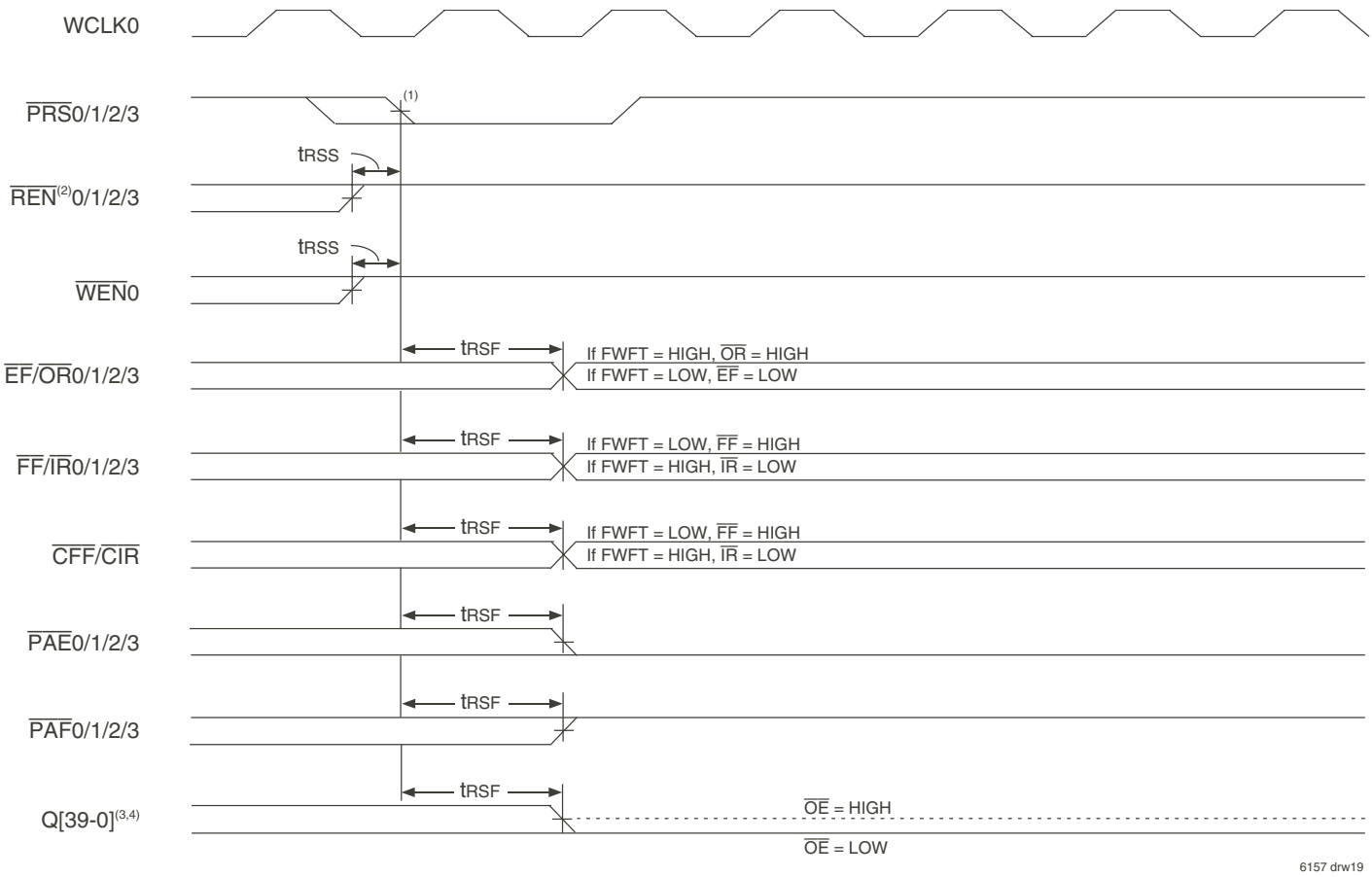
NOTES:
1. During the output selection of two Queues, partial reset of the two Queues involved are prohibited.
2. During partial reset the high-impedance control of the output is provided by $\overline{OE}$ only.
3. $\overline{PRS}$0/1 must go LOW after the fourth rising edge of RCLK0.
4. This is the output data from Queue0 and Queue1.

Figure 11 . Partial Reset for Mux mode



NOTES:
1. During the output selection of two Queues, partial reset of the two Queues involved are prohibited.
2. During partial reset the high-impedance control of the output is provided by $\overline{OE}$ only.
3. $\overline{PRS}$0/1 must go LOW after the fourth rising edge of WCLK0.
4. This is the output data from Queue0.
5. This is the output data from Queue1.
6. This is the output data from Queue2.
7. This is the output data from Queue3.

Figure 12 . Partial Reset for Demux mode



NOTES:
1. If the write port is configured in double data rate, partial reset must be initiated after the falling edge of WCLK0 to ensure falling edge data is written into memory.
2. Only the read enable of the Queue involved in partial reset need to be HIGH.
3. During partial reset the high-impedance control of the outputs is provided by $\overline{OE}$ only.
4. Only affects the output of the Queue partial reset is applied to.

Figure 13. Partial Reset for Broadcast mode

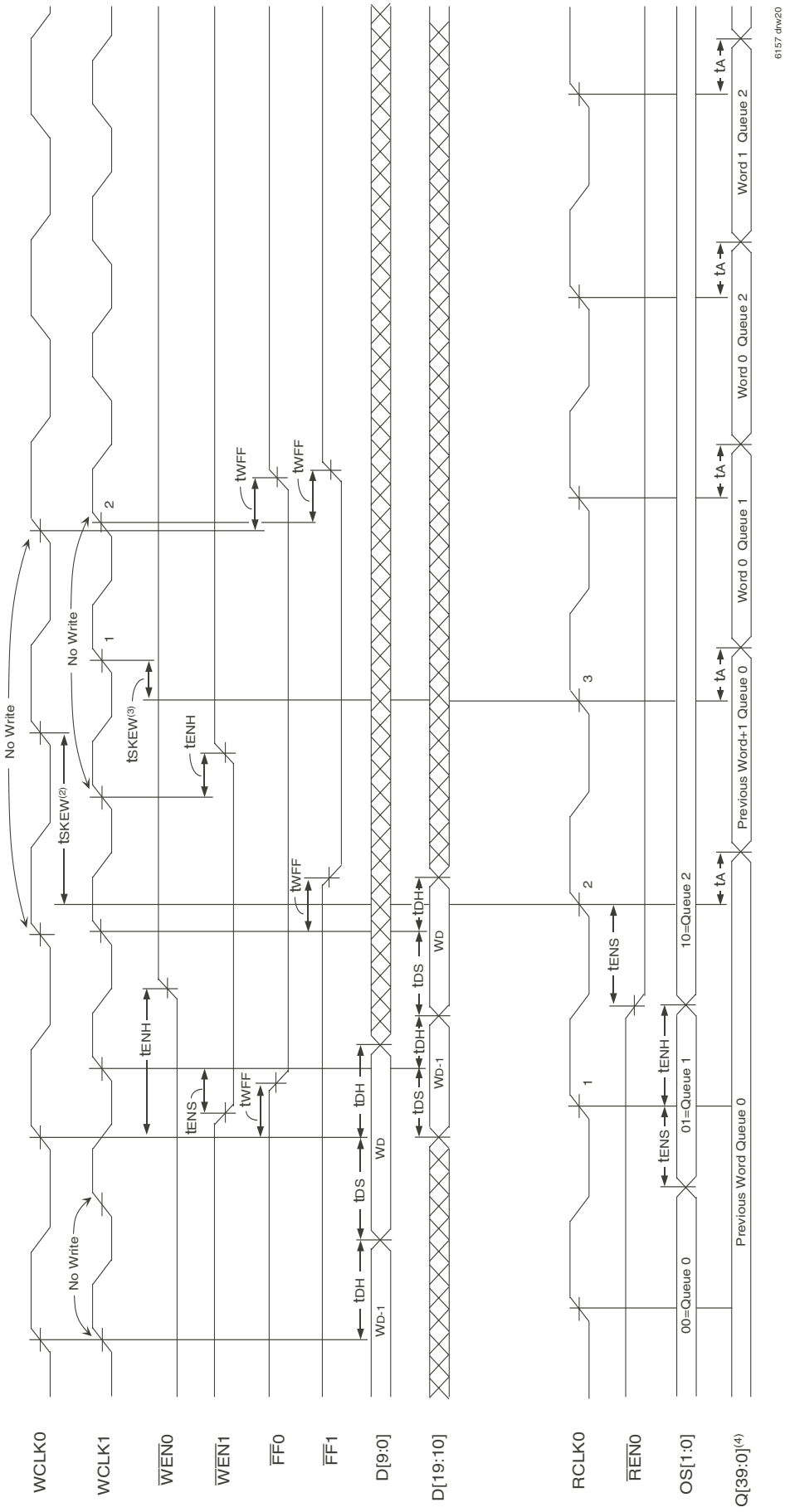
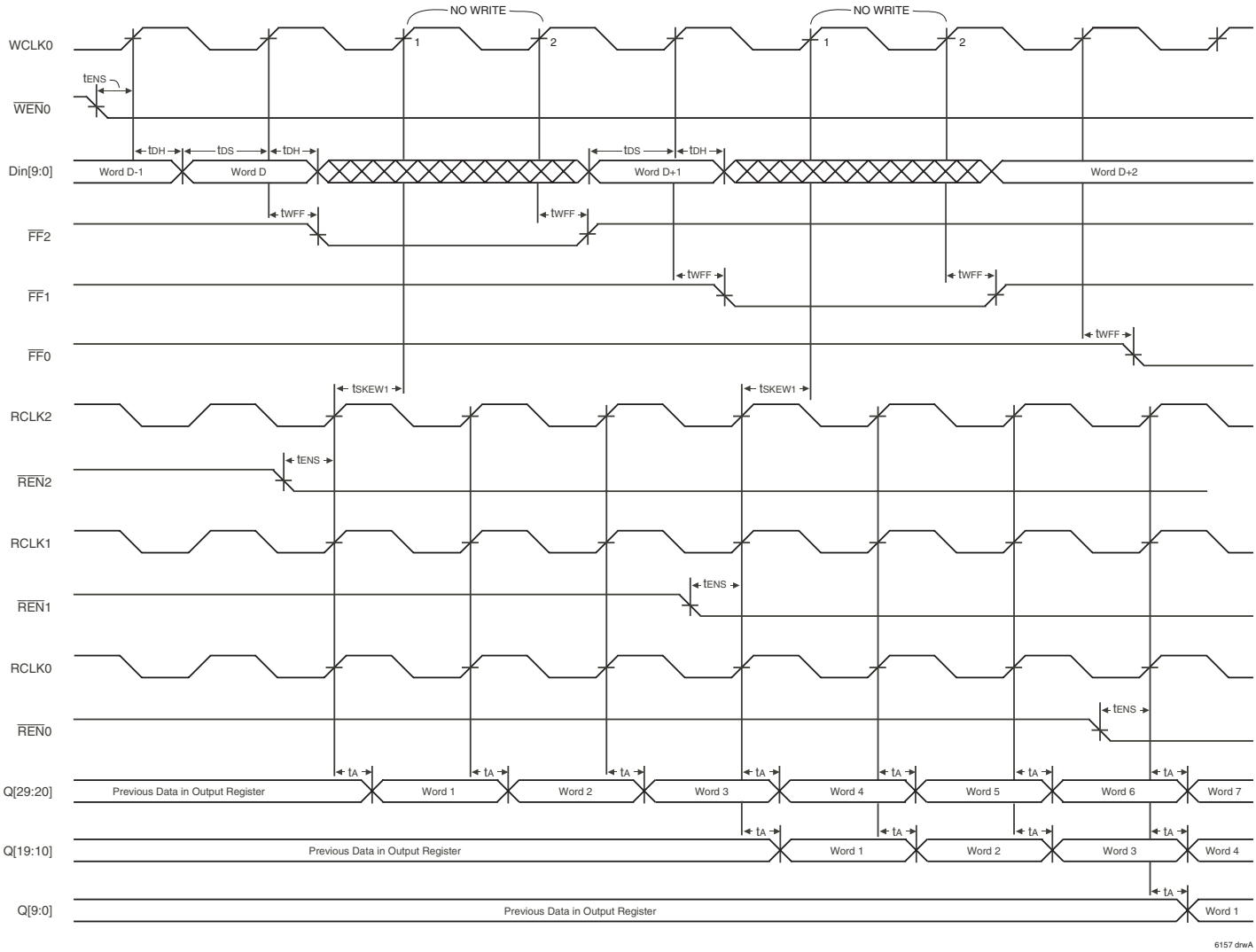


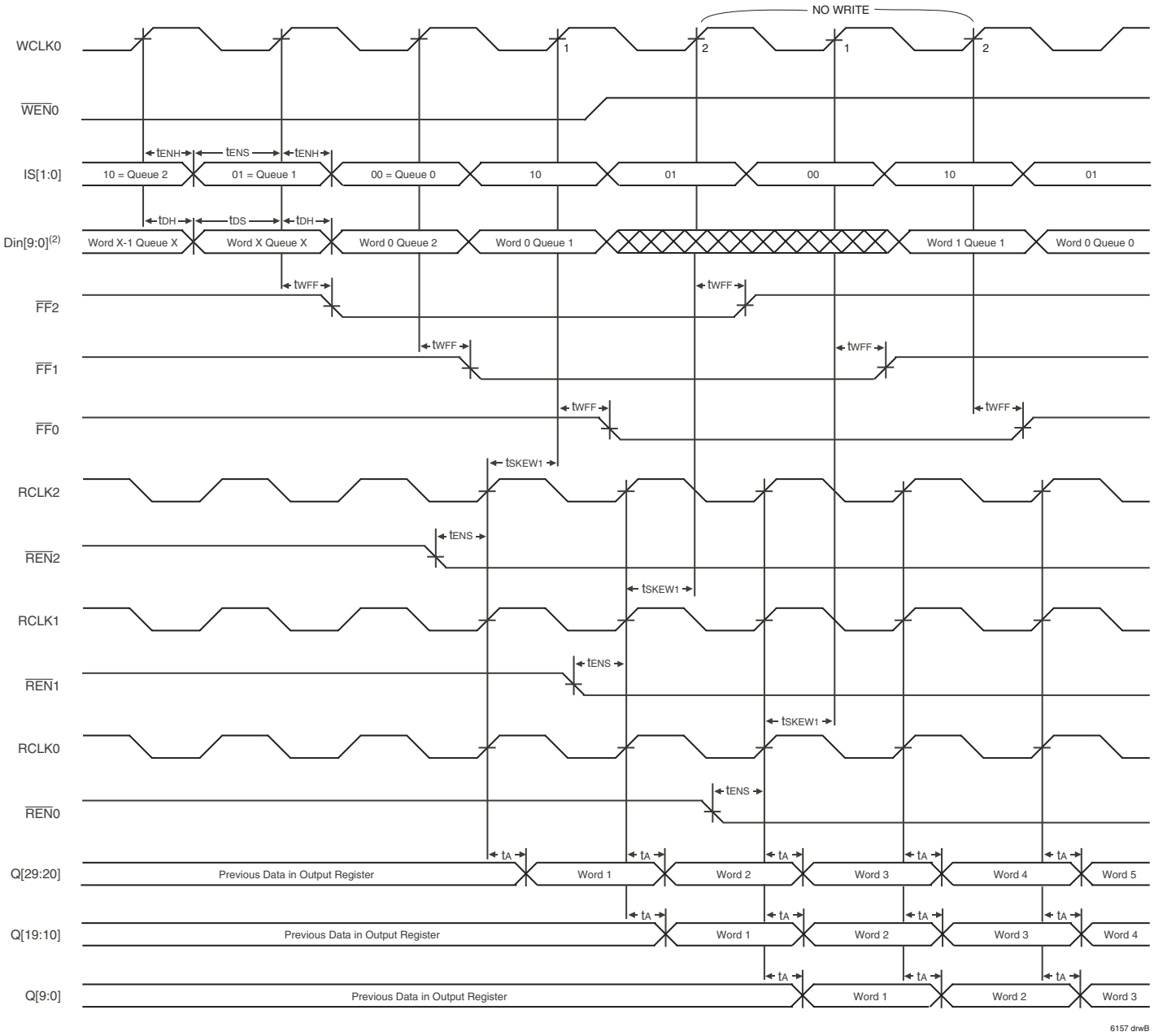
Figure 14. Write Cycle and Full Flag Timing (Mux mode, IDT Standard mode, SDR to SDR) x10 In to x40 Out

NOTES:
1. $\overline{WCS0}$, $\overline{WCS1}$ are LOW.
2. This is the skew between RCLK0 and WCLK0 for Queue0.
3. This is the skew between RCLK0 and WCLK1 for Queue1.
4. There is a two-stage pipeline so each read appears in the data bus two cycles or three rising edges of RCLK later.



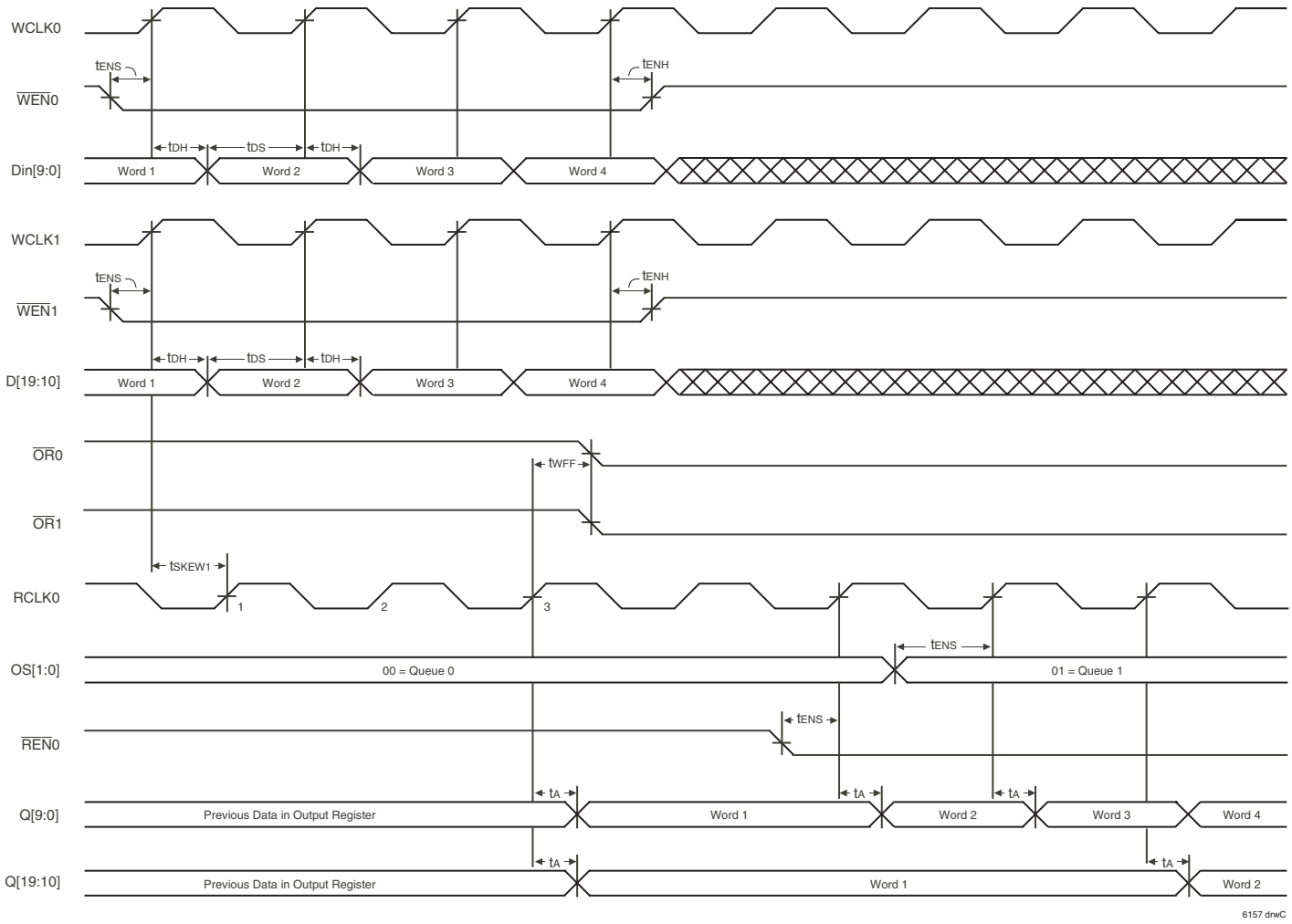
NOTE:
1. $\overline{WCS}0$, $\overline{RCS}0/1/2$, and $\overline{OE}0/1/2$ are LOW.

Figure 15. Write Cycle and Full Flag Timing (Broadcast Write mode, IDT Standard mode, SDR to SDR) x10 In to x10 Out



NOTES:
1. WCS0, RCS0/1/2, and OE0/1/2 are LOW.
2. There is a two-stage pipeline so each read appears in the queue two cycles or three rising edges of WCLK later.

Figure 16. Write Cycle and Full Flag Timing (Demux mode, IDT Standard mode, SDR to SDR) x10 In to x10 Out



NOTE:
1. $\overline{WCS}$0/1, and $\overline{OE}$0/1 are LOW.

Figure 17. Write Timing (Mux mode, FWFT mode, SDR to SDR) x10 In to x10 Out

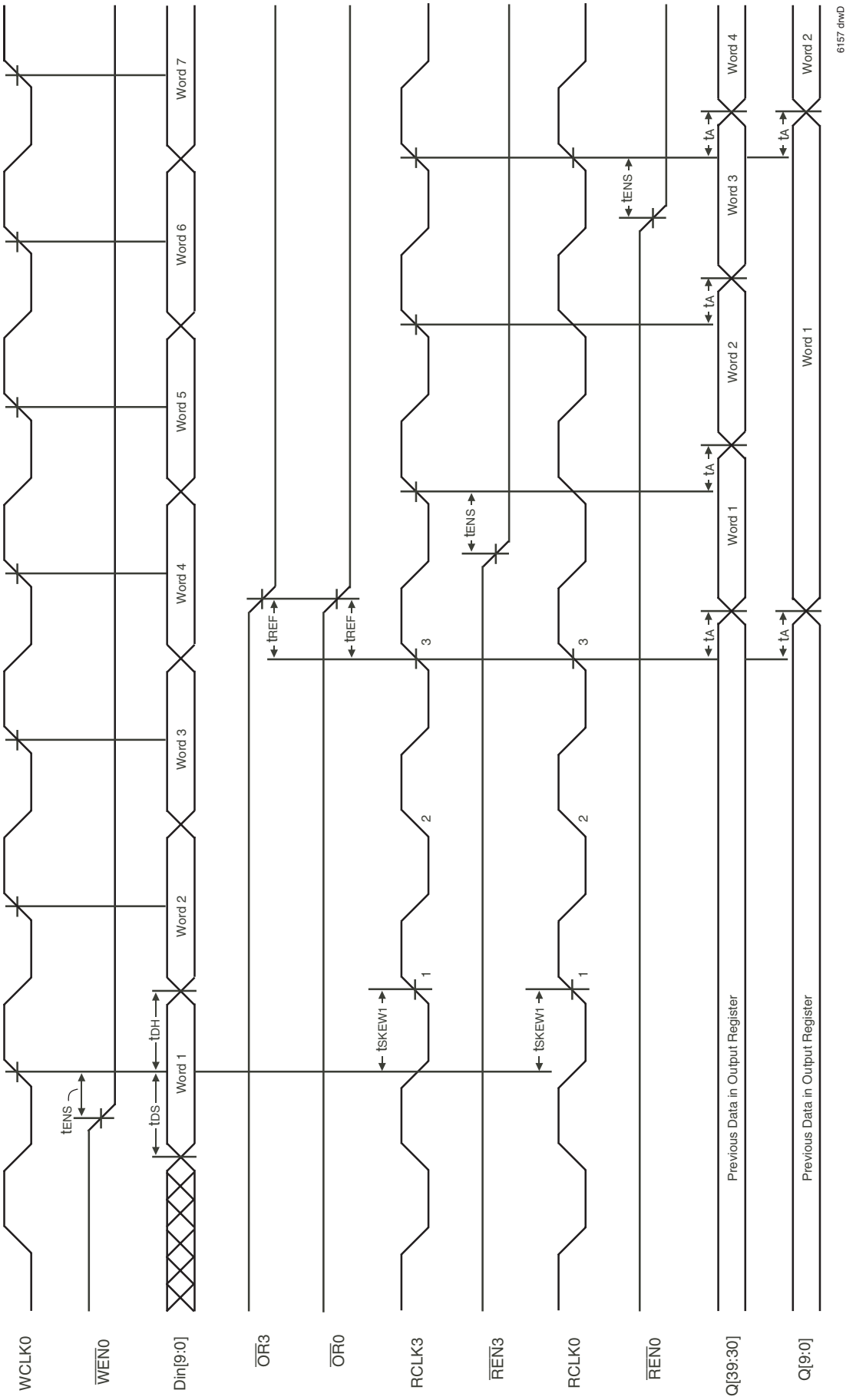
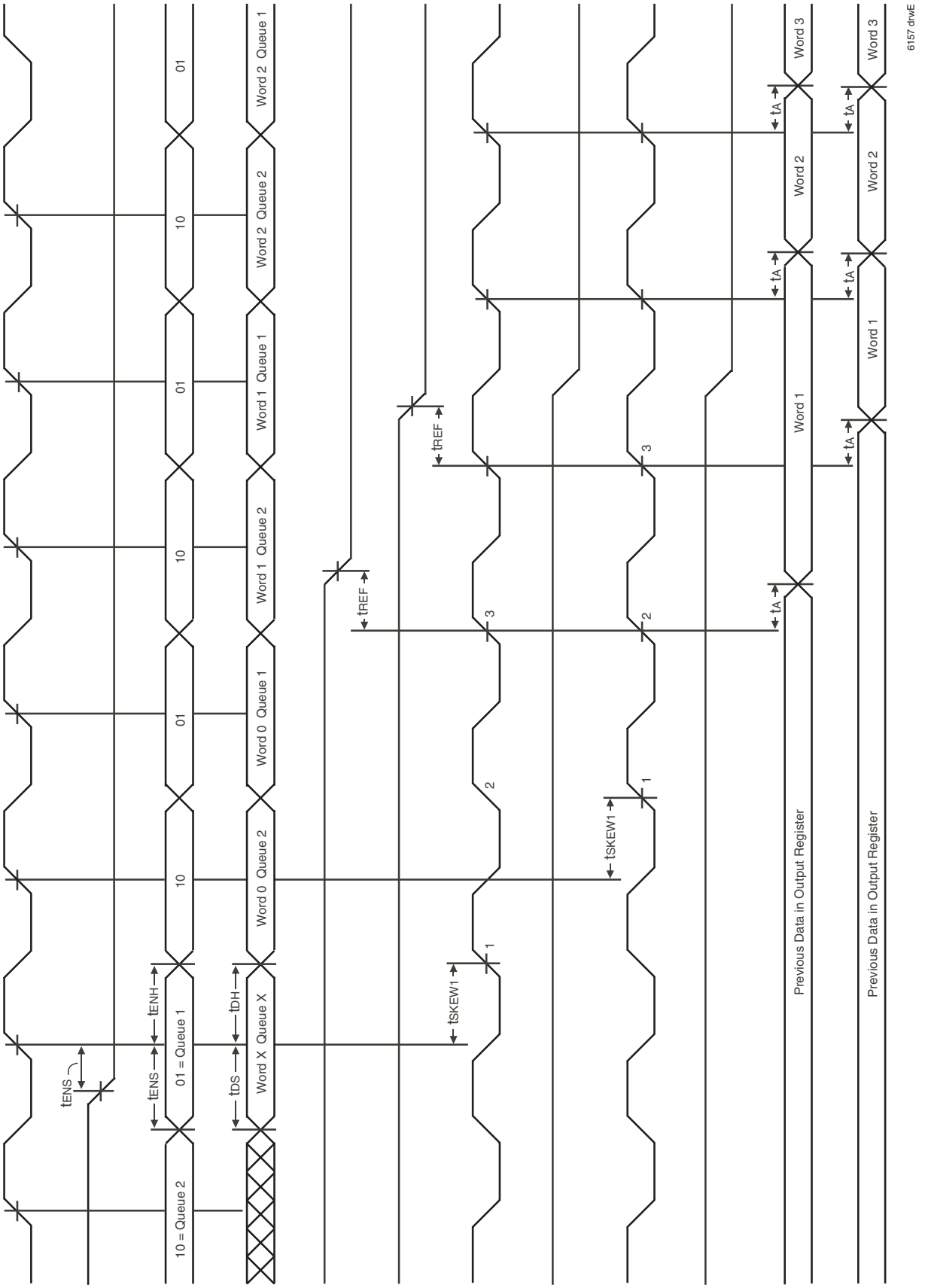


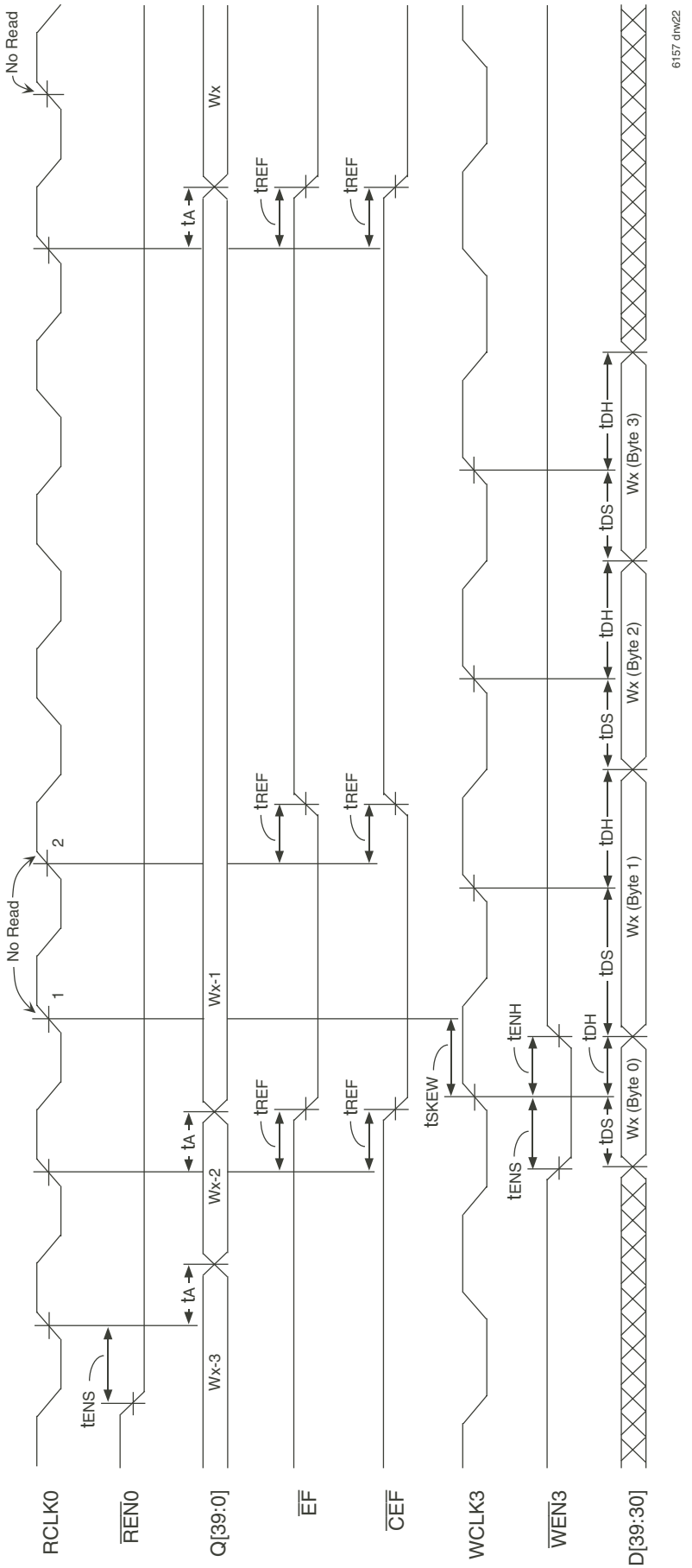
Figure 18. Write Timing (Broadcast Write mode, FWFT mode, SDR to SDR) x10 In to x10 Out

NOTE:
1. $\overline{WCS0}$, $\overline{RCS0/3}$, and $\overline{OE0/3}$ are LOW.



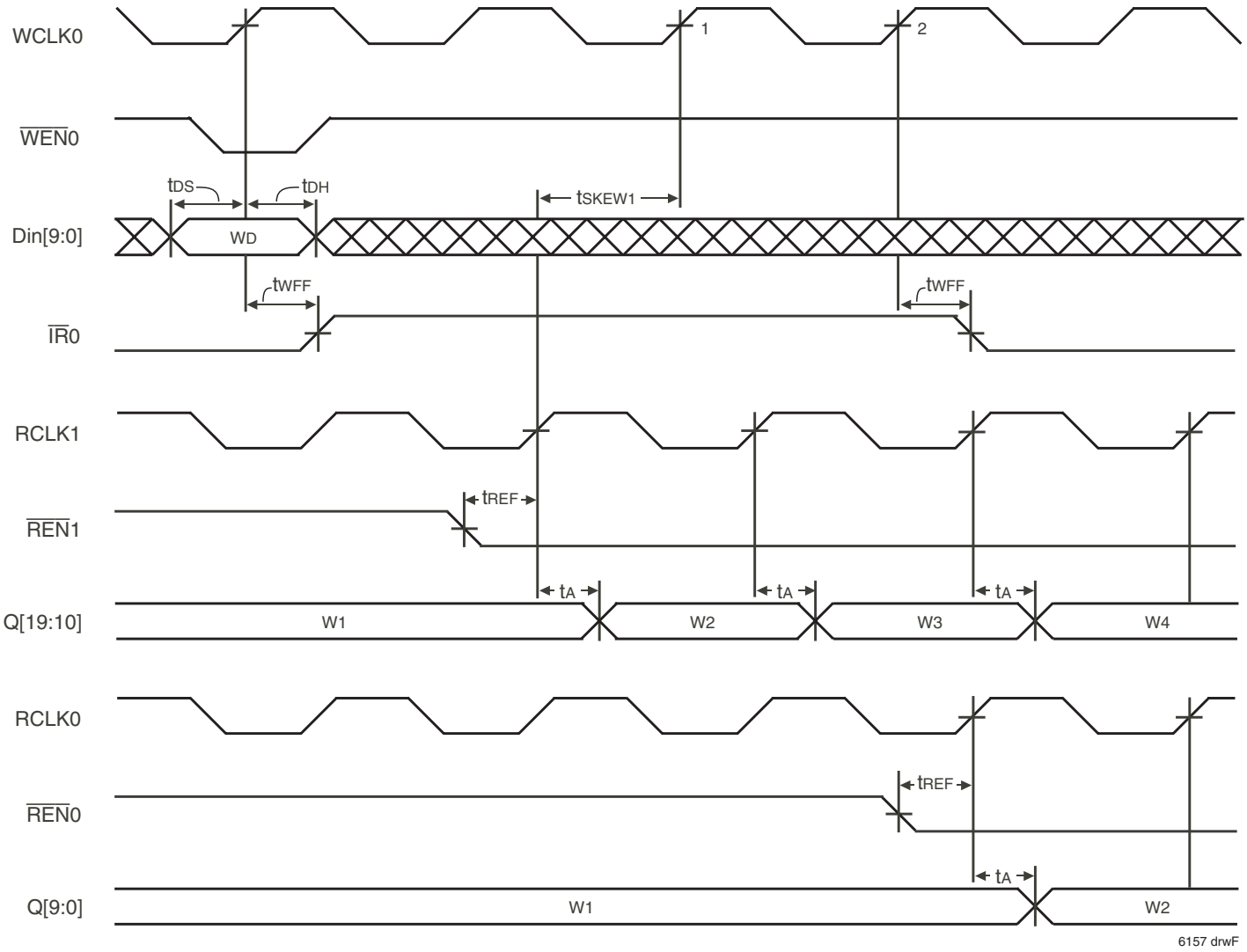
NOTES:
1. $\overline{WCS0}$, $\overline{RCS1/2}$, and $\overline{OE1/2}$ are LOW.
2. There is a two-stage pipeline so each read appears in the queue two cycles or three rising edges of WCLK later.

Figure 19. Write Timing (Demux mode, FWFT mode, SDR to SDR) x10 In to x10 Out



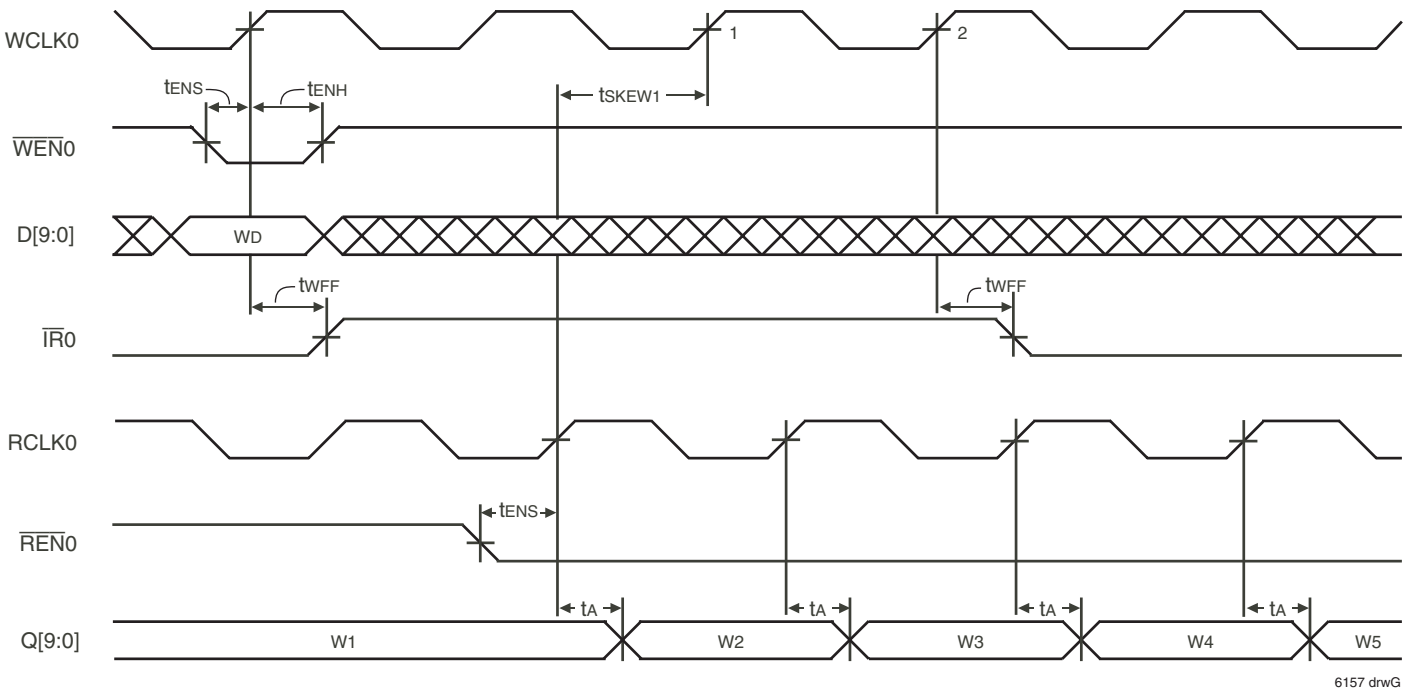
NOTES:
1. $\overline{RCS0}$, $\overline{WCS3}$, $\overline{OE3}$ are LOW.
2. OS[1:0] = 11.
3. Wx (Byte 0) = Q[9:0], Wx (Byte 1) = Q[19:10], Wx (Byte 2) = Q[29:20], Wx (Byte 3) = Q[39:30].

Figure 20. Read Cycle, Empty Flag and First Word Latency (Mux mode, IDT Standard mode, SDR to SDR) x10 In to x40 Out



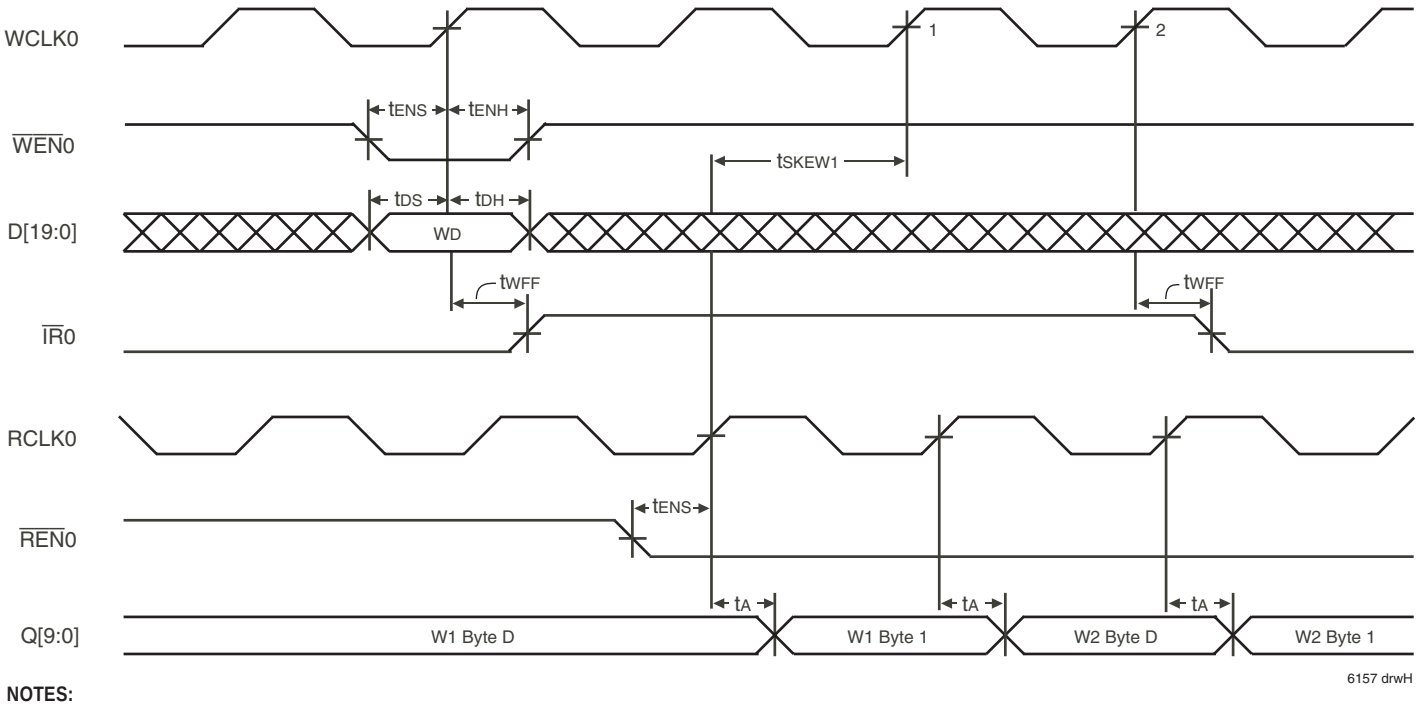
NOTES:
1. WCS0, RCS0/1, and OE0/1 are LOW.
2. Q[39:10] = 0.

Figure 21. Read Timing (Broadcast Write mode, FWFT mode, SDR to SDR) x10 In to x10 Out



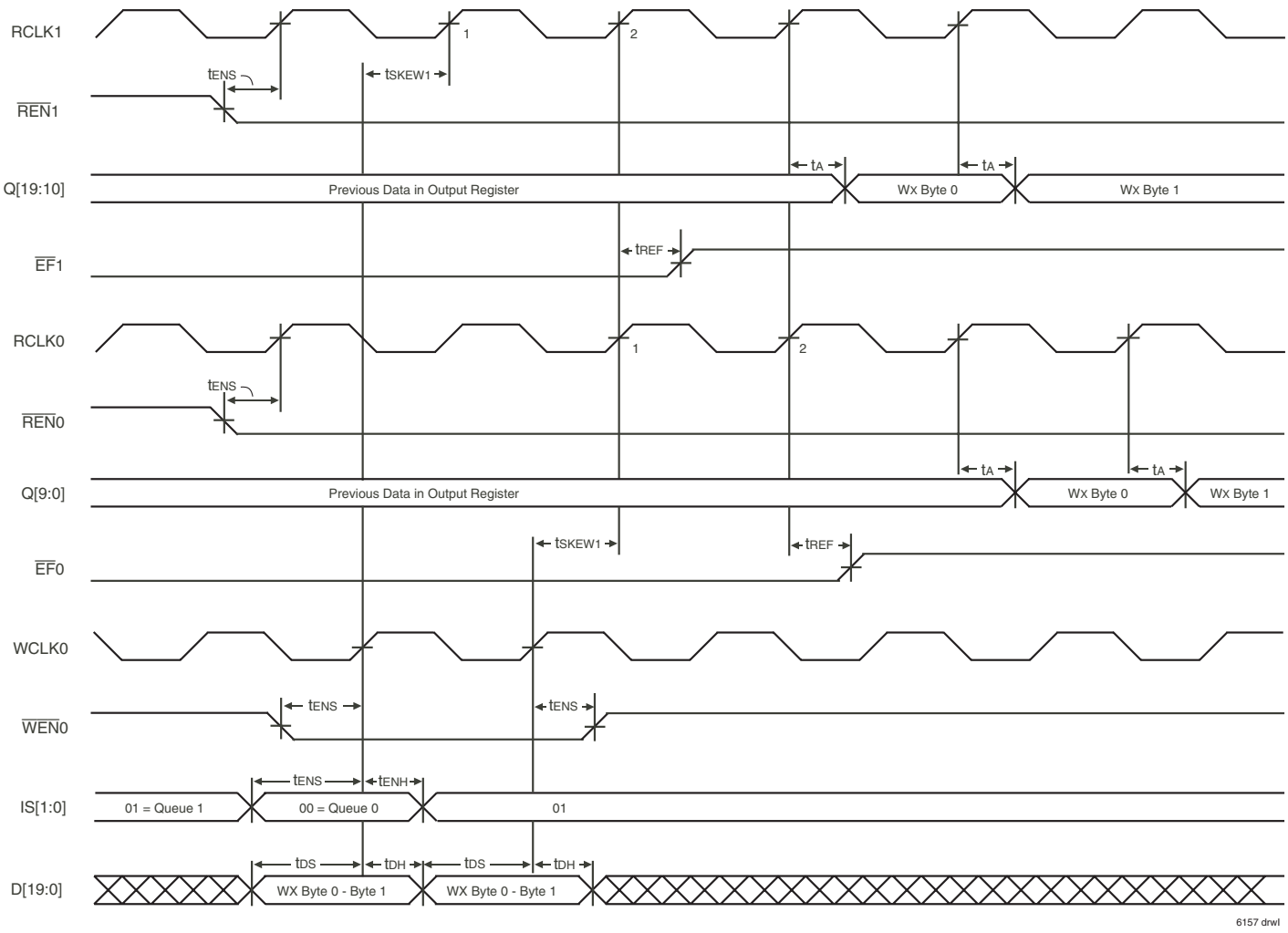
NOTES:
1. WCS0, RCS0, and OE0 are LOW.
2. OS[1:0] = 00.
3. Q[39:10] = 0.

Figure 22. Read Timing (Mux mode, FWFT mode, SDR to SDR) x10 In to x10 Out



NOTES:
1. WCS0, RCS0, and OE0 are LOW.
2. IS[1:0] = 00. Q[39:10] = 0.
3. WD is a 20-bit word. Q[9:0] = Byte 0, Q[19:10] = Byte 1.

Figure 23. Read Timing (Demux mode, FWFT mode, SDR to SDR) x20 In to x10 Out



NOTES:
1. $\overline{WCS}$0, $\overline{RCS}$0/1, and $\overline{OE}$0/1 are LOW.
2. Wx is a 20-bit word. LSB = Byte 0, MSB = Byte 1.

Figure 24. Read Cycle, Empty Flag and First Word Latency (Demux mode, IDT Standard mode, SDR to SDR) x20 In to x10 Out

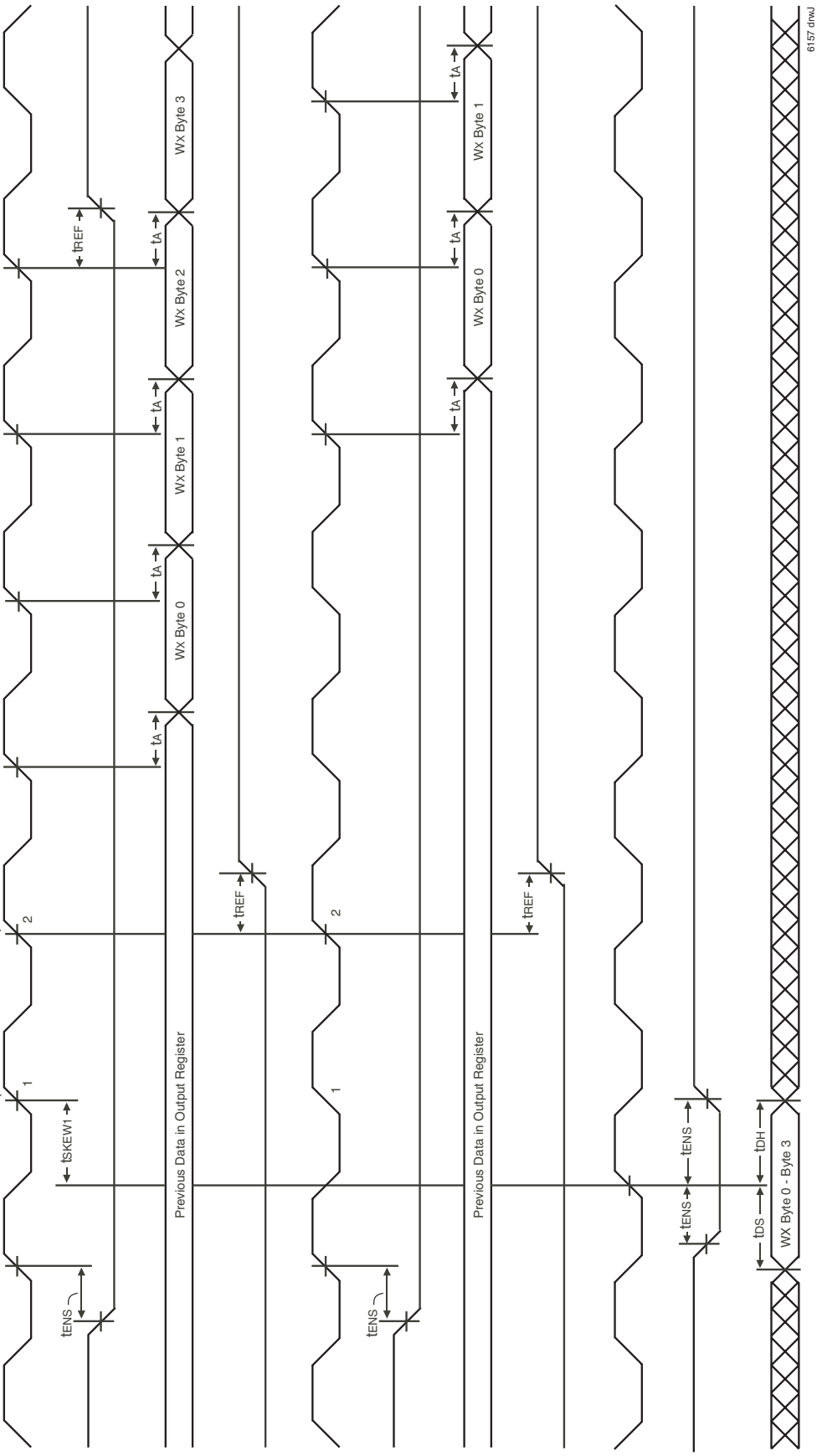
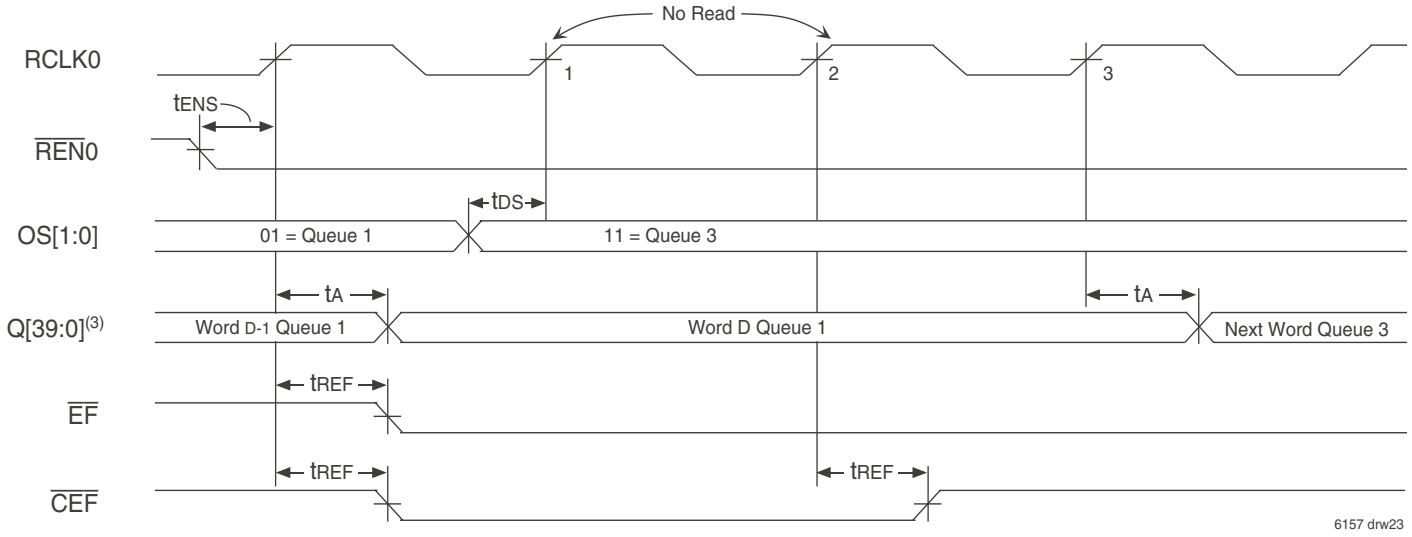


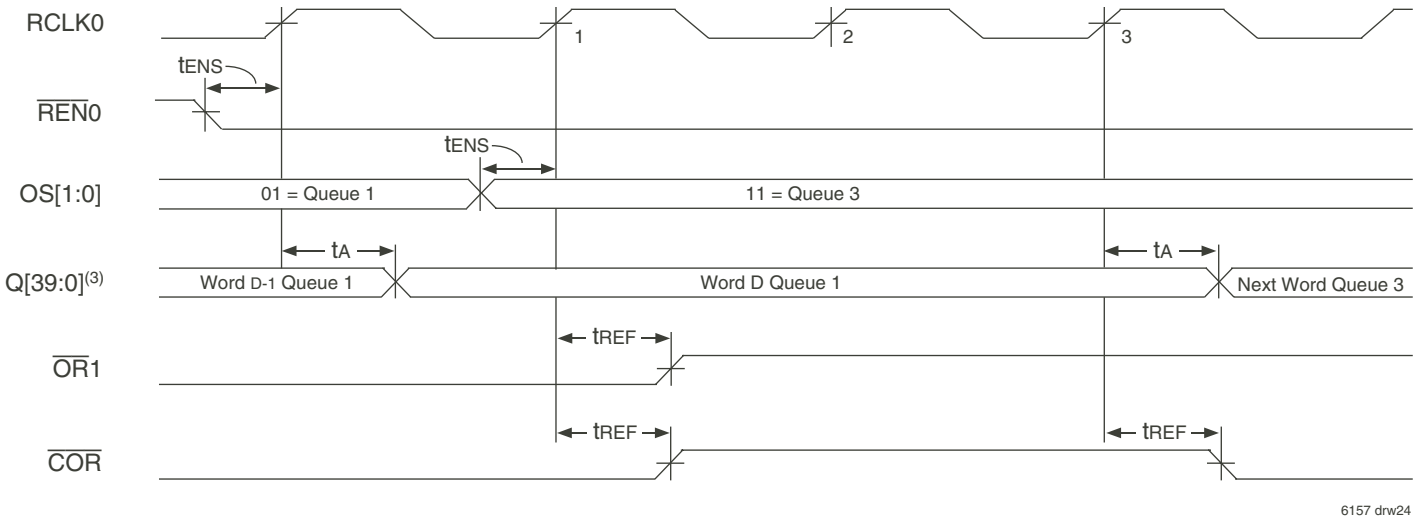
Figure 25. Read Cycle, Empty Flag and First Word Latency (Broadcast Write mode, IDT Standard mode, SDR to SDR) x40 In to x10 Out

NOTES:
1. $\overline{WCS0}$, $\overline{RCS1/2}$, and $\overline{OE1/2}$ are LOW.
2. Wx is a 40-bit word. LSB = Byte 0-Byte 1, MSB = Byte 2-Byte 3.



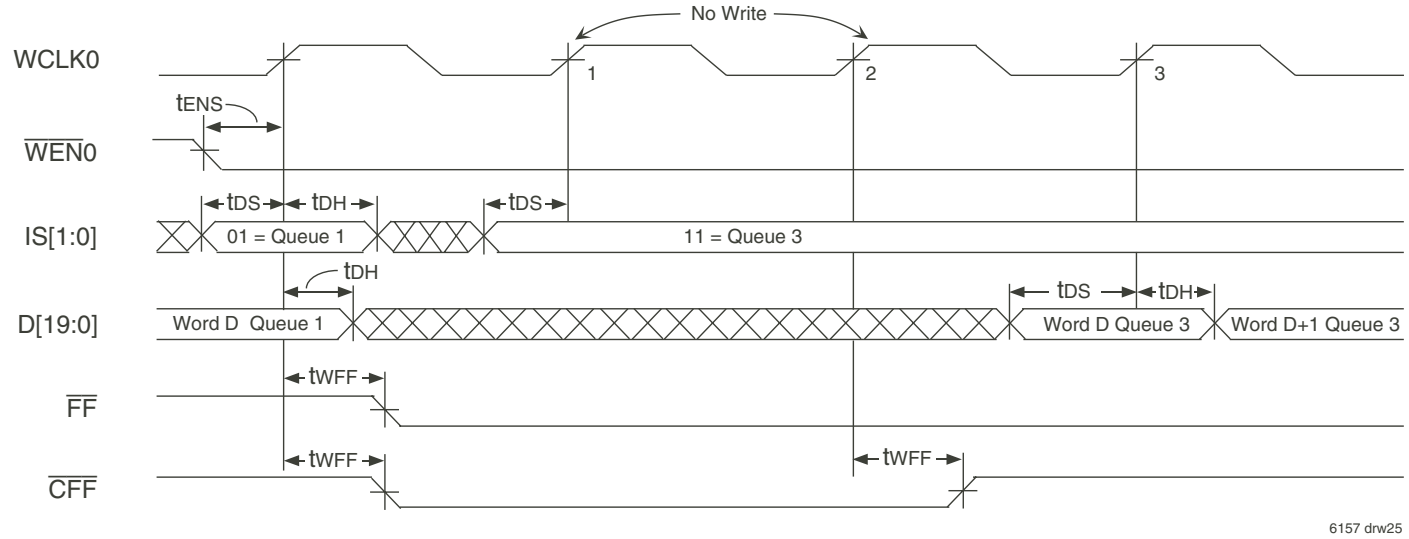
NOTES:
1. RCS0 and OE0 are LOW.
2. EF3 is HIGH.
3. Word D-1 is the second and last word in Queue 1. Word D is the last word in Queue 1.

Figure 26. Composite Empty Flag (Mux mode, IDT Standard mode, SDR to SDR) x10 In to x40 Out



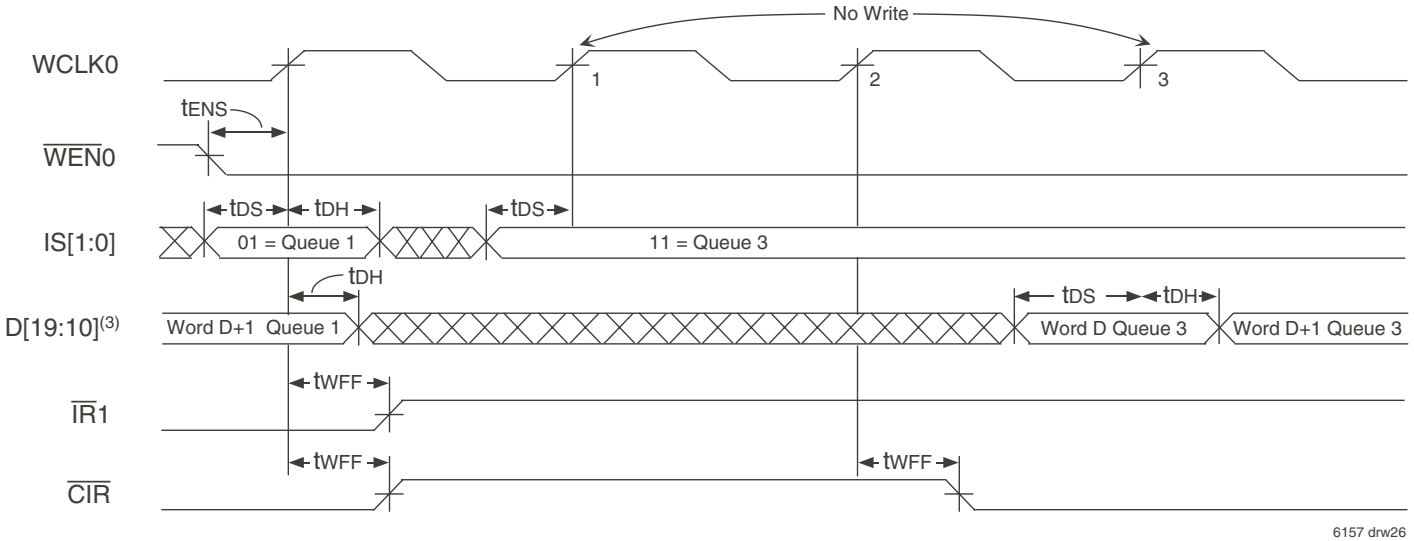
NOTES:
1. RCS0 and OE0 are LOW.
2. OR3 is LOW.
3. Word D-1 is the second and last word in Queue 1. Word D is the last word in Queue 1.

Figure 27. Composite Output Ready Flag (Mux mode, FWFT mode, SDR to SDR) x10 In to x40 Out



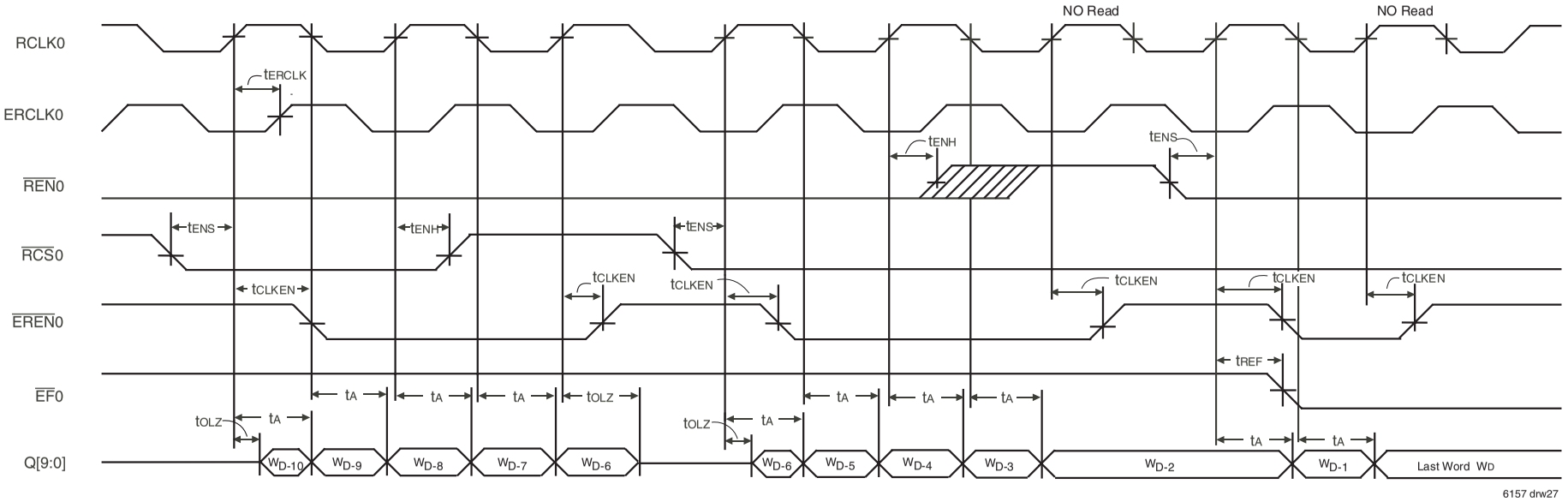
NOTES:
1. WCS0 is LOW.
2. FF3 is HIGH.

Figure 28. Composite Full Flag (Demux mode, IDT Standard mode, SDR to SDR) x20 In to x10 Out



NOTES:
1. WCS0 is LOW.
2. IR3 is LOW.
3. Word D is the first word written and fell through to output (FWFT).

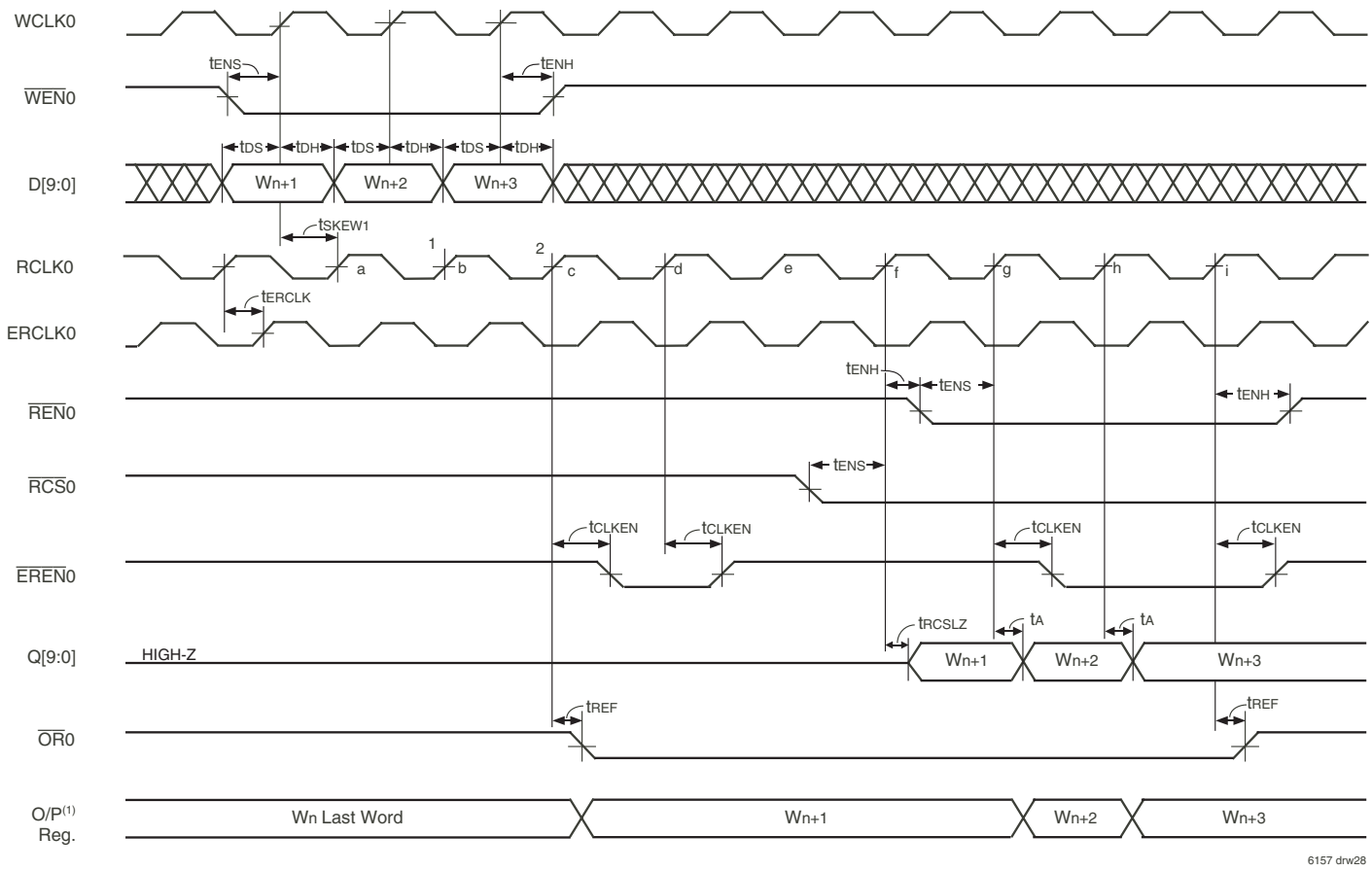
Figure 29. Composite Input Ready Flag (Demux mode, FWFT mode, SDR to SDR) x20 In to x10 Out



NOTES:
1. The $\overline{EREN}$0 output is "or gated" to $\overline{RCS}$0 and $\overline{REN}$0 and will follow these inputs provided that the Queue is not empty. If the Queue is empty, $\overline{EREN}$0 will go HIGH to indicate that there is no new word available.
2. The $\overline{EREN}$0 output is synchronous to RCLK0.
3. $\overline{OE}$0 = LOW, WDDR = HIGH, and RDDR = HIGH.
4. Q[39:10] = 0.
5. The truth table for $\overline{EREN}$ is shown below:

RCLK	$\overline{EF}$	$\overline{RCS}$	$\overline{REN}$	$\overline{EREN}$
↑	1	0	0	0
↑	1	0	1	1
↑	1	1	0	1
↑	1	1	1	1
↑	0	X	X	1

Figure 30. Echo Read Clock and Read Enable Operation (Mux/Demux/Broadcast mode, IDT Standard mode, DDR to DDR) x10 In to x10 Out



NOTE:

1. The O/P Register is the internal output register. Its contents are available on the Qn output bus only when $\overline{RCS}0$ and $\overline{OE}0$ are both active, LOW, that is the bus is not in High-Impedance state.
2. $\overline{OE}0$ is LOW.
3. Q[39:10] = 0.

Cycle:

a&b. At this point the Queue is empty, $\overline{OR}0$ is HIGH.
$\overline{RCS}0$ and $\overline{REN}0$ are both disabled, the output bus is High-Impedance.

c. Word Wn+1 falls through to the output register, $\overline{OR}0$ goes active, LOW.
$\overline{RCS}0$ is HIGH, therefore the Qn outputs are High-Impedance. $\overline{EREN}0$ goes LOW to indicate that a new word has been placed into the output register.

d. $\overline{EREN}0$ goes HIGH, no new word has been placed on the output register into this cycle.

e. No Operation.

f. $\overline{RCS}0$ is LOW on this cycle, therefore the Qn outputs go to Low-Impedance and the contents of the output register (Wn+1) are made available.
NOTE: In FWFT mode it is important to take $\overline{RCS}0$ active LOW at least one cycle ahead of $\overline{REN}0$, this ensures the word (Wn+1) currently in the output register is made available for at least one cycle, otherwise Wn+1 will overwritten by Wn+2.

g. $\overline{REN}0$ goes active LOW, this reads out the second word, Wn+2.
$\overline{EREN}0$ goes active LOW to indicate a new word has been placed into the output register.

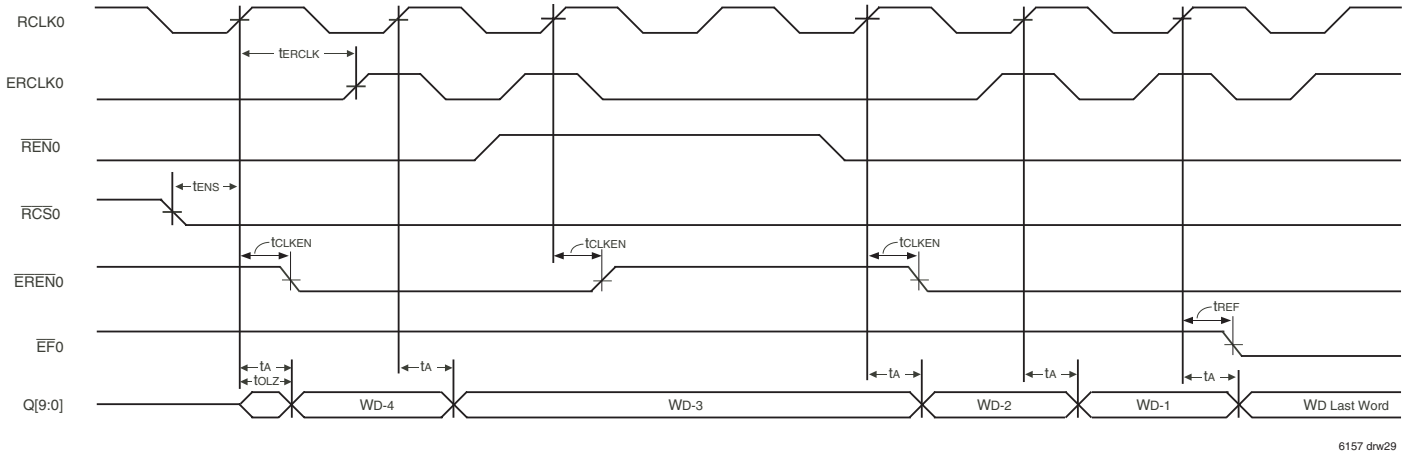
h. Word Wn+3 is read out, $\overline{EREN}0$ remains active, LOW indicating a new word has been read out.
NOTE: Wn+3 is the last word in the Queue.

i. This is the next enabled read after the last word, Wn+3 has been read out. $\overline{OR}0$ flag goes HIGH and $\overline{EREN}0$ goes HIGH to indicate that there is no new word available.

4. $\overline{OE}0$ is LOW, WDDR = LOW, and RDDR = LOW.
5. The truth table for $\overline{EREN}$ is shown below:

RCLK	$\overline{OR}$	$\overline{RCS}$	$\overline{REN}$	$\overline{EREN}$
↑	0	0	0	0
↑	0	0	1	1
↑	0	1	0	1
↑	0	1	1	1
↑	1	X	X	1

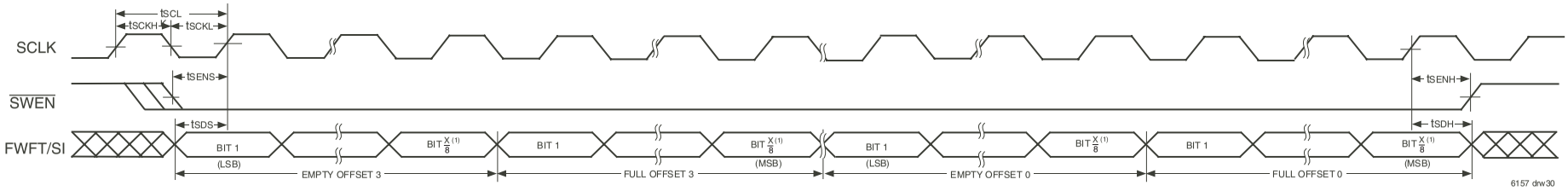
Figure 31. Echo RCLK and Echo Read Enable Operation (Mux/Demux/Broadcast mode, FWFT mode, SDR to SDR)



NOTES:
1. The $\overline{EREN}$0 output is "or gated" to $\overline{RCS}$0 and $\overline{REN}$0 and will follow these inputs provided that the Queue is not empty. If the Queue is empty, $\overline{EREN}$0 will go HIGH to indicate that there is no new word available.
2. The $\overline{EREN}$0 output is synchronous to RCLK0.
3. $\overline{OE}$0 = LOW, WDDR = HIGH, and RDDR = HIGH.
4. Q[39:10] = 0.
5. The truth table for $\overline{EREN}$ is shown below:

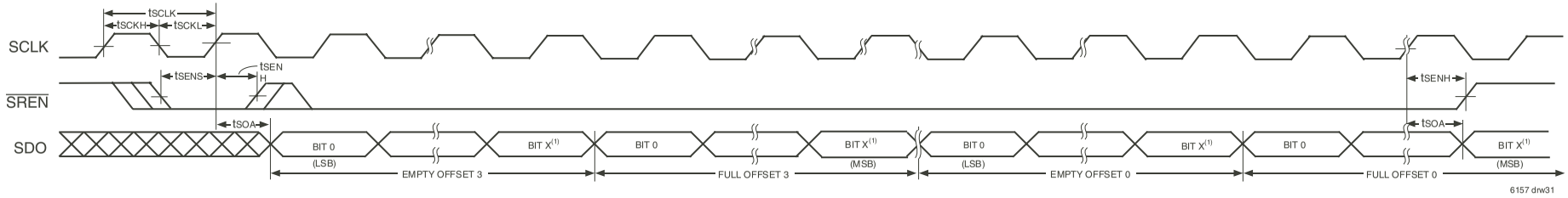
RCLK	$\overline{EF}$	$\overline{RCS}$	$\overline{REN}$	$\overline{EREN}$
↑	1	0	0	0
↑	1	0	1	1
↑	1	1	0	1
↑	1	1	1	1
↑	0	X	X	1

Figure 32. Echo Read Clock and Read Enable Operation (Mux/Demux/Broadcast mode, IDT Standard mode, SDR to SDR) x10 In to x10 Out



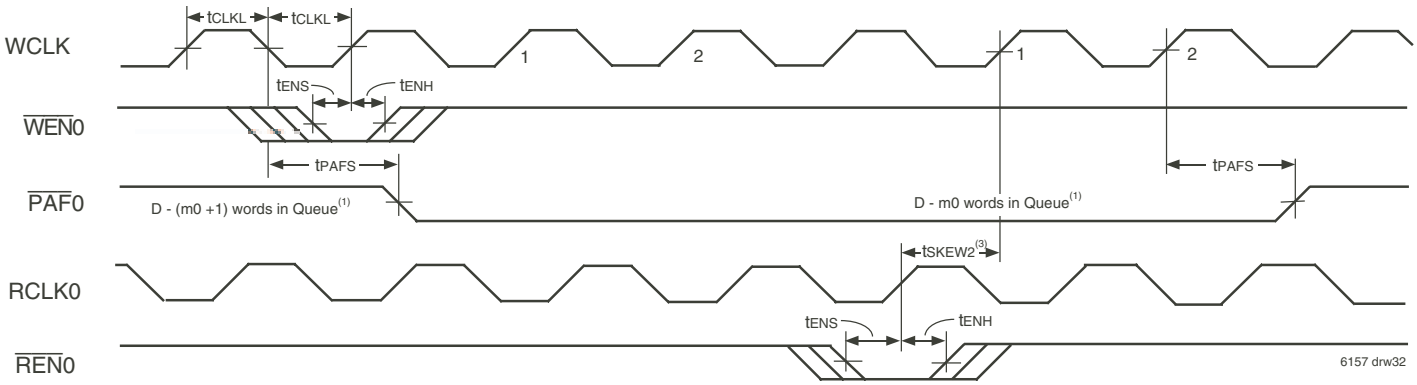
NOTE:
1. If IW/OW = x40, X = 104 for the IDT72T55248, X = 112 for the IDT72T55258, X = 120 for the IDT72T55268.
   If IW/OW = x20, X = 112 for the IDT72T55248, X = 120 for the IDT72T55258, X = 128 for the IDT72T55268.
   If IW/OW = x10, X = 120 for the IDT72T55248, X = 128 for the IDT72T55258, X = 136 for the IDT72T55268.

Figure 33. Loading of Programmable Flag Registers (IDT Standard and FWFT modes)



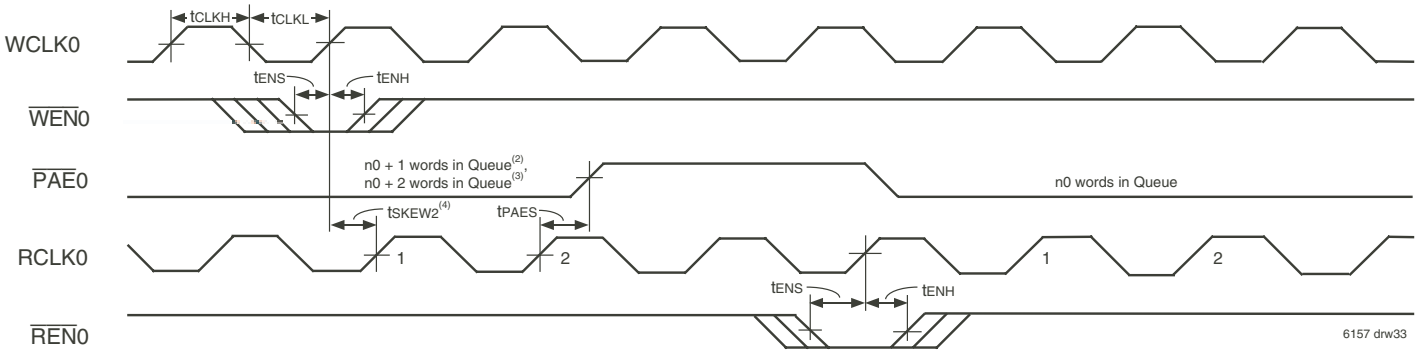
NOTE:
1. If IW/OW = x40, X = 104 for the IDT72T55248, X = 112 for the IDT72T55258, X = 120 for the IDT72T55268.
   If IW/OW = x20, X = 112 for the IDT72T55248, X = 120 for the IDT72T55258, X = 128 for the IDT72T55268.
   If IW/OW = x10, X = 120 for the IDT72T55248, X = 128 for the IDT72T55258, X = 136 for the IDT72T55268.

Figure 34. Reading of Programmable Flag Registers (IDT Standard and FWFT modes)



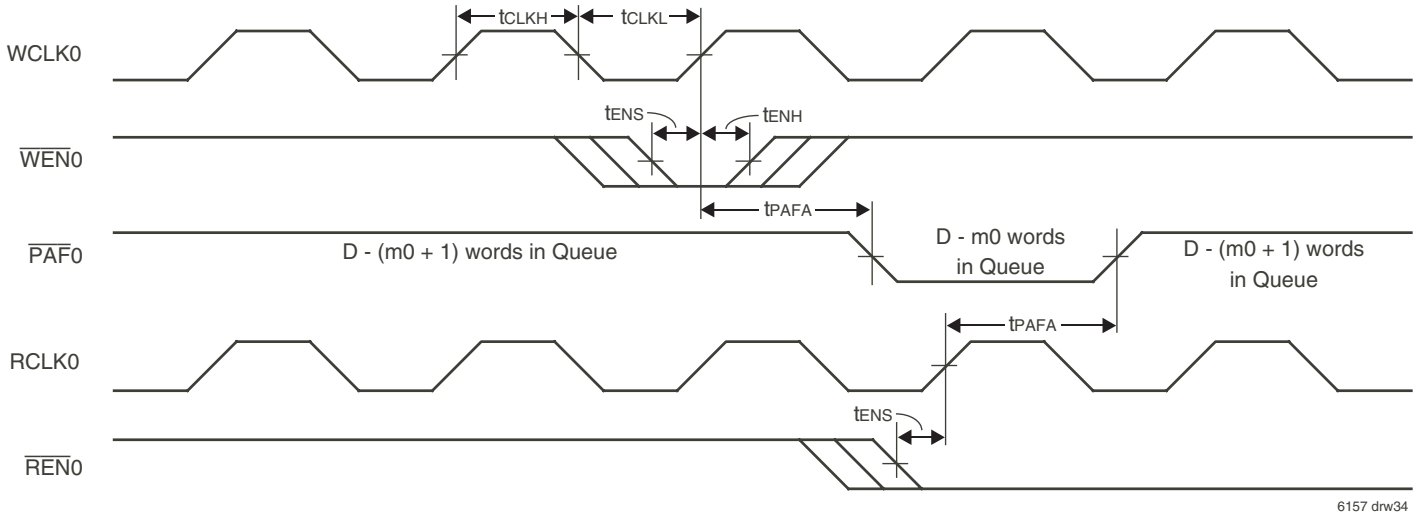
NOTES:
1. m0 = PAF0 offset .
2. D = maximum Queue depth. For density of Queue with bus-matching, refer to the bus-matching section on page 19.
3. t_{SKEW2} is the minimum time between a rising RCLK0 edge and a rising WCLK0 edge to guarantee that PAF0 will go HIGH (after one WCLK0 cycle plus t_{PAFS}). If the time between the rising edge of RCLK0 and the rising edge of WCLK0 is less than t_{SKEW2}, then the PAF0 deassertion time may be delayed one extra WCLK0 cycle.
4. PAF0 is asserted and updated on the rising edge of WCLK0 only.
5. Select this mode by setting PFM HIGH during Master Reset.
6. RCS0 = LOW, WCS0 = LOW, WDDR = LOW, and RDDR = LOW.

Figure 35. Synchronous Programmable Almost-Full Flag Timing (Mux/Demux/Broadcast mode, IDT Standard and FWFT mode, SDR to SDR) x10 In to x10 Out



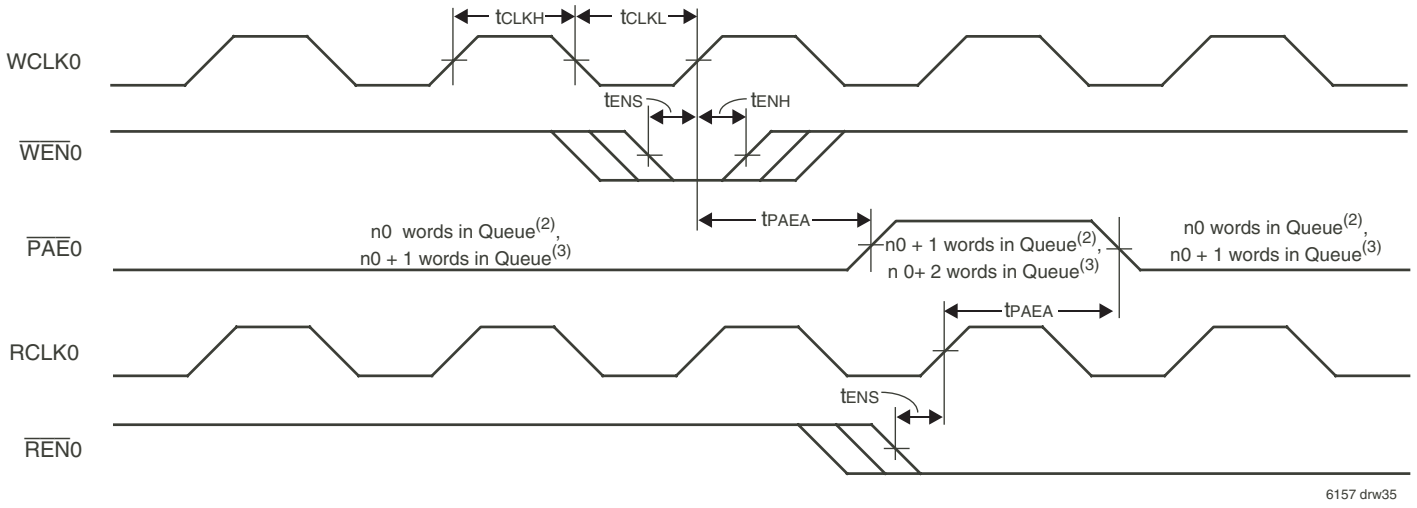
NOTES:
1. The timing diagram shown is for Queue0. Queues1-3 exhibit the same behavior.
2. n0 = PAE0 offset.
3. For IDT Standard mode
4. For FWFT mode.
5. t_{SKEW2} is the minimum time between a rising WCLK0 edge and a rising RCLK0 edge to guarantee that PAE0 will go HIGH (after one RCLK0 cycle plus t_{PAES}). If the time between the rising edge of WCLK0 and the rising edge of RCLK0 is less than t_{SKEW2}, then the PAE0 deassertion may be delayed one extra RCLK0 cycle.
6. PAE0 is asserted and updated on the rising edge of WCLK0 only.
7. Select this mode by setting PFM HIGH during Master Reset.
8. RCS0 = LOW, WCS0 = LOW, WDDR = LOW, and RDDR = LOW.

Figure 36. Synchronous Programmable Almost-Empty Flag Timing (Mux/Demux/Broadcast mode, IDT Standard and FWFT mode, SDR to SDR) x10 In to x10 Out



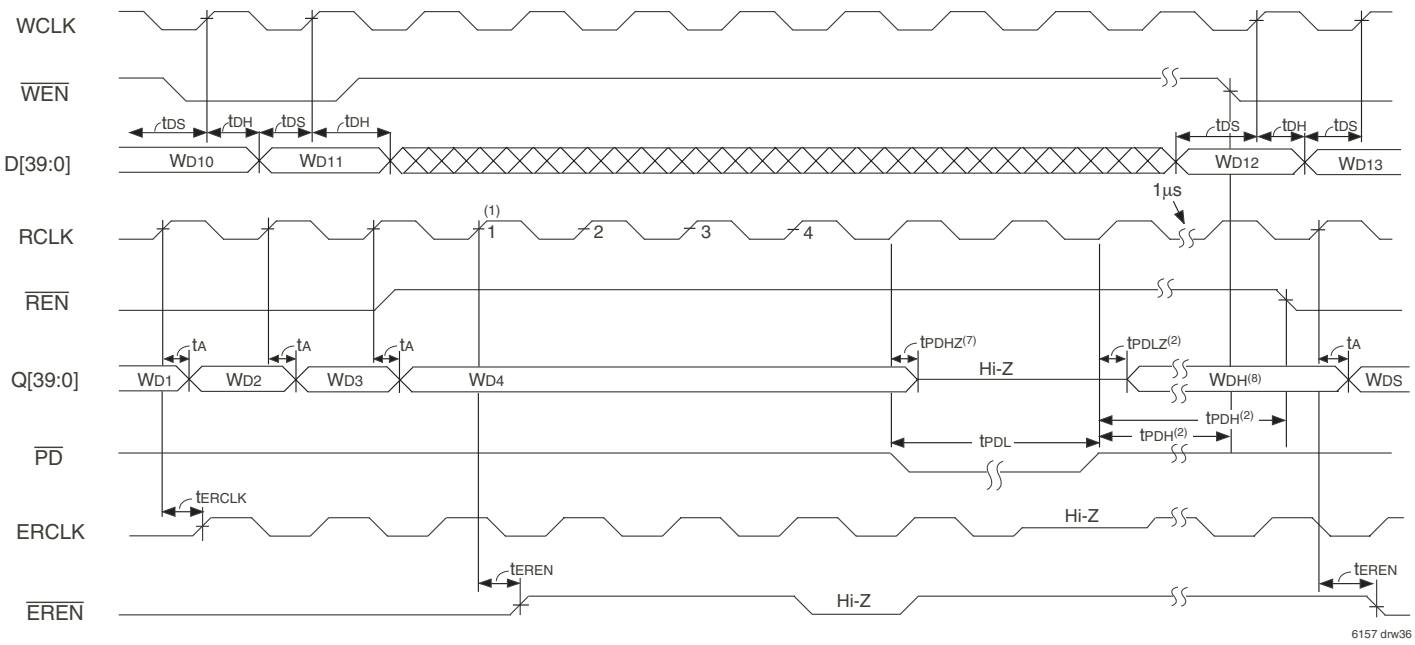
NOTES:
1. m0 = $\overline{PAF}$0 offset.
2. D = maximum Queue depth. For density of Queue with bus-matching, refer to the bus-matching section on page 19.
3. $\overline{PAF}$0 is asserted to LOW on WCLK0 transition and reset to HIGH on RCLK0 transition.
4. Select this mode by setting PFM LOW during Master Reset.
5. $\overline{RCS}$0 is LOW, $\overline{WCS}$0 is LOW, WDDR = LOW, and RDDR = LOW.

Figure 37. Asynchronous Programmable Almost-Full Flag Timing (Mux/Demux/Broadcast mode, IDT Standard and FWFT mode, SDR to SDR) x10 In to x10 Out



NOTES:
1. n0 = $\overline{PAE}$0 offset.
2. For IDT Standard Mode.
3. For FWFT Mode.
4. $\overline{PAE}$0 is asserted LOW on RCLK0 transition and reset to HIGH on WCLK0 transition.
5. Select this mode by setting PFM LOW during Master Reset.
6. $\overline{RCS}$0 is LOW, $\overline{WCS}$0 is LOW, WDDR = LOW, and RDDR = LOW.

Figure 38. Asynchronous Programmable Almost-Empty Flag Timing (Mux/Demux/Broadcast mode, IDT Standard and FWFT mode, SDR to SDR) x10 In to x10 Out

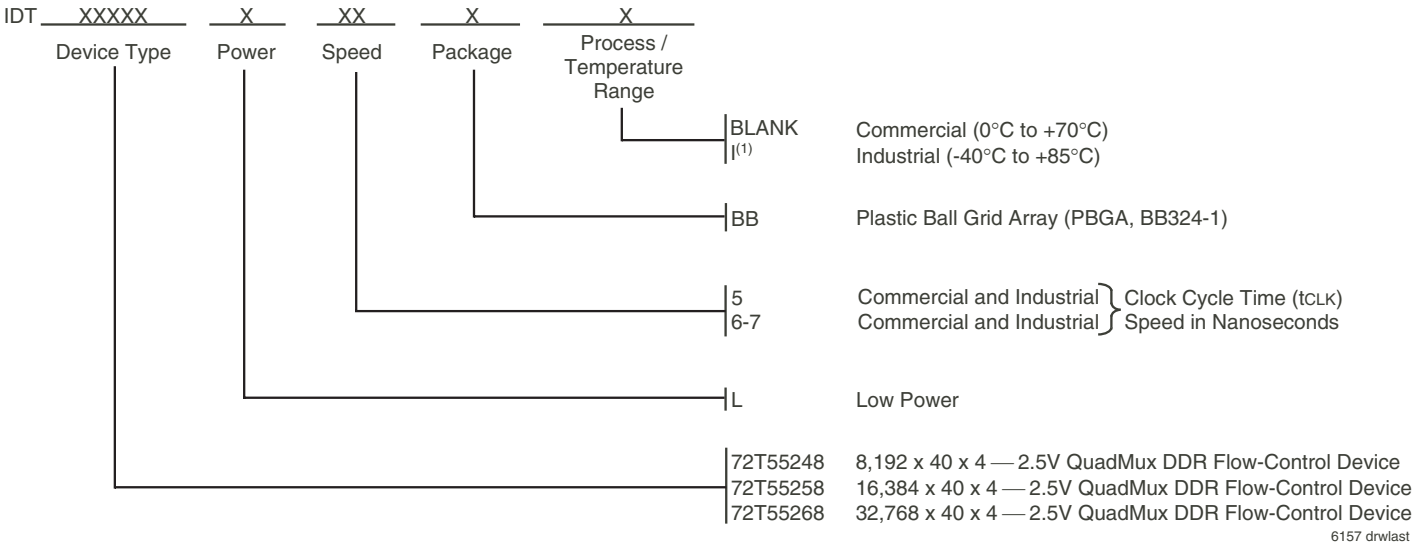


NOTES:

1. All read and write operations must have ceased a minimum of 4 WCLK and 4 RCLK cycles before power down is asserted.
2. When the $\overline{PD}$ input becomes deasserted, there will be a 1µs waiting period before read and write operations can resume. All input and output signals will also resume after this time period.
3. Set-up and configuration static inputs are not affected during power down.
4. Serial programming and JTAG programming port are inactive during power down.
5. $\overline{RCS}$ = 0, $\overline{WCS}$ = 0 and $\overline{OE}$ = 0. These signals can toggle during and after power down.
6. All flags remain active and maintain their current states.
7. During power down, all outputs will be in high-impedance.

Figure 39. Power Down Operation

ORDERING INFORMATION



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