



3.3V CMOS 1-BIT TO 4-BIT ADDRESS REGISTER/DRIVER WITH 3-STATE OUTPUTS

IDT74ALVC16831

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{sk(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015;
> 200V using machine model (C = 200pF, R = 0)
- 0.40mm pitch TVSOP, SSOP, and TSSOP package
- Extended commercial range of - 40°C to +85°C
- $V_{cc} = 3.3V \pm 0.3V$, Normal Range
- $V_{cc} = 2.7V$ to $3.6V$, Extended Range
- $V_{cc} = 2.5V \pm 0.2V$
- CMOS power levels (0.4μW typ. static)
- Rail-to-Rail output swing for increased noise margin

Drive Features for ALVC16831:

- High Output Drivers: $\pm 24mA$
- Suitable for heavy loads

APPLICATIONS:

- Memory subsystems
- PC Motherboards
- Workstations
- Telecommunication applications

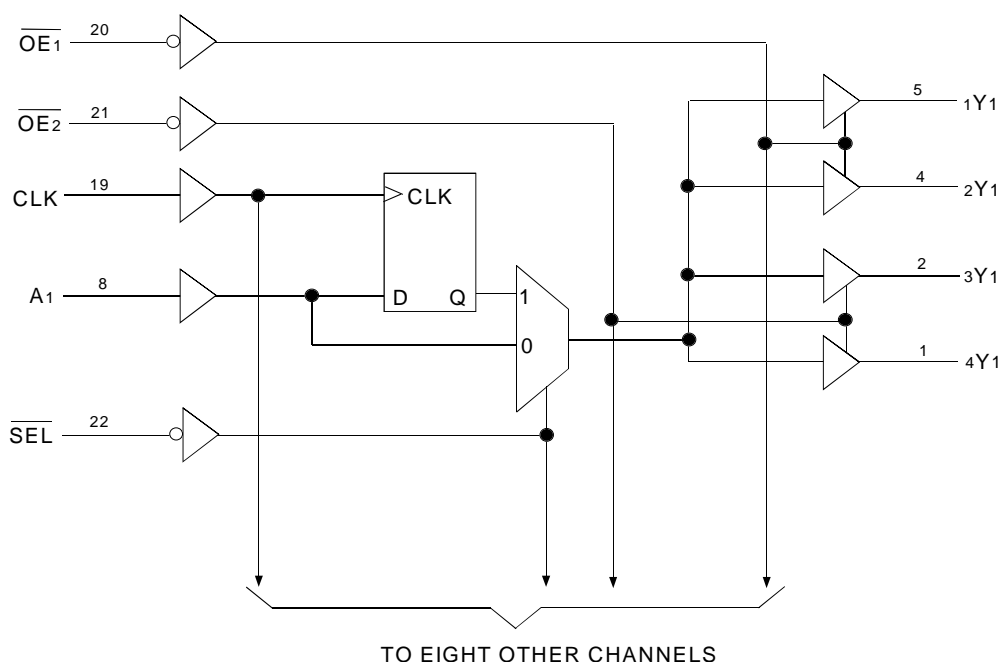
DESCRIPTION:

This 1-bit to 4-bit address register/driver is built using advanced dual metal CMOS technology. This device is ideal for use in applications in which a single address bus is driving four separate memory locations. The ALVC16831 can be used as a buffer or a register, depending on the logic level of the select (\overline{SEL}) input.

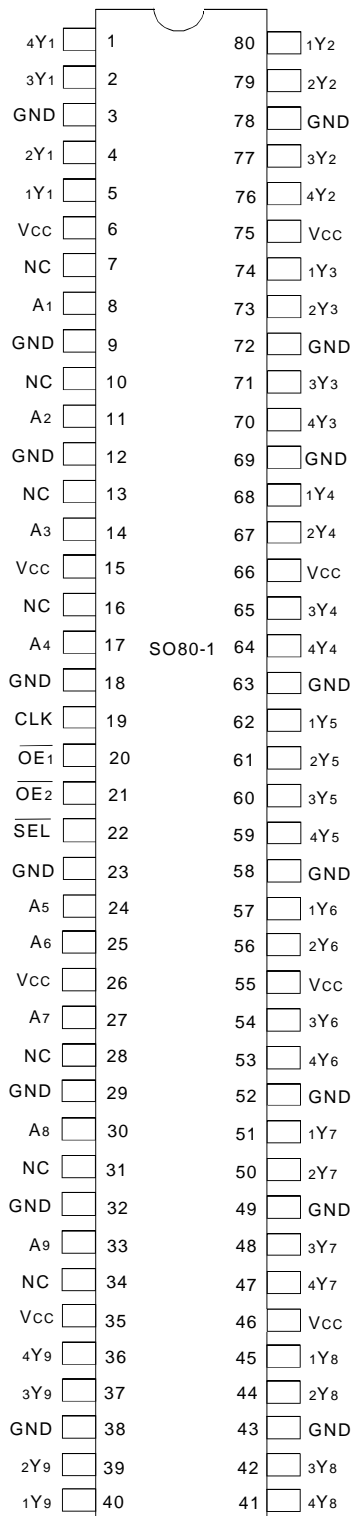
When \overline{SEL} is logic high, the device is in the buffer mode. The outputs follow the inputs and are controlled by the two output-enable (\overline{OE}) controls. Each \overline{OE} controls two groups of nine outputs. When \overline{SEL} is logic low, the device is in the register mode. The register is an edge-triggered D-type flip-flop. On the positive transition of the clock (CLK) input, data set up at the A inputs is stored in the internal registers. \overline{OE} controls operate the same as in buffer mode.

The ALVC16831 has been designed with a $\pm 24mA$ output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



TVSOP
TOP VIEW

ABSOLUTE MAXIMUM RATING (1)

Symbol	Description	Max.	Unit
$V_{TERM}^{(2)}$	Terminal Voltage with Respect to GND	- 0.5 to + 4.6	V
$V_{TERM}^{(3)}$	Terminal Voltage with Respect to GND	- 0.5 to $V_{CC} + 0.5$	V
TSTG	Storage Temperature	- 65 to + 150	°C
I _{OUT}	DC Output Current	- 50 to + 50	mA
I _{IK}	Continuous Clamp Current, $V_I < 0$ or $V_I > V_{CC}$	± 50	mA
I _{OK}	Continuous Clamp Current, $V_O < 0$	- 50	mA
I _{CC}	Continuous Current through each V _{CC} or GND	± 100	mA

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NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- All terminals except V_{CC}.

CAPACITANCE ($T_A = +25^\circ\text{C}$, $f = 1.0\text{MHz}$)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	$V_{IN} = 0V$	5	7	pF
C _{OUT}	Output Capacitance	$V_{OUT} = 0V$	7	9	pF
C _{I/O}	I/O Port Capacitance	$V_{IN} = 0V$	7	9	pF

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NOTE:

- As applicable to the device type.

PIN DESCRIPTION

Pin Names	Description
$\overline{\text{OEx}}$	3-State Output Enable Inputs (Active LOW)
CLK	Register Input Clock
$\overline{\text{SEL}}$	Select Input
Ax	Data Inputs
xYx	3-State Outputs
NC	No Internal Connection

FUNCTION TABLE (1)

Inputs				Outputs
$\overline{\text{OEx}}$	$\overline{\text{SEL}}$	CLK	Ax	xYx
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance
↑ = LOW-to-HIGH Transition

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = -40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
VIH	Input HIGH Voltage Level	VCC = 2.3V to 2.7V		1.7	—	—	V
		VCC = 2.7V to 3.6V		2	—	—	
VIL	Input LOW Voltage Level	VCC = 2.3V to 2.7V		—	—	0.7	V
		VCC = 2.7V to 3.6V		—	—	0.8	
IiH	Input HIGH Current	VCC = 3.6V	Vi = VCC	—	—	± 5	μA
IiL	Input LOW Current	VCC = 3.6V	Vi = GND	—	—	± 5	
IoZH	High Impedance Output Current (3-State Output pins)	VCC = 3.6V	Vo = VCC	—	—	± 10	μA
IoZL			Vo = GND	—	—	± 10	μA
Vik	Clamp Diode Voltage	VCC = 2.3V, IIN = -18mA		—	-0.7	-1.2	V
VH	Input Hysteresis	VCC = 3.3V		—	100	—	mV
ICCL	Quiescent Power Supply Current	VCC = 3.6V		—	0.1	40	μA
ICCH		VIN = GND or VCC					
IC CZ							
ΔICC	Quiescent Power Supply Current Variation	One input at VCC - 0.6V, other inputs at VCC or GND		—	—	750	μA

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NOTE:

1. Typical values are at VCC = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
VOH	Output HIGH Voltage	VCC = 2.3V to 3.6V	IOH = -0.1mA	VCC - 0.2	—	V
		VCC = 2.3V	IOH = -6mA	2	—	
		VCC = 2.3V	IOH = -12mA	1.7	—	
		VCC = 2.7V		2.2	—	
		VCC = 3.0V		2.4	—	
		VCC = 3.0V	IOH = -24mA	2	—	
VOL	Output LOW Voltage	VCC = 2.3V to 3.6V	IOL = 0.1mA	—	0.2	V
		VCC = 2.3V	IOL = 6mA	—	0.4	
			IOL = 12mA	—	0.7	
		VCC = 2.7V	IOL = 12mA	—	0.4	
		VCC = 3.0V	IOL = 24mA	—	0.55	

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NOTE:

1. VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate VCC range. TA = -40°C to +85°C.

OPERATING CHARACTERISTICS, $T_A = 25^\circ\text{C}$

Symbol	Parameter	Test Conditions	$V_{CC} = 2.5V \pm 0.2V$	$V_{CC} = 3.3V \pm 0.3V$	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance Outputs enabled	$C_L = 0\text{pF}$, $f = 10\text{MHz}$	119	132	pF
CPD	Power Dissipation Capacitance Outputs disabled		22	25	pF

SWITCHING CHARACTERISTICS⁽¹⁾

Symbol	Parameter	$V_{CC} = 2.5V \pm 0.2V$		$V_{CC} = 2.7V$		$V_{CC} = 3.3V \pm 0.3V$		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{MAX}		150	—	150	—	150	—	MHz
t_{PLH} t_{PHL}	Propagation Delay Ax to xYx	1.2	4		4.1	1.6	3.6	ns
t_{PLH} t_{PHL}	Propagation Delay SEL to xYx	1.3	5.2		5.2	1.7	4.4	ns
t_{PLH} t_{PHL}	Propagation Delay CLK to xYx	1.1	4.5		4.4	1.5	3.9	ns
t_{PZH} t_{PZL}	Output Enable Time OEx to xYx	1.1	5.1		5	1.2	4.3	ns
t_{PHZ} t_{PLZ}	Output Disable Time OEx to xYx	1.4	5.5		4.7	1.6	4.5	ns
t_w	Pulse Duration, CLK HIGH or LOW	3.3	—	3.3	—	3.3	—	ns
t_{SU}	Setup Time, Ax data before CLK \uparrow	2	—	2	—	1.6	—	ns
t_H	Hold Time, Ax data after CLK \uparrow	0.7	—	0.5	—	1.1	—	ns
$t_{sk(0)}$	Output Skew ⁽²⁾	—	—	—	—	—	500	ps

NOTES:

- See test circuits and waveforms. $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.
- Skew between any two outputs of the same package and switching in the same direction.

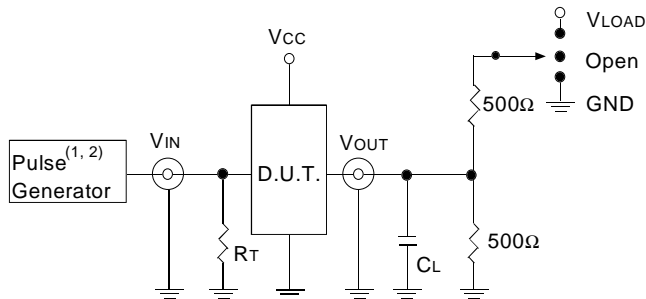
TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	V _{CC} (1)= 3.3V±0.3V	V _{CC} (1)= 2.7V	V _{CC} (2)= 2.5V±0.2V	Unit
V _{LOAD}	6	6	2 x V _{CC}	V
V _{IH}	2.7	2.7	V _{CC}	V
V _T	1.5	1.5	V _{CC} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF

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TEST CIRCUITS FOR ALL OUTPUTS



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DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

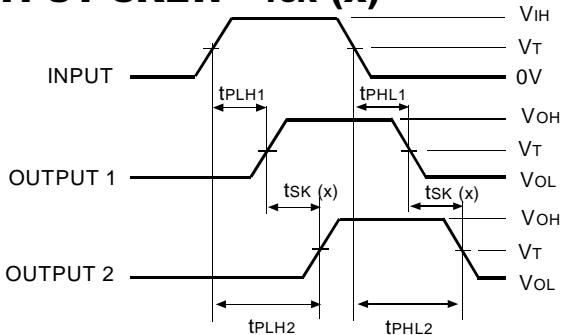
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other tests	Open

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OUTPUT SKEW - TSK (x)



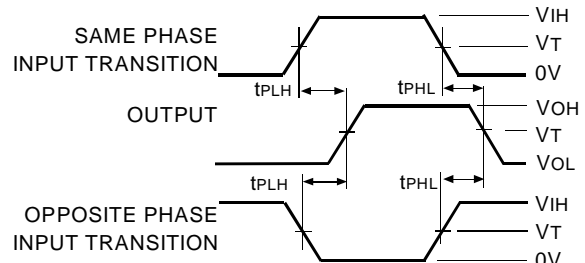
$$tsk(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

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NOTES:

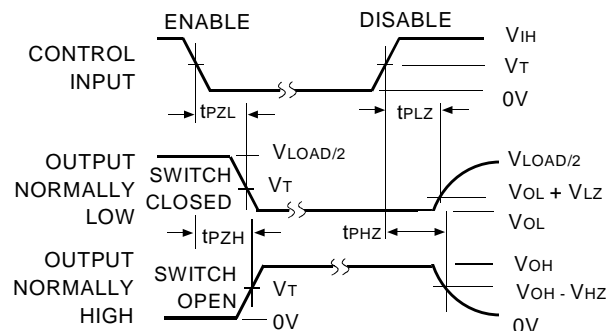
1. For tsk(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For tsk(b) OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



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ENABLE AND DISABLE TIMES

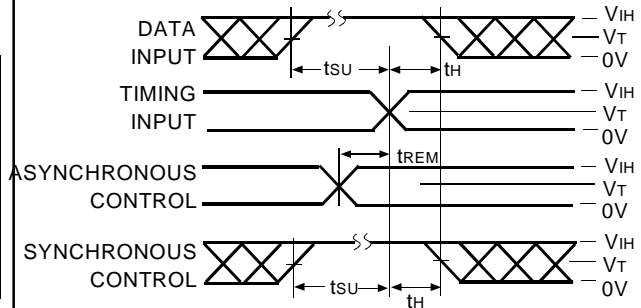


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NOTE:

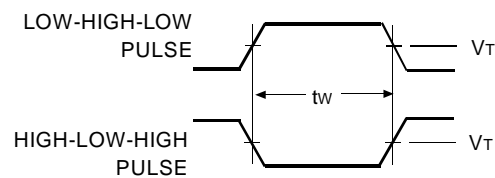
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



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PULSE WIDTH



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ORDERING INFORMATION

IDT	XX	ALVC	X	XXX	XXX	XX	
	Temp. Range		Bus-Hold	Family	Device Type	Package	
						DF	Thin Very Small Outline Package (SO80-1)
					831		1-Bit to 4-Bit Address Register/Driver with 3-State Outputs
				16			Double-Density with Resistors, ±24mA
			Blank				No Bus-Hold
						74	-40°C to +85°C



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