



3.3V CMOS QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUTS AND 5 VOLT TOLERANT I/O

IDT74LVC125A

FEATURES:

- 0.5 MICRON CMOS Technology
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 1.27mm pitch SOIC, 0.65mm pitch SSOP and 0.65mm pitch TSSOP packages
- Extended commercial range of - 40°C to +85°C
- V_{CC} = 3.3V ±0.3V, Normal Range
- V_{CC} = 2.3V to 3.6V, Extended Range
- CMOS power levels (0.4μW typ. static)
- Rail-to-Rail output swing for increased noise margin
- All inputs, outputs and I/O are 5 Volt tolerant
- Supports hot insertion

Drive Features for LVC125A:

- High Output Drivers: ±24mA
- Reduced system switching noise

APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

DESCRIPTION:

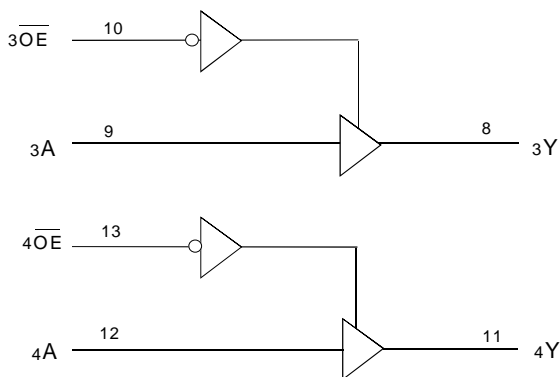
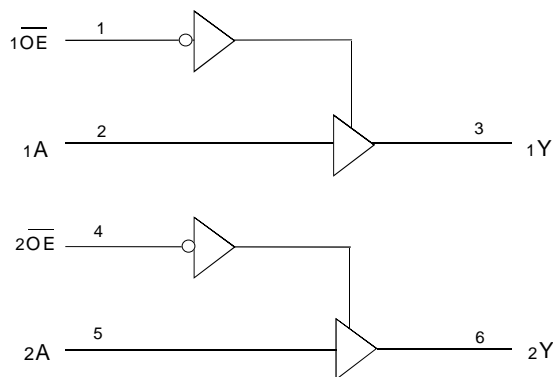
The LVC125A quadruple bus buffer gate is built using advanced dual metal CMOS technology. The LVC125A features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (\overline{OE}) input is high.

To ensure the high impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

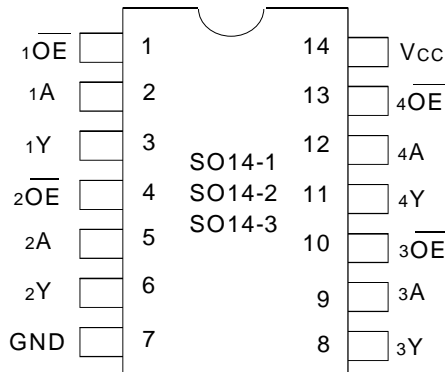
Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V system environment.

The LVC125A has been designed with a ±24mA output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SOIC/ SSOP/ TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

Symbol	Description	Max.	Unit
V _{TERM}	Terminal Voltage with Respect to GND	- 0.5 to +6.5	V
T _{STG}	Storage Temperature	- 65 to +150	°C
I _{OUT}	DC Output Current	- 50 to +50	mA
I _{IK}	Continuous Clamp Current, V _I < 0 or V _O < 0	- 50	mA
I _{OK}			
I _{CC}	Continuous Current through each V _{CC} or GND	±100	mA
I _{SS}			

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NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8	pF
C _{I/O}	I/O Port Capacitance	V _{IN} = 0V	6.5	8	pF

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NOTE:

- As applicable to the device type.

PIN DESCRIPTION

Pin Names	Description
x \overline{OE}	Output-Enable Inputs (Active LOW)
xA	Data Inputs
xY	3-State Outputs

FUNCTION TABLE (each buffer) ⁽¹⁾

Inputs		Outputs
x \overline{OE}	xA	xY
L	H	H
L	L	L
H	X	Z

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V _{IH}	Input HIGH Voltage Level	V _{CC} = 2.3V to 2.7V		1.7	—	—	V
		V _{CC} = 2.7V to 3.6V		2	—	—	
V _{IL}	Input LOW Voltage Level	V _{CC} = 2.3V to 2.7V		—	—	0.7	V
		V _{CC} = 2.7V to 3.6V		—	—	0.8	
I _{IH} I _{IL}	Input Leakage Current	V _{CC} = 3.6V	V _I = 0 to 5.5V	—	—	±5	μA
I _{OZH} I _{OZL}	High Impedance Output Current (3-State Output pins)	V _{CC} = 3.6V	V _O = 0 to 5.5V	—	—	±10	μA
I _{OFF}	Input/Output Power Off Leakage	V _{CC} = 0V, V _{IN} or V _O ≤ 5.5V		—	—	±50	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = 2.3V, I _{IN} = -18mA		—	-0.7	-1.2	V
V _H	Input Hysteresis	V _{CC} = 3.3V		—	100	—	mV
I _{CCL} I _{CCH} I _{CCZ}	Quiescent Power Supply Current	V _{CC} = 3.6V	V _{IN} = GND or V _{CC}	—	—	10	μA
ΔI _{CC}	Quiescent Power Supply Current Variation	One input at V _{CC} - 0.6V other inputs at V _{CC} or GND		—	—	500	μA

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NOTE:

1. Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = 2.3V to 3.6V	I _{OH} = -0.1mA	V _{CC} - 0.2	—	V
		V _{CC} = 2.3V	I _{OH} = -6mA	2	—	
		V _{CC} = 2.3V	I _{OH} = -12mA	1.7	—	
		V _{CC} = 2.7V		2.2	—	
		V _{CC} = 3.0V		2.4	—	
		V _{CC} = 3.0V	I _{OH} = -24mA	2.2	—	
V _{OL}	Output LOW Voltage	V _{CC} = 2.3V to 3.6V	I _{OL} = 0.1mA	—	0.2	V
		V _{CC} = 2.3V	I _{OL} = 6mA	—	0.4	
			I _{OL} = 12mA	—	0.7	
		V _{CC} = 2.7V	I _{OL} = 12mA	—	0.4	
		V _{CC} = 3.0V	I _{OL} = 24mA	—	0.55	

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NOTE:

1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

OPERATING CHARACTERISTICS, $T_A = 25^\circ\text{C}$

Symbol	Parameter	Test Conditions	V _{CC} = 2.5V±0.2V	V _{CC} = 3.3V±0.3V	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance per gate	C _L = 0pF, f = 10Mhz	11.3	15	pF

SWITCHING CHARACTERISTICS (1)

Symbol	Parameter	V _{CC} = 2.5V±0.2V		V _{CC} = 2.7V		V _{CC} = 3.3V±0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{PLH} t _{PHL}	Propagation Delay x _A to x _Y	1	6.3	—	5.5	1	4.8	ns
t _{PZH} t _{PZL}	Output Enable Time x _{OE} to x _Y	1	7.4	—	6.6	1	5.4	ns
t _{PHZ} t _{PLZ}	Output Disable Time x _{OE} to x _Y	1	5.6	—	5	1	4.6	ns
t _{SK (o)}	Output Skew (2)	—	—	—	—	—	1	ns

NOTES:

1. See test circuits and waveforms. $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.
2. Skew between any two outputs of the same package and switching in the same direction.

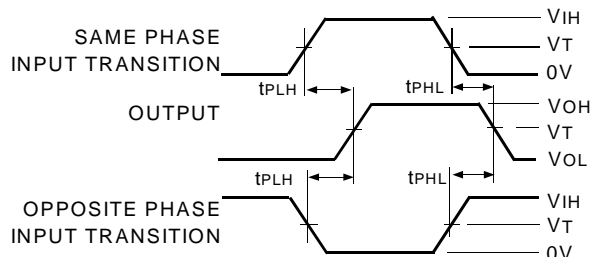
TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	V _{CC} (1)= 2.5V ±0.2V	V _{CC} (2)= 3.3V ±0.3V & 2.7V	Unit
V _{LOAD}	2 x V _{CC}	6	V
V _{IH}	V _{CC}	2.7	V
V _T	V _{CC} / 2	1.5	V
V _{LZ}	150	300	mV
V _{HZ}	150	300	mV
C _L	30	50	pF

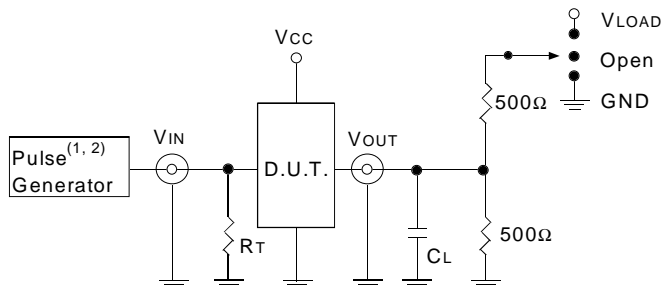
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PROPAGATION DELAY



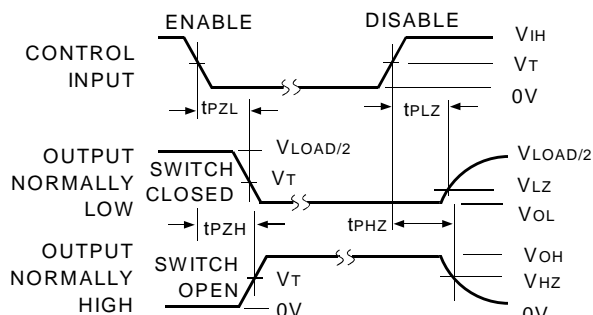
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TEST CIRCUITS FOR ALL OUTPUTS



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ENABLE AND DISABLE TIMES



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DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

NOTE:

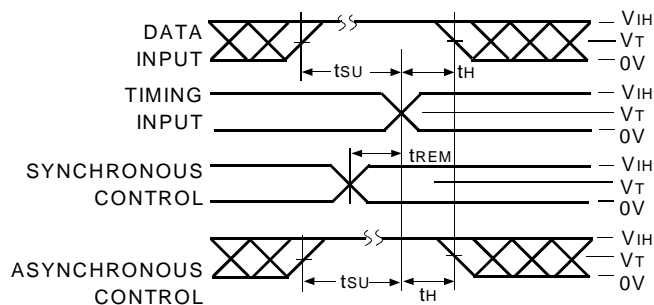
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other tests	Open

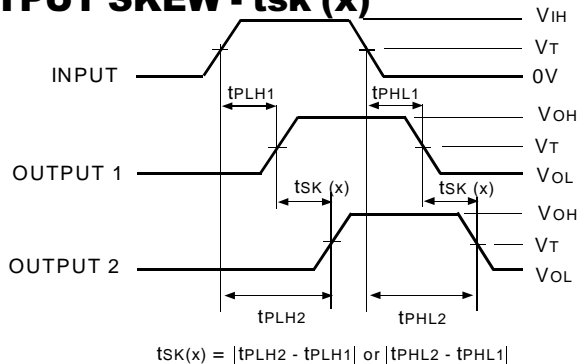
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SET-UP, HOLD, AND RELEASE TIMES



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OUTPUT SKEW - t_{SK}(x)



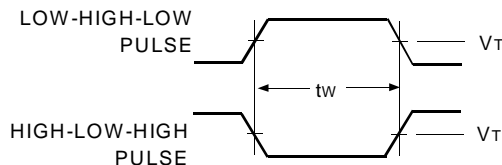
$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

NOTES:

1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

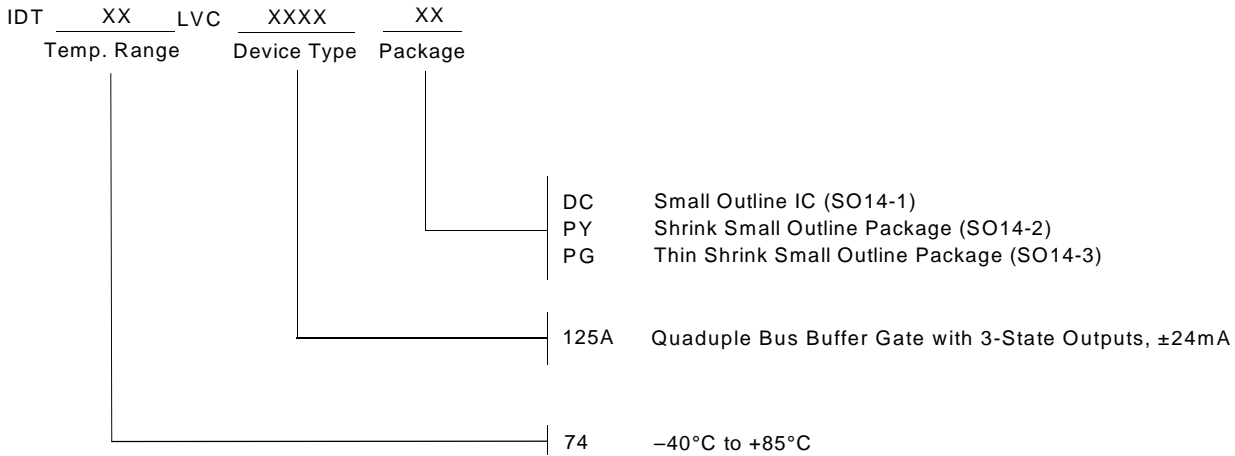
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PULSE WIDTH



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ORDERING INFORMATION



CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
800-345-7015 or 408-727-6116
fax: 408-492-8674
www.idt.com*

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