Quad Port PHY (Physical Layer) for 25.6, 51.2, and 204.8 Mbps ATM Networks and Backplane Applications

IDT77V1264L200

Features List

- Performs the PHY-Transmission Convergence (TC) and Physical Media Dependent (PMD) Sublayer functions for four 204.8 Mbps ATM channels
- Compliant to ATM Forum (af-phy-040.000) and ITU-T I.432.5 specifications for 25.6 Mbps physical interface
- Operates at 25.6, 51.2, 102.4, 204.8 Mbps data rates
- Individual Selection of Port Data Rates
- Backwards Compatible with 77V1254L25
- UTOPIA Level 1, UTOPIA Level 2, or DPI-4 Interface
- 3-Cell Transmit and Receive FIFOs
- LED Interface for status signalling
- Supports UTP Category 3 and 5 physical media
- Low-Power CMOS
- 3.3V supply with 5V tolerant inputs
- 144-pin PQFP Package (28 x 28 mm)
- Commercial and Industrial Temperature Ranges

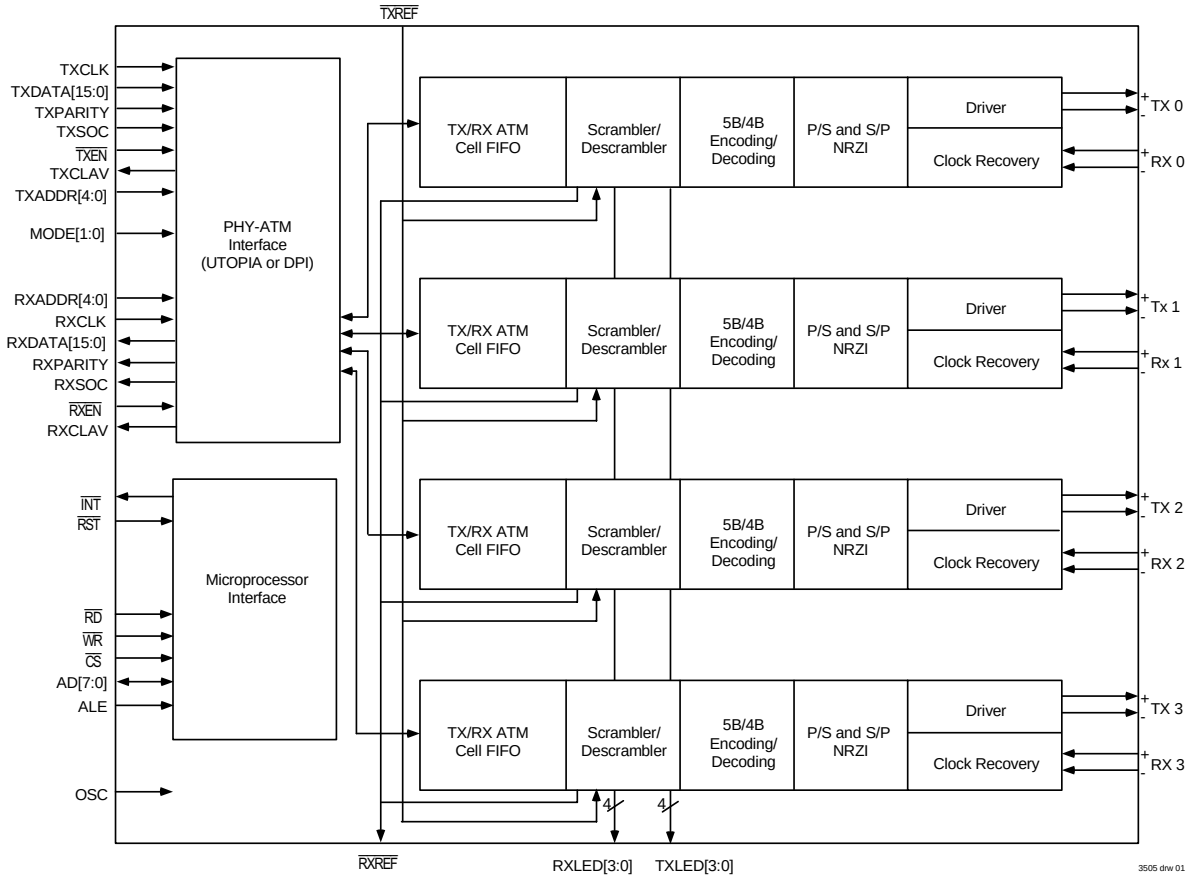
Description

The IDT77V1264L200 is a member of IDT's family of products supporting Asynchronous Transfer Mode (ATM) data communications and networking. The IDT77V1264L200 implements the physical layer for 25.6 Mbps ATM, connecting four serial copper links (UTP Category 3 and 5) to one ATM layer device such as a SAR or a switch ASIC. The IDT77V1264L200 also operates at 51.2 Mbps and 204.8 Mbps, and is well suited to backplane driving applications.

The 77V1264L200-ATM layer interface is selectable as either: 16-bit UTOPIA Level 2, 8-bit UTOPIA Level 1 Multi-PHY, or quadruple 4-bit DPI (Data Path Interface).

The IDT77V1264L200 is fabricated using IDT's state-of-the-art CMOS technology, providing the highest levels of integration, performance and reliability, with the low-power consumption characteristics of CMOS.

Block Diagram



Applications

- Up to 204.8Mbps backplane transmission
- Rack-to-rack short links
- ATM Switches

77V1264L200 Overview

The 77V1264L200 is a four port implementation of the physical layer standard for 25.6Mbps ATM network communications as defined by ATM Forum document af-phy-040.000 and ITU-T I.432.5. The physical layer is divided into a Physical Media Dependent sub layer (PMD) and Transmission Convergence (TC) sub layer. The PMD sub layer includes the functions for the transmitter, receiver and clock recovery for operation across 100 meters of category 3 and 5 unshielded twisted pair (UTP) cable. This is referred to as the Line Side Interface. The TC sub layer defines the line coding, scrambling, data framing and synchronization.

On the other side, the 77V1264L200 interfaces to an ATM layer device (such as a switch core or SAR). This cell level interface is configurable as either an 8-bit Utopia Level 1 Multi-PHY, 16-bit Utopia Level 2, or four 4-bit DPI interface, as determined by two MODE pins. This is referred to as the PHY-ATM Interface. The pinout and front page block diagram are based on the Utopia 2 configuration. Table 3 shows the corresponding pin functions for the other two modes, and Figure 2 and Figure 3 show functional block diagrams.

The 77V1264L200 is based on the 77105, and maintains significant register compatibility with it. The 77V1264L200, however, has additional register features, and also duplicates most of its registers to provide significant independence between the four ports.

Access to these status and control registers is through the utility bus. This is an 8-bit muxed address and data bus, controlled by a conventional asynchronous read/write handshake.

Additional pins permit insertion and extraction of an 8kHz timing marker, and provide LED indication of receive and transmit status.

Auto-Synchronization and Good Signal Indication

The 77V1264L200 features a new receiver synchronization algorithm that allow it to achieve 4b/5b symbol framing on any valid data stream. This is an improvement on earlier products which could frame only on the escape symbol, which occurs only in start-of-cell or 8kHz (X8) timing marker symbol pairs.

ATM25 transceivers always transmit valid 4b/5b symbols, allowing the 77V1264L200 receive section to achieve symbol framing and properly indicate receive signal status, even in the absence of ATM cells or 8kHz (X8) timing markers in the receive data stream. A state machine monitors the received symbols and asserts the “Good Signal” status bit when a valid signal is being received. “Good Signal” is deasserted and the receive FIFO is disabled when the signal is lost. This is sometimes referred to as Loss of Signal (LOS).

Operation at Speeds Above 25 Mbps

In addition to operation at the standard rate of 25.6 Mbps, the 77V1264L200 can be operated at a range of data rates, up to 204.8 Mbps, as shown in Table 3. For 204.8Mbps data rate applications, ST6200T magnetics from Pulse Engineering can be used. These magnetics have been tested to work over 10 meters of UTP 5 cable at 204.8Mbps. The rate is determined by the frequency of the OSC clock, multiplied by the internal PLL clock multiplier factor (1x, 2x or 4x) as determined in the Enhanced Control 2 Registers. Although the OSC clock frequency is common to all ports of the PHY, the clock multiplier factor can be set individually for each port. As an example, with a 64 MHz oscillator, this allows some ports to operate at 51.2 Mbps while other ports are simultaneously operating at 204.8 Mbps.

When operating at clock multiples other than 1x, use of the $\overline{\text{RXREF}}$ pin requires that the $\overline{\text{RXREF}}$ Pulse Width Select field in the LED Driver and HEC Status/Control Registers be programmed to a value greater than the default of 1 cycle.

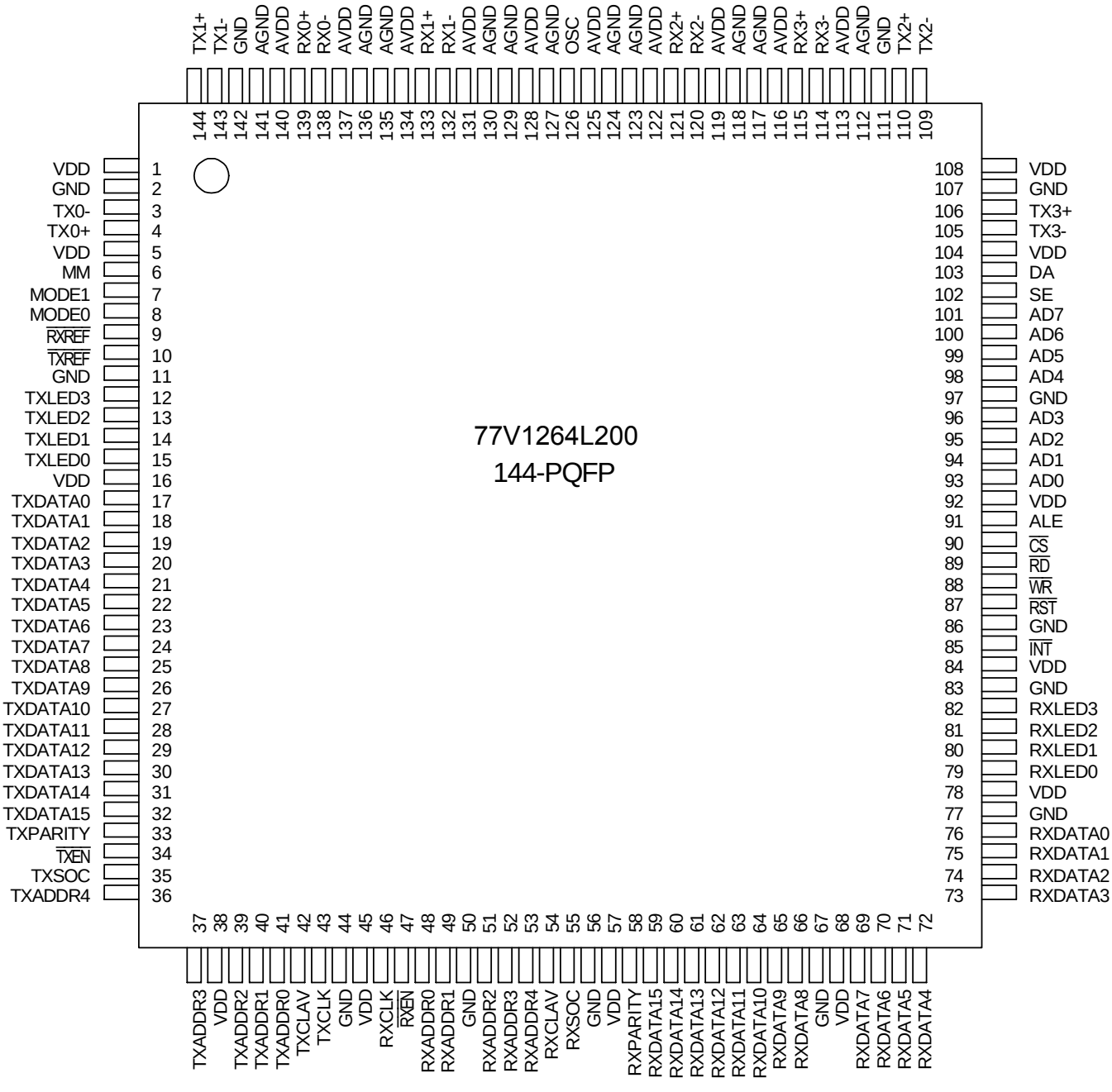
Also, the PHY loopback mode without clock recovery (10) in the Diagnostic Control Registers works only when the clock multiplier is 1x. For higher multiples, the PHY loopback mode (01) with clock recovery must be used.

Except as noted above, these higher speed configurations operate exactly the same as the basic 25.6 Mbps configuration. The scrambling and encoding are unchanged.

Table 1 shows some of the different data rates the PHY can operate at with a 32MHz or 64MHz oscillator. Note that any oscillator frequency between 32MHz and 64MHz can be used. For example, if a 48MHz oscillator is used and the multiplier is set to 4x, the data rate would be 153.6Mbps.

Reference Clock (OSC)	Clock Multiplier Control Bits (Enhanced Control 2 Registers)	Line Bit Rate (MHz)	Data Rate (Mbps)
32 MHz	00 (1x)	32	25.6
	01 (2x)	64	51.2
	10 (4x)	128	102.4
64 MHz	00 (1x)	64	51.2
	01 (2x)	128	102.4
	10 (4x)	256	204.8

Table 1 200 Speed Grade Option



3505 drw 02

Figure 1 Pin Assignments

Signal Descriptions

Line Side Signals			
Signal Name	**Pin Number**	**I/O**	**Signal Description**
RX0+,-	139, 138	In	Port 0 positive and negative receive differential input pair.
RX1+,-	133, 132	In	Port 1 positive and negative receive differential input pair.
RX2+,-	121, 120	In	Port 2 positive and negative receive differential input pair.
RX3+,-	115, 114	In	Port 3 positive and negative receive differential input pair.
TX0+,-	4, 3	Out	Port 0 positive and negative transmit differential output pair.
TX1+,-	144, 143	Out	Port 1 positive and negative transmit differential output pair.
TX2+,-	110, 109	Out	Port 2 positive and negative transmit differential output pair.
TX3+,-	106, 105	Out	Port 3 positive and negative transmit differential output pair.
Utility Bus Signals			
Signal Name	**Pin Number**	**I/O**	**Signal Description**
AD[7:0]	101, 100, 99, 98, 96, 95, 94, 93	In/Out	Utility bus address/data bus. The address input is sampled on the falling edge of ALE. Data is output on this bus when a read is performed. Input data is sampled at the completion of a write operation.
ALE	91	In	Utility bus address latch enable. Asynchronous input. An address on the AD bus is sampled on the falling edge of ALE. ALE must be low when the AD bus is being used for data.
$\overline{CS}$	90		Utility bus asynchronous chip select. $\overline{CS}$ must be asserted to read or write an internal register. It may remain asserted at all times if desired
$\overline{RD}$	89	In	Utility bus read enable. Active low asynchronous input. After latching an address, a read is performed by deasserting $\overline{WR}$ and asserting $\overline{RD}$ and $\overline{CS}$.
$\overline{WR}$	88	In	Utility bus write enable. Active low asynchronous input. After latching an address, a write is performed by deasserting $\overline{RD}$, placing data on the AD bus, and asserting $\overline{WR}$ and $\overline{CS}$. Data is sampled when $\overline{WR}$ or $\overline{CS}$ is deasserted.
Miscellaneous Signals			
Signal Name	**Pin Number**	**I/O**	**Signal Description**
DA	103	In	Reserved signal. This input must be connected to logic low.
$\overline{INT}$	85	Out	Interrupt. $\overline{INT}$ is an open-drain output, driven low to indicate an interrupt. Once low, $\overline{INT}$ remains low until the interrupt status in the appropriate interrupt Status Register is read. Interrupt sources are programmable via the interrupt Mask Registers.
MM	6	In	Reserved signal. This input must be connected to logic low.
MODE[1:0]	7, 8	In	Mode Selects. They determine the configuration of the PHY/ATM interface. 00 = UTOPIA Level 2. 01 = UTOPIA Level 1. 10 = DPI. 11 is reserved.
OSC	126	In	TTL line rate clock source, driven by a 100 ppm oscillator. 32 MHz or 64 MHz.
$\overline{RST}$	87	In	Reset. Active low asynchronous input resets all control logic, counters and FIFOs. A reset must be performed after power up prior to normal operation of the part.
RXLED[3:0]	82, 81, 80, 79	Out	Receive LED drivers. Driven low for 223 cycles of OSC, beginning with RXSOC when that port receives a good (non-null and non-errored) cell. Drives 8 mA both high and low. One per port.
$\overline{RXREF}$	9	Out	Receive Reference. Active low, synchronous to OSC. $\overline{RXREF}$ pulses low for a programmable number of clock cycles when an x_8 command byte is received. Register 0x40 is programmed to indicate which port is referenced. Note that when operating the 77V1264L200 at 2x or 4x multiple of OSC (See Enhanced Control 2 Registers) the $\overline{RXREF}$ pulse width (See LED Driver and HEC Status/Control Registers) must be programmed to any value greater than the default for proper operation of $\overline{RXREF}$.

Table 2 Signal Descriptions (Part 1 of 3)

SE	102	In	Reserved signal. This input must be connected to logic low.
TXLED[3:0]	12, 13, 14, 15	Out	Ports 3 through 0 Transmit LED driver. Goes low for 223 cycles of OSC, beginning with TXSOC when this port receives a cell for transmission. 8 mA drive current both high and low. One per port.
$\overline{\text{TXREF}}$	10	In	Transmit Reference. Synchronous to OSC. On the falling edge, an X_8 command byte is inserted into the transmit data stream. Logic for this signal is programmed in register 0x40. Typical application is WAN timing.
Power Supply Signals			
Signal Name	**Pin Number**	**I/O**	**Signal Description**
AGND	112, 117, 118, 123, 124, 127, 129, 130, 135, 136, 141	____	Analog ground. AGND supply a ground reference to the analog portion of the ship, which sources a more constant current than the digital portion.
AVDD	113, 116, 119, 122, 125, 128, 131, 134, 137, 140	____	Analog power supply 3.3 ± 0.3V AVDD supply power to the analog portion of the chip, which draws a more constant current than the digital portion.
GND	2, 11, 44, 50, 56, 67, 77, 83, 86, 97, 107, 111, 142	____	Digital Ground.
VDD	1, 5, 16, 38, 45, 57, 68, 78, 84, 92, 104, 108	____	Digital power supply. 3.3 ± 0.3V.
16-BIT UTOPIA 2 Signals (MODE[1:0] = 00)			
Signal Name	**Pin Number**	**I/O**	**Signal Description**
RXADDR[4:0]	53, 52, 51, 49, 48	In	Utopia 2 Receive Address Bus. This bus is used in polling and selecting the receive port. The port addresses are defined in bits [4:0] of the Enhanced Control Registers.
RXCLAV	54	Out	Utopia 2 Receive Cell Available. Indicates the cell available status of the addressed port. It is asserted when a full cell is available for retrieval from the receive FIFO. When non of the four ports is addressed. RXCLAV is high impedance.
RXCLK	46	In	Utopia 2 Receive Clock. This is a free running clock input.
RXDATA[15:0]	59, 60, 61, 62, 63, 64, 65, 66, 69, 70, 71, 72, 73, 74, 75, 76	Out	Utopia 2 Receive Data. When one of the four ports is selected, the 77V1264L200 transfers received cells to an ATM device across this bus. Also see RXPARITY.
$\overline{\text{RXEN}}$	47	In	Utopia 2 Receive Enable. Driven by an ATM device to indicate its ability to receive data across the RXDATA bus.
RXPARITY	58	Out	Utopia 2 Receive Data Parity. Odd parity over RXDATA[15:0].
RXSOC	55	Out	Utopia 2 Receive Start of Cell. Asserted coincident with the first word of data for each cell on RXDATA.
TXADDR[4:0]	36, 37, 39, 40, 41	In	Utopia 2 Transmit Address Bus. This bus is used in polling and selecting the transmit port. The port addresses are defined in bits [4:0] of the Enhanced Control Registers.
TXCLAV	42	Out	Utopia 2 Transmit Cell Available. Indicates the availability of room in the transmit FIFO of the addressed port for a full cell. When none of the four ports is addressed, TXCLAV is high impedance.
TXCLK	43	In	Utopia Transmit Clock. This is a free running clock input.
TXDATA[15:0]	32, 31, 30, 29, 28, 27, 26, 25, 24, 23, 22, 21, 20, 19, 18, 17	In	Utopia 2 Transmit Data. An ATM device transfers cells across this bus to the 77V1264L200 for transmission. Also see TXPARITY.
$\overline{\text{TXEN}}$	34	In	Utopia 2 Transmit Enable. Driven by an ATM device to indicate it is transmitting data across the TXDATA bus.
TXPARITY	33	In	Utopia 2 Transmit Data Parity. Odd parity across TXDATA[15:0]. Parity is checked and errors are indicated in the Interrupt Status Registers, as enabled in the Master Control Registers. No other action is taken in the event of an error. Tie high or low if unused.
TXSOC	35	In	Utopia 2 Transmit Start of Cell. Asserted coincident with the first word of data for each cell on TXDATA.

Table 2 Signal Descriptions (Part 2 of 3)

8-BIT UTOPIA Level 1 Signals (MODE[1:0] = 01)			
Signal Name	**Pin Number**	**I/O**	**Signal Description**
RXCLAV[3:0]	64, 65, 66, 54	Out	Utopia 1 Receive Cell Available. Indicates the cell available status of the respective port. It is asserted when a full cell is available for retrieval from the receive FIFO.
RXCLK	46	In	Utopia 1 Receive Clock. This is a free running clock input.
RXDATA[7:0]	69, 70, 71, 72, 73, 74, 75, 76	Out	Utopia 1 Receive Data. When one of the four ports is selected, the 77V1264L200 transfers received cells to an ATM device across this bus. Bit 5 in the Diagnostic Control Registers determines whether RXDATA tri-states when $\overline{\text{RXEN}}$[3:0] are high. Also see RXPARITY.
$\overline{\text{RXEN}}$[3:0]	51, 49, 48, 47	In	Utopia 1 Receive Enable. Driven by an ATM device to indicate its ability to receive data across the RXDATA bus. One for each port
RXPARITY	58	Out	Utopia 1 Receive Data Parity. Odd parity over RXDATA[7:0].
RXSOC	55	Out	Utopia 1 Receive Start of Cell. Asserted coincident with the first word of data for each cell on RXDATA. Tri-statable as determined by bit 5 in the Diagnostic Control Registers.
TXCLAV[3:0]	39, 40, 41, 42	Out	Utopia 1 Transmit cell Available. Indicates the availability of room in the transmit FIFO of the respective port for a full cell.
TXCLK	43	In	Utopia 1 Transmit Clock. This is a free running clock input.
TXDATA[7:0]	24, 23, 22, 21, 20, 19, 18, 17	In	Utopia 1 Transmit Data. An ATM device transfers cells across the bus to the 77V1264L200 for transmission. Also see TXPARITY.
$\overline{\text{TXEN}}$[3:0]	27, 26, 25, 34	In	Utopia 1 Transmit Enable. Driven by an ATM device to indicate it is transmitting data across the TXDATA bus. One for each port.
TXPARITY	33	In	Utopia 1 Transmit Data Parity. Odd parity across TXDATA[7:0]. Parity is checked and errors are indicated in the Interrupt Status Registers, as enabled in the Master Control Registers. No other action is taken in the event of an error. Tie high or low if unused.
TXSOC	35	In	Utopia 1 Transmit Start of Cell. Asserted coincident with the first word of data for each cell on TXDATA.
DPI Mode Signals (MODE[1:0] = 10)			
Signal Name	**Pin Number**	**I/O**	**Signal Description**
DPICLK	43	In	DPI Source Clock for Transmit. This is the free-running clock used as the source to generate Pn_TCLK.
Pn_RCLK	52, 51, 49, 48	In	DPI Port 'n' Receive Clock. Pn_RCLK is cycled to indicate that the interfacing device is ready to receive a nibble of data on Pn_RD[3:0] of port 'n'.
Pn_RD[3:0]	59, 60, 61, 62, 63, 64, 65, 66, 69, 70, 71, 72, 73, 74, 75, 76	Out	DPI Port 'n' Receive Data. Cells received on port 'n' are passed to the interfacing device across this bus. Each port has its own dedicated bus.
Pn_RFRM	53, 58, 54, 55	Out	DPI Port 'n' Receive Frame. Pn_RFRM is asserted for one cycle immediately preceding the transfer of each cell on Pn_RD[3:0].
Pn_TCLK	37, 39, 40, 41	Out	DPI Port 'n' Transmit Clock. Pn_TCLK is derived from DPICLK and is cycled when the respective port is ready to accept another 4 bits of data on Pn_TD[3:0].
Pn_TD[3:0]	32, 31, 30, 29, 28, 27, 26, 25, 24, 23, 22, 21, 20, 19, 18, 17	In	DPI Port 'n' Transmit Data. Cells are passed across this bus to the PHY for transmission on port 'n'. Each port has its own dedicated bus.
Pn_TFRM	36, 33, 34, 35	In	DPI Port 'n' Transmit Frame. Start of cell signal which is asserted for one cycle immediately preceding the first 4 bits of each cell on Pn_TD[3:0].

Table 2 Signal Descriptions (Part 3 of 3)

Signal Assignment as a Function of PHY/ATM Interface Mode

SIGNAL NAME	PIN NUMBER	16-BIT UTOPIA 2 MODE[1,0] = 00	8-BIT UTOPIA 1 MODE[1,0] = 01	DPI MODE[1,0] = 10
VDD	1			
GND	2			
TX0-	3			
TX0+	4			
VDD	5			
MM	6			
MODE1	7			
MODE0	8			
$\overline{\text{RXREF}}$	9			
$\overline{\text{TXREF}}$	10			
GND	11			
TXLED3	12			
TXLED2	13			
TXLED1	14			
TXLED0	15			
VDD	16			
TXDATA0	17	TXDATA0	TXDATA0	P0_TD[0]
TXDATA1	18	TXDATA1	TXDATA1	P0_TD[1]
TXDATA2	19	TXDATA2	TXDATA2	P0_TD[2]
TXDATA3	20	TXDATA3	TXDATA3	P0_TD[3]
TXDATA4	21	TXDATA4	TXDATA4	P1_TD[0]
TXDATA5	22	TXDATA5	TXDATA5	P1_TD[1]
TXDATA6	23	TXDATA6	TXDATA6	P1_TD[2]
TXDATA7	24	TXDATA7	TXDATA7	P1_TD[3]
TXDATA8	25	TXDATA8	$\overline{\text{TXEN}}$[1]	P2_TD[0]
TXDATA9	26	TXDATA9	$\overline{\text{TXEN}}$[2]	P2_TD[1]
TXDATA10	27	TXDATA10	$\overline{\text{TXEN}}$[3]	P2_TD[2]
TXDATA11	28	TXDATA11	see note 2	P2_TD[3]
TXDATA12	29	TXDATA12	see note 2	P3_TD[0]
TXDATA13	30	TXDATA13	see note 2	P3_TD[1]
TXDATA14	31	TXDATA14	see note 2	P3_TD[2]
TXDATA15	32	TXDATA15	see note 2	P3_TD[3]
TXPARITY	33	TXPARITY	TXPARITY	P2_TFRM
$\overline{\text{TXEN}}$	34	$\overline{\text{TXEN}}$	$\overline{\text{TXEN}}$[0]	P1_TFRM
TXSOC	35	TXSOC	TXSOC	P0_TFRM
TXADDR4	36	TXADDR4	see note 2	P3_TFRM

Table 3 Signal Assignment as a Function of PHY/ATM Interface Mode (Part 1 of 4)

SIGNAL NAME	PIN NUMBER	16-BIT UTOPIA 2 MODE[1,0] = 00	8-BIT UTOPIA 1 MODE[1,0] = 01	DPI MODE[1,0] = 10
TXADDR3	37	TXADDR3	see note 2	P3_TCLK
VDD	38			
TXADDR2	39	TXADDR2	TXCLAV[3]	P2_TCLK
TXADDR1	40	TXADDR1	TXCLAV[2]	P1_TCLK
TXADDR0	41	TXADDR0	TXCLAV[1]	P0_TCLK
TXCLAV	42	TXCLAV	TXCLAV[0]	see note 1
TXCLK	43	TXCLK	TXCLK	DPICLK
GND	44			
VDD	45			
RXCLK	46	RXCLK	RXCLK	see note 2
$\overline{\text{RXEN}}$	47	$\overline{\text{RXEN}}$	$\overline{\text{RXEN}}$[0]	see note 2
RXADDR0	48	RXADDR0	$\overline{\text{RXEN}}$[1]	P0_RCLK
RXADDR1	49	RXADDR1	$\overline{\text{RXEN}}$[2]	P1_RCLK
GND	50			
RXADDR2	51	RXADDR2	$\overline{\text{RXEN}}$[3]	P2_RCLK
RXADDR3	52	RXADDR3	see note 2	P3_RCLK
RXADDR4	53	RXADDR4	see note 2	P3_RFRM
RXCLAV	54	RXCLAV	RXCLAV[0]	P1_RFRM
RXSOC	55	RXSOC	RXSOC	P0_FRM
GND	56			
VDD	57			
RXPARITY	58	RXPARITY	RXPARITY	P2_RFRM
RXDATA15	59	RXDATA15	see note 1	P3_RD[3]
RXDATA14	60	RXDATA14	see note 1	P3_RD[2]
RXDATA13	61	RXDATA13	see note 1	P3_RD[1]
RXDATA12	62	RXDATA12	see note 1	P3_RD[0]
RXDATA11	63	RXDATA11	see note 1	P2_RD[3]
RXDATA10	64	RXDATA10	RXCLAV[3]	P2_RD[2]
RXDATA9	65	RXDATA9	RXCLAV[2]	P2_RD[1]
RXDATA8	66	RXDATA8	RXCLAV[1]	P2_RD[0]
GND	67			
VDD	68			
RXDATA7	69	RXDATA7	RXDATA7	P1_RD[3]
RXDATA6	70	RXDATA6	RXDATA6	P1_RD[2]
RXDATA5	71	RXDATA5	RXDATA5	P1_RD[1]
RXDATA4	72	RXDATA4	RXDATA4	P1_RD[0]
RXDATA3	73	RXDATA3	RXDATA3	P0_RD[3]

Table 3 Signal Assignment as a Function of PHY/ATM Interface Mode (Part 2 of 4)

SIGNAL NAME	PIN NUMBER	16-BIT UTOPIA 2 MODE[1,0] = 00	8-BIT UTOPIA 1 MODE[1,0] = 01	DPI MODE[1,0] = 10
RXDATA2	74	RXDATA2	RXDATA2	P0_RD[2]
RXDATA1	75	RXDATA1	RXDATA1	P0_RD[1]
RXDATA0	76	RXDATA0	RXDATA0	P0_RD[0]
GND	77			
VDD	78			
RXLED0	79			
RXLED1	80			
RXLED2	81			
RXLED3	82			
GND	83			
VDD	84			
$\overline{INT}$	85			
GND	86			
$\overline{RST}$	87			
$\overline{WR}$	88			
$\overline{RD}$	89			
$\overline{CS}$	90			
ALE	91			
VDD	92			
AD0	93			
AD1	94			
AD2	95			
AD3	96			
GND	97			
AD4	98			
AD5	99			
AD6	100			
AD7	101			
SE	102			
DA	103			
VDD	104			
TX3-	105			
TX3+	106			
GND	107			
VDD	108			
TX2-	109			
TX2+	110			

Table 3 Signal Assignment as a Function of PHY/ATM Interface Mode (Part 3 of 4)

SIGNAL NAME	PIN NUMBER	16-BIT UTOPIA 2 MODE[1,0] = 00	8-BIT UTOPIA 1 MODE[1,0] = 01	DPI MODE[1,0] = 10
GND	111			
AGND	112			
AVDD	113			
RX3-	114			
RX3+	115			
AVDD	116			
AGND	117			
AGND	118			
AVDD	119			
RX2-	120			
RX2+	121			
AVDD	122			
AGND	123			
AGND	124			
AVDD	125			
OSC	126			
AGND	127			
AVDD	128			
AGND	129			
AGND	130			
AVDD	131			
RX1-	132			
RX1+	133			
AVDD	134			
AGND	135			
AGND	136			
AVDD	137			
RX0-	138			
RX0+	139			
AVDD	140			
AGND	141			
GND	142			
TX1-	143			
TX1+	144			

Table 3 Signal Assignment as a Function of PHY/ATM Interface Mode (Part 4 of 4)

Note: 1.This output signal is unused in this mode. It must be left unconnected.
2.This input signal is unused in this mode. It must be connected to either logic high or logic low.

Functional Description

Transmission Convergence (TC) Sub Layer

Introduction

The TC sub layer defines the line coding, scrambling, data framing and synchronization. Under control of a switch interface or Segmentation and Reassembly (SAR) unit, the 25.6Mbps ATM PHY accepts a 53-byte ATM cell, scrambles the data, appends a command byte to the beginning of the cell, and encodes the entire 53 bytes before transmission. These data transformations ensure that the signal is evenly distributed across the frequency spectrum. In addition, the serialized bit stream is NRZI coded. An 8kHz timing sync pulse may be used for isochronous communications.

Data Structure and Framing

Each 53-byte ATM cell is preceded with a command byte. This byte is distinguished by an escape symbol followed by one of 17 encoded symbols. Together, this byte forms one of seventeen possible command bytes. Three command bytes are defined:

1. **X_X** (read: 'escape' symbol followed by another 'escape'): Start-of-cell with scrambler/descrambler reset.
2. **X_4** ('escape' followed by '4'): Start-of-cell without scrambler/descrambler reset.
3. **X_8** ('escape' followed by '8'): 8kHz timing marker. This command byte is generated when the 8kHz sync pulse is detected, and has priority over all line activity (data or command bytes). It is transmitted immediately when the sync pulse is detected. When this occurs during a cell transmission, the data transfer is temporarily interrupted on an octet boundary, and the X_8 command byte is inserted. This condition is the only allowed interrupt in an otherwise contiguous transfer.

Below is an illustration of the cell structure and command byte usage:

{X_X} {53-byte ATM cell} {X_4} {53-byte ATM {X_8} cell}...

In the above example, the first ATM cell is preceded by the X_X start-of-cell command byte which resets both the transmitter-scrambler and receiver-descrambler pseudo-random nibble generators (PRNG) to their initial states. The following cell illustrates the insertion of a start-of-cell command without scrambler/descrambler reset. During this cell's transmission, an 8kHz timing sync pulse triggers insertion of the X_8 8kHz timing marker command byte.

Transmission Description

Refer to Figure 4. Cell transmission begins with the PHY-ATM Interface. An ATM layer device transfers a cell into the 77V1264L200 across the Utopia transmit bus or DPI transmit bus. This cell enters a 3-cell deep transmit FIFO. Once a complete cell is in the FIFO, transmission begins by passing the cell, four bits (MSB first) at a time to the 'Scrambler'.

The 'Scrambler' takes each nibble of data and exclusive-ORs them against the 4 high order bits (X(t), X(t-1), X(t-2), X(t-3)) of a 10 bit pseudo-random nibble generator (PRNG). Its function is to provide the appropriate frequency distribution for the signal across the line.

The PRNG is clocked every time a nibble is processed, regardless of whether the processed nibble is part of a data or command byte. Note however that only data nibbles are scrambled. The entire command byte (X _C) is NOT scrambled before it's encoded (see diagram for illustration). The PRNG is based upon the following polynomial:

$X^{10} + X^7 + 1$

With this polynomial, the four output data bits (D3, D2, D1, D0) will be generated from the following equations:

D3 = d3 xor X(t-3)

D2 = d2 xor X(t-2)

D1 = d1 xor X(t-1)

D0 = d0 xor X(t)

The following nibble is scrambled with X(t+4), X(t+3), X(t+2), and X(t+1).

A scrambler lock between the transmitter and receiver occurs each time an X_X command is sent. An X_X command is initiated only at the beginning of a cell transfer after the PRNG has cycled through all of its states (2^{10} - 1 = 1023 states). The first valid ATM data cell transmitted after power on will also be accompanied with an X_X command byte. Each time an X_X command byte is sent, the first nibble after the last escape (X) nibble is XOR'd with 1111b (PRNG = 3FFx).

Because a timing marker command (X_8) may occur at any time, the possibility of a reset PRNG start-of-cell command and a timing marker command occurring consecutively does exist (e.g. X_X_X_8). In this case, the detection of the last two consecutive escape (X) nibbles will cause the PRNG to reset to its initial 3FFx state. Therefore, the PRNG is clocked only after the first nibble of the second consecutive escape pair.

Once the data nibbles have been scrambled using the PRNG, the nibbles are further encoded using a 4b/5b process. The 4b/5b scheme ensures that an appropriate number of signal transitions occur on the line. A total of seventeen 5-bit symbols are used to represent the sixteen 4-bit data nibbles and the one escape (X) nibble. The table below lists the 4-bit data with their corresponding 5-bit symbols:

Data	Symbol
0000	10101
0100	00111
1000	10010
1100	10111

Data	Symbol
0001	01001
0101	01101
1001	11001
1101	11101

Data	Symbol
0010	01010
0110	01110
1010	11010
1110	11110

Data	Symbol
0011	01011
0111	01111
1011	11011
1111	11111

ESC(X) = 00010

3505 drw 05a

This encode/decode implementation has several very desirable properties. Among them is the fact that the output data bits can be represented by a set of relatively simple symbols;

- Run length is limited to <= 5;
- Disparity never exceeds +/- 1.

On the receiver, the decoder determines from the received symbols whether a timing marker command (X_8) or a start-of-cell command was sent (X_X or X_4). If a start-of-cell command is detected, the next 53 bytes received are decoded and forwarded to the descrambler. (See TC Receive Block Diagram, Figure 5).

The output of the 4b/5b encoder provides serial data to the NRZI encoder. The NRZI code transitions the wire voltage each time a '1' bit is sent. This, together with the previous encoding schemes guarantees that long run lengths of either '0' or '1's are prevented. Each symbol is shifted out with its most significant bit sent first.

When no cells are available to transmit, the 77V1264L200 keeps the line active by continuing to transmit valid symbols. But it does not transmit another start-of-cell command until it has another cell for transmission. The 77V1264L200 never generates idle cells.

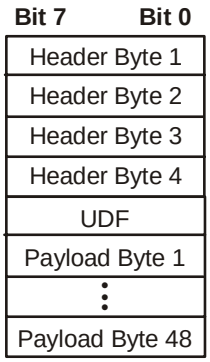
Transmit HEC Byte Calculation/Insertion

Byte #5 of each ATM cell, the HEC (Header Error Control) is calculated automatically across the first 4 bytes of the cell header, depending upon the setting of bit 5 of registers 0x03, 0x13, 0x23 and 0x33. This byte is then either inserted as a replacement of the fifth byte transferred to the PHY by the external system, or the cell is transmitted as received. A third operating mode provides for insertion of "Bad" HEC codes which may aid in communication diagnostics. These modes are controlled by the LED Driver and HEC Status/Control Registers.

Receiver Description

The receiver side of the TC sublayer operates like the transmitter, but in reverse. The data is NRZI decoded before each symbol is reassembled. The symbols are then sent to the 5b/4b decoder, followed by the Command Byte Interpreter, De-Scrambler, and finally through a FIFO to the UTOPIA or DPI interface to an ATM Layer device.

ATM Cell Format



3505 drw 52

UDF = User Defined Field (or HEC)

Note that although the IDT77V1264L200 can detect symbol and HEC errors, it does not attempt to correct them.

Upon reset or the re-connect, each port's receiver is typically not symbol-synchronized. When not symbol-synchronized, the receiver will indicate a significant number of bad symbols, and will deassert the Good Signal Bit as described below. Synchronization is established immediately once that port receives an Escape symbol, usually as part of the start-of-cell command byte preceding the first received cell.

The IDT77V1264L200 monitors line conditions and can provide an interrupt if the line is deemed 'bad'. The Interrupt Status Registers (registers 0x01, 0x11, 0x21 and 0x31) contain a Good Signal Bit (bit 6, set to 0 = Bad signal initially) which shows the status of the line per the following algorithm:

To declare 'Good Signal' (from "Bad" to "Good")

There is an up-down counter that counts from 7 to 0 and is initially set to 7. When the clock ticks for 1,024 cycles (32MHz clock, 1,024 cycles = 204.8 symbols) and no "bad symbol" has been received, the counter decreases by one. However, if at least one "bad symbol" is detected during these 1,024 clocks, the counter is increased by one, to a maximum of 7. The Good Signal Bit is set to 1 when this counter reaches 0. The Good Signal Bit could be set to 1 as quickly as 1,433 symbols (204.8 x 7) if no bad symbols have been received.

To declare 'Bad Signal' (from "Good" to "Bad")

The same up-down counter counts from 0 to 7 (being at 0 to provide a "Good" status). When the clock ticks for 1,024 cycles (32MHz clock, 1,024 cycles = 204.8 symbols) and there is at least one "bad symbol", the counter increases by one. If it detects all "good symbols" and no "bad symbols" in the next time period, the counter decreases by one. The "Bad Signal" is declared when the counter reaches 7. The Good Signal Bit could be set to 0 as quickly as 1,433 symbols (204.8 x 7) if at least one "bad symbol" is detected in each of seven consecutive groups of 204.8 symbols.

8kHz Timing Marker

The 8kHz timing marker, described earlier, is a completely optional feature which is essential for some applications requiring synchronization for voice or video, and unnecessary for other applications. Figure 7 shows the options available for generating and receiving the 8kHz timing marker.

The source of the marker is programmable in the $\overline{\text{RXREF}}$ and $\overline{\text{TXREF}}$ Control Register (0x40). Each port is individually programmable to either a local source or a looped remote source. The local source is $\overline{\text{TXREF}}$, which is an 8kHz clock of virtually any duty cycle. When unused, $\overline{\text{TXREF}}$ should be tied high. Also note that it is not limited to 8kHz, should a different frequency be desired. When looped, a received X_8 command byte causes one to be generated on the transmit side.

A received X_8 command byte causes the 77V1264L200 to issue a negative pulse on $\overline{\text{RXREF}}$. The source channel of the marker is programmable. When the clock multiplier in the Enhanced Control 2 register(s) is set to 2x or 4x, it is also necessary to set the $\overline{\text{RXREF}}$ Pulse Width Select in the LED Driver and HEC Status/Control register(s) to any value greater than the default for proper operation of $\overline{\text{RXREF}}$.

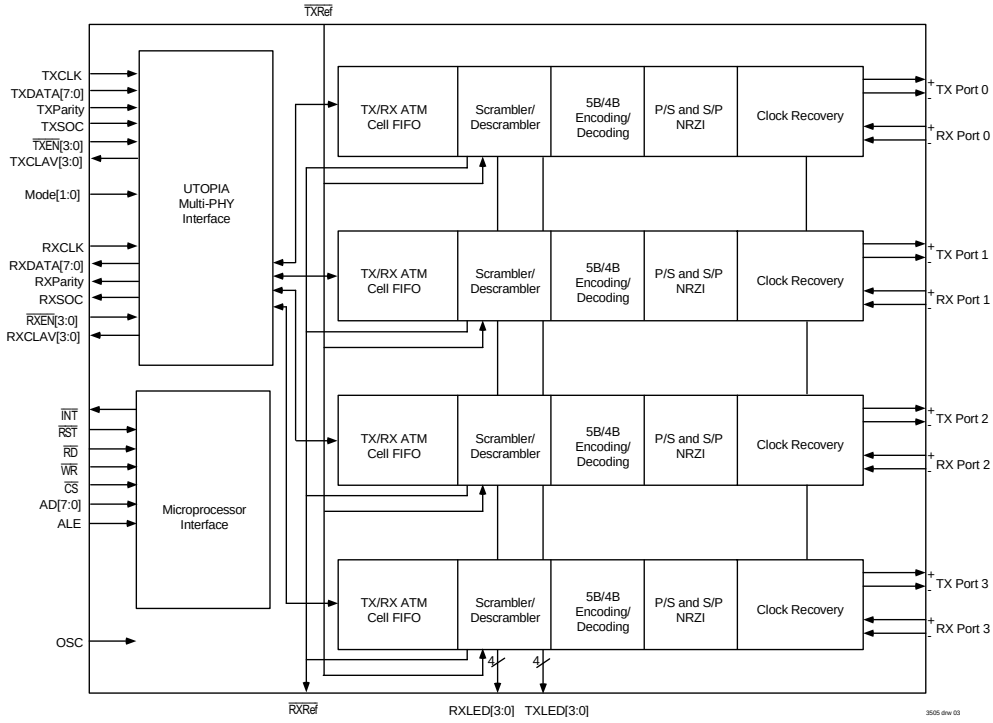


Figure 2 Block Diagram for Utopia Level 1 Configuration (MODE[1:0] = 01)

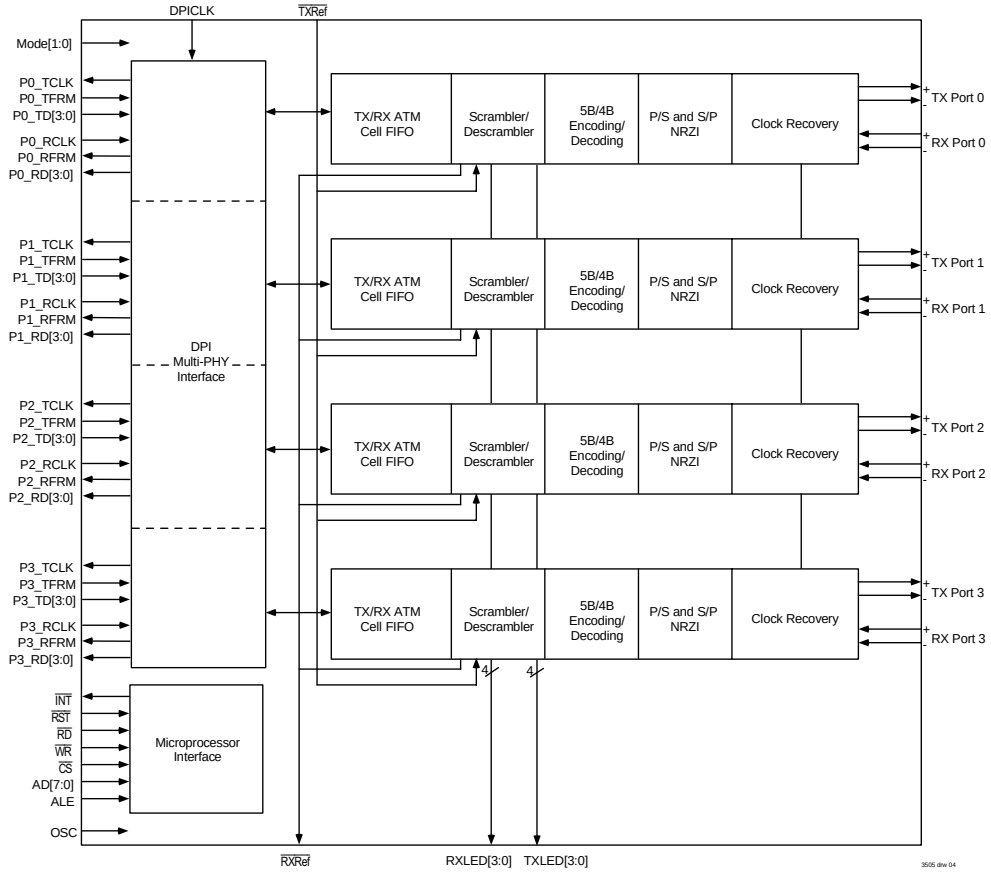


Figure 3 Block Diagram for DPI Configuration (MODE[1:0] = 10)

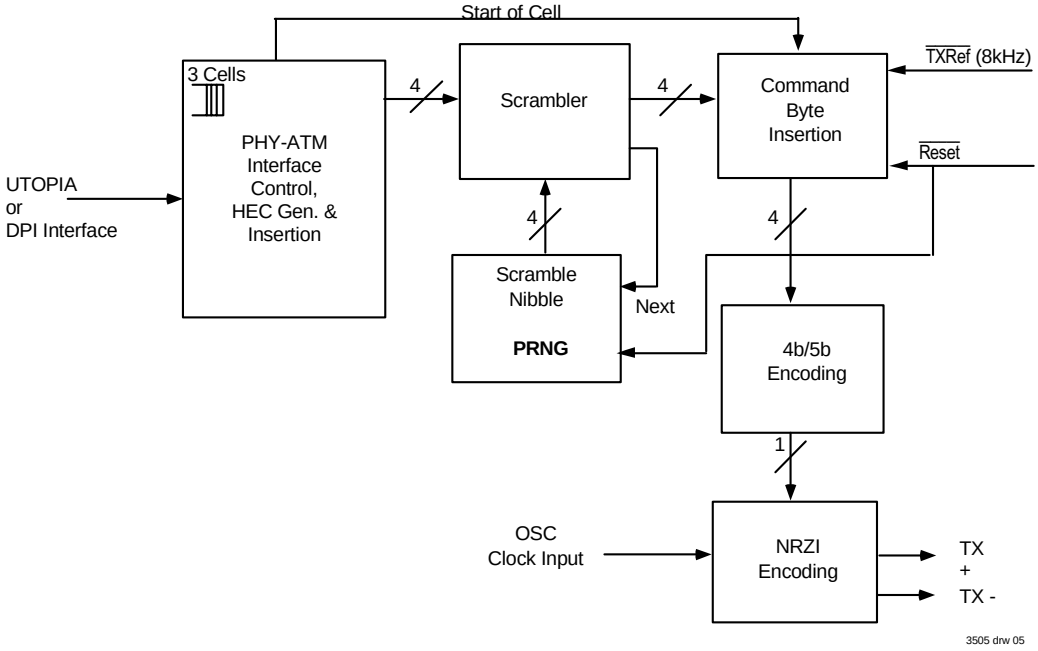


Figure 4 TC Transmit Block Diagram

PHY-ATM Interface

The 77V1264L200 PHY offers three choices in interfacing to ATM layer devices such as segmentation and reassembly (SAR) and switching chips. MODE[1:0] are used to select the configuration of this interface, as shown in the table below.

UTOPIA is a Physical Layer to ATM Layer interface standardized by the ATM Forum. It has separate transmit and receive channels and specific handshaking protocols. UTOPIA Level 2 has dedicated address signals for both the transmit and receive directions that allow the ATM layer device to specify with which of the four PHY channels it is communicating. UTOPIA Level 1 does not have address signals.

Instead, key handshaking signals are duplicated so that each channel has its own signals. In both versions of UTOPIA, all channels share a single transmit data bus and a single receive data bus for data transfer.

DPI is a low-pin count Physical Layer to ATM Layer interface. The low-pin count characteristic allows the 77V1264L200 to incorporate four separate DPI 4-bit ports, one for each of the four serial ports. As with the UTOPIA interfaces, the transmit and receive directions have their own data paths and handshaking.

UTOPIA Level 2 Interface Option

The 16-bit Utopia Level 2 interface operates as defined in ATM Forum document af-phy-0039. This PHY-ATM interface is selected by setting the MODE[1:0] pins both low.

This mode is configured as a single 16-bit data bus in the transmit (ATM-to-PHY) direction, and a single 16-bit data bus in the receive (PHY-to-ATM) direction. In addition to the data bus, each direction also includes a single optional parity bit, an address bus, and several handshaking signals. The UTOPIA address of each channel is determined by bits 4 to 0 in the Enhanced Control Registers. Please note that the transmit bus and the receive bus operate completely independently. The Utopia 2 signals are summarized below:

TXDATA[15:0]	ATM to PHY
TXPARITY	ATM to PHY
TXSOC	ATM to PHY
TXADDR[4:0]	ATM to PHY
$\overline{\text{TXEN}}$	ATM to PHY
TXCLAV	PHY to ATM
TXCLK	ATM to PHY
RXDATA[15:0]	PHY to ATM
RXPARITY	PHY to ATM
RXSOC	PHY to ATM
RXADDR[4:0]	ATM to PHY
$\overline{\text{RXEN}}$	ATM to PHY
RXCLAV	PHY to ATM
RXCLK	ATM to PHY

To determine if any of them has room to accept a cell for transmission (TXCLAV), or has a receive cell available to pass on to the ATM device (RXCLAV). To poll, the ATM device drives an address (TXADDR or RXADDR) then observes TXCLAV or RXCLAV on the next cycle of TXCLK or RXCLK. A port must tri-state TXCLAV and RXCLAV except when it is addressed.

If TXCLAV or RXCLAV is asserted, the ATM device may select that port, then transfer a cell to or from it. Selection of a port is performed by driving the address of the desired port while $\overline{\text{TXEN}}$ or $\overline{\text{RXEN}}$ is high, then driving $\overline{\text{TXEN}}$ or $\overline{\text{RXEN}}$ low. When $\overline{\text{TXEN}}$ is driven low, TXSOC (start of cell) is driven high to indicate that the first 16 bits of the cell are being driven on TXDATA. The ATM device may chose to temporarily suspend transfer of the cell by deasserting $\overline{\text{TXEN}}$. Otherwise, $\overline{\text{TXEN}}$ remains asserted as the next 16 bits are driven onto TXDATA with each cycle of TXCLK.

In the receive direction, the ATM device selects a port if it wished to receive the cell that the port is holding. It does this by asserting $\overline{\text{RXEN}}$. The PHY then transfers the data 16 bits each clock cycle, as determined by $\overline{\text{RXEN}}$. As in the transmit direction, the ATM device may suspend transfer by deasserting $\overline{\text{RXEN}}$ at any time. Note that the PHY asserts RXSOC coincident with the first 16 bits of each cell.

TXPARITY and RXPARITY are parity bits for the corresponding 16-bit data fields. Odd parity is used.

Figures 9 through 14 may be referenced for Utopia 2 bus examples.

Because this interface transfers an even number of bytes, rather than the ATM standard of 53 bytes, a filler byte is inserted between the 5-byte header and the 48-byte payload. This is shown in Figure 8.

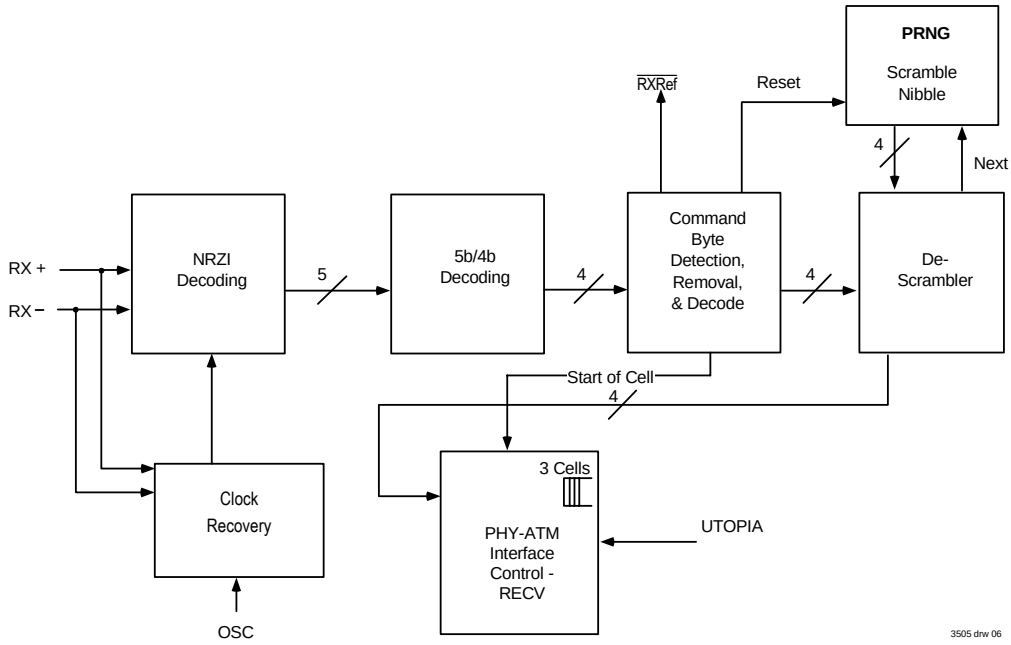


Figure 5 TC Receive Block Diagram

UTOPIA Level 1 Multi-phy Interface Option

The UTOPIA Level 1 MULTI-PHY interface is based on ATM Forum document af-phy-0017. Utopia Level 1 is essentially the same as Utopia Level 2, but without the addressing, polling and selection features.

	Bit 15	Bit 0
First	Header byte 1	Header byte 2
	Header byte 3	Header byte 4
	Header byte 5	stuff byte
	Payload byte 1	Payload byte 2
	Payload byte 3	Payload byte 4
	Payload byte 5	Payload byte 6
	~~	~~~
	Payload byte 45	Payload byte 46
Last	Payload byte 47	Payload byte 48

Figure 6 Utopia Level 2 Data Format and Sequence

Instead of addressing, this mode utilizes separate TXCLAV, $\overline{\text{TXEN}}$, RXCLAV and $\overline{\text{RXEN}}$ signals for each channel of the 77V1264L200. There are just one each of the TXSOC and RXSOC signals, which are shared across all four channels.

In addition to Utopia Level 2's cell mode transfer protocol, Utopia Level 1 also offers the option of a byte mode protocol. Bit 1 of the Master Control Registers is used to program whether the UTOPIA Level 1 bus is in cell mode or byte mode. In byte mode, the PHY is allowed to control data transfer on a byte-by-byte basis via the TXCLAV and RXCLAV signals. In cell mode, TXCLAV and RXCLAV are ignored once the transfer of a cell has begun. In every other way the two modes are identical. Cell mode is the default configuration and is the one described later.

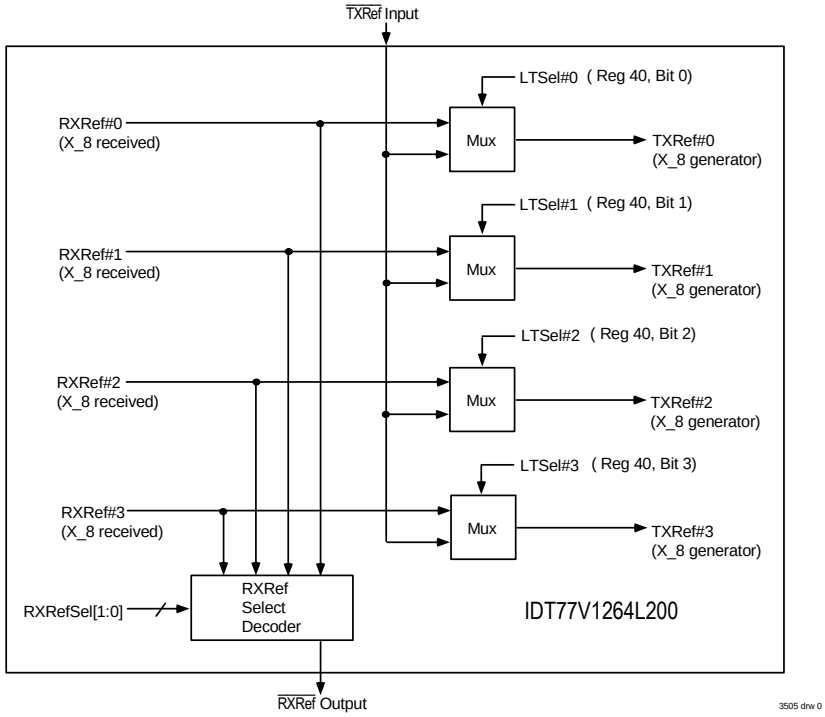


Figure 7 $\overline{\text{RXREF}}$ and $\overline{\text{TXREF}}$ Block Diagram

The Utopia 1 signals are summarized below:

TXDATA[7:0]	ATM to PHY
TXPARITY	ATM to PHY
TXSOC	ATM to PHY
$\overline{\text{TXEN}}$[3:0]	ATM to PHY
TXCLAV[3:0]	PHY to ATM
TXCLK	ATM to PHY
RXDATA[7:0]	PHY to ATM
RXPARITY	PHY to ATM
RXSOC	PHY to ATM
$\overline{\text{RXEN}}$[3:0]	ATM to PHY
RXCLAV[3:0]	PHY to ATM
RXCLK	ATM to PHY

Transmit and receive both utilize free running clocks, which are inputs to the 77V1264L200. All Utopia signals are timed to these clocks.

In the transmit direction, the PHY first asserts TXCLAV (transmit cell available) to indicate that it has room in its transmit FIFO to accept at least one 53-byte ATM cell. When the ATM layer device is ready to begin passing the cell, it asserts $\overline{\text{TXEN}}$ (transmit enable) and TXSOC (start of cell), coincident with the first byte of the cell on TXDATA. $\overline{\text{TXEN}}$ remains asserted for the duration of the cell transfer, but the ATM device may deassert $\overline{\text{TXEN}}$ at any time once the cell transfer has begun, but data is transferred only when $\overline{\text{TXEN}}$ is asserted.

In the receive direction, $\overline{\text{RXEN}}$ indicates when the ATM device is prepared to receive data. As with transmit, it may be asserted or deasserted at any time. Note, however, that not more than one $\overline{\text{RXEN}}$ should be asserted at a time. Also, once a given RX port is selected, that port's FIFO must be emptied of cells (as indicated by RXCLAV) before a different RX port may be enabled.

In both transmit and receive, TXSOC and RXSOC (start of cell) is asserted for one clock, coincident with the first byte of each cell. Odd parity is utilized across each 8-bit data field.

Figure 8 shows the data sequence for an ATM cell over Utopia Level 1, and Figures 15 through 21 are examples of the Utopia Level 1 handshake.

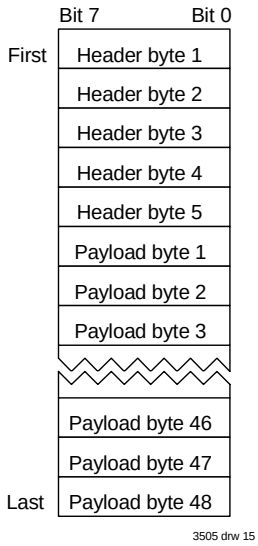


Figure 8 Utopia 1 Data Format and Sequence

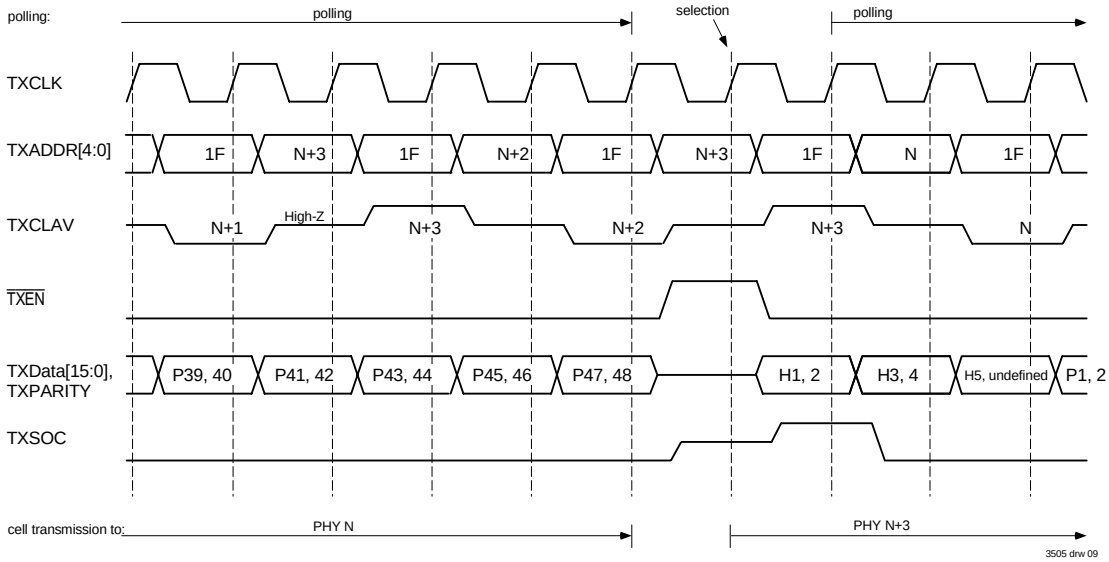


Figure 9 Utopia 2 Transmit Handshake - Back to Back Cells

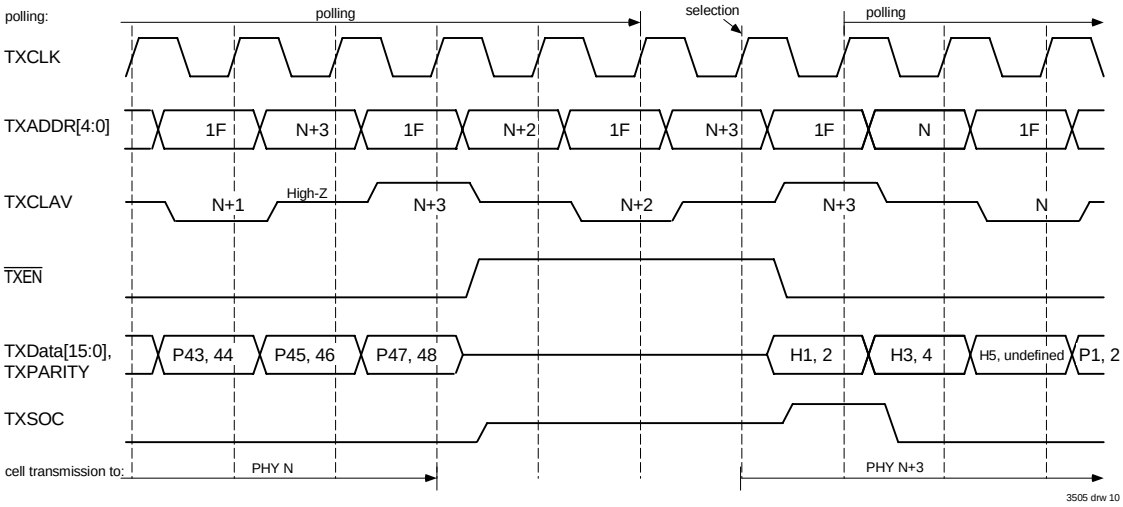


Figure 10 Utopia 2 Transmit Handshake - Delay Between Cells

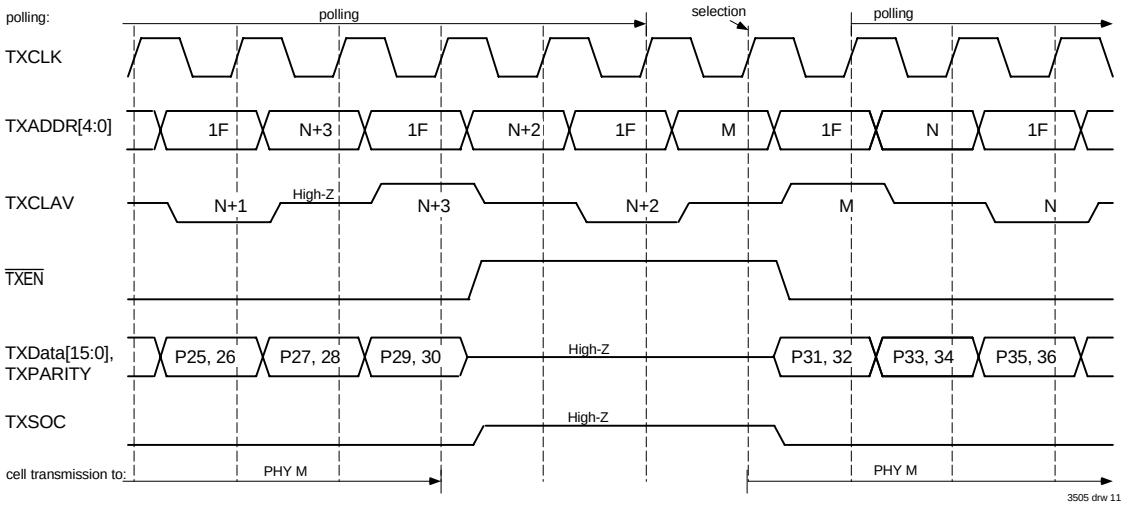


Figure 11 Utopia 2 Transmit Handshake - Transmission Suspended

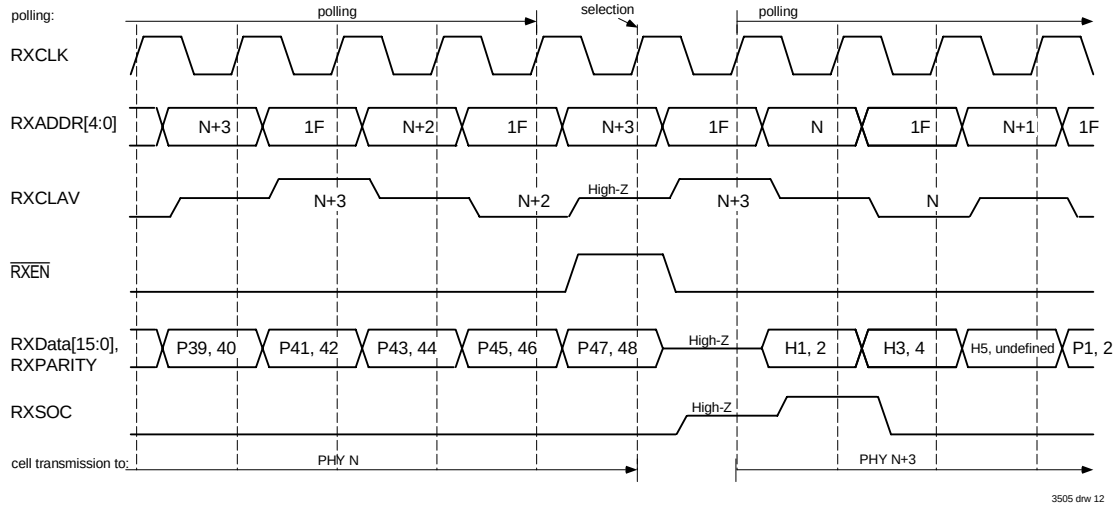


Figure 12 Utopia 2 Receive Handshake - Back to Back Cells

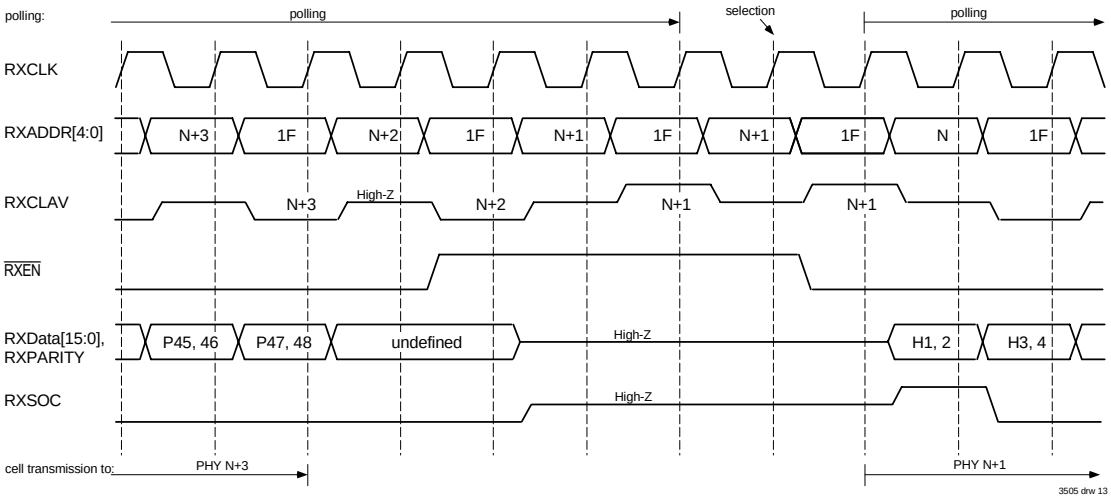


Figure 13 Utopia 2 Receive Handshake - Delay Between Cells

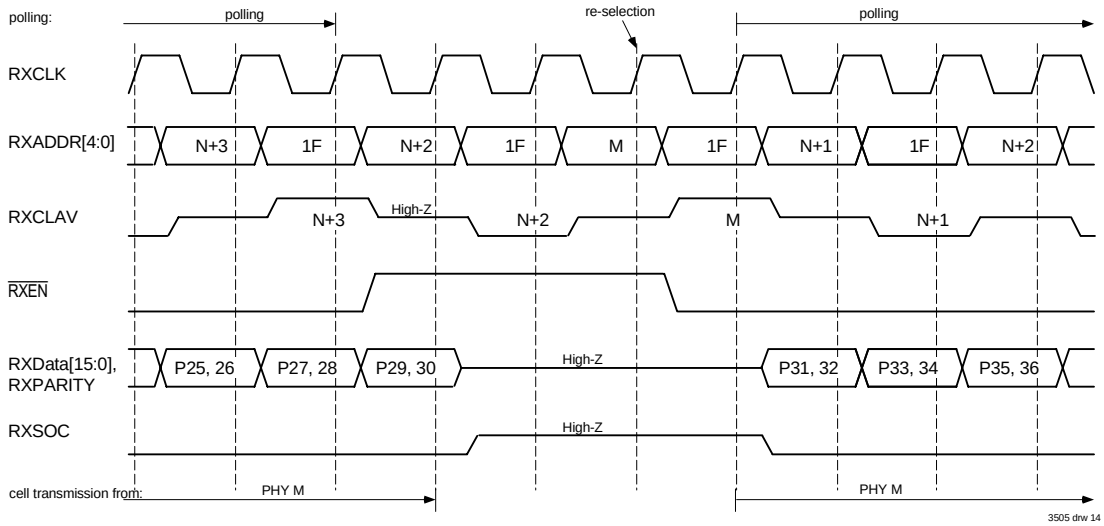


Figure 14 Utopia 2 Receive Handshake - Suspended Transfer of Data

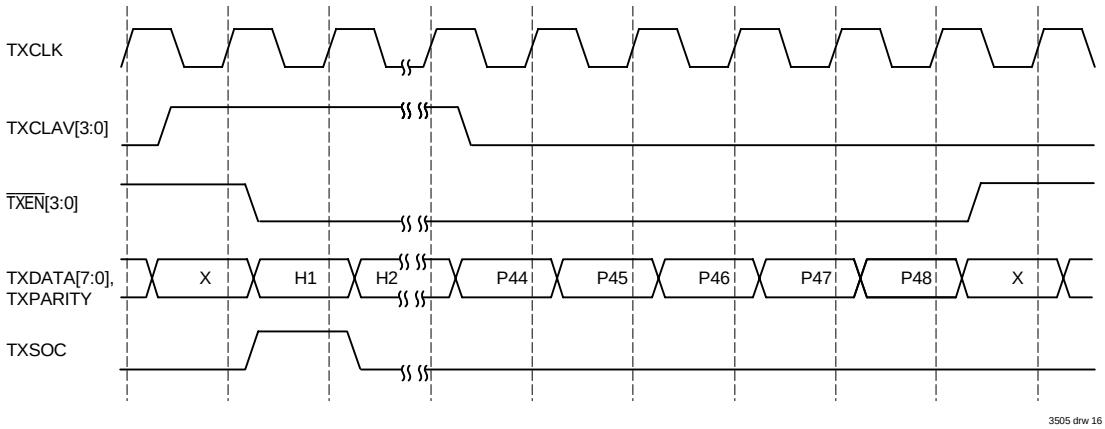


Figure 15 Utopia 1 Transmit Handshake - Single Cell

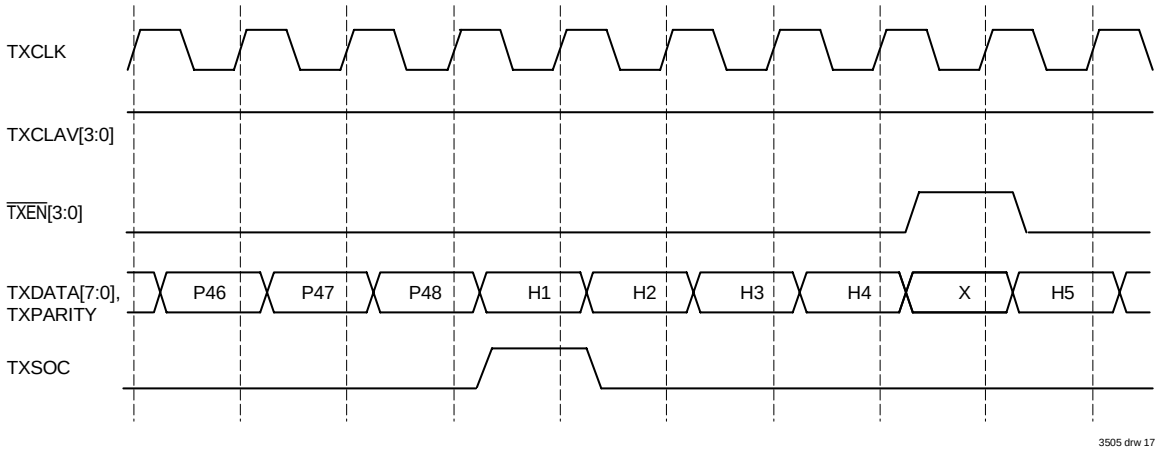


Figure 16 Utopia 1 Transmit Handshake - Back-to-Back Cells, and $\overline{\text{TXEN}}$ Suspended Transmission

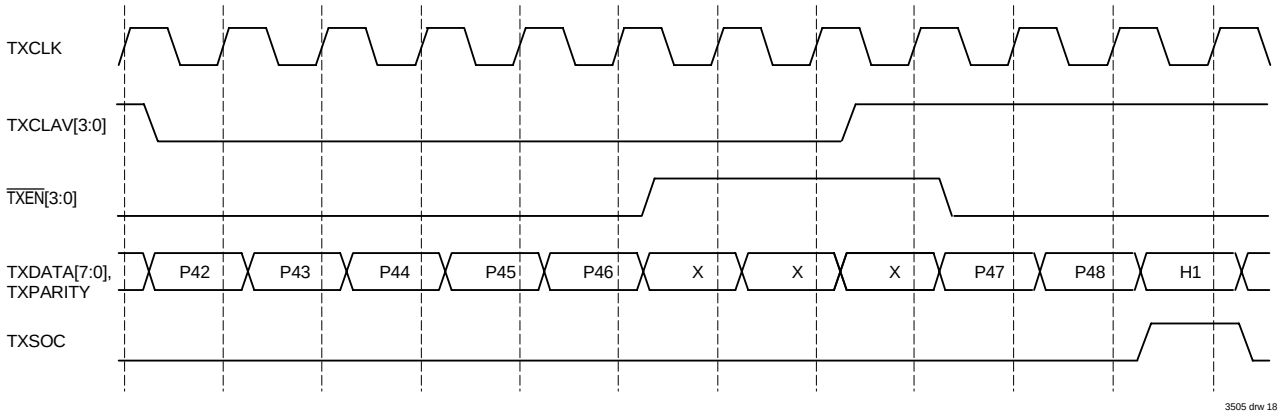


Figure 17 Utopia 1 Transmit Handshake - $\overline{\text{TXEN}}$ Suspended Transmission and Back-to-Back Cells (Byte Mode Only)

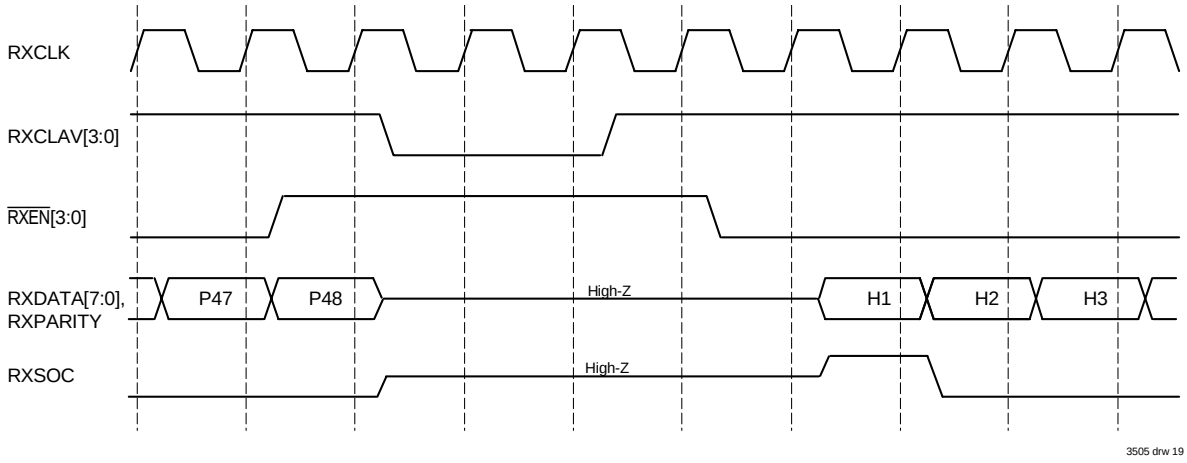


Figure 18 Utopia 1 Receive Handshake - Delay Between Cells

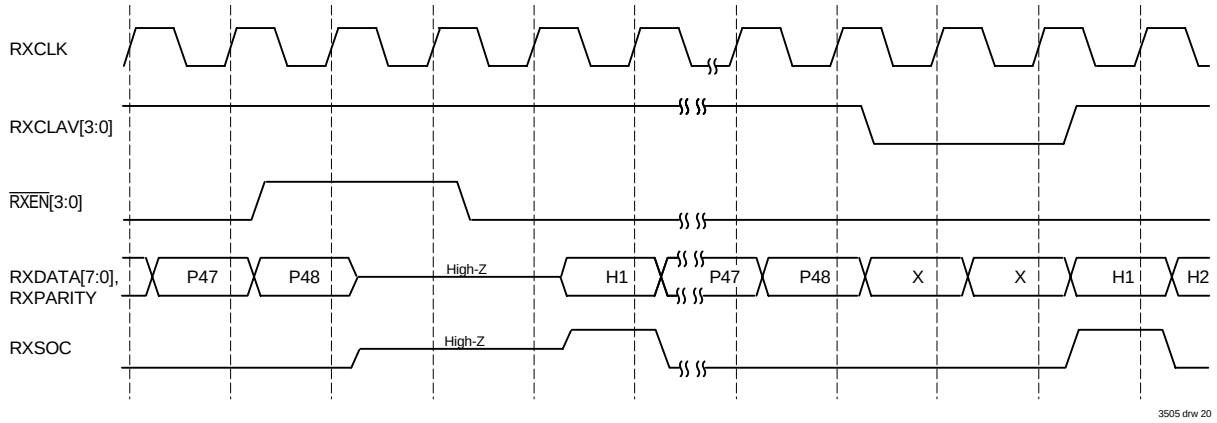


Figure 19 Utopia 1 Receive Handshake - $\overline{\text{RXEN}}$ and RXCLAV Control

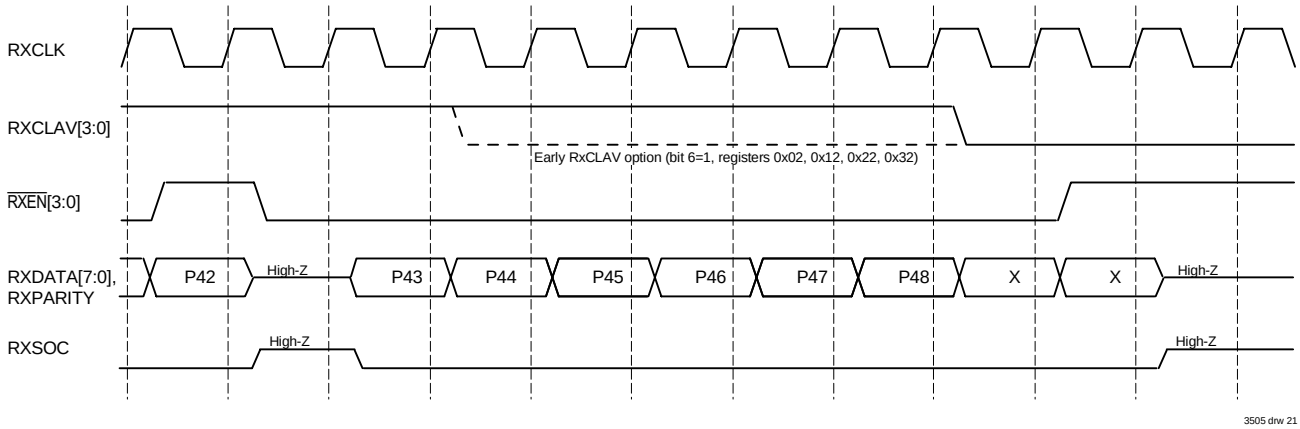


Figure 20 Utopia 1 Receive Handshake - RXCLAV Deassertion

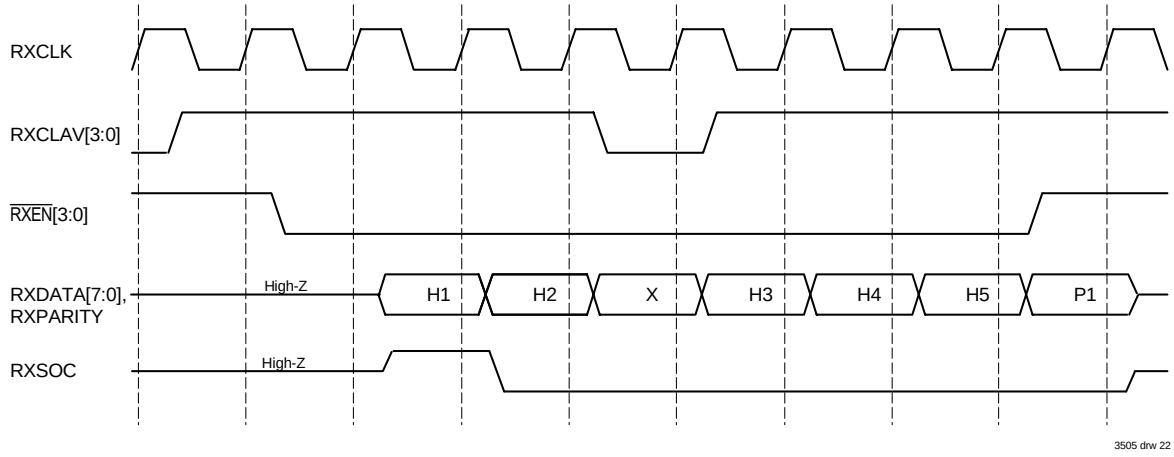


Figure 21 Utopia 1 Receive Handshake - RXCLAV Suspended Transfer (Byte Mode Only)

DPI Interface Option

The DPI interface is relatively new and worth additional description. The biggest difference between the DPI configurations and the UTOPIA configurations is that each channel has its own DPI interface. Each interface has a 4-bit data path, a clock and a start-of-cell signal, for both the transmit direction and the receive direction. Therefore, each signal is point-to-point, and none of these signals has high-Z capability. Additionally, there is one master DPI clock input (DPICLK) into the 77V1254L25 which is used as a source for the DPI transmit clock outputs. DPI is a cell-based transfer scheme like Utopia Level 2, whereas UTOPIA Level 1 transfers can be either byte- or cell-based.

Another unique aspect of DPI is that it is a symmetrical interface. It is as easy to connect two PHYs back-to-back as it is to connect a PHY to a switch fabric chip. In contrast, Utopia is asymmetrical. Note that for the 77V1254L25 the nomenclature "transmit" and "receive" is used in the naming of the DPI signals, whereas other devices may use more generic "in" and "out" nomenclature for their DPI signals.

The DPI signals are summarized below, where "Pn_" refers to the signals for channel number "n":

DPICLK	input to PHY
Pn_TCLK	PHY to ATM
Pn_TD[3:0]	ATM to PHY
Pn_TFRM	ATM to PHY
Pn_RCLK	ATM to PHY
Pn_RD[3:0]	PHY to ATM
Pn_RFRM	PHY to ATM

In the transmit direction (ATM to PHY), the ATM layer device asserts start-of-cell signal (Pn_TFRM) for one clock cycle, one clock prior to driving the first nibble of the cell on Pn_TD[3:0]. Once the ATM side has begun sending a cell, it is prepared to send the entire cell without interruption. The 77V1254L25 drives the transmit DPI clocks (Pn_TCLK) back to the ATM device, and can modulate (gap) it to control the flow of data. Specifically, if it cannot accept another nibble, the 77V1254L25 disables Pn_TCLK and does not generate another rising edge until it has room for the nibble. Pn_TCLK are derived from the DPICLK free running clock source.

The DPI protocol is exactly symmetrical in the receive direction, with the 77V1254L25 driving the data and start-of-cell signals while receiving Pn_RCLK as an input.

The DPI data interface is four bits, so the 53 bytes of an ATM cell are transferred in 106 cycles. Figure 22 shows the sequence of that data transfer. igures 23 through 31 show how the handshake operates.

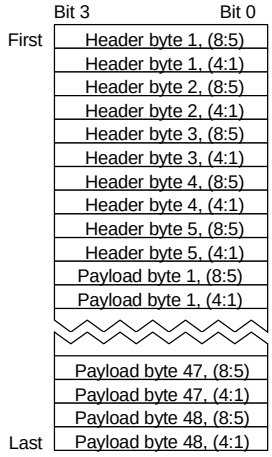


Figure 22 DPI Data Format and Sequence

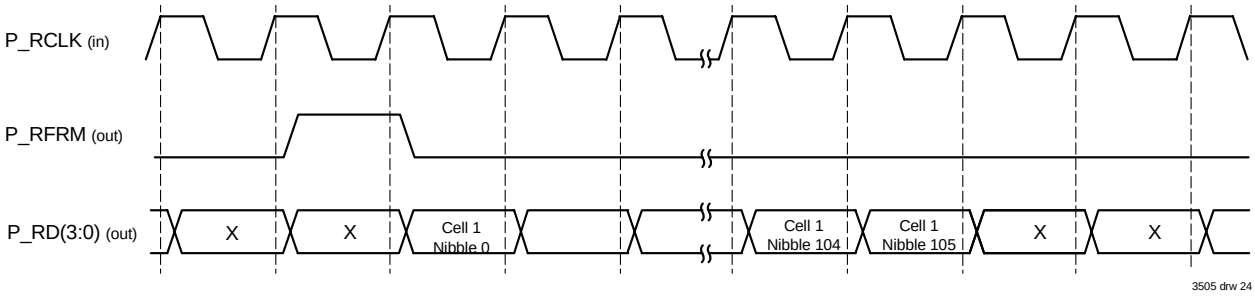


Figure 23 DPI Receive Handshake - One Cell Received

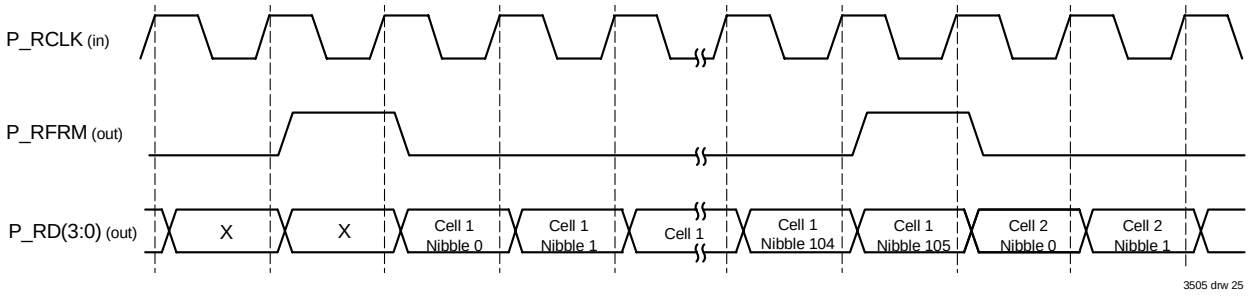


Figure 24 DPI Receive Handshake - Back-to-Back Cells

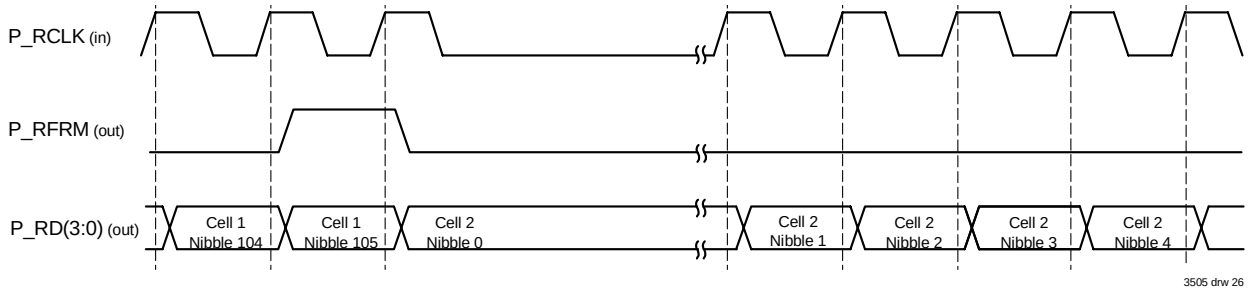


Figure 25 DPI Receive Handshake - ATM Layer Device Suspends Transfer

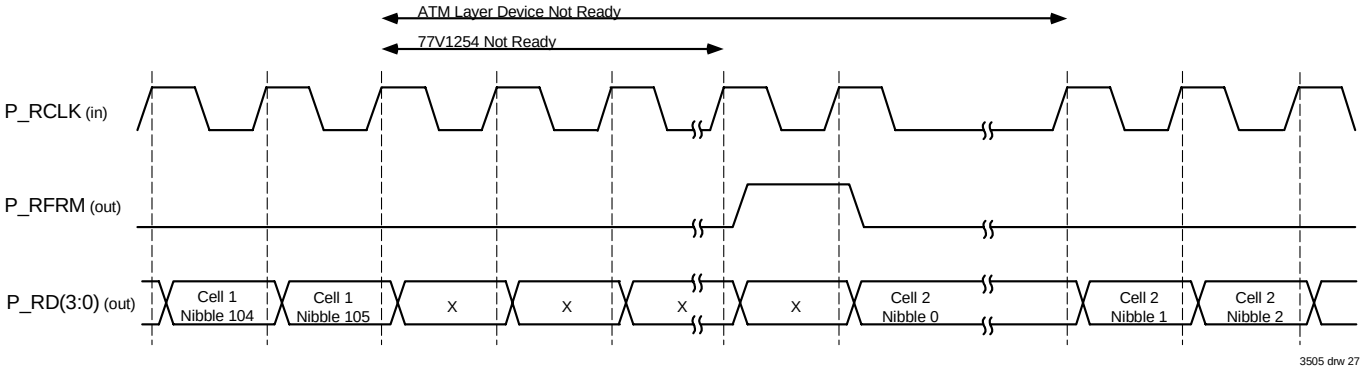


Figure 26 DPI Receive Handshake - Neither Device Ready

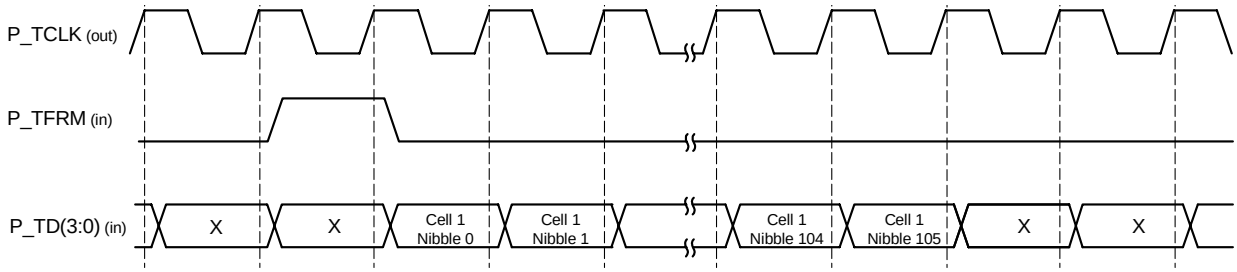


Figure 27 DPI Transmit Handshake - One Cell for Transmission

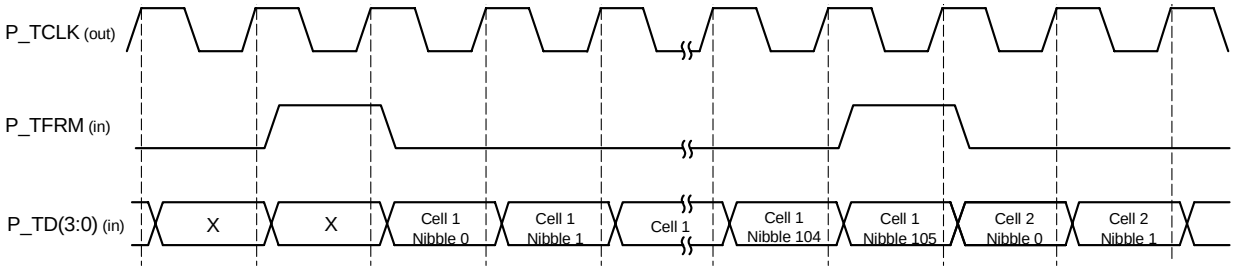


Figure 28 DPI Transmit Handshake - Back-to-Back Cells for Transmission

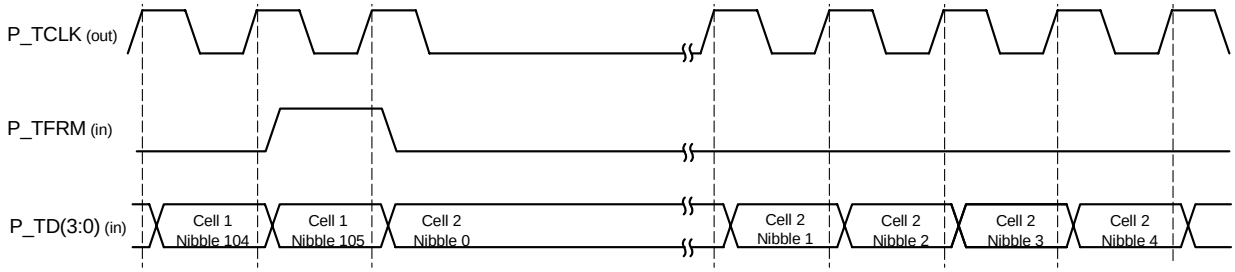


Figure 29 DPI Transmit Handshake - 77V1254L25 Transmit FIFO Full

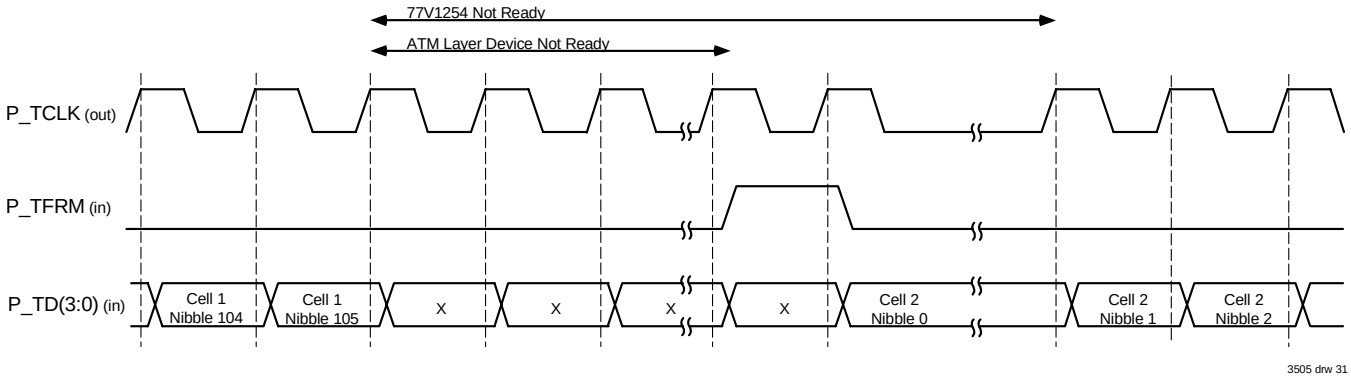


Figure 30 DPI Transmit Handshake - Neither Device Ready

Control and Status Interface

Utility Bus

The Utility Bus is a byte-wide interface that provides access to the registers within the IDT77V1264L200. These registers are used to select desired operating characteristics and functions, and to communicate status to external systems.

The Utility Bus is implemented using a multiplexed address and data bus (AD[7:0]) where the register address is latched via the Address Latch Enable (ALE) signal.

The Utility Bus interface is comprised of the following pins:

AD[7:0], ALE, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$

Read Operation

Refer to the Utility Bus timing waveforms in Figures 43 - 44. A register read is performed as follows:

1. Initial condition:
   - *$\overline{RD}$, $\overline{WR}$, $\overline{CS}$ not asserted (logic 1)*
   - *ALE not asserted (logic 0)*
2. Set up register address:
   - *place desired register address on AD[7:0]*
   - *set ALE to logic 1;*
   - *latch this address by setting ALE to logic 0.*
3. Read register data:
   - *Remove register address data from AD[7:0]*
   - *assert $\overline{CS}$ by setting to logic 0;*
   - *assert $\overline{RD}$ by setting to logic 0*
   - *wait minimum pulse width time (see AC specifications)*

Write Operation

A register write is performed as described below:

1. Initial condition:
   - *$\overline{RD}$, $\overline{WR}$, $\overline{CS}$ not asserted (logic 1)*
   - *ALE not asserted (logic 0)*
2. Set up register address:
   - *place desired register address on AD[7:0]*
   - *set ALE to logic 1;*
   - *latch this address by setting ALE to logic 0.*
3. Write data:
   - *place data on AD[7:0]*
   - *assert $\overline{CS}$ by setting to logic 0;*
   - *assert $\overline{WR}$ (logic 0) for minimum time (according to timing specification); reset $\overline{WR}$ to logic 1 to complete register write cycle.*

Interrupt Operations

The IDT77V1264L200 provides a variety of selectable interrupt and signalling conditions which are useful both during 'normal' operation, and as diagnostic aids. Refer to the Status and Control Register List section.

Overall interrupt control is provided via bit 0 of the Master Control Registers. When this bit is cleared (set to 0), interrupt signalling is prevented on the respective port. The Interrupt Mask Registers allow individual masking of different interrupt sources. Additional interrupt signal control is provided by bit 5 of the Master Control Registers. When this bit is set (=1), receive cell errors will be flagged via interrupt signalling and all other interrupt conditions are masked. These errors include:

- Bad receive HEC
- Short (fewer than 53 bytes) cells
- Received cell symbol error

Normal interrupt operations are performed by setting bit 0 and clearing bit 5 in the Master Control Registers. $\overline{INT}$ (pin 85) will go to a low state when an interrupt condition is detected. The external system should then interrogate the 77V1264L200 to determine which one (or more) conditions caused this flag, and reset the interrupt for further occurrences. This is accomplished by reading the Interrupt Status Registers. Decoding the bits in these bytes will tell which error condition caused the interrupt. Reading these registers also:

- clears the (sticky) interrupt status bits in the registers that are read
- resets $\overline{INT}$

This leaves the interrupt system ready to signal an alarm for further problems.

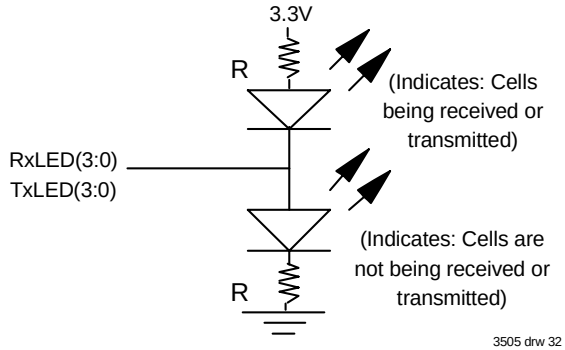
LED Control and Signalling

The LED outputs provide bi-directional LED drive capability of 8 mA. As an example, the RXLED outputs are described in the truth table:

State	Pin Voltage
Cells being received	Low
Cells not being received	High

As illustrated in the following drawing, this could be connected to provide for a two-LED condition indicator. These could also be different colors to provide simple status indication at a glance. (The minimum value for R should be 330Ω).

LED Indicator



TXLED Truth Table

State	Pin Voltage
Cells being transmitted	Low
Cells not being transmitted	High

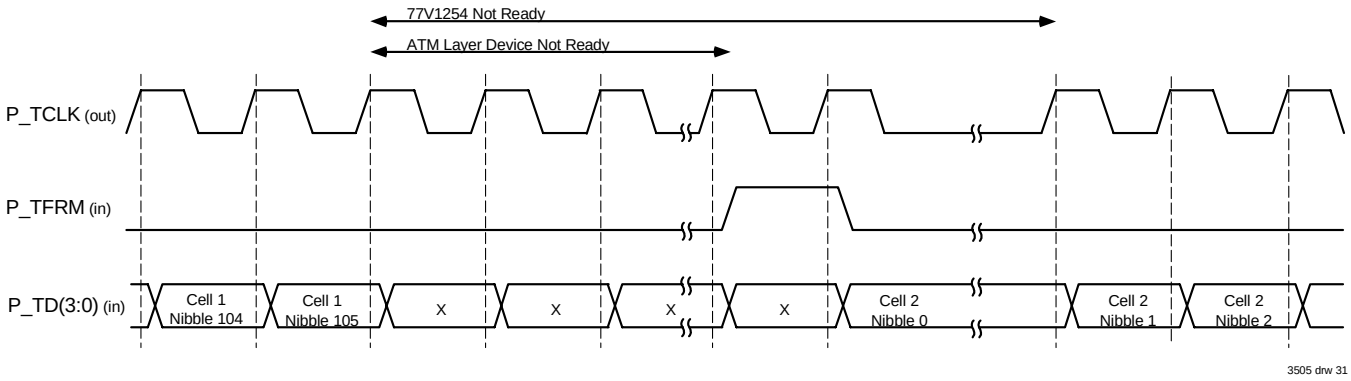


Figure 31 DPI Transmit Handshake - Neither Device Ready

Diagnostic Functions

Loopback

There are two loopback modes supported by the 77V1264L200. The loopback mode is controlled via bits 1 and 0 of the Diagnostic Control Registers:

Bit 1	Bit 0	Mode
0	0	Normal operating mode
1	0	PHY Loopback
1	1	Line Loopback

Normal Mode

This mode, Figure 32, supports normal operating conditions: data to be transmitted is transferred to the TC, where it is queued and formatted for transmission by the PMD. Receive data from the PMD is decoded along with its clock for transfer to the receiving "upstream system".

PHY Loopback

As Figure 33 illustrates below, this loopback mode provides a connection within the PHY from the transmit PHY-ATM interface to the PHY-ATM receive interface. Note that while this mode is operating, no data is forwarded to or received from the line interface. When Bits [1:0] in the Diagnostic Control Registers are set to 10, the PHY loopback mode works only if clock multiplier is 1x. For higher multiplies, these bits must be set to 01.

Line Loopback

Figure 34 might also be called “remote loopback” since it provides for a means to test the overall system, including the line. Since this mode will probably be entered under direction from another system (at a remote location), receive data is also decoded and transferred to the upstream system to allow it to listen for commands. A common example would be a command asking the upstream system to direct the TC to leave this loopback state, and resume normal operations.

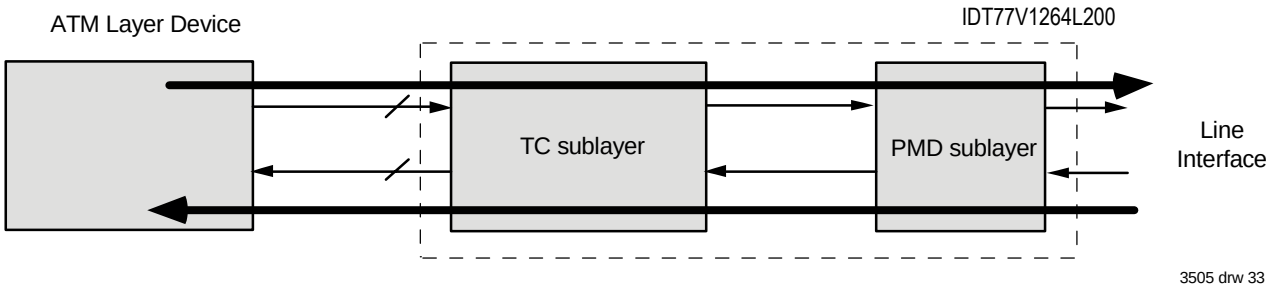


Figure 32 Normal Mode

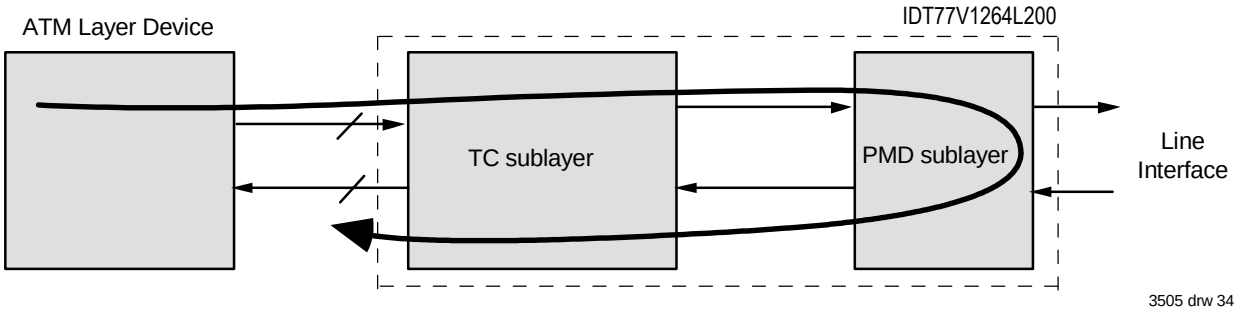


Figure 33 PHY Loopback

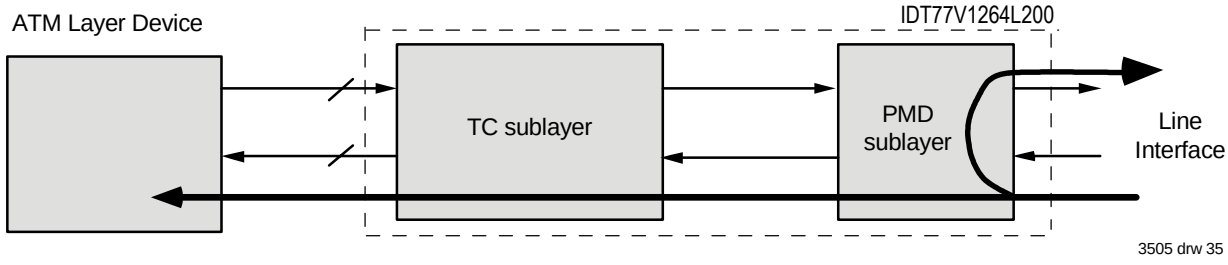


Figure 34 Line Loopback

Counters

Several condition counters are provided to assist external systems (e.g. software drivers) in evaluating communications conditions. It is anticipated that these counters will be polled from time to time (user selectable) to evaluate performance. A separate set of registers exists for each channel of the PHY.

- Symbol Error Counters
  - *8 bits*
  - *counts all invalid 5-bit symbols received*
- Transmit Cell Counters
  - *16 bits*
  - *counts all transmitted cells*
- Receive Cell Counters
  - *16 bits*
  - *counts all received cells, excluding idle cells and HEC errored cells*
- Receive HEC Error Counters
  - *5 bits*
  - *counts all HEC errors received*

The TXCell and RXCell counters are sized (16 bits) to provide a full cell count (without roll over) if the counter is read once/second. The Symbol Error counter and HEC Error counter were given sufficient size to indicate exact counts for low error-rate conditions. If these counters overflow, a gross condition is occurring, where additional counter resolution does not provide additional diagnostic benefit.

Reading Counters

1. Decide which counter value is desired. Write to the Counter Select Register(s) (0x06, 0x16, 0x26 and 0x36) to the bit location corresponding to the desired counter. This loads the High and Low Byte Counter Registers with the selected counter's value, and resets this counter to zero.

   Note: Only one counter may be enabled at any time in each of the Counter Select Registers.

2. Read the Counter Registers (0x04, 0x14, 0x24 or 0x34 (low byte)) and (0x05, 0x15, 0x25 or 0x35 (high byte)) to get the value.

Further reads may be accomplished in the same manner by writing to the Counter Select Registers.

Note: The PHY takes some time to set up the low and high byte counters after a specific counter has been selected in the Counter Selector register. This time delay (in µS) varies with the line rate and can be calculated as follows:

$$\text{Time delay (µS)} = \frac{12.5}{\text{line rate (Mbps)}}$$

Loop Timing Feature

The 77V1264L200 also offers a loop timing feature for specific applications where data needs to be repeated / transmitted using the recovered clock. If the loop timing mode is enabled in the Enhanced Control Register 1 bit 6, the recovered receive clock is used as to clock out data on transmit side. This mode is port specific, i.e., the user can select one or more ports to be in loop timing mode. In normal mode, the transmitter transmits data using the multiplied oscillator clock.

Jitter in Loop Timing Mode

One of the primary concerns when using loop timing mode is the amount of jitter that gets added each time data is transmitted. Table 4 shows the jitter measured at various data rates. The set-up shown in Figure 35 was used to perform these tests. The maximum jitter seen was at TX point 5 and the minimum jitter was at point 2. The loop timing jitter is defined as the amount of jitter generated by each TX node. In other words, the loop timing jitter or the jitter added by a loop-timed port in the set-up below is the difference between the Total Output Jitter and the Total Input Jitter.

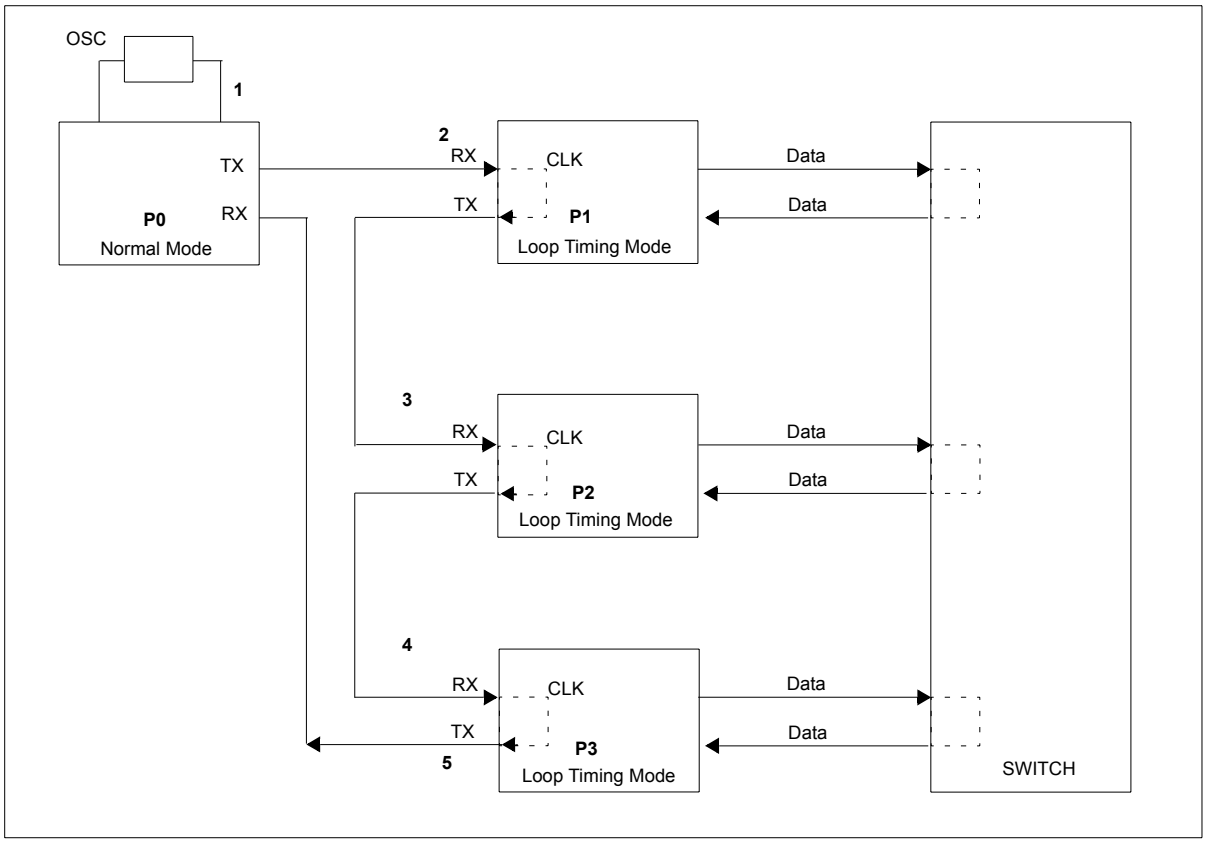


Figure 35 Test Setup for Loop Timing Jitter Measurements

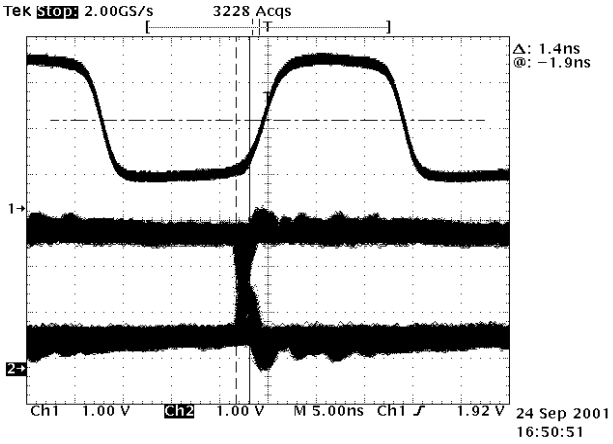
Loop Timing Jitter Specification

Line Rate Mbps	Data Rate Mbps	Min.	Typ.	Max.	Note
32	25.6	--	100 ps	--	Using 32Mhz OSC, multiplier at 1x
64	51.2	--	100 ps	--	Using 64Mhz OSC, multiplier at 1x
128	102.4	--	80 ps	--	Using 32Mhz OSC, multiplier at 4x
256	204.8	--	20 ps	--	Using 64Mhz OSC, multiplier at 4x

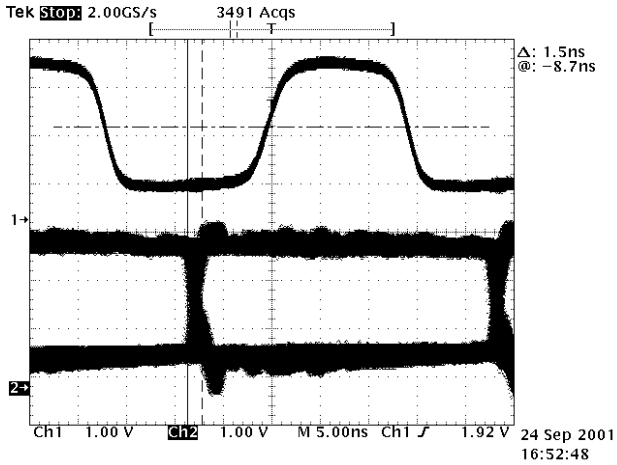
Table 4 Loop Timing Jitter

The waveforms below show some of the measurements taken with the set-up in Figure 35. Using the formula above, the jitter specification was derived. For example, at data rate of 25.6Mbps, jitter added going through Line Card 3 is 1.5ns -1.4ns (as shown in the waveforms below).

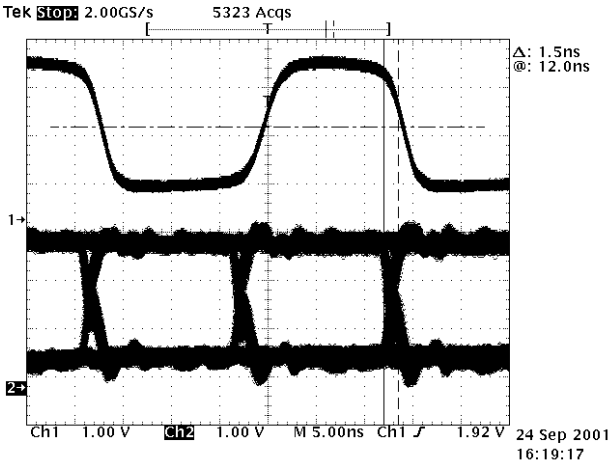
Jitter at 25.6Mbps at point 4 with respect to point 1



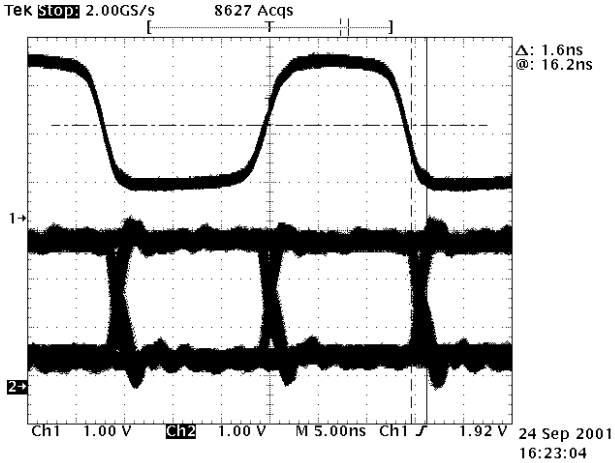
Jitter at 25.6Mbps at point 5 with respect to point 1



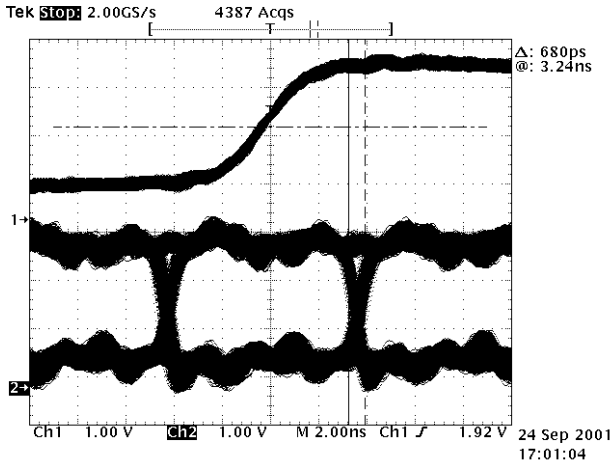
Jitter at 51.2Mbps at point 4 with respect to point 1



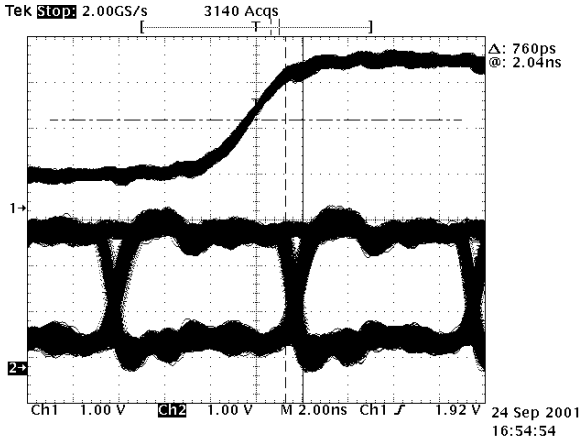
Jitter at 51.2Mbps at point 5 with respect to point 1



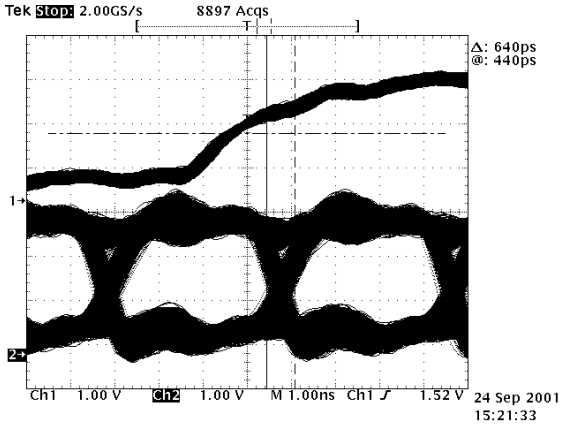
Jitter at 102.4Mbps at point 4 with respect to point 1



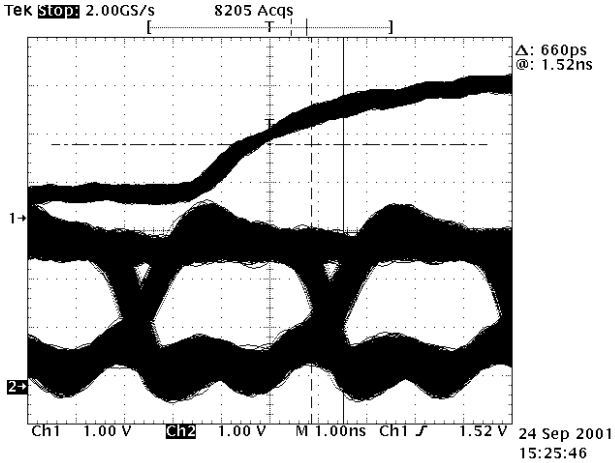
Jitter at 102.4Mbps at point 5 with respect to point 1



Jitter at 256Mbps at point 4 with respect to point 1



Jitter at 256Mbps at point 5 with respect to point 1



From the above measurements taken, the amount of jitter being added at each TX point is not significant. These tests were also run at line rates of 256Mbps for extended periods of time (64 hours) and no bit errors were seen.

VPI/VCI Swapping

For compatibility with IDT's SwitchStar products (77V400 and 77V500), the 77V1254L25 has the ability to swap parts of the VPI/VCI address space in the header of receive cells. This function is controlled by the VPI/VCI Swap bits, which are bit 5 of the Enhanced Control Registers (0x08, 0x18, 0x28 and 0x38). The portions of the VPI/VCI that are swapped are shown below. Bits X(7:0) are swapped with Y(7:0) when the VPI/VCI Swap bit is set and the chip is in DPI mode.

7							0	
GFC/VPI				VPI				Byte 0
VPI				VCI				Byte 1
VCI								Byte 2
VCI				PTI			CLP	Byte 3
HEC								Byte 4

7							0	
X7	X6	X5	X4	X3	X2	X1	X0	Byte 0
				Y7	Y6	Y5	Y4	Byte 1
Y3	Y2	Y1	Y0					Byte 2
								Byte 3
								Byte 4

Line Side (Serial) Interface

Each of the four ports has two pins for differential serial transmission, and two pins for differential serial receiving.

PHY to Magnetics Interface

A standard connection to 100Ω and 120Ω unshielded twisted pair cabling is shown in Figure 36. Note that the transmit signal is somewhat attenuated in order to meet the launch amplitude specified by the standards. The external receive circuitry is designed to attenuate low frequencies in order to compensate for the high frequency attenuation of the cable.

Also, the receive circuitry biases the positive and negative RX inputs to slightly different voltages. This is done so that the receiver does not receive false signals in the absence of a real signal. This can be important because the 77V1264L200 does not disable error detection or interrupts when an input signal is not present.

When connecting to UTP at 51.2Mbps and 204.8Mbps, it is necessary to use magnetics with sufficient bandwidth. Refer to Table 6 for the recommended magnetics.

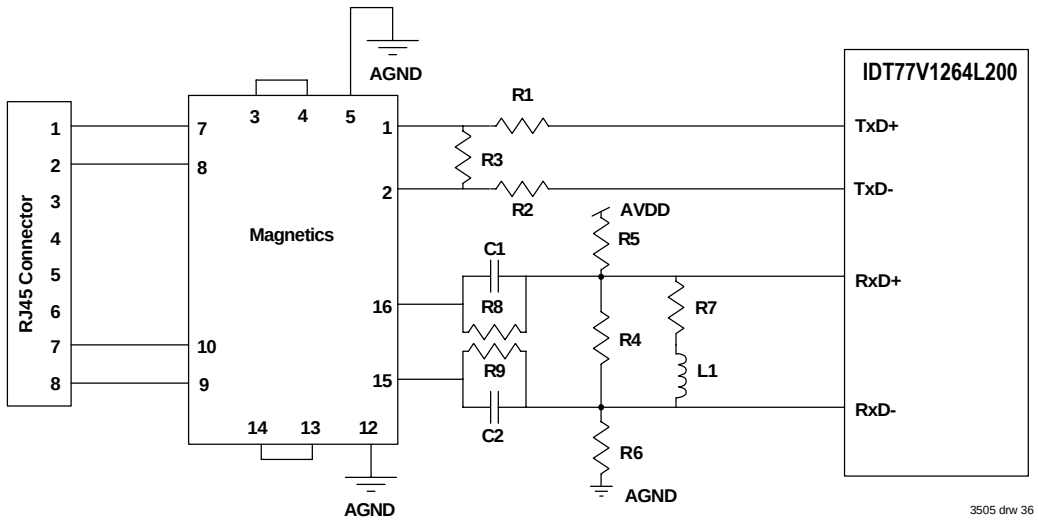


Figure 36 Recommended Connection to Magnetics

Component	Value	Tolerance
R1	47Ω	±5%
R2	47Ω	±5%
R3	620Ω	±5%
R4	110Ω	±5%
R5	2700Ω	±5%
R6	2700Ω	±5%
R7	82Ω	±5%
R8	33Ω	±5%
R9	33Ω	±5%

Table 5 Analog Component Values

Component	Value	Tolerance
C1	470pF	±20%
C2	470pF	±20%
L1	3.3μH	±20%

Table 5 Analog Component Values

Magnetics Modules for 25.6 Mbps	
Pulse PE-67583 or R4005	www.pulseeng.com
TDK TLA-6M103	www.component.tdk.com
Magnetics Module for 51.2 Mbps	
Pulse R4005	www.pulseeng.com
Magnetics Module for 204.8 Mbps	
Pulse ST6200T	www.pulseeng.com

Table 6 Magnetics Modules

Status and Control Register List

The 77V1264L200 has 41 registers that are accessible through the utility bus. Each of the four ports has 9 registers dedicated to that port. There is only one register (0x40) which is not port specific.

For those register bits which control operation of the Utopia interface, the operation of the Utopia interface is determined by the registers corresponding to the port which is selected at that particular time. For consistent operation, the Utopia control bits should be programmed the same for all four ports, except for the Utopia 2 port addresses in the Enhanced Control Registers.

Register Name	Register Address				
	Port 0	Port 1	Port 2	Port 3	All Ports
Master Control Registers	0x00	0x10	0x20	0x30	
Interrupt Status Registers	0x01	0x11	0x21	0x31	
Diagnostic Control Registers	0x02	0x12	0x22	0x32	
LED Driver and HEC Status/control	0x03	0x13	0x23	0x33	
Low Byte Counter Register [7:0]	0x04	0x14	0x24	0x34	
High Byte Counter Register [15:8]	0x05	0x15	0x25	0x35	
Counter Registers Read Select	0x06	0x16	0x26	0x36	
Interrupt Mask Registers	0x07	0x17	0x27	0x37	
Enhanced Control 1 Registers	0x08	0x18	0x28	0x38	
Enhanced Control 2 Registers	0x09	0x19	0x29	0x39	
$\overline{\text{RXREF}}$ and $\overline{\text{TXREF}}$ Control Register					0x40

Nomenclature

"Reserved" register bits, if written, should always be written "0"
R-only or W-only = register is read-only or write-only
"0" = 'cleared' or 'not set'
R/W = register may be read and written via the utility bus
sticky = register bit is cleared after the register containing it is read; all sticky bits are read-only
"1" = 'set'

Master Control Registers

Addresses: 0x00, 0x10, 0x20, 0x30

Bit	Type	Initial State	Function
7	R/W	0	**Reserved**
6	R/W	1 = discard errored cells	**Discard Receive Error Cells -** On receipt of any cell with an error (e.g. short cell, invalid command mnemonic, receive HEC error (if enabled), this cell will be discarded and will not enter the receive FIFO.
5	R/W	0 = all interrupts	**Enable Cell Error Interrupts Only -** If Bit 0 in this register is set (Interrupts Enabled), setting of this bit enables only "Received Cell Error" (as defined in bit 6) to trigger interrupt line.
4	R/W	0 = disabled	**Transmit Data Parity Check -** Directs TC to check parity of TXDATA against parity bit located in TXPARITY.
3	R/W	1 = discard idle cells	**Discard Received Idle Cells -** Directs TC to discard received idle (VPI/VCI = 0) cells from PMD without signalling external systems.
2	R/W	0 = not halted	**Halt Transmit -** Halts transmission of data from TC to PMD and forces the TXD outputs to the "0" state
1	R/W	0 = cell mode	**UTOPIA Level 1 mode select: -** 0 = cell mode, 1 = byte mode. Not applicable for Utopia 2 or DPI modes.
0	R/W	1 = enable interrupts	**Enable Interrupt Pin (Interrupt Mask Bit) -** Enables interrupt output pin (pin 85). If cleared, pin is always high and interrupt is masked. If set, an interrupt will be signaled by setting the interrupt pin to "0". It doesn't affect the Interrupt Status Registers.

Interrupt Status Registers

Addresses: 0x01, 0x11, 0x21, 0x31

Bit	Type	Initial State	Function
7		Reserved	
6	R	0 = Bad Signal	**Good Signal Bit -** See definition on page 14. 1 - Good Signal 0 - Bad Signal
5	sticky	0	**HEC error cell received -** Set when a HEC error is detected on received cell.
4	sticky	0	**"Short Cell" Received -** Interrupt signal which flags received cells with fewer than 53 bytes. This condition is detected when receiving Start-of-Cell command bytes with fewer than 53 bytes between them.
3	sticky	0	**Transmit Parity Error -** If Bit 4 of Register 0x00 / 0x10 / 0x20 / 0x30 is set (Transmit Data Parity Check), this interrupt flags a transmit data parity error condition. Odd parity is used.
2	sticky	0	**Receive Signal Condition change -** This interrupt is set when the received 'signal' changes either from 'bad to good' or from 'good to bad'.
1	sticky	0	**Received Symbol Error -** Set when an undefined 5-bit symbol is received.
0	sticky	0	**Receive FIFO Overflow -** Interrupt which indicates when the receive FIFO has filled and cannot accept additional data.

Diagnostic Control Registers

Addresses: 0x02, 0x12, 0x22, 0x32

Bit	Type	Initial State	Function
7	R/W	0 = normal	**Force TXCLAV deassert -** (applicable only in Utopia 1 and 2 modes) Used during line loopback mode to prevent upstream system from continuing to send data to the 77V1264L200. Not applicable in DPI mode.

Addresses: 0x02, 0x12, 0x22, 0x32

Bit	Type	Initial State	Function
6	R/W	0 = UTOPIA	**RXCLAV Operation Select -** (for Utopia 1 mode) The UTOPIA standard dictates that during cell mode operation, if the receive FIFO no longer has a complete cell available for transfer from PHY, RXCLAV is deasserted following transfer of the last byte out of the PHY to the upstream system. With this bit set, early deassertion of this signal will occur coincident with the end of Payload byte 44 (as in octet mode for TXCLAV). This provides early indication to the upstream system of this impending condition. 0 = "Standard UTOPIA RXCLAV' 1 = "Cell mode = Byte mode"
5	R/W	1 = tri-state	**Single/Multi-PHY configuration select -** (applicable and writable only in Utopia 1 mode) 0 = single: Never tri-state RXDATA, RXPARITY and RXSOC 1 = Multi-PHY mode: Tri-state RXDATA, RXPARITY and RXSOC when $\overline{\text{RXEN}}$ = 1
4	R/W	0 = normal	**RFLUSH = Clear Receive FIFO -** This signal is used to tell the TC to flush (clear) all data in the receive FIFO. The TC signals this completion by clearing this bit.
3	R/W	0 = normal	**Insert Transmit Payload Error -** Tells TC to insert cell payload errors in transmitted cells. This can be used to test error detection and recovery systems at destination station, or, under loopback control, at the local receiving station. This payload error is accomplished by flipping bit 0 of the last cell payload byte.
2	R/W	0 = normal	**Insert Transmit HEC Error -** Tells TC to insert HEC error in Byte 5 of cell. This can be used to test error detection and recovery systems in downstream switches, or, under loopback control, the local receiving station. The HEC error is accomplished by flipping bit 0 of the HEC byte.
1,0	R/W	00 = normal	**Loopback Control** **bit # 1 0** 0 0 Normal mode (receive from network) 1 0 PHY Loopback (with clock recovery)[1] 1 1 Line Loopback 0 1 PHY Loopback (with clock recovery)[1]

1. When Bits [1:0] in the Diagnostic Control Registers are set to 10, the PHY loopback mode works only if clock multiplier is 1x. For higher multiplies, these bits must be set to 01.

LED Driver and HEC Status/Control Registers

Addresses: 0x03, 0x13, 0x23, 0x33

Bit	Type	Initial State	Function
7		0	Reserved
6	R/W	0 = enable checking	**Disable Receive HEC Checking (HEC Enable) -** When not set, the HEC is calculated on first 4 bytes of received cell, and compared against the 5th byte. When set (= 1), the HEC byte is not checked.
5	R/W	0 = enable calculate & replace	**Disable Transmit HEC Calculate & Replace -** When set, the 5th header byte of cells queued for transmit is not replaced with the HEC calculated across the first four bytes of that cell.
4, 3	R/W	00 = 1 cycle	**$\overline{\text{RXREF}}$ Pulse Width Select -** See notes about 8KHz Timing Marker in the Functional Description Section. **bit # 4 3 .** 0 0 $\overline{\text{RXREF}}$ active for 1 OSC cycle 0 1 $\overline{\text{RXREF}}$ active for 2 OSC cycles 1 0 $\overline{\text{RXREF}}$ active for 4 OSC cycles 1 1 $\overline{\text{RXREF}}$ active for 8 OSC cycles
2	R	1 = empty	**FIFO Status** 1 = TxFIFO empty 0 = TxFIFO not empty
1	R	1	**TXLED Status** 0 = Cell Transmitted 1 = Cell Not Transmitted
0	R	1	**RXLED Status** 0 = Cell Received 1 = Cell Not Received

Low Byte Counter Registers [7:0]

Addresses: 0x04, 0x14, 0x24, 0x34

Bit	Type	Initial State	Function
[7:0]	R	0x00	Provides low byte of counter value selected via registers 0x06, 0x16, 0x26, and 0x36

High Byte Counter Registers [15:8]

Addresses: 0x05, 0x15, 0x25, 0x35

Bit	Type	Initial State	Function
[7:0]	R	0x00	Provides high-byte of counter value selected via registers 0x06, 0x16, 0x26, and 0x36

Counter Select Registers

Addresses: 0x06, 0x16, 0x26, 0x36

Bit	Type	Initial State	Function
7	—	—	Reserved.
6	—	—	Reserved.
5	—	—	Reserved.
4	—	—	Reserved.
3	W	0	Symbol Error Counter.
2	W	0	TXCell Counter.
1	W	0	RXCell Counter. Cells with HEC errors are never counted.
0	W	0	Receive HEC Error Counter.

Note: For proper operation, only one bit may be set in a Counter Select Register at any time.

Interrupt Mask Registers

Addresses: 0x07, 0x17, 0x27, 0x37

Bit	Type	Initial State	Function
7		0	Reserved.
6		0	Reserved.
5	R/W	0 = interrupt enabled	HEC Error Cell.
4	R/W	0 = interrupt enabled	Short Cell Error.
3	R/W	0 = interrupt enabled	Transmit Parity Error.
2	R/W	0 = interrupt enabled	Receive Signal Condition Change.
1	R/W	0 = interrupt enabled	Receive Cell Symbol Error.
0	R/W	0 = interrupt enabled	Receive FIFO Overflow.

Note: When set to "1", these bits mask the corresponding interrupts going to the interrupt pin ($\overline{INT}$). When set to "0", the interrupts are unmasked. These interrupts correspond to the interrupt status bits in the Interrupt Status Registers.

Enhanced Control 1 Registers

Addresses: 0x08, 0x18, 0x28, 0x38

Bit	Type	Initial State	Function
7	W	0 = not reset	**Individual Port Software Reset 1= Reset.** This bit is self-clearing; It isn't necessary to write "0" to exit reset. This bit does not clear the clock multiplier or Utopia Port Address bits.
6	R/W	0 = OSC	**Transmit Line Clock (or Loop Timing Mode).** When set to 0, the OSC input is used as the transmit line clock. When set to 1, the recovered receive clock is used as the transmit line clock.
5	R/W	0 = no swap	**VPI/VCI Swap** DPI mode only. Receive direction only. See description earlier.
4-0	R/W	Port 0 (Reg 0x08) 00000 Port 1 (Reg 0x18) 00001 Port 2 (Reg 0x28) 00010 Port 3 (Reg 0x38) 00011	**Utopia 2 Port Address** When operating in Utopia 2 Mode, these register bits determine the Utopia 2 port address

Enhanced Control 2 Registers

Addresses: 0x09, 0x19, 0x29, 0x39

Bit	Type	Initial State	Function
7-6	R/W	00	**Line Rate Control** These bits determine the line bit rate relative to the reference clock, as well as the pre-driver strength for the TXD+/- outputs. 00 Clock multiplier = 1x, pre-driver strength is "standard" 01 Clock multiplier = 2x, pre-driver strength is "standard" 10 Clock multiplier = 4x, pre-driver strength is "strong" 11 Reserved
5	R/W	0	Reserved
4	R/W	0	Reserved
3	R/W	0	Reserved
2	R/W	0 ——	Reserved
1	R/W	0	Reserved
0	R/W	0	Reserved

$\overline{\text{RXREF}}$ and $\overline{\text{TXREF}}$ Control Register

Addresses: 0x40

Bit	Type	Initial State	Function
7-6	R/W	0 = $\overline{\text{RXREF}}$0 (Port 0)	**$\overline{\text{RXREF}}$ Source Select** Selects which of the four ports (0-3) is the source of $\overline{\text{RXREF}}$.
5	W	0 = not reset	**Master Software Reset** 1 = Reset. This bit is self-clearing; it isn't necessary to write "0" to exit reset.
4		0	Reserved
3-0	R/W	0000 = not looped	**$\overline{\text{RXREF}}$ to $\overline{\text{TXREF}}$ Loop Select** When set to 0, $\overline{\text{TXREF}}$ is used to generate X_8 timing marker commands. When set to 1, $\overline{\text{TXREF}}$ input is ignored, and received X_8 timing commands are looped back and added to the transmit stream of that same port. It is recommended that the $\overline{\text{RXREF}}$ pulse width be set to 2x, 4x, and 8x or greater when the clock multiplier is set to 1x, 2x, or 4x respectively and bits 3-0 are set to 1. Refer to Figure 7. bit 3: port 3 bit 2: port 2 bit 1: port 1 bit 0: port 0

Absolute Maximum Ratings

Symbol	Rating	Value	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +5.5	V
TBIAS	Temperature Under Bias	-55 to +125	°C
TSTG	Storage Temperature	-55 to +120	°C
IOUT	DC Output Current	50	mA

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD	Digital Supply Voltage	3.13	3.3	3.47	V
GND	Digital Ground Voltage	0	0	0	V
VIH	Input High Voltage	2.0	____	5.25	V
VIL	Input Low Voltage	-0.3	____	0.8	V
AVDD	Analog Supply Voltage	3.13	3.3	3.47	V
AGND	Analog Ground Voltage	0	0	0	V
VDIF	VDD - AVDD	-0.5	0	0.5	V

Capacitance (TA = +25°C, F = 1MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	10	pF
C_{IO}[1]	I/O Capacitance	V_{OUT} = 0V	10	pF

1. Characterized values, not tested.

DC Electrical Characteristics (All Pins except TX+/- and RX+/-)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Leakage Current	Gnd ≤ VIN ≤ VDD	-5	5	µA
I_{LO}	/O (as input) Leakage Current	Gnd ≤ VIN ≤ VDD	-10	10	µA
V_{OH1}[1]	Output Logic "1" Voltage	I_{OH} = -2mA, VDD = min.	2.4	—	V
V_{OH2}[2]	Output Logic "1" Voltage	I_{OH} = -8mA, VDD = min.	2.4	—	V
V_{OL}[3]	Output Logic "0" Voltage	I_{OL} = -8mA, VDD = min.	—	0.4	V
I_{DD1}[4, 5]	Digital Power Supply Current - VDD	OSC = 32 MHz, all outputs unloaded	—	91	mA
		OSC = 64 MHz, all outputs unloaded	—	169	mA
		OSC = 256 MHz, all outputs unloaded	—	197	mA
I_{DD2}[5]	Analog Power Supply Current - AVDD	OSC = 32 MHz, all outputs unloaded	—	44	mA
		OSC = 64 MHz, all outputs unloaded	—	54	mA
		OSC = 256 MHz, all outputs unloaded	—	61	mA

1. For AD[7:0] pins only.
2. For all output pins except AD[7:0], $\overline{INT}$ and TX+/-.
3. For all output pins except TX+/-.
4. Add 15mA for each TX+/- pair that is driving a load.
5. Total supply current is the sum of IDD1 and IDD2

DC Electrical Characteristics (TX+/- Output Pins Only)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH1}	Output Logic High Voltage	I_{OH} = -20mA	VDD - 0.5V	—	V
V_{OL}	Output Logic Low Voltage	I_{OL} = -20mA	—	0.5	V

DC Electrical Characteristics (RXD+/- Input Pins Only)

Symbol	Parameter	Min.	Typ	Max.	Unit
V_{IR}	RXD+/- input voltage range	0	—	VDD	V
V_{IP}	RXD+/- input peak-to-peak differential voltage	0.6	—	2*VDD	V
V_{ICM}	RXD+/- input common mode voltage	1.0	VDD/2	VDD-0.5	V

UTOPIA Level 2 Bus Timing Parameters

Symbol	Parameter	Min.	Max.	Unit
t1	TXCLK Frequency	0.2	50	MHz
t2	TXCLK Duty Cycle (% of t1)	40	60	%
t3	TXDATA[15:0], TXPARITY Setup Time to TXCLK	4	—	ns
t4	TXDATA[15:0], TXPARITY Hold Time to TXCLK	1.5	—	ns
t5	TXADDR[4:0], Setup Time to TXCLK	4	—	ns
t6	TXADDR[4:0], Hold Time to TXCLK	1.5	—	ns
t7	TXSOC, $\overline{\text{TXEN}}$ Setup Time to TXCLK	4	—	ns
t8	TXSOC, $\overline{\text{TXEN}}$ Hold Time to TXCLK	1.5	—	ns
t9	TXCLK to TXCLAV High-Z	2	10	ns
t10	TXCLK to TXCLAV Low-Z (min) and Valid (max)	2	10	ns
t12	RXCLK Frequency	0.2	50	MHz
t13	RXCLK Duty Cycle (% of t12)	40	60	%
t14	$\overline{\text{RXEN}}$ Setup Time to RXCLK	4	—	ns
t15	RXCLK Hold Time to RXCLK	1.5	—	ns
t16	RXADDR[4:0] Setup Time to RXCLK	4	—	ns
t17	RXADDR[4:0] Hold Time to RXCLK	1.5	—	ns
t18	RXCLK to RXCLAV High-Z	2	10	ns
t19	RXCLK to RXCLAV Low-Z (min) and Valid (max)	2	10	ns
t20	RXCLK to RXSOC High-Z	2	10	ns
t21	RXCLK to RXSOC Low-Z (min) and Valid (max)	2	10	ns
t22	RXCLK to RXDATA, RXPARITY High-Z	2	10	ns
t23	RXCLK to RXDATA, RXPARITY Low-Z (min) and Valid (max)	2	10	ns

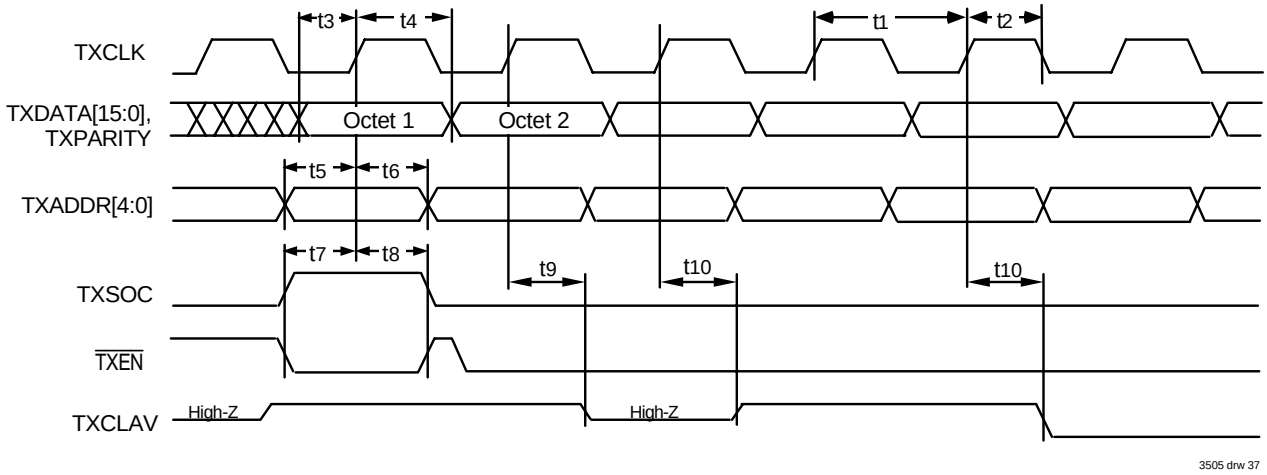


Figure 37 UTOPIA Level 2 Transmit

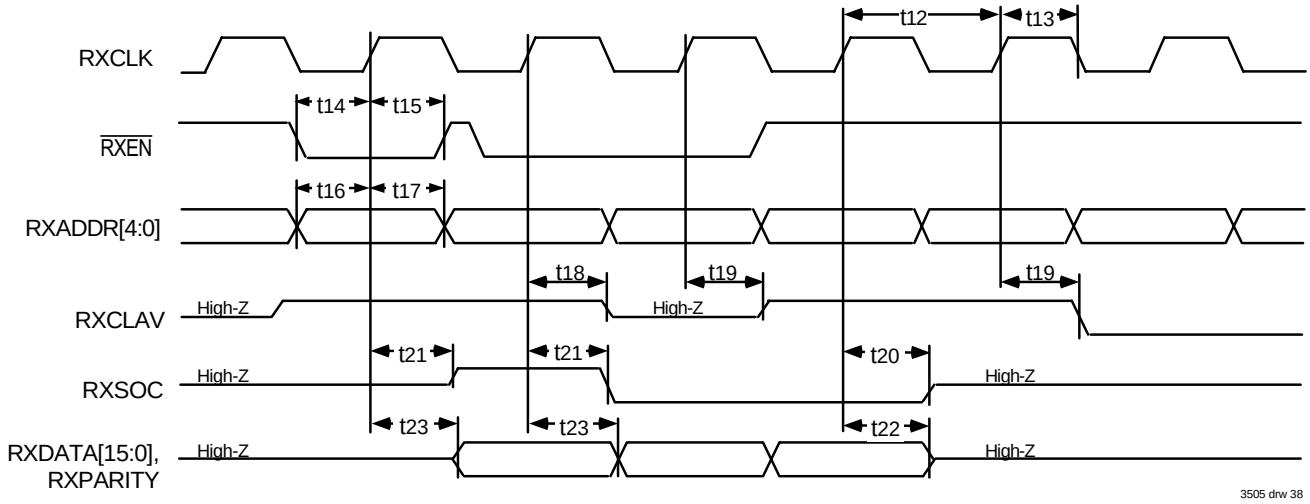


Figure 38 UTOPIA Level 2 Receive

UTOPIA Level 1 Bus Timing Parameters

Symbol	Parameter	Min.	Max.	Unit
t31	TXCLK Frequency	0.2	50	MHz
t32	TXCLK Duty Cycle (% of t31)	40	60	%
t33	TXDATA[7:0], TXPARITY Setup Time to TXCLK	4	—	ns
t34	TXDATA[7:0], TXPARITY Hold Time to TXCLK	1.5	—	ns
t35	TXSOC, $\overline{\text{TXEN}}$[3:0] Setup Time to TXCLK	4	—	ns
t36	TXSOC, $\overline{\text{TXEN}}$[3:0] Hold Time to TXCLK	1.5	—	ns
t37	TXCLK to TXCLAV[3:0] Invalid (min) and Valid (max)	2	10	ns
t39	RXCLK Frequency	0.2	50	MHz
t40	RXCLK Duty Cycle (% of t39)	40	60	%
t41	$\overline{\text{RXEN}}$[3:0] Setup Time to RXCLK	4	—	ns
t42	$\overline{\text{RXEN}}$[3:0] Hold Time to RXCLK	1.5	—	ns
t43	RXCLK to RXCLAV[3:0] Invalid (min) and Valid (max)	2	10	ns
t44	RXCLK to RXSOC High-Z	2	10	ns
t45	RXCLK to RXSOC Low-Z (min) and Valid (max)	2	10	ns
t46	RXCLK to RXDATA, RXPARITY High-Z	2	10	ns
t47	RXCLK to RXDATA, RXPARITY Low-Z (min) and Valid (max)	2	10	ns

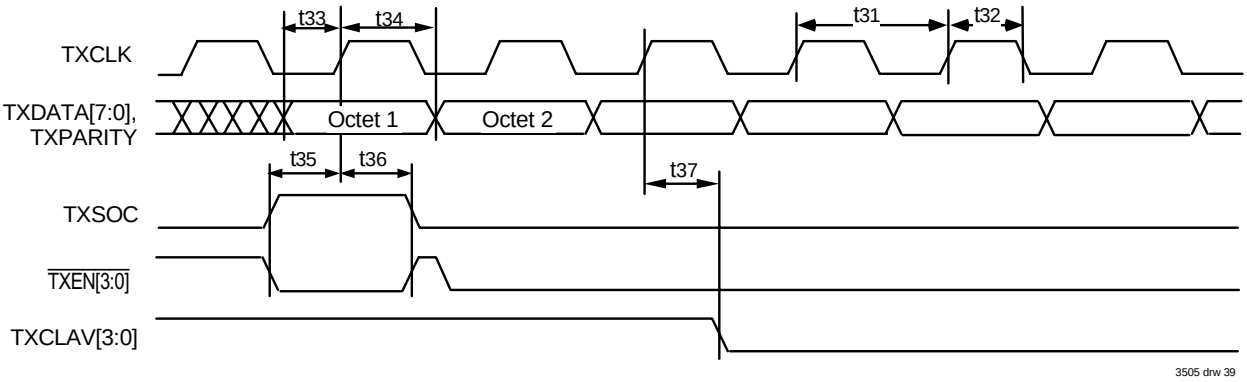


Figure 39 UTOPIA Level 1 Transmit

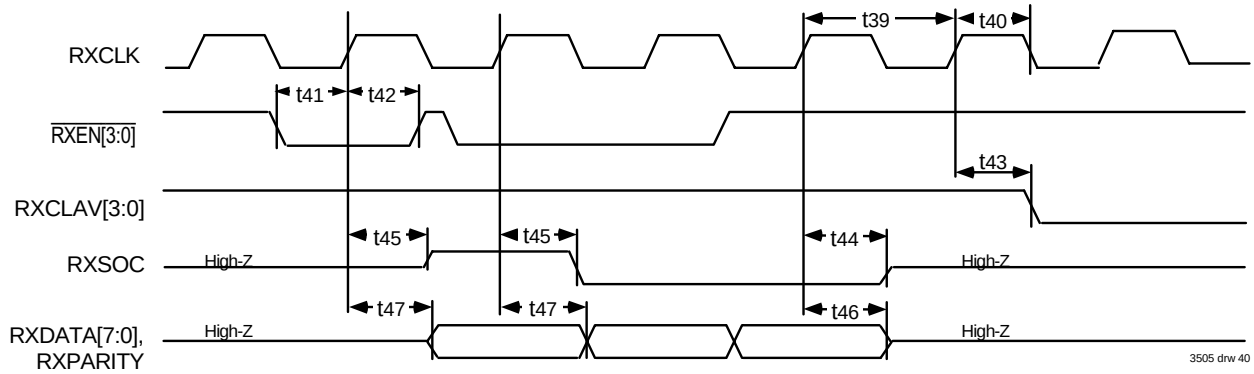


Figure 40 UTOPIA Level 1 Receive

DPI Bus Timing Parameters

Symbol	Parameter	Min.	Max.	Unit
t51	DPICLK Frequency	0.2	50	MHz
t52	DPICLK Duty Cycle (% of t51)	40	60	%
t53	DPICLK to Pn_TCLK Propagation Delay	2	14	ns
t54	Pn_TFRM Setup Time to Pn_TCLK	4	—	ns
t55	Pn_TFRM Hold Time to Pn_TCLK	1	—	ns
t56	Pn_TD[3:0] Setup Time to Pn_TCLK	4	—	ns
t57	Pn_TD[3:0] Hold Time to Pn_TCLK	1	—	ns
t61	Pn_RCLK Period	25	—	ns
t62	Pn_RCLK High Time	10	—	ns
t63	Pn_RCLK Low Time	10	—	ns
t64	Pn_RCLK to Pn_TFRM Invalid (min) and Valid (max)	2	12	ns
t65	Pn_RCLK to Pn_RD Invalid (min) and Valid (max)	2	12	ns

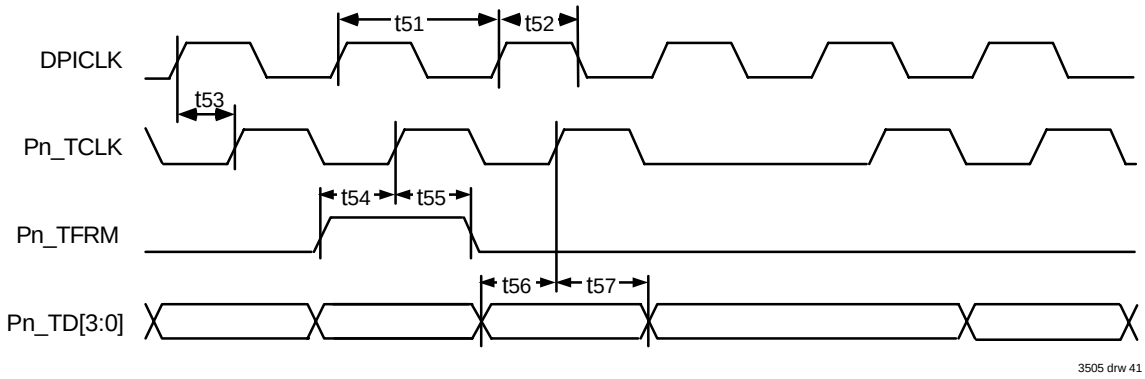


Figure 41 DPI Transmit

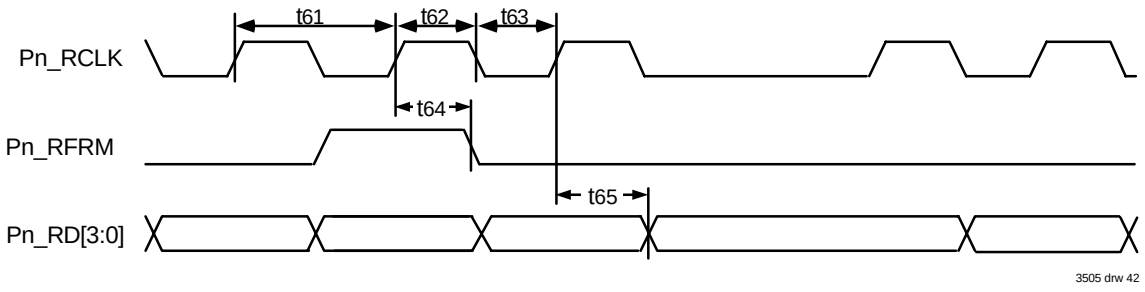


Figure 42 DPI Receive

Utility Bus Read Cycle

Name	Min.	Max.	Unit	Description
Tas	10	—	MHz	Address setup to ALE
Tcsrd	0	—	%	Chip select to read enable
Tah	5	—	ns	Address hold to ALE
Tapw	10	—	ns	ALE min pulse width
Ttria	0	—	ns	Address tri-state to $\overline{RD}$ assert
Trdpw	20	—	ns	Min. $\overline{RD}$ pulse width
Tdh	0	—	ns	Data Valid hold time
Tch	0	—	ns	$\overline{RD}$ deassert to $\overline{CS}$ deassert
Ttrid	—	10	ns	$\overline{RD}$ deassert to data tri-state
Trd	—	18	ns	Read Data access
Tar	5	—	ns	ALE low to start of read
Trdd	0	—	ns	Start of read to Data low-Z

Utility Bus Write Cycle

Name	Min.	Max.	Unit	Description
Tapw	10	—	ns	ALE min pulse width
Tas	10	—	ns	Address set up to ALE
Tah	5	—	ns	Address hold time to ALE
Tcswr	0	—	ns	$\overline{CS}$ Assert to $\overline{WR}$
Twrpw	20	—	ns	Min. $\overline{WR}$ pulse width
Tdws	20	—	ns	Write Data set up
Tdwh	10	—	ns	Write Data hold time
Tch	0	—	ns	$\overline{WR}$ deassert to $\overline{CS}$ deassert
Taw	20	—	ns	ALE low to end of write

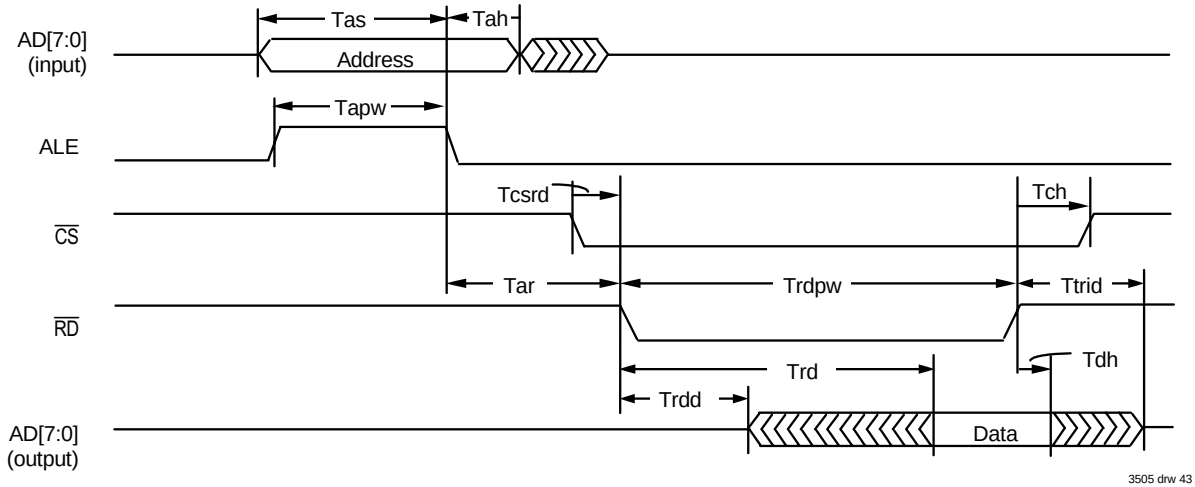


Figure 43 Utility Bus Read Cycle

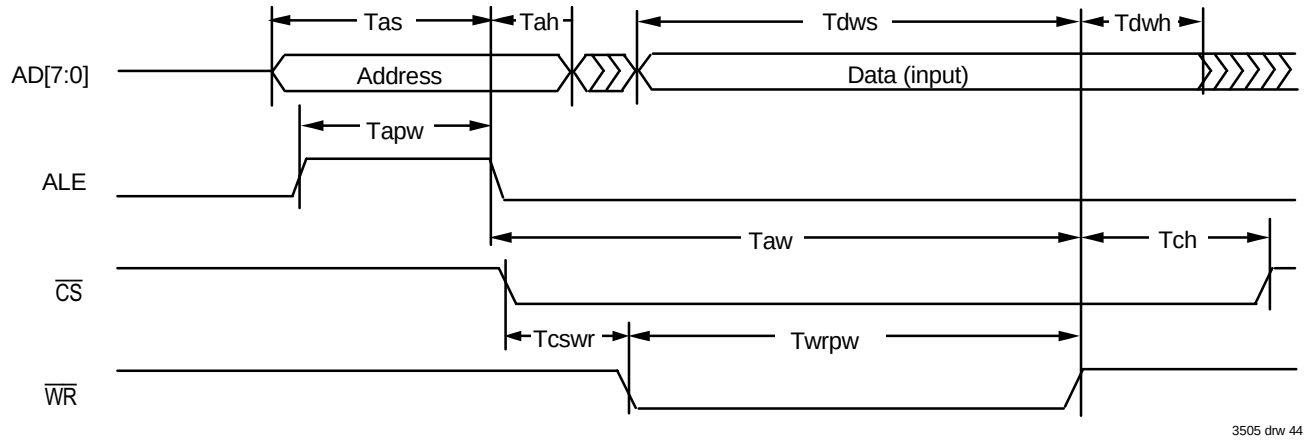


Figure 44 Utility Bus Write Cycle

OSC, RXREF, TXREF and Reset Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
Tcyc	OSC cycle period	30 15	31.25 15.625	33 16.5	ns ns
Tch	OSC high tim	40	—	60	%
Tcl	OSC low time	40	—	60	%
Tcc	OSC cycle to cycle period variation	—	—	1	%
Trrpd[1]	OSC to RXREF Propagation Delay	1	—	30	ns
Ttrh	TXREF High Time	35	—	—	ns
Ttrl	TXREF Low Time	35	—	—	ns
Trspw	Minimum RST Pulse Width	two OSC cycles	—	—	—

1. The width of the RXREF pulse is programmable in the LED Driver and HEC Status/Control Registers.

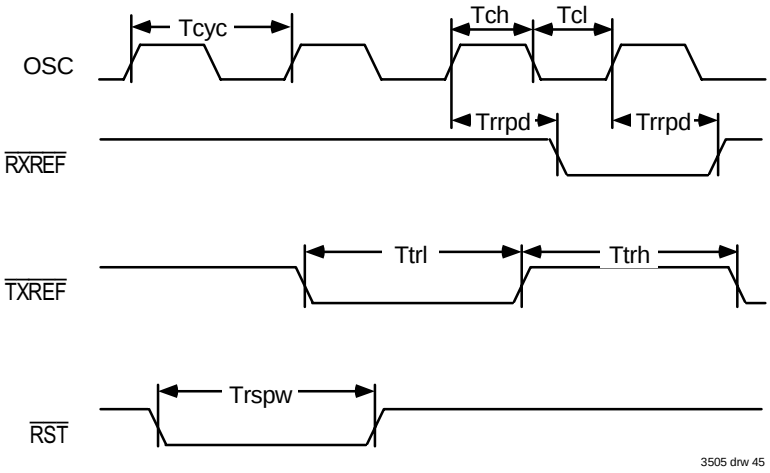


Figure 45 OSC, RXREF, TXREF and Reset Timing

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 46

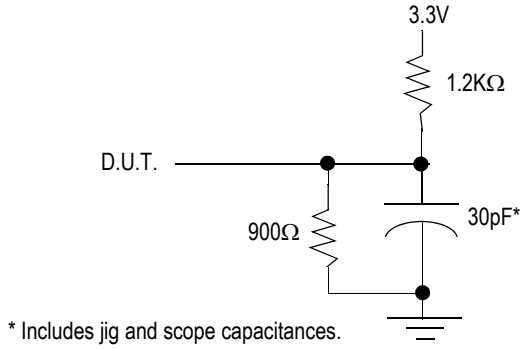


Figure 46 Output Load

A note about Figures 47 and 48: The ATM Forum and ITU-T standards for 25 Mbps ATM define "Network" and "User" interfaces. They are identical except that transmit and receive are switched between the two. A Network device can be connected directly to a User device with a straight-through cable. User-to-User or Network-to-Network connections require a cable with 1-to-7 and 2-to-8 crossovers.

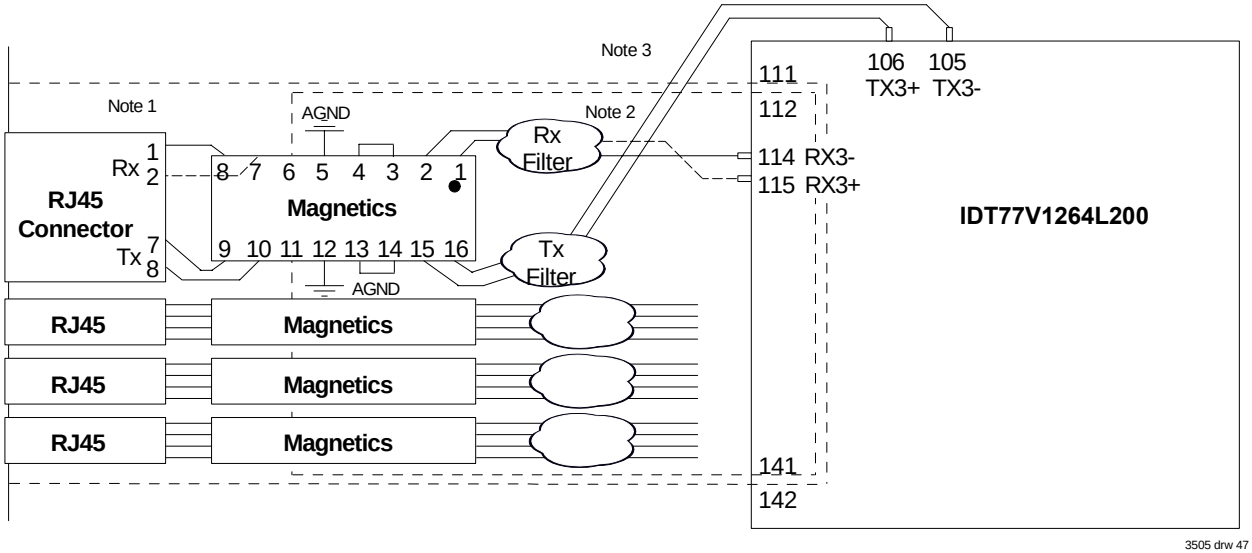


Figure 47 PC Board Layout for ATM Network

Note: 1.No power or ground plane inside this area.
2.Analog power plane inside this area.
3.Digital power plane inside this area.
4.A single ground plane should extend over the area covered by the analog and digital power planes, without breaks.
5.All analog signal traces should avoid 90° corners.

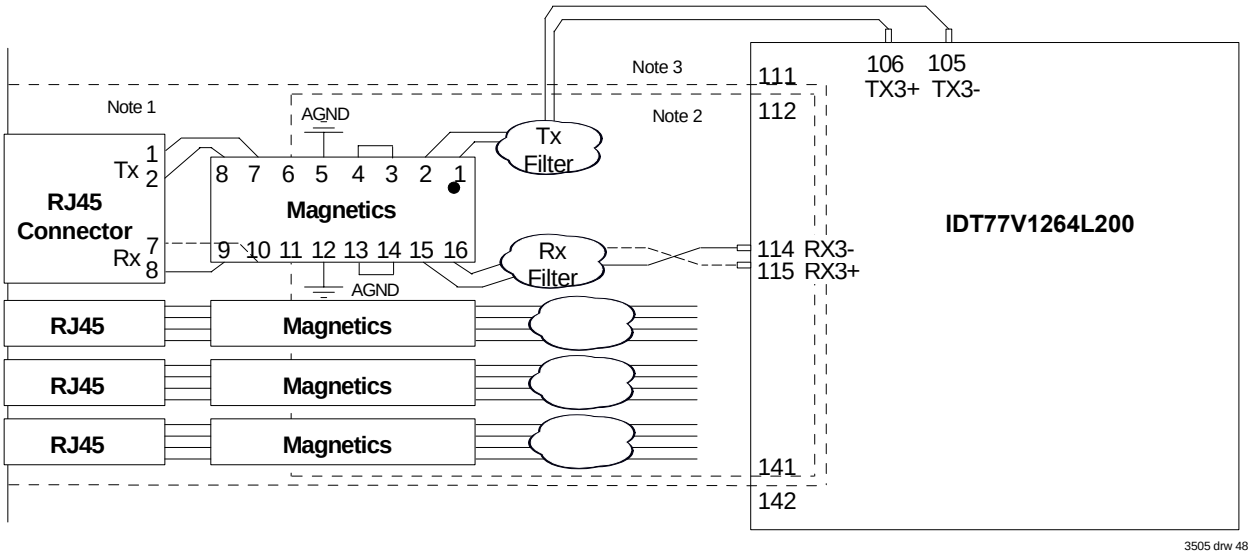
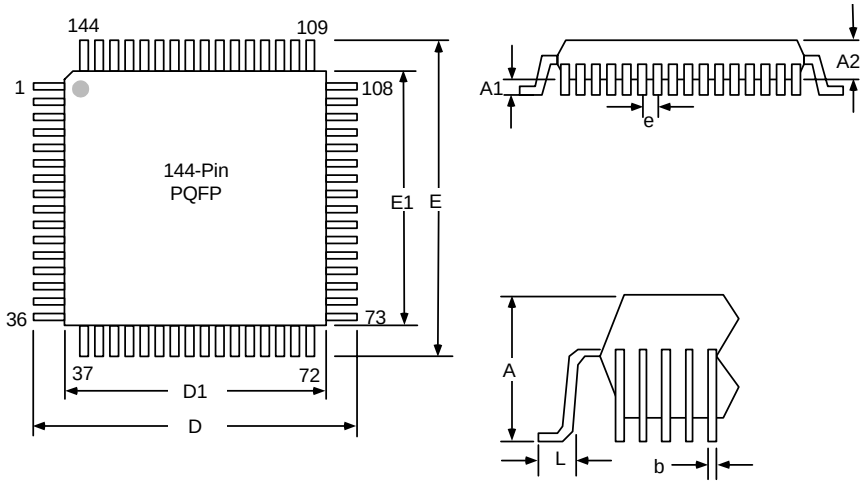


Figure 48 PC Board Layout for ATM User

Note: 1.No power or ground plane inside this area.
2.Analog power plane inside this area.
3.Digital power plane inside this area.
4.A single ground plane should extend over the area covered by the analog and digital power planes, without breaks.
5.All analog signal traces should avoid 90° corners.

Package Dimensions



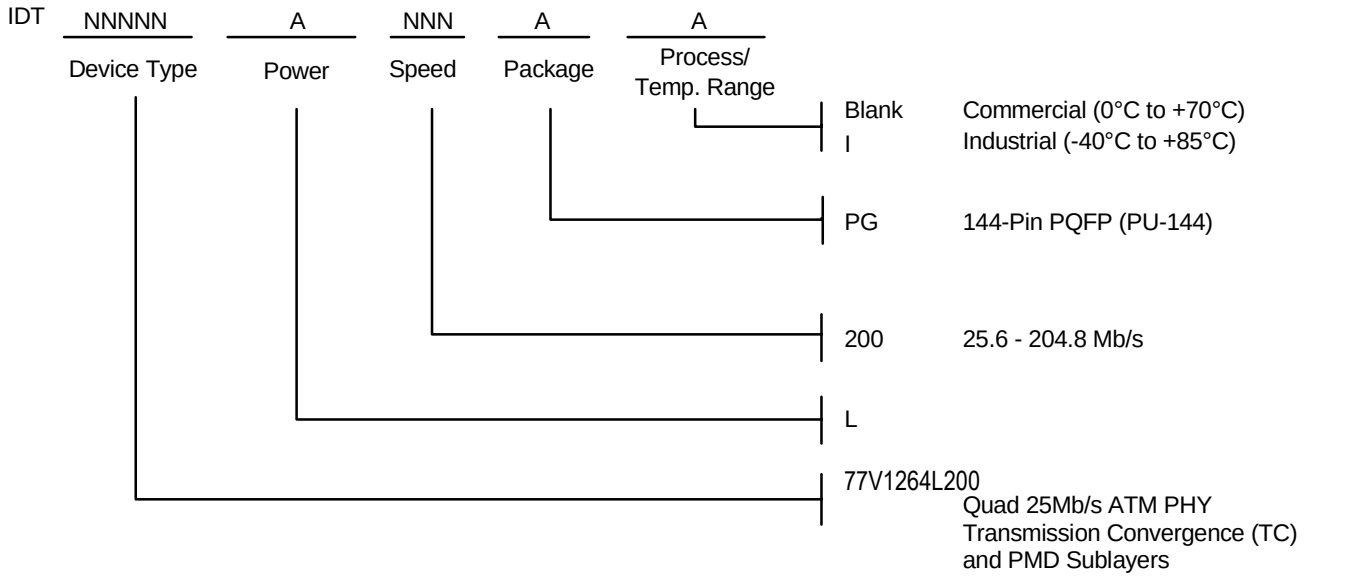
SYMBOL	MIN.	NOM.	MAX.
A	-	3.70	4.07
A1	0.25	0.33	-
A2	3.20	3.37	3.60
D	-	31.20	-
D1	-	28.00	-
E	-	31.20	-
E1	-	28.00	-
L	0.73	0.88	1.03
e	-	0.65	-
b	0.22	-	0.38

Dimensions are in millimeters

3505 drw 49

PSC-4053 is a more comprehensive package outline drawing which is available from the packaging section of the IDT web site.

Ordering Information



3505 drw 50 200

Revision History

September 20, 2001: Initial publication.

December 6, 2001: Added DPI information.

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