LONG HAUL SLIC
IDT821621

Version -
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2975 Stender Way, Santa Clara, California 95054
Telephone: (800) 345-7015 • • FAX: (408) 492-8674
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LONG HAUL SLIC

ADVANCE INFORMATION
IDT821621

FEATURES

- SLIC operating states: Active, Ringing, Standby and Disconnect
- Low Standby power consumption (35 mW)
- –19 V to –58 V battery operation
- On-hook transmission
- Two-wire impedance set by single external impedance
- Programmable constant-current feed
- Programmable loop-detect threshold
- Programmable ring-trip detect threshold
- +3.3 V / +5 V compatible power supply
- No –5 V supply required
- On-chip Thermal Management (TMG)
- Four on-chip relay drivers and relay snubbers, 1 ringing and 3 general purpose
- Package available: 32 pin PLCC

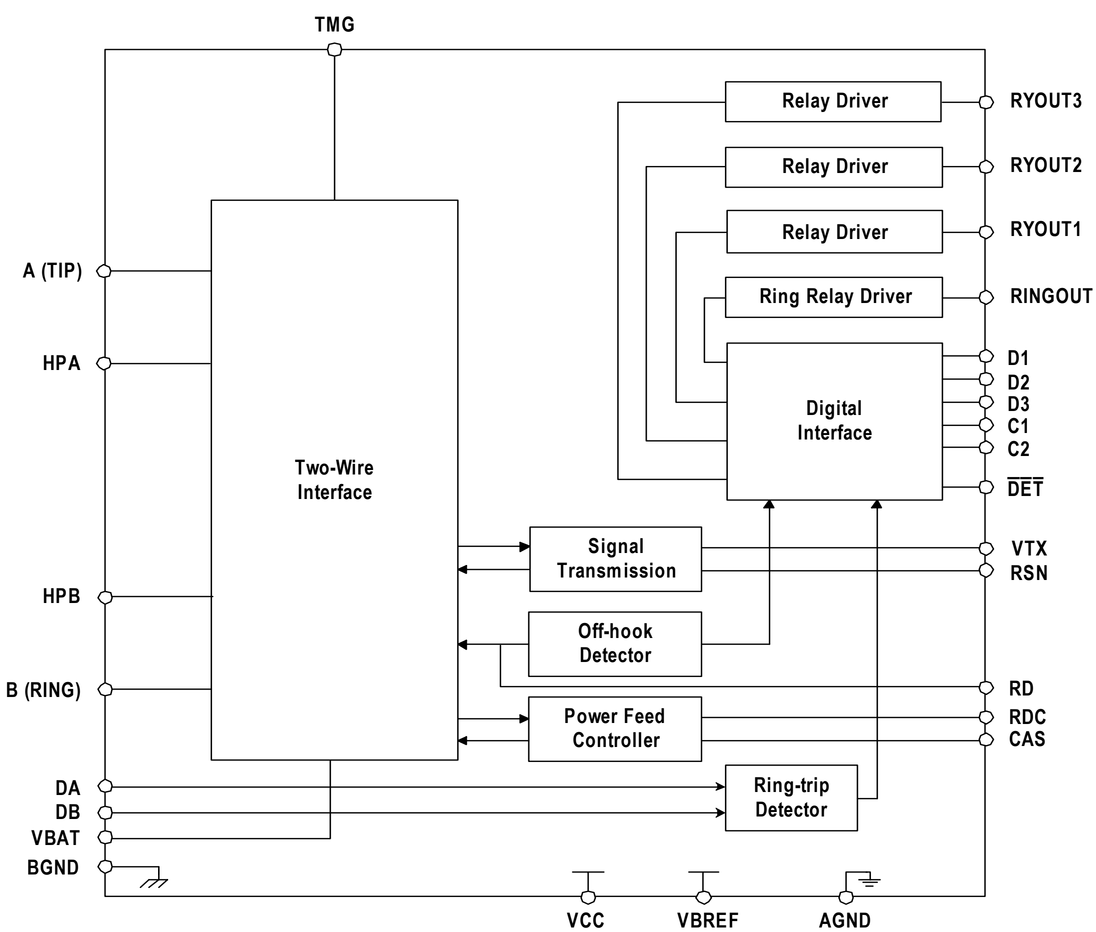
DESCRIPTION

The IDT821621 is a long haul Subscriber Line Interface Circuit. It implements the basic telephone line interface functions such as battery feeding, impedance matching, off-hook detection and ring-trip detection.

The IDT821621 allows battery feeding between –19 V and –58 V and has the capability for driving long loops. The architecture of operating the SLIC in different states according to different loop states minimizes the system power dissipation.

This long haul SLIC is pin-to-pin compatible with AMD7920. It provides a cost-effective solution for PBX and Central Office applications.

FUNCTIONAL BLOCK DIAGRAM



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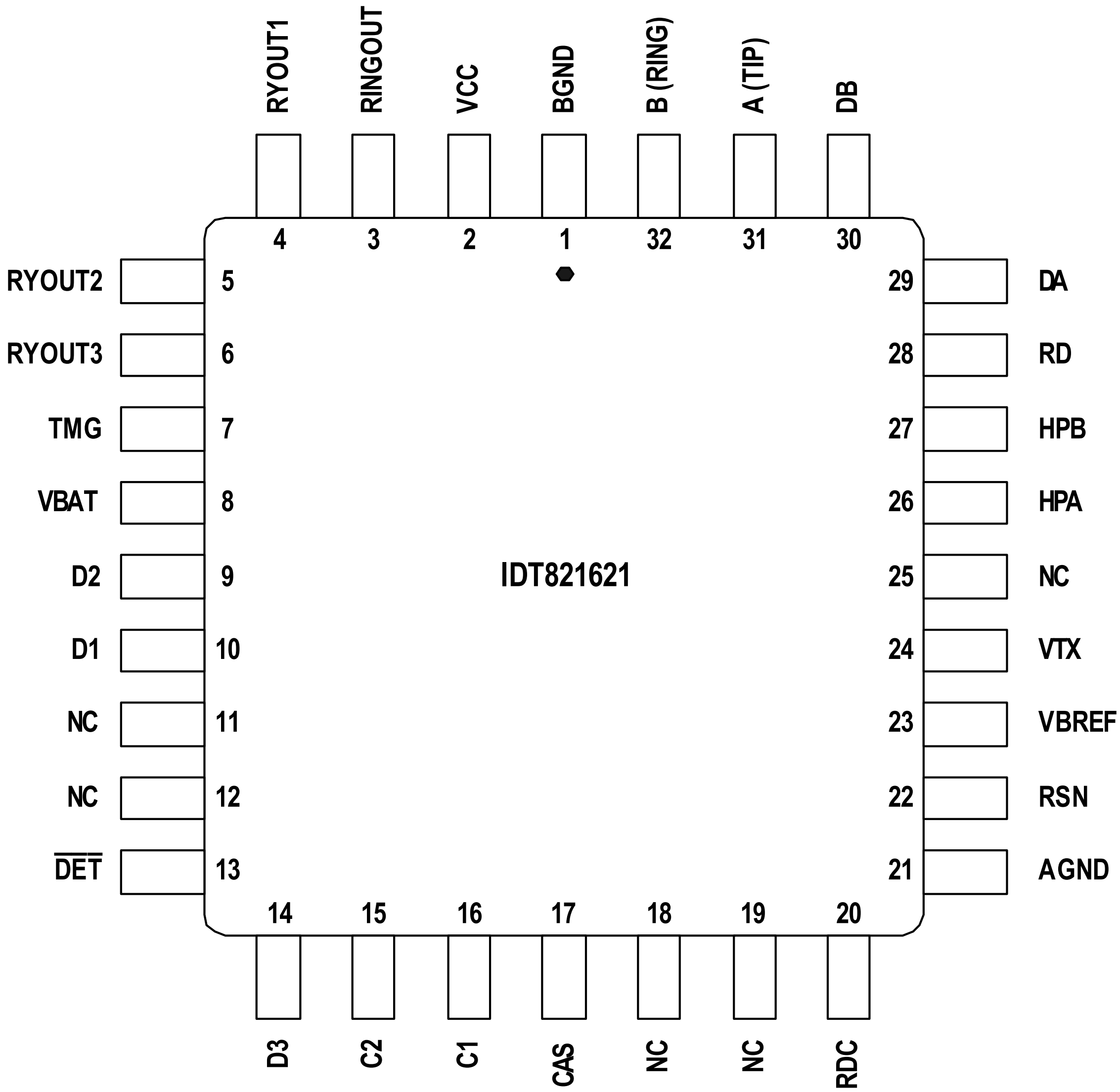
PIN CONFIGURATION



PIN DESCRIPTION

Table 1 — Pin Description

Pin Name	Type	PLCC Pin No.	Description
AGND	Ground	21	Analog ground.
BGND	Ground	1	Battery ground.
VBAT	Battery	8	Battery supply and connection to substrate.
VBREF	–	23	Battery reference pin. It should be connected to VBAT.
VCC	Power	2	+3.3 V / +5 V compatible power supply.
A (TIP)	I/O	31	Connection to the Tip wire of the subscriber loop.
B (RING)	I/O	32	Connection to the Ring wire of the subscriber loop.
HPA	Capacitor	26	A (TIP) side of high-pass filter capacitor.
HPB	Capacitor	27	B (RING) side of high-pass filter capacitor.
DA	Input	29	Negative input to ring-trip comparator.
DB	Input	30	Positive input to ring-trip comparator.
RSN	Input	22	Receive summing node.
VTX	Output	24	Transmit output.
C1 C2	Inputs	16 15	SLIC state control. TTL compatible. C2 is MSB and C1 is LSB. Refer to Table 2 for details.
D1 D2 D3	Inputs	10 9 14	Relay driver control. TTL compatible. D1, D2 and D3 control the relay drivers RYOUT1, RYOUT2 and RYOUT3 respectively. Logic low on D1 activates the RYOUT1 relay driver. Logic low on D2 activates the RYOUT2 relay driver. Logic low on D3 activates the RYOUT3 relay driver.
RYOUT1	Output	4	Relay/switch driver. Open-collector driver with emitter internally connected to BGND.
RYOUT2	Output	5	Relay/switch driver. Open-collector driver with emitter internally connected to BGND.
RYOUT3	Output	6	Relay/switch driver. Open-collector driver with emitter internally connected to BGND.
RINGOUT	Output	3	Ringing relay driver. Open-collector driver with emitter internally connected to BGND.
$\overline{DET}$	Output	13	Detector output. Open-collector with a built-in 15 kΩ pull-up resistor. This output provides on-hook/off-hook status of the loop based on the selected operating state. Refer to Table 2 for details. The detected output will either be hook switch or ring-trip. Logic low indicates that a hook switch event or ring-trip event has been detected.
RD	–	28	Detect resistor. An external resistor connected to this pin is used to set the loop-detect threshold.
RDC	–	20	DC feed resistor. The DC feed current is programmed by a network connected between this pin and RSN.
CAS	Capacitor	17	Anti-saturation capacitor. An external capacitor is connected to this pin to filter battery voltage when operating in anti-saturation region.
TMG	–	7	Thermal management. An external resistor is connected between this pin and VBAT to offload power from SLIC.
NC	–	11, 12, 18, 19, 25	No Connect.

FUNCTIONAL DESCRIPTION

The IDT821621 implements the basic telephone line interface functions. It provides many user programmable features including 2-wire impedance matching, loop-detect threshold and ring-trip threshold setting, constant current feeding, 4-wire to 2-wire gain setting, etc. The following sections describe these functions in detail.

SLIC STATES CONTROL

The IDT821621 can be operated in Disconnect, Ringing, Active or Standby state. A combination of the control pins C2 and C1 select one of the possible four operating states. See Table 2 for details. The IDT821621 provides an off-hook detector and a ring-trip detector on chip to support the necessary signaling functions. The selection of the detectors is based on the SLIC operating state. The output of the detectors is reported through the $\overline{DET}$ pin. Once a hook switch event or ring-trip event occurs, the $\overline{DET}$ pin goes low.

Table 2 — SLIC Operating States

State	Control Pins		Two-Wire Status	$\overline{DET}$ Output
	C2	C1		
0	0	0	Disconnect	Ring-trip Detector
1	0	1	Ringing	Ring-trip Detector
2	1	0	Active	Off-hook Detector
3	1	1	Standby	Off-hook Detector

- **Disconnect**

When the SLIC is in Disconnect state, both the TIP and RING outputs are in high impedance condition. In this state, the off-hook detector is inoperative and the power dissipation reduces to the lowest. The Disconnect state is useful for out-of-service lines.

- **Ringing**

When the SLIC is in Ringing state, the ring relay driver (RINGOUT) is activated and the TIP and RING outputs are in high impedance condition. The ringing source is connected by an external ring relay to the line. In Ringing state, the status of the ring-trip detector is reported by the $\overline{DET}$ pin.

- **Active**

In Active state, the SLIC is fully functional. The standard battery convention applies. All signal transmission and loop supervision functions are active. The status of the off-hook detector is gated to the $\overline{DET}$ pin.

- **Standby**

In Standby state, most of the internal circuitry is powered down, resulting in low power dissipation. The off-hook detection function operates normally, but signal transmission is not enabled. This state allows for monitoring off-hook transitions while maintaining lowest possible power consumption.

OFF-HOOK DETECTOR

The off-hook detector monitors the hook switch of the loop during Active or Standby state. The output of the $\overline{DET}$ pin goes low when an off-hook event is detected.

The loop-detect threshold is programmed by an external resistor R_D, which is connected between the RD and AGND pins. See Figure 1 for details.

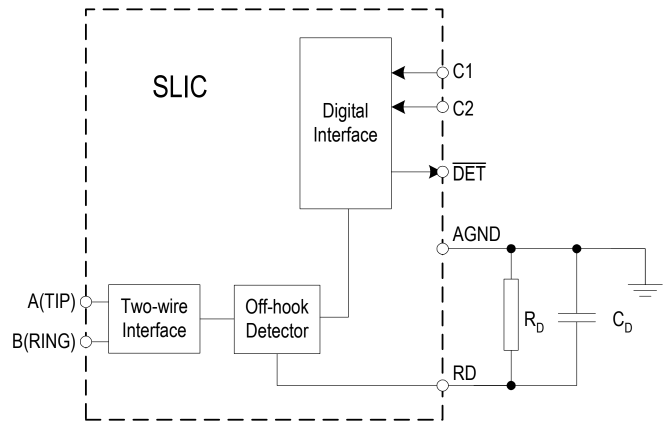


Figure 1 Loop-Detect Threshold Setting

The loop current threshold I_{ON} and I_{OFF} are calculated by the following equations:

$$I_{ON} = \frac{510}{R_D} \qquad I_{OFF} = \frac{415}{R_D}$$

The R-C network, formed by the capacitor C_D and the resistor R_D, determines the on-hook to off-hook time constant. The value of C_D for a typical on-hook to off-hook time constant of 0.5 ms is calculated by:

$$C_D = \frac{0.5ms}{R_D}$$

RING-TRIP DETECTOR

Figure 2 shows a general ringing circuit for the IDT821621. During Ringing state, the on-chip ring relay driver (RINGOUT) is activated and the ringing source is connected by the ring relay to the Tip and Ring lines through the resistors R_1 and R_2.

The ring-trip detector monitors the loop status and reports it via the $\overline{DET}$ pin. When the loop goes off-hook, the bridging resistors R_{B1}, R_{B2}, R_3 and R_4, and the filter capacitors C_{RT1} and C_{RT2} cause the voltage on DB to go positive with respect to DA and the $\overline{DET}$ pin goes low.

If R_{LMAX} is the maximum line resistance to be detected as an off-hook, the bridging resistors should be chosen as that:

$$\frac{R_{B1}}{R_3} = \frac{R_{B2}}{R_4} = \frac{(R_{LMAX} + R_{FEED})}{R_{LMAX}}$$

Where: $R_{FEED} = R_1 + R_2$

If the line resistance is less than R_{LMAX}, it means that an off-hook event occurs, otherwise, the loop is in on-hook state.

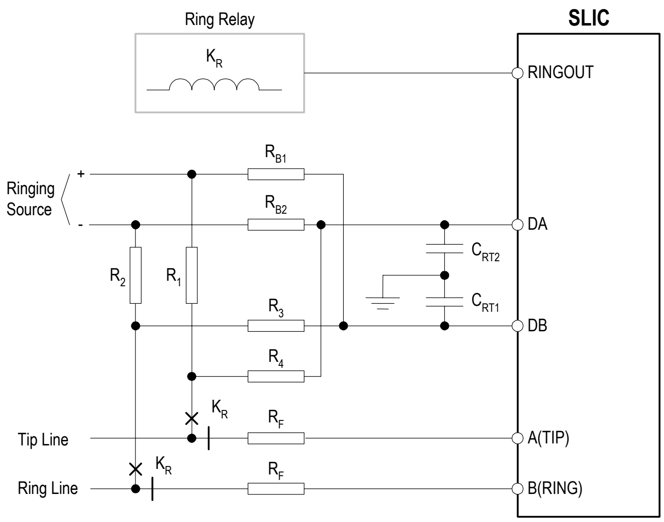


Figure 2 Ring-trip Detection

RELAY DRIVERS CONTROL

The IDT821621 provides an on-chip ring relay driver (RINGOUT) to control the external ring relay. This ring relay driver is active only in Ringing state. It is an internal transistor with the emitter internally connected to BGND and the collector as the driver output (see Figure 3). During ringing, the ring relay driver is activated and the ringing source is connected by an external ring relay to the Tip and Ring lines through ring feed resistors.

The IDT821621 also provides three additional relay drivers (RYOUT1, RYOUT2 and RYOUT3) on the chip. All of them are open-collector drivers with emitters internally connected to BGND. They allow for direct operation of external test relays. The digital pins D1 to D3 are used to control the relay drivers RYOUT1, RYOUT2 and RYOUT3 respectively. Logic low on D1 to D3 activates their respective relay drivers.

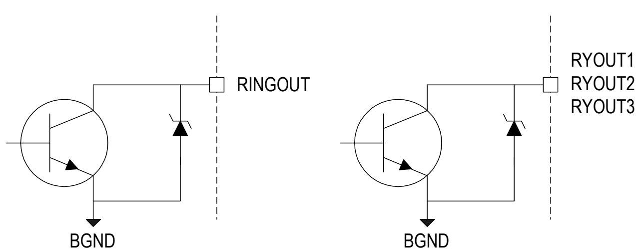


Figure 3 Relay Drivers Schematic

DC FEEDING

The IDT821621 provides constant-current feeding as shown in Figure 4.

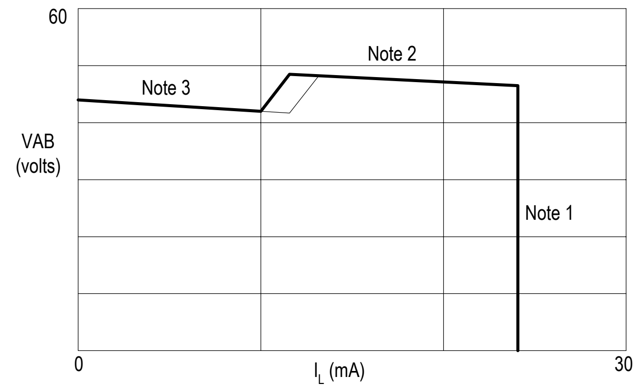


Figure 4 DC Feeding Characteristics

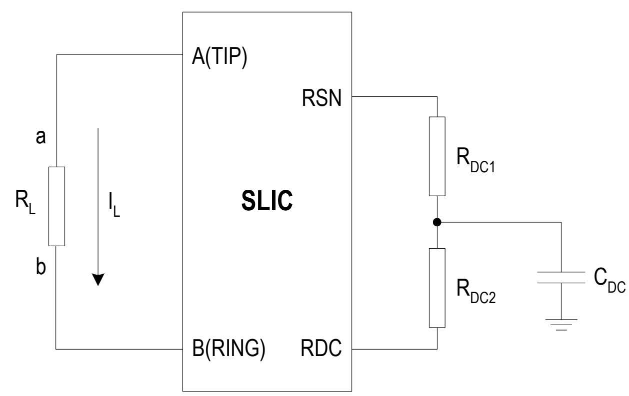
Notes:

1. $V_{AB} = I_L R_L' = \frac{1250}{R_{DC1} + R_{DC2}} R_L', \text{where } R_L' = R_L + 2R_F$

2. $V_{AB} = 0.857(|V_{BAT}| + 3.3) - I_L \frac{R_{DC1} + R_{DC2}}{300}$

3. $V_{AB} = 0.857(|V_{BAT}| + 1.2) - I_L \frac{R_{DC1} + R_{DC2}}{300}$

The feed current is programmable. Two resistors R_{DC1} and R_{DC2}, and a capacitor C_{DC} form the network for programming the feed current. See Figure 5,



Feed current is programmed by R_{DC1} and R_{DC2}.

Figure 5 DC Feed Programming Circuit

The feed current I_{FEED} is calculated by the following equation:

$$I_{FEED} = \frac{1250}{R_{DC1} + R_{DC2}}$$

An external capacitor C_{CAS} connected to the CAS pin is used to filter noise that may originate from the battery source and prevent the output amplifiers from saturating. The value of this anti-saturation capacitor is calculated by the equation below:

$$C_{CAS} = \frac{1}{1.7 \bullet 10^5 \pi f_C}$$

Where, f_C is the desired filter cut-off frequency.

IMPEDANCE MATCHING

The two-wire AC input impedance R_{2WIN} is programmed by means of an external impedance (R_T) connected between the RSN and VTX pins (see Figure 13). R_T is calculated by the following equation:

$$R_T = 250(R_{2WIN} - 2R_F)$$

Where, R_F is the value of the fuse resistor. Note that when computing R_T, the internal current amplifier pole and any external stray capacitance between the RSN and VTX pins must be taken into account.

RECEIVE GAIN SETTING

The 4-wire to 2-wire gain (G_{42L}) is defined as the receive gain. It is calculated by the following equation:

$$G_{42L} = \frac{R_L}{R_{RX}} \bullet \frac{500R_T}{R_T + 250(R_L + 2R_F)}$$

Where, R_L is the terminating impedance; R_{RX} is connected between VRX and RSN; R_T is defined above; R_F is the fuse resistor. See Figure 11 for details.

THERMAL MANAGEMENT

The IDT821621 uses a power management technique of offloading the thermal energy from the SLIC to an external resistor R_{TMG}. R_{TMG} is connected between the TMG and VBAT pins as shown in Figure 13. This resistor shares some of the loop current and limits the on-chip power dissipation in Active state.

The selection of R_{TMG} normally needs to satisfy the following condition: with the programmed loop current being fed into a short circuit loop from the nominal battery, all of the loop current is supplied by R_{TMG}. So, R_{TMG} can be calculated by the equation below:

$$R_{TMG} \geq \left(\frac{|V_{BAT}| - 8V}{I_{LOOP}} - 70\Omega\right)$$

The power dissipated in the resistor R_{TMG} during Active state is:

$$P_{RTMG} = \frac{(|V_{BAT}| - 8V - (I_L \bullet R_L))^2}{(R_{TMG} + 70\Omega)^2} \bullet R_{TMG}$$

The power dissipated in the SLIC during Active state is:

$$P_{SLIC} = |V_{BAT}| \bullet I_L - P_{RTMG} - R_L(I_L)^2 + 0.12W$$

DC ELECTRICAL CHARACTERISTICS

Table 3 — Absolute Maximum Ratings

Rating	Com'l & Ind'l	Unit
Power Supply Voltage VCC	-0.4 to +7	V
Battery Voltage VBAT	0.4 to -70	V
Voltage on Any Pin with Respect to Ground (Low Voltage Portion)	-0.4 to VCC+0.4	V
Voltage on Any Pin with Respect to Ground (High Voltage Portion)	+1 to VBAT	V
Package Power Dissipation	1.7	W
Storage Temperature	-65 to +150	°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 4 — Recommended Operating Conditions

Parameters	Min.	Max.	Unit
Ambient Temperature	-40	+85	°C
Power Supply Voltage VCC +3.3 V nominal +5 V nominal	 3.15 4.75	 3.45 5.25	 V V
Battery Voltage VBAT	-58	-19	V

AC ELECTRICAL CHARACTERISTICS

Unless otherwise stated, test conditions are VBAT = -52 V, VCC = +5 V, R_L = 600 Ω, R_{DC1} = R_{DC2} = 27.17 kΩ, R_{TMG} = 2350 Ω, R_D = 35.4 kΩ, no fuse resistors, C_{HP} = 0.22 µF, C_{DC} = 0.1 µF, C_{CAS} = 0.33 µF, D1 = 1N400x, 2-wire AC input impedance is a 600 Ω resistance synthesized by the programming network as shown below.

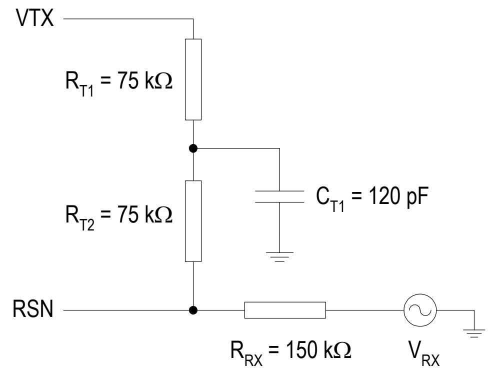


Figure 6 Two-Wire AC Input Impedance Programming Network

Table 5 — Transmission Performance

Description	Test Conditions (See Figure 7)	Min.	Typ.	Max.	Unit	Note
2-wire Return Loss	200 Hz to 3.4 kHz	26			dB	
Analog Output VTX Impedance			3	20	Ω	
Analog Output VTX Offset Voltage		-50		+50	mV	
Overload Level, 2-wire and 4-wire	Active state	2.5			Vpk	
Overload Level	On-hook, R_{LAC} = 600 Ω	0.77			Vrms	
THD, Total Harmonic Distortion	0 dBm		-64	-50	dB	
	+7 dBm		-55	-40		
THD, On-hook	0 dBm, R_{LAC} = 600 Ω			-36		

Table 6 — Longitudinal Capability

Description	Test Conditions (See Figure 8, Figure 9)	Min.	Typ.	Max.	Unit	Note
Longitudinal to metallic L-T, L-4 balance	200 Hz to 1 kHz 0 to 70 °C -40 to +85 °C	 63 58			dB	
	1 kHz to 3.4 kHz 0 to 70 °C -40 to +85 °C	 58 53				
Longitudinal Signal Generation 4-L	200 Hz to 3.4 kHz	40				
Longitudinal Current per pin	Active state	20	27	35	mArms	
Longitudinal Impedance at A or B	0 to 100 Hz		25		Ω/pin	

Table 7 — Idle Channel Noise

Description	Test Conditions		Min.	Typ.	Max.	Unit	Note
C-message Weighted Noise	R_L = 600 Ω R_L = 600 Ω	0 to 70°C -40 to +85°C		7	+10 +12	dBrnc	
Psophometric Weighted Noise	R_L = 600 Ω R_L = 600 Ω	0 to 70°C -40 to +85°C		-83	-80 -78	dBmp	

Table 8 — Insertion Loss and Balance Return Loss Signal

Description	Test Conditions (See Figure 10, Figure 11)	Min.	Typ.	Max.	Unit	Note
Gain Accuracy, 4- to 2-wire	0 dBm, 1 kHz	-0.20		+0.20	dB	
Gain Accuracy, 2- to 4-wire, 4- to 4-wire	0 dBm, 1 kHz	-6.22	-6.02	-5.82		
Gain Accuracy, 4- to 2-wire	On-hook	-0.35		+0.35		
Gain Accuracy, 2- to 4-wire, 4- to 4-wire	On-hook	-6.37	-6.02	5.67		
Gain Accuracy Over Frequency	300 to 3.4 kHz, relative to 1 kHz	-0.15		+0.15		
Gain Tracking	+3 dBm to -55 dBm, relative to 0 dBm	-0.15		+0.15		
Gain Tracking, On-hook	0 dBm to -37 dBm +3 dBm to 0 dBm	-0.15 -0.35		+0.15 +0.35		
Group Delay	0 dBm, 1 kHz		4		μs	

Table 9 — Line Characteristics

Description	Test Conditions	Min.	Typ.	Max.	Unit	Note
I_L, Short Loops, Active State	R_{LDC} = 600 Ω	20	23	26	mA	
I_L, Long Loops, Active State	R_{LDC} = 1930 Ω, VBAT = -42.75 V, T_A = 25 °C	18	19			
I_L, Accuracy, Standby State	$I_L = \frac{\lvert VBAT\rvert - 3V}{R_L + 200}$ T_A = 25 °C	$0.7I_L$	I_L	$1.3I_L$		
	Constant-current region	18	30			
I_L, Loop Current, Disconnect State	R_L = 0			100	μA	
I_L LIM	Active, A and B to ground		65		mA	
VAB, Open Circuit Voltage	V_{BAT} = -52 V	-42.75	-44		V	

Table 10 — Power Supply Rejection Ratio (V_{Ripple}=100 mVrms), Active State

Description	Test Conditions	Min.	Typ.	Max.	Unit	Note
VCC	50 Hz to 3.4 kHz	30	40		dB	
VBAT	50 Hz to 3.4 kHz	28	50			
Effective Internal Resistance	CAS pin to VBAT		335		kΩ	

Table 11 — Power Dissipation

Description	Test Conditions	Min.	Typ.	Max.	Unit	Note
On-hook, Disconnect State			18	70	mW	
On-hook, Standby State			32	100		
On-hook, Active State			210	270		
Off-hook, Standby State	R_L = 600 Ω		930	1200		
Off-hook, Active State	R_L = 300 Ω, R_{TMG} = 2350 Ω		760	900		

Table 12 — Supply Currents, Battery = -48V

Description	Test Conditions	Min.	Typ.	Max.	Unit	Note
I_{CC}, On-hook VCC Supply Current	Disconnect state Standby state Active state		2.6 1.9 4.3	4.0 4.0 8.5	mA	
I_{BAT}, On-hook VBAT Supply Current	Disconnect state Standby state Active state		0.25 0.55 3.8	1.0 1.5 4.8		

Table 13 — Receive Summing Node (RSN)

Description	Test Conditions	Min.	Typ.	Max.	Unit	Note
RSN DC Voltage	I_{RSN} = 0 mA		0		V	
RSN Impedance	200 Hz to 3.4 kHz		10	20	Ω	

Table 14 — Logic Inputs (C2-C1 and D3-D1)

Description	Test Conditions	Min.	Typ.	Max.	Unit	Note
V_{IH}, Input High Voltage		2.0			V	
V_{IL}, Input Low Voltage				0.8		
I_{IH}, Input High Current		-75		40	µA	
I_{IL}, Input Low Current		-400				

Table 15 — Logic Output ($\overline{DET}$)

Description	Test Conditions	Min.	Typ.	Max.	Unit	Note
V_{OL}, Output Low Voltage	I_{OUT} = 0.3 mA, 15 kΩ to VCC			0.4	V	
V_{OH}, Output High Voltage	I_{OUT} = -0.1 mA, 15 kΩ to VCC	2.4				

Table 16 — Ring-trip Detector Input (DA, DB)

Description	Test Conditions	Min.	Typ.	Max.	Unit	Note
Bias Current		-500	-50		nA	
Offset Voltage	Source Resistance = 2 MΩ	-50	0	+50	mV	

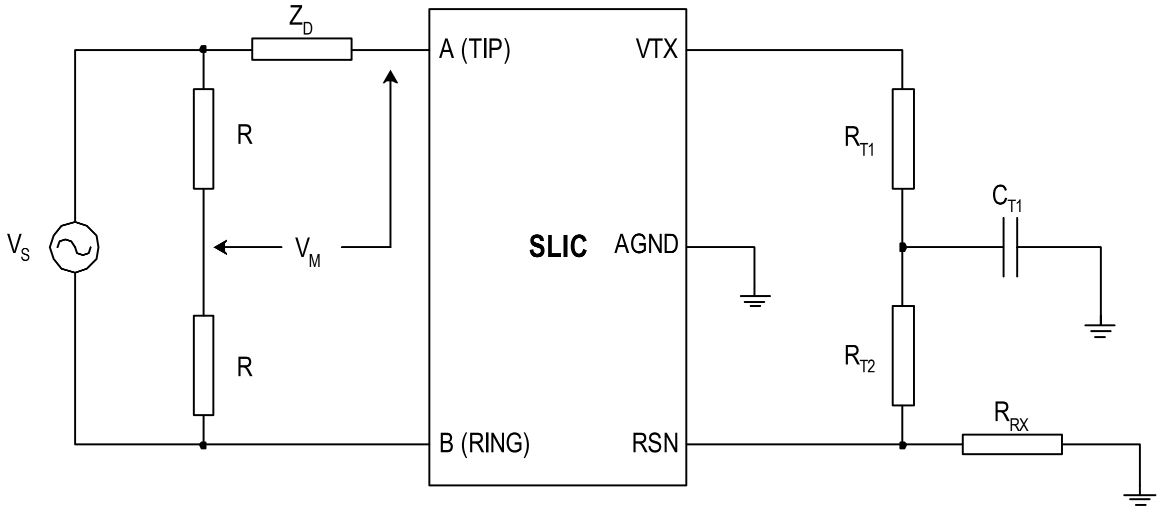
Table 17 — Loop Detector

Description	Test Conditions (See Figure 12)	Min.	Typ.	Max.	Unit	Note
On Threshold	R_D = 35.4 KΩ	11.5		17.3	mA	
Off Threshold	R_D = 35.4 KΩ	9.4		14.1	mA	
Hysteresis	R_D = 35.4 KΩ	0		4.4	mA	

Table 18 — Relay Driver Output (RINGOUT, RYOUT1, RYOUT2, RYOUT3)

Description	Test Conditions	Min.	Typ.	Max.	Unit	Note
On Voltage	I_{OL} = 40 mA		+0.3	+0.7	V	
Off Leakage	V_{OH} = +5 V			100	μA	
Zener Breakover	I_Z = 100 μA		9.4		V	
Zener On Voltage	I_Z = 30 mA		10		V	

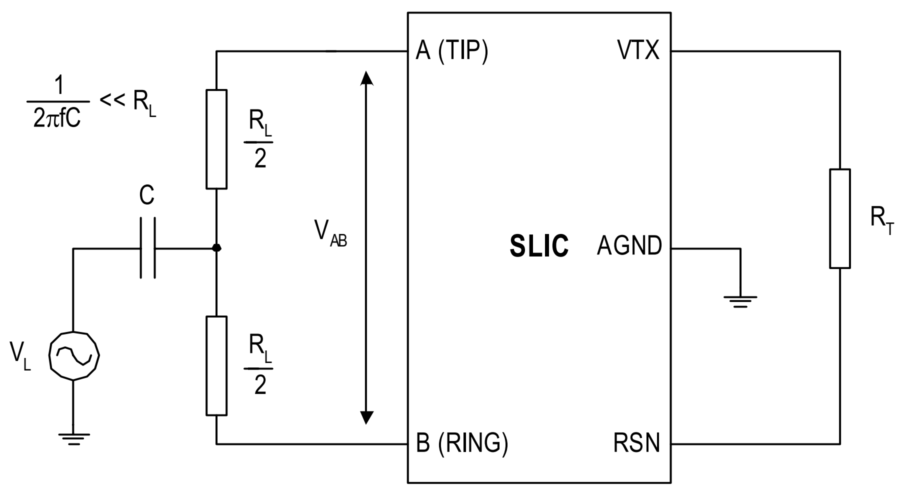
TEST CIRCUITS



Z_D: The desired impedance (e.g., the characteristic impedance of the line)

Return Loss = $-20 \log (2 V_M / V_S)$

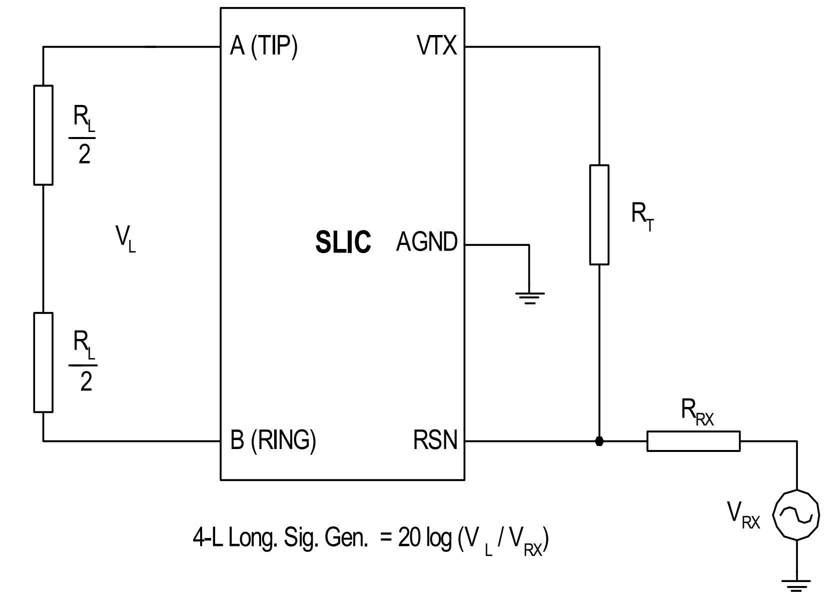
Figure 7 Two-Wire Return Loss



Longitudinal to Two-Wire Balance = $20 \log (V_{AB} / V_L)$

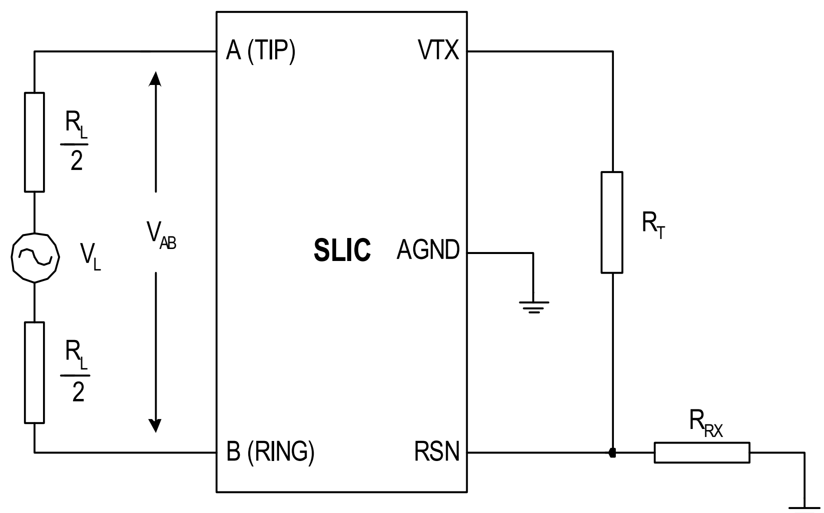
Longitudinal to Four-Wire Balance = $20 \log (VTX / V_L)$

Figure 8 Longitudinal Balance



4-L Long. Sig. Gen. = 20 log (V_L / V_{RX})

Figure 9 Four-Wire Longitudinal Signal Generation



Gain 2-4 = 20 log (VTX / V_{AB})

Figure 10 Two-to-Four Wire Gain

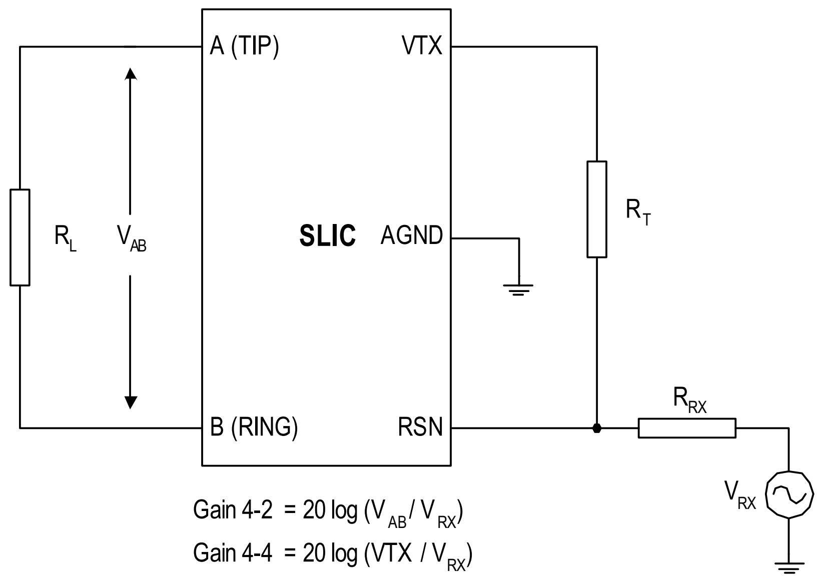


Figure 11 Four-to-Two Wire Gain and Four-to-Four Wire Gain

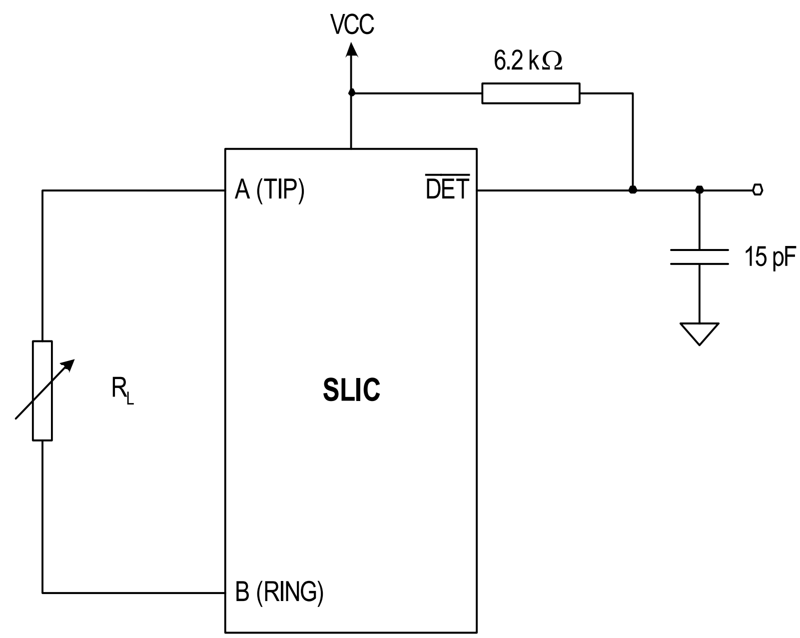


Figure 12 Loop Detector Switching

BASIC APPLICATION CIRCUIT

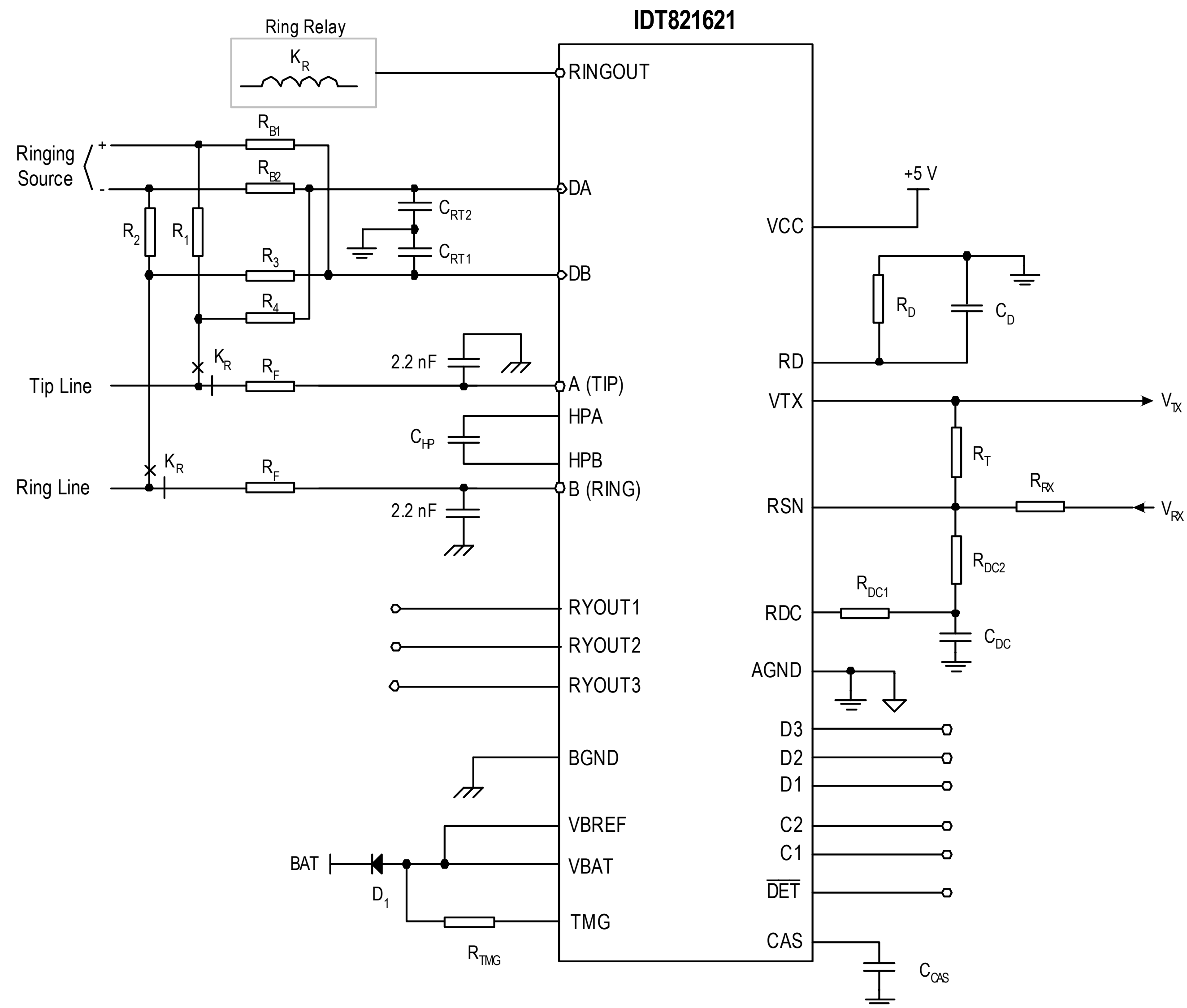
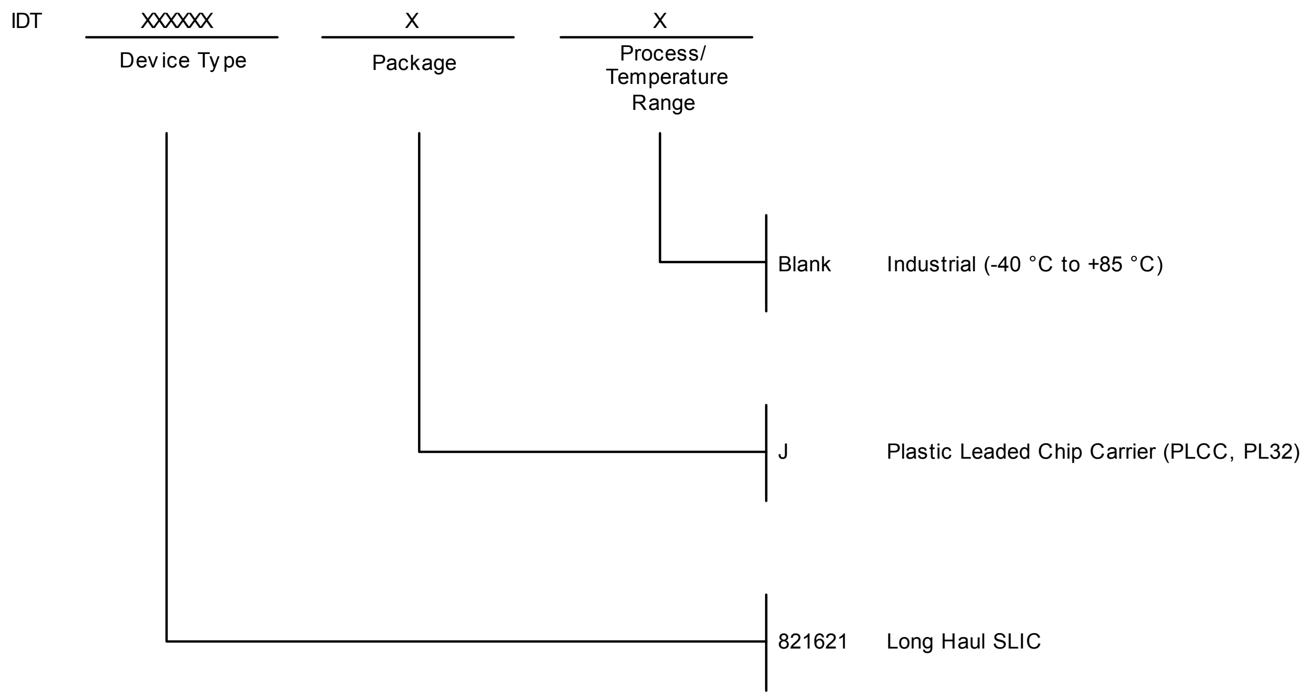


Figure 13 Basic Application Circuit

ORDERING INFORMATION



CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
800-345-7015 or 408-727-5116
fax: 408-492-8674
www.idt.com

for Tech Support:
408-330-1753
email:TELECOMhelp@idt.com