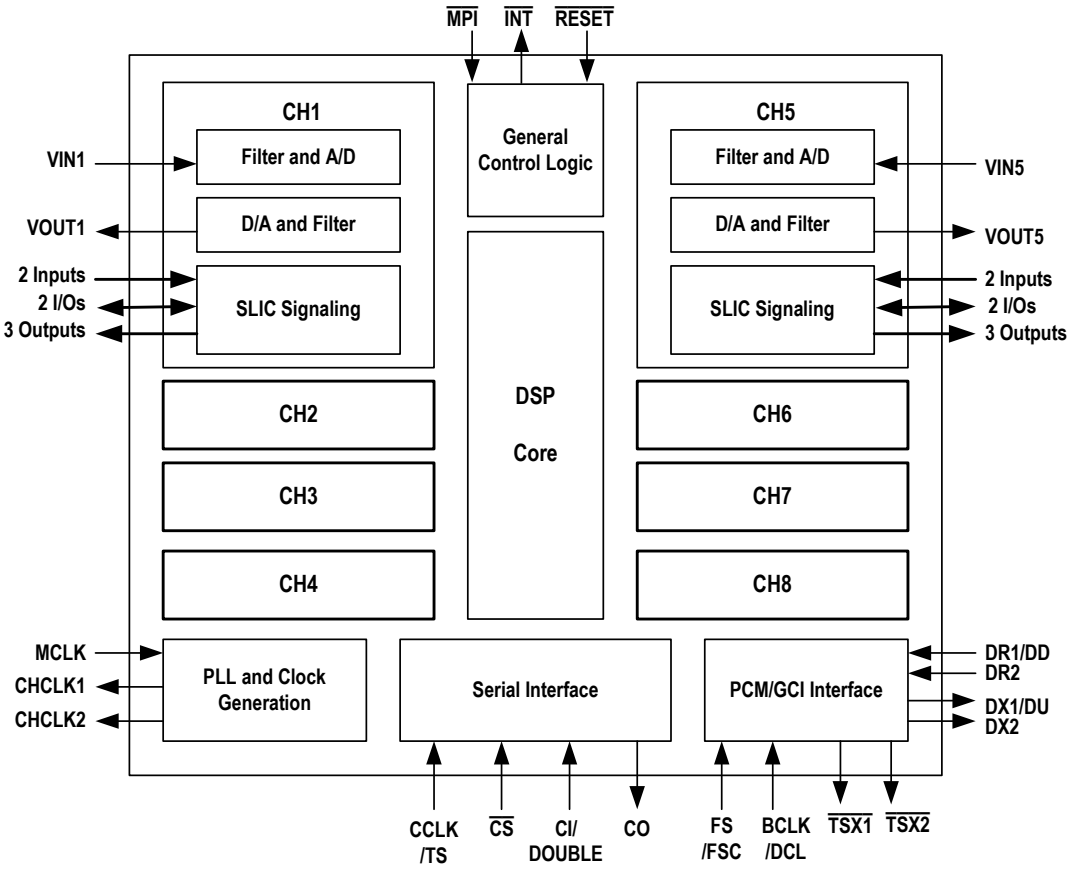
OCTAL PROGRAMMABLE PCM CODEC

PRELIMINARY
IDT82V1068

FEATURES

- 8 channel CODEC with on-chip digital filters
- Programmable A/μ-law compressed or linear code conversion
- Meets ITU-T G.711 - G.714 requirements
- Programmable digital filters adapting to system requirements:
  - AC impedance matching
  - Transhybrid balance
  - Frequency response correction
  - Gain setting
- Supports two programmable PCM buses and one GCI bus
- Flexible PCM interface with up to 128 programmable time slots, data rate from 512 kbit/s to 8.192 Mbit/s
- Broadcast mode for coefficient setting
- 7 SLIC signaling pins (including 2 debounced pins) per channel
- Fast hardware ring trip mechanism
- Two programmable tone generators per channel for testing, ringing and DTMF generation
- 4 FSK generators shared by all 8 channels
- Two programmable chopper clocks
- Notch filters for 12 kHz and 16 kHz frequencies
- Master clock frequency selectable: 1.536 MHz, 1.544 MHz, 2.048 MHz, 3.072 MHz, 3.088 MHz, 4.096 MHz, 6.144 MHz, 6.176 MHz or 8.192 MHz
- Advanced test capabilities
  - 5 analog loopback tests
  - 6 digital loopback tests
  - Level metering function
- High analog driving capability (300 Ω AC)
- CODEC identification
- 3 V digital I/O with 5 V tolerance
- 3.3 V single power supply
- Operating temperature range: - 40°C to + 85°C
- Package available: 128 pin TQFP

FUNCTIONAL BLOCK DIAGRAM



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DESCRIPTION

The IDT82V1068 is a feature rich, single-chip, programmable 8 channel PCM CODEC with on-chip filters. Besides the A-Law/μ-Law companding and linear coding/decoding (16-bit 2's complement), the IDT82V1068 provides 2 programmable tone generators per channel (which can also generate ring signals), 4 FSK generators shared by 8 channels and 2 programmable chopper clocks for the SLIC.

The digital filters in the IDT82V1068 provide the necessary transmit and receive filtering for voice telephone circuits to interface with time-division multiplexed systems. An integrated programmable DSP realizes AC impedance matching, transhybrid balance, frequency response correction and gain adjusting functions. The IDT82V1068 supports 2 PCM buses with programmable sampling edge, that allows an extra delay of up to 7 clocks. Once the delay is determined, it is effective to all eight channels of the IDT82V1068. The device also provides 7 signaling pins to the SLIC on per channel basis.

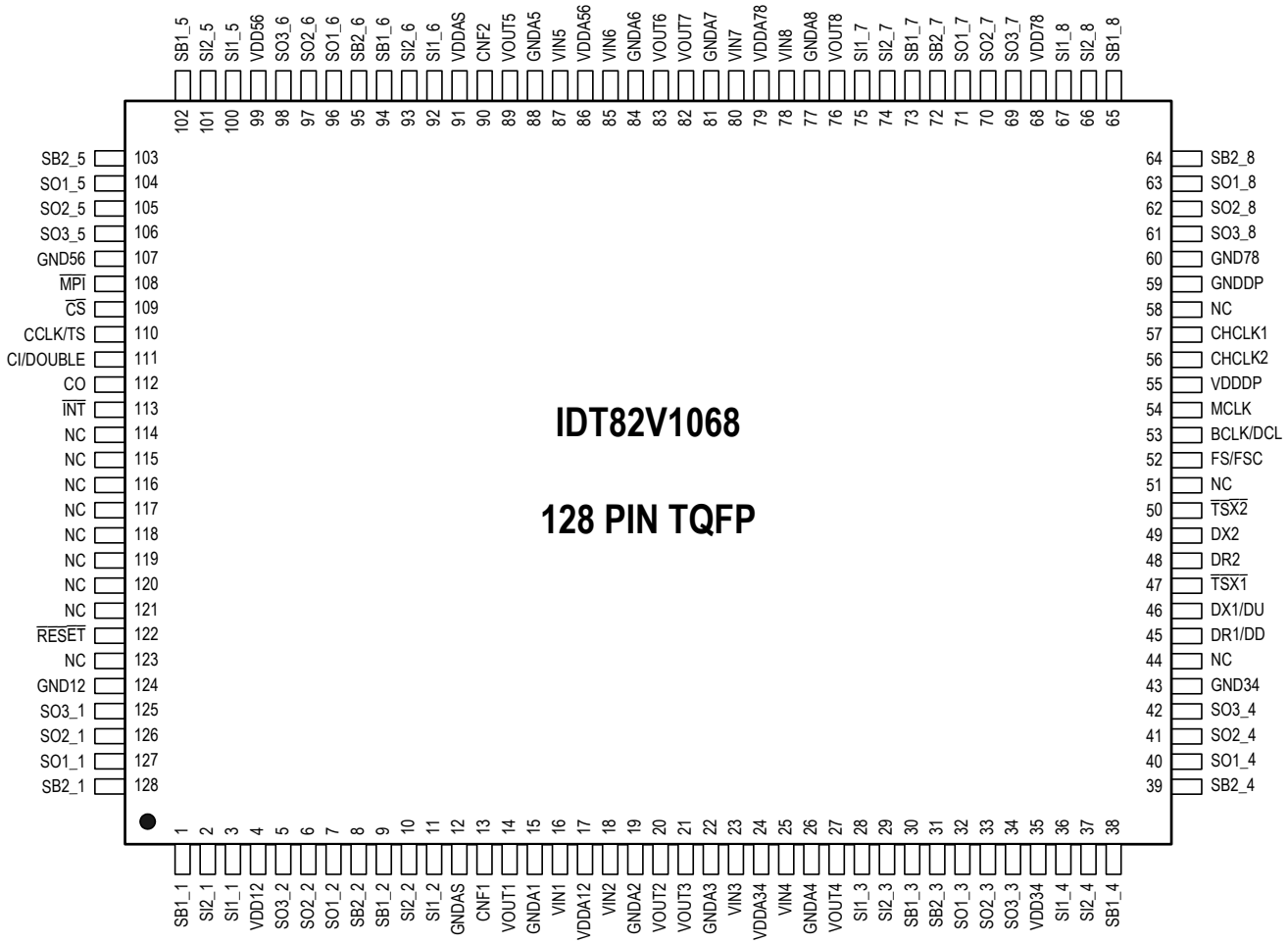
The IDT82V1068 provides 2 programming interfaces: the Microprocessor Interface (MPI) and the General Control Interface (GCI). The latter is also known as ISDN Oriented Module (IOM®-2). For both MPI and GCI programming, the device supports compressed and linear data formats.

The device also provides strong test capability with several analog/ digital loopbacks and level metering function. This brings convenience to system maintenance and diagnosis.

A unique feature of "Hardware Ring Trip" is implemented in the IDT82V1068. When an off-hook signal is detected, the IDT82V1068 can reverse an output pin to stop ringing immediately.

The IDT82V1068 can be used in digital telecommunication applications such as Central Office Switch, PBX, DLC and Integrated Access Devices (IADs), i.e. VoIP and VoDSL.

PIN CONFIGURATION



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1 PIN DESCRIPTION

Name	Type	Pin Number	Description
GNDA1 GNDA2 GNDA3 GNDA4 GNDA5 GNDA6 GNDA7 GNDA8	Power	15 19 22 26 88 84 81 77	**Analog Ground.** All ground pins should be connected together.
GNDAS	Power	12	**Analog Ground for Bias.** All ground pins should be connected together.
GND12 GND34 GND56 GND78	Power	124 43 107 60	**Digital Ground.** All ground pins should be connected together.
GNDDP	Power	59	**Digital Ground for PLL.** All ground pins should be connected together.
VDDA12 VDDA34 VDDA56 VDDA78	Power	17 24 86 79	**+3.3 V Analog Power Supply.** These pins should be connected to the ground via a 0.1μF capacitor. All power supply pins should be connected together.
VDDAS	Power	91	**+3.3 V Analog Power Supply for Bias.** This pin should be connected to the ground via a 0.1μF capacitor. All power supply pins should be connected together.
VDD12 VDD34 VDD56 VDD78	Power	4 35 99 68	**+3.3 V Digital Power Supply.** These pins should be connected to the ground via a 0.1μF capacitor. All power supply pins should be connected together.
VDDDP	Power	55	**+3.3 V Digital Power Supply for PLL.** This pin should be connected to the ground via a 0.1μF capacitor. All power supply pins should be connected together.
VIN1 VIN2 VIN3 VIN4 VIN5 VIN6 VIN7 VIN8	I	16 18 23 25 87 85 80 78	**Analog Voice Input for Channel 1 to 8.** Each of these pins is connected to the corresponding SLIC via a capacitor (0.22 μF).
VOUT1 VOUT2 VOUT3 VOUT4 VOUT5 VOUT6 VOUT7 VOUT8	O	14 20 21 27 89 83 82 76	**Voice Frequency Receiver Output of Channel 1 to 8.** These pins can drive 300 Ω AC load. They allows the direct driving of a transformer.
SI1_1 SI1_2 SI1_3 SI1_4 SI1_5 SI1_6 SI1_7 SI1_8	I	3 11 28 36 100 92 75 67	**Debounce SLIC Signaling Input 1 for Channel 1 to 8.** The input signals on these pins will be filtered by their respective debounce filters.

Name	Type	Pin Number	Description
SI2_1 SI2_2 SI2_3 SI2_4 SI2_5 SI2_6 SI2_7 SI2_8	I	2 10 29 37 101 93 74 66	**Debounce SLIC Signaling Input 2 for Channel 1 to 8.** The input signals on these pins will be filtered by their respective debounce filters.
SB1_1 SB1_2 SB1_3 SB1_4 SB1_5 SB1_6 SB1_7 SB1_8	I/O	1 9 30 38 102 94 73 65	**SLIC Signaling I/O 1 for Channel 1 to 8.** The directions of the these pins are software programmable.
SB2_1 SB2_2 SB2_3 SB2_4 SB2_5 SB2_6 SB2_7 SB2_8	I/O	128 8 31 39 103 95 72 64	**SLIC Signaling I/O 2 for Channel 1 to 8.** The directions of the these pins are software programmable.
SO1_1 SO1_2 SO1_3 SO1_4 SO1_5 SO1_6 SO1_7 SO1_8	O	127 7 32 40 104 96 71 63	**SLIC Signaling Output 1 of Channel 1 to 8.**
SO2_1 SO2_2 SO2_3 SO2_4 SO2_5 SO2_6 SO2_7 SO2_8	O	126 6 33 41 105 97 70 62	**SLIC Signaling Output 2 of Channel 1 to 8.**
SO3_1 SO3_2 SO3_3 SO3_4 SO3_5 SO3_6 SO3_7 SO3_8	O	125 5 34 42 106 98 69 61	**SLIC Signaling Output 3 of Channel 1 to 8.**
DX1/DU	O	46	**DX1: Transmit PCM Data Output 1 (for MPI Mode)** In MPI mode, the DX1 pin remains in high-impedance state until a pulse appears on the FS pin. The PCM data is output through the DX1 or DX2 pin as selected by Local Command 7, following the bit clock signal on the BCLK pin. **DU: GCI Data Upstream (for GCI Mode)** In GCI mode, the data upstream of all eight channels is sent out through the DU pin. The time slot assignment for the eight channels is determined by the CCLK/TS pin.

Name	Type	Pin Number	Description
DX2	O	49	**Transmit PCM Data Output 2 (for MPI Mode)** This pin remains in high-impedance state until a pulse appears on the FS pin. The PCM data is output through the DX1 or DX2 pin as selected by Local Command 7, following the bit clock signal on the BCLK pin. This pin is not used in GCI mode.
DR1/DD	I	45	**DR1: Receive PCM Data Input 1 (for MPI Mode)** In MPI mode, the PCM data is received from the DR1 or DR2 pin as selected by Local Command 8, following the bit clock signal on the BCLK. **DD: GCI Data Downstream (for GCI Mode)** In GCI mode, the data downstream of all eight channels is received serially on the DD pin. The time slot assignment for the eight channels is determined by the CCLK/TS pin.
DR2	I	48	**Receive PCM Data Input 2 (for MPI Mode).** In MPI mode, the PCM data is received from the DR1 or DR2 pin as selected by Local Command 8, following the bit clock signal on the BCLK pin. This pin is not used in GCI mode.
FS/FSC	I	52	**FS: Frame Synchronization signal (for MPI Mode)** In MPI mode, the FS signal is an 8 kHz synchronization signal that identifies the beginning of the PCM frame. **FSC: Frame Sync signal (for GCI Mode)** In GCI mode, the FSC signal is an 8 kHz synchronization signal that identifies the beginning of the GCI frame.
BCLK/DCL	I	53	**BCLK: Bit Clock (for MPI Mode)** In MPI mode, the PCM data is transmitted through the DX1 or DX2 pin and received from the DR1 or DR2 pin following the signal on the BCLK pin. The frequency of the BCLK may vary from 512 kHz to 8.192 MHz. The BCLK signal is required to be synchronous to the FS signal. **DCL: Data Clock (for GCI Mode)** In GCI mode, the DCL signal is either 2.048 MHz or 4.096 MHz, selected by the CI/DOUBLE pin. If the CI/DOUBLE pin is logic low, the DCL signal is 2.048 MHz; If the CI/DOUBLE pin is logic high, the DCL signal is 4.096 MHz. It is recommended to connect the MCLK and DCL pins together.
$\overline{\text{TSX1}}$	O	47	**Transmit Output Indicator 1 (for MPI Mode)** This is an open drain output. It becomes low when the PCM data is transmitted through the DX1 pin. This pin is not used in GCI mode.
$\overline{\text{TSX2}}$	O	50	**Timeslot Indicator Output 2 (for MPI Mode)** This is an open drain output. It becomes low when the PCM data is transmitted through the DX2 pin. This pin is not used in GCI mode.
$\overline{\text{CS}}$	I	109	**Chip Selection (for MPI Mode).** In MPI mode, a logic low on this pin enables the Serial Control Interface.
CI/DOUBLE	I	111	**CI: Serial Control Interface Data Input (for MPI Mode)** In MPI mode, the control data from the master processor is input to the CODEC through the CI pin. The data rate is determined by the CCLK signal. **DOUBLE: Double/Single DCL Selection (for GCI Mode)** In GCI mode, the DOUBLE pin is used to determine the frequency of the DCL signal. When low, the DCL frequency is 2.048 MHz; when high, the DCL frequency is 4.096 MHz.
CO	O	112	**Serial Control Interface Data Output (tri-state) (for MPI Mode)** In MPI mode, the serial control interface data is output from the CODEC to the master processor through the CO pin. The data rate is determined by the CCLK signal. This pin is in high impedance state when the $\overline{\text{CS}}$ pin is logic high. The CO pin is not used in GCI mode.
CCLK/TS	I	110	**CCLK: Serial Control Interface Clock (for MPI Mode)** In MPI mode, this is the clock for the Serial Control Interface. It can be up to 8.192 MHz. **TS: Timeslot Selection (for GCI Mode)** In Compressed GCI mode, the TS pin indicates which half of the 8 continuous GCI timeslots is used. When the TS pin is low, timeslots 0-3 are selected; when this pin is high, timeslots 4-7 are selected. In Linear GCI mode, the TS pin indicates which half of the 8 continuous GCI timeslots is used for voice signals. When this pin is low, timeslots 0-3 are used for linear voice data, timeslots 4-7 are used for Monitor channel and C/I octet. When this pin is high, timeslots 4-7 are used for linear voice data, timeslots 0-3 are used for Monitor channel and C/I octet.

Name	Type	Pin Number	Description
$\overline{\text{MPI}}$	I	108	**MPI/GCI Mode Selection** This pin is used to select one of the two interfaces, the Microprocessor Interface (MPI) and the General Control Interface (GCI). A logic low selects MPI and a logic high selects GCI.
$\overline{\text{RESET}}$	I	122	**Reset Input.** A logic low on this pin resets the IDT82V1068 and forces it to the default mode.
$\overline{\text{INT}}$	O	113	**Interrupt Output Pin.** Active low interrupt signal for Channel 1 to 8, open-drain. It reflects the changes on the SLIC pins.
MCLK	I	54	**Master Clock Input** The master clock provides the clock for the DSP of the CODEC. In MPI mode, the frequency of the MCLK signal can be 1.536 MHz, 1.544 MHz, 2.048 MHz, 3.072 MHz, 3.088 MHZ, 4.096 MHz, 6.144 MHz, 6.176 MHz or 8.192 MHz. The MCLK signal can be asynchronous to the BCLK signal. In GCI mode, it is recommended to connect the MCLK pin to the DCL pin. The frequency of the MCLK signal can be 2.048 MHz or 4.096 MHz. Refer to the description on the DCL pin for details.
CHCLK1	O	57	**Chopper Clock Output 1** This pin provides a programmable (2 -28 ms) output signal synchronous to the MCLK.
CHCLK2	O	56	**Chopper Clock Output 2** This pin provides a programmable 256 kHz, 512 kHz or 16.384 MHz output signal synchronous to the MCLK.
CNF1 CNF2	–	13 90	**Capacitor for noise filtering.**
NC	–	44, 51 58, 114 115, 116 117, 118 119, 120 121, 123	**No Connection.**

2 FUNCTION DESCRIPTION

The IDT82V1068 performs the CODEC/filter functions required by the subscriber line interface circuitry in telecommunications system. The IDT82V1068 converts analog voice signals to digital PCM samples and digital PCM samples back to analog voice signals. High performance oversampling Analog-to-Digital Converters (ADC) and Digital-to-Analog Converters (DAC) in the IDT82V1068 provide the required conversion accuracy. The associated decimation and interpolation filters are realized with both dedicated hardware and the Digital Signal Processor (DSP). The DSP also handles all other necessary functions such as PCM bandpass filtering, sample rate conversion and PCM companding.

2.1 MPI MODE AND GCI MODE

The Microprocessor Interface (MPI) and the General Control Interface (GCI) help the user to program and control the CODEC. The $\overline{MPI}$ pin selects the interface: '0' selects MPI mode and '1' selects GCI mode.

2.1.1 MPI CONTROL INTERFACE

In MPI mode, the internal configuration registers (local/global), the SLIC signaling interface and the Coefficient-RAM, FSK-RAM of the IDT82V1068 are programmed by microprocessor via the serial control interface, which consists of four lines (pins): CCLK, $\overline{CS}$, CI and CO. All the commands and data transmitted or received are aligned in byte (8 bits). The CCLK is the Serial Control Interface Clock, it can be up to 8.192 MHz. The $\overline{CS}$ is the Chip Select pin, a low level on it enables the serial control interface. The CI and CO pins are the serial control interface data input and output, carrying the control commands and data bytes to/from the IDT82V1068.

The data transfer is synchronized to the CCLK input. The contents of CI is latched on the rising edges of CCLK, while CO changes on the falling edges of CCLK. When finishing a read or write command, the CLCK must last at least one cycle after the $\overline{CS}$ is set high. During the execution of commands that are followed by output data (read commands), the device will not accept any new commands from CI. The data transfer sequence can be interrupted by setting $\overline{CS}$ high. See Figure 1 and Figure 2 for details.

The clock of the serial control interface (CCLK) is the only reference of the CI and CO pins. Its duty and frequency may not necessarily be standard.

2.1.2 PCM BUS

In MPI mode, the IDT82V1068 provides two flexible PCM buses for all 8 channels. The digital PCM data can be compressed (A/μ-law) or linear format, depending on the DMS bit in Global Command 7. The data rate can be configured as same as the Bit Clock (BCLK) or half of it. The data can be transmitted or received either on the rising edges of BCLK or on falling edges of it. The data transfer time slots can be offset from Frame Synchronization (FS) by 0 BCLK period to 7 BCLK periods. See Figure 3. Global Command 7 makes these selections for all 8 channels.

The PCM data of each channel can be assigned to any time slot of the PCM bus. The number of available time slots is determined by the BCLK frequency. For example, when BCLK is 512 kHz, eight time slots (time slot 0-7) are available; when BCLK is 8.192 MHz, 128 time slots (time slot 0-127) are available. The IDT82V1068 accepts any BCLK frequency between 512 kHz and 8.192 MHz at increment of 64 kHz.

When compressed format (8-bit) is selected, the voice data of one channel occupies one time slot. The TT[6:0] bits in Local Command 7 selects the transmit time slot for each channel, while the RT[6:0] bits in Local Command 8 selects the receive time slot for each channel.

When linear format is selected, the voice data is a 16-bit 2's complement number (b13 to b0 are effective bits, b15 and b14 are the same as the sign bit b13). The voice data of one channel occupies one time slot group consisting of 2 successive time slots. The TT[6:0] bits in Local Command 7 select the transmit time slot group for each channel. For example, if TT[6:0] = 0000000, it means TS0 and TS1 are selected; if TT[6:0] = 0000001, it means TS2 and TS3 are selected. The RT[6:0] bits in Local Command 8 select the receive time slot group for each channel in the same way.

The PCM data for each individual channel is transmitted through the DX1 or DX2 pin on the programmed edges of BCLK, according to time slot assignment. The transmit highway (DX1/2) is selected by the THS bit in Local Command 7. The frame sync (FS) pulse identifies the beginning of a transmit frame (time slot 0). The PCM data is transmitted serially through DX1 or DX2 with MSB first.

The PCM data for each channel is received from the DR1 or DR2 pin on the programmed edges of BCLK, according to time slot assignment. The receive highway (DR1/2) is selected by the RHS bit in Local Command 8. The frame sync (FS) pulse identifies the beginning of a receive frame (time slot 0). The PCM data is received serially from DR1 or DR2 with MSB first.

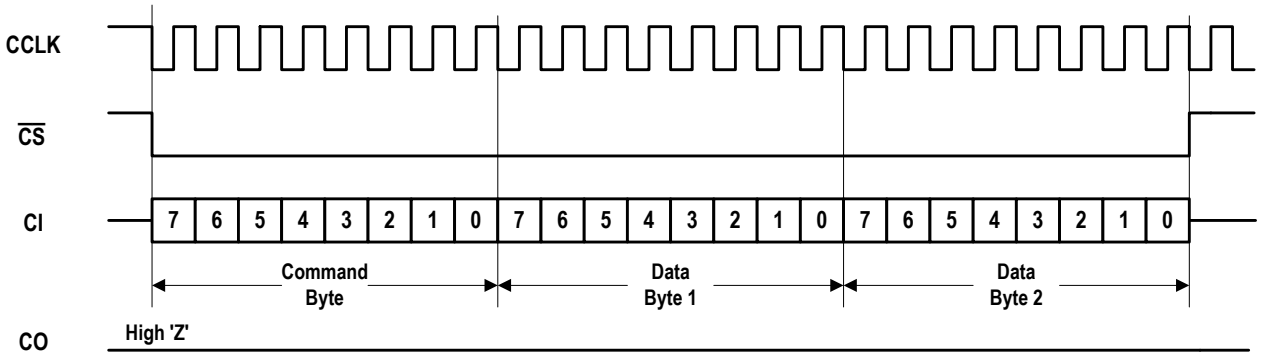


Figure 1 An Example of Serial Interface Write Mode

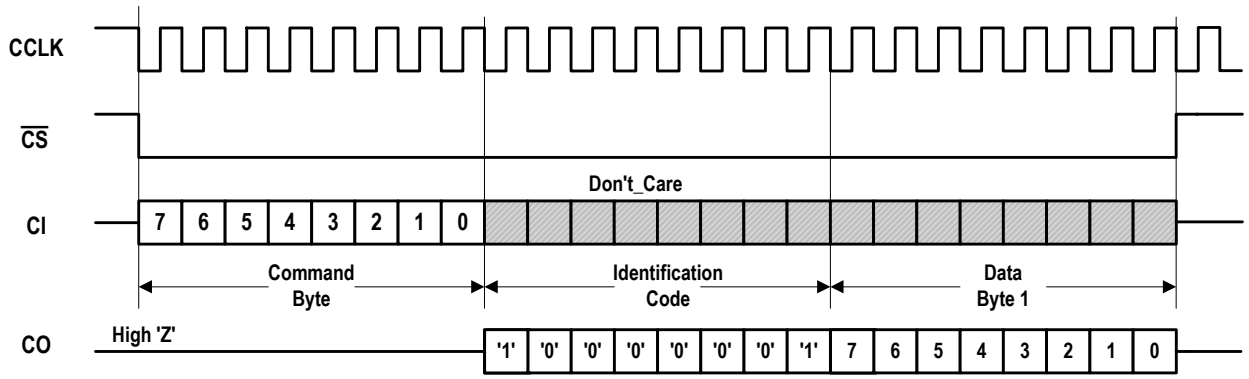


Figure 2 An Example of Serial Interface Read Mode (ID = 81H)

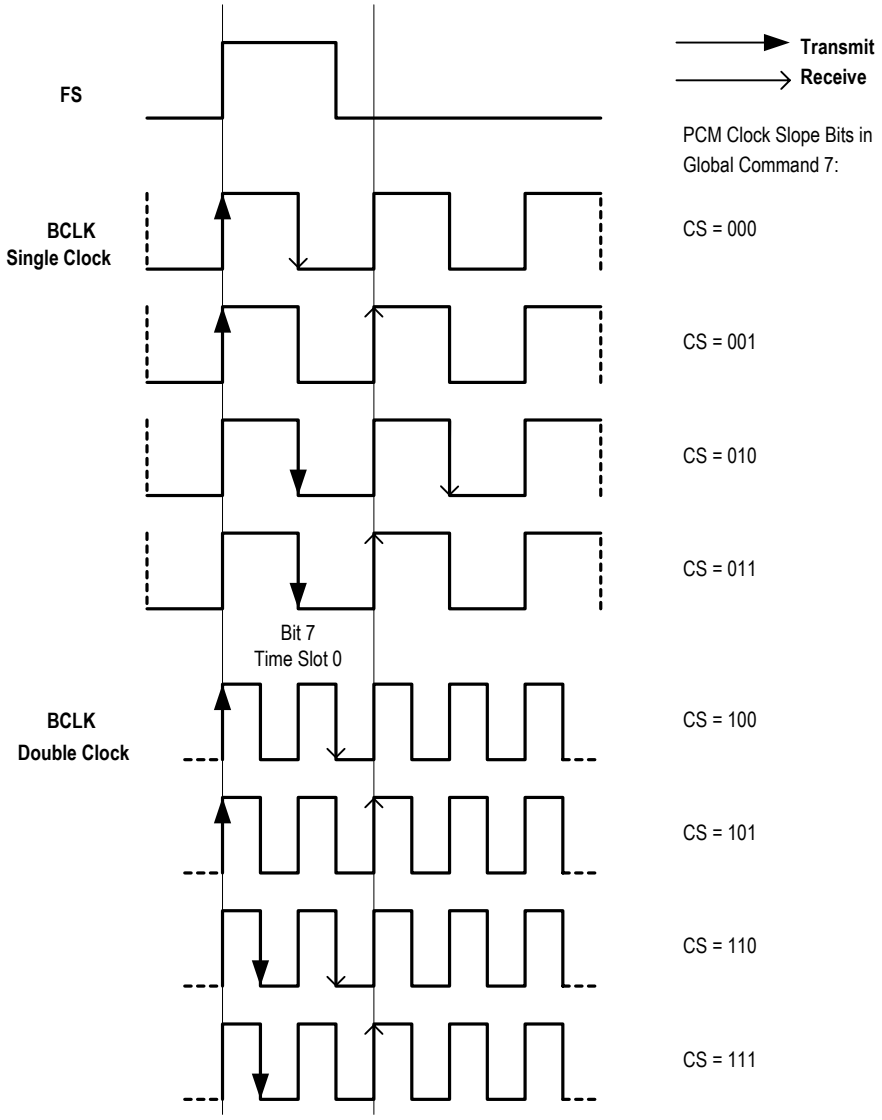


Figure 3 Sampling Edge Select Waveform

2.1.3 GCI MODE

In GCI mode, the GCI interface provides communication of both control and voice data between the GCI bus and the CODEC over a pair of pins (DD and DU). The IDT82V1068 follows the GCI standard where voice and control data for eight channels are combined into one serial bit stream: Data Upstream is sent out via the DU pin and Data Downstream is received via the DD pin. The data transmission is controlled by the Data Clock (DCL) and Frame Synchronization (FSC) signal. The FSC signal identifies the beginning of the transmit/receive frame and all GCI time slots refer to it. The DCL signal can be 2.048MHz or 4.096 MHz, corresponding to logic low and logic high on the DOUBLE pin respectively. The IDT82V1068 adjusts internal timing to accommodate single (2.048 MHz) or double (4.096 MHz) clock rate and keep the data rate in 2.048 MHz. A complete GCI frame is sent upstream via the DU pin and received downstream via the DD pin every 125 µs.

In GCI mode, the IDT82V1068 also supports both compressed and linear voice data formats. A '0' in the DMS bit in Global Command 7 selects the compressed GCI mode while a '1' in this bit selects the linear GCI mode.

2.1.3.1 Compressed GCI Structure

In GCI compressed mode, the data interface logic (upstream/downstream) controls the transmission/reception of data onto/from the GCI bus. One GCI frame consists of 8 GCI time slots, each GCI time slot consists of four bytes as follows:

- Two A-law or µ-law compressed voice data bytes from/to two different channels (named as Channel A and Channel B).
- One Monitor channel byte, which is used for receiving/transmitting control data from/to the master device for Channel A and B;
- One C/I channel byte, which contains a 6-bit wide sub-byte together with an MX bit and an MR bit. All real time signaling information is carried on the C/I channel sub-byte. The MX (Monitor Transmit) bit and MR (Monitor Receive) bits are used for handshaking functions for Channel A and B. Both MX and MR are active low.

Figure 4 shows the overall compressed GCI frame structure.

In compressed GCI mode, four time slots are required to access all eight channels of the IDT82V1068. The GCI time slot assignment is determined by the Time Selection pin TS as illustrated in Table 1.

Table 1 Time Slot Selection for Compressed GCI Mode

IDT82V1068 Channel	TS = 0		TS = 1	
	Time Slot	Voice Channel	Time Slot	Voice Channel
Channel 1	Time Slot 0	A	Time Slot 4	A
Channel 2	Time Slot 0	B	Time Slot 4	B
Channel 3	Time Slot 1	A	Time Slot 5	A
Channel 4	Time Slot 1	B	Time Slot 5	B
Channel 5	Time Slot 2	A	Time Slot 6	A
Channel 6	Time Slot 2	B	Time Slot 6	B
Channel 7	Time Slot 3	A	Time Slot 7	A
Channel 8	Time Slot 3	B	Time Slot 7	B

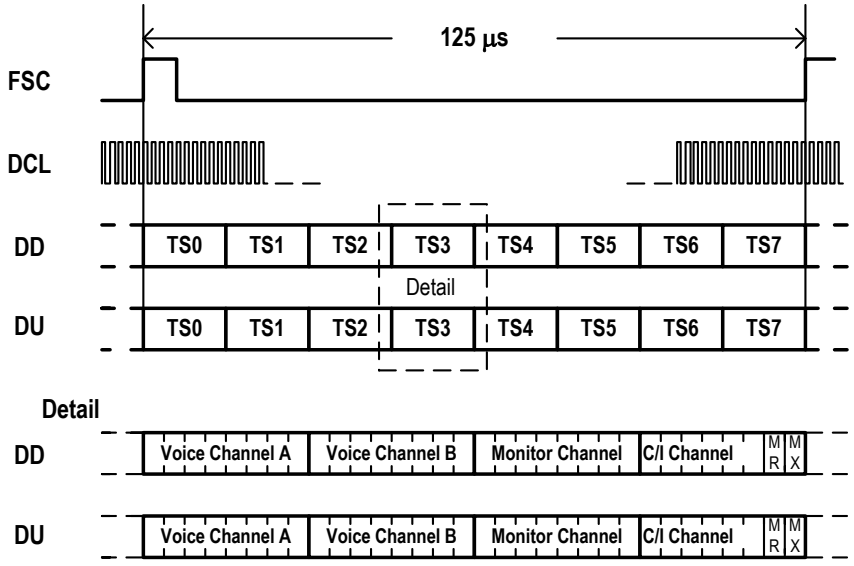


Figure 4 Compressed GCI Frame Structure

2.1.3.2 Linear GCI Structure

In GCI linear mode, one GCI frame consists of 8 GCI time slots, each GCI time slot consists of four bytes. In one GCI frame, four of the 8 time slots are used as Monitor Channel and C/I channel. These four time slots have a common data structure as follows:

- Two don't_care bytes.
- One Monitor Channel byte used for reading/writing control data/ coefficients from/to the device for Channel A and B.
- One C/I byte containing a 6-bit wide sub-byte together with an MX bit and an MR bit. All real time signaling information is carried on the C/I channel sub-byte. The MX (Monitor Transmit) bit and MR (Monitor Receive) bits are used for handshaking functions for Channel A and B. Both MX and MR bits are active low.

Other four GCI time slots are used to transfer the linear voice data (16-bit 2's complement). Each of these time slots consists four bytes: two bytes of linear voice data of Channel A, two bytes of linear voice data of Channel B.

The GCI time slot assignment is determined by the Time Selection pin TS, as shown in Table 2.

In linear GCI mode, total eight GCI time slots are required to access all eight channels of the IDT82V1068. When the TS pin is low, the linear GCI frame structure is as shown in Figure 5.

Table 2 Time Slot Selection for Linear GCI Mode

IDT82V1068 Channel	TS = 0				IDT82V1068 Channel	TS = 1			
	Time Slot	Monitor Channel and C/I Channel	Time Slot	Voice Channel		Time Slot	Monitor Channel and C/I Channel	Time Slot	Voice Channel
Channel 1	Time Slot 0	A	Time Slot 4	A	Channel 1	Time Slot 4	A	Time Slot 0	A
Channel 2	Time Slot 0	B	Time Slot 4	B	Channel 2	Time Slot 4	B	Time Slot 0	B
Channel 3	Time Slot 1	A	Time Slot 5	A	Channel 3	Time Slot 5	A	Time Slot 1	A
Channel 4	Time Slot 1	B	Time Slot 5	B	Channel 4	Time Slot 5	B	Time Slot 1	B
Channel 5	Time Slot 2	A	Time Slot 6	A	Channel 5	Time Slot 6	A	Time Slot 2	A
Channel 6	Time Slot 2	B	Time Slot 6	B	Channel 6	Time Slot 6	B	Time Slot 2	B
Channel 7	Time Slot 3	A	Time Slot 7	A	Channel 7	Time Slot 7	A	Time Slot 3	A
Channel 8	Time Slot 3	B	Time Slot 7	B	Channel 8	Time Slot 7	B	Time Slot 3	B

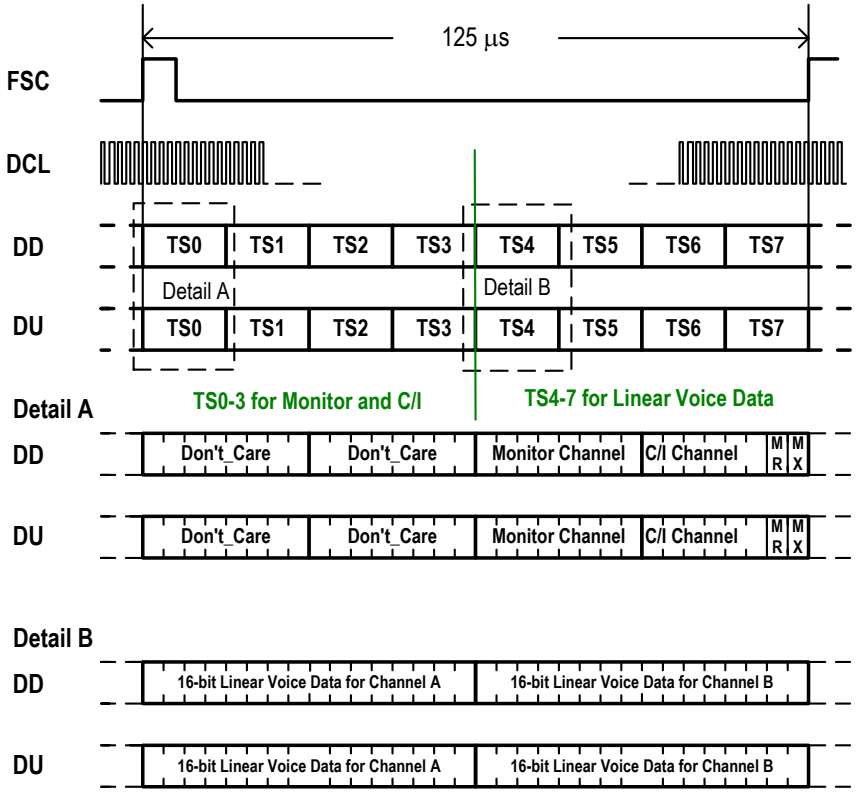


Figure 5 Linear GCI Frame Structure (TS = 0)

2.1.4 C/I CHANNEL

In both compressed GCI and linear GCI modes, the upstream and downstream C/I channel bytes are continuously carrying I/O information every frame to and from the IDT82V1068. In this way, the upstream processor can have an immediate access to the SLIC output data present on IDT82V1068's programmable I/O port on the SLIC side through downstream C/I channel, as well as to the SLIC input data through upstream C/I channel. The IDT82V1068 transmits or receives the C/I channel data with the Most Significant Bit first.

The MR and MX bits are used for handshaking during data exchanges on the monitor channel.

2.1.4.1 Upstream C/I Channel

The C/I Channel byte which includes six C/I bits, is transmitted upstream by the IDT82V1068 every frame. The upstream C/I channel byte is defined as:

Upstream C/I Octet

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0
SI1(A)	SI2(A)	SB1(A)	SI1(B)	SI2(B)	SB1(B)	MR	MX

The logic state data of the input ports SI1 and SI2 for Channel A and Channel B, as well as the bidirectional port SB1 for Channel A and B if SB1 is configured as an input, are transmitted via the upstream C/I channel. If SB2 is configured as input, it can be read by Global Command 12 only.

2.1.4.2 Downstream C/I Channel

The downstream C/I octet is defined as:

Downstream C/I Octet

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0
$\overline{A}$/B	SO3	SO2	SO1	SB1	SB2	MR	MX

Herein, the $\overline{A}$/B bit indicates the control data carried by the b[6:2] bits of the downstream C/I byte is for Channel A or Channel B:

$\overline{A}$/B = 0: for Channel A; $\overline{A}$/B = 1: for Channel B.

The data for controlling the SLIC output ports SO1 to SO3, as well as the SB1 and SB2 when SB1 and SB2 are configured as outputs, are received via the downstream C/I channel.

2.1.5 MONITOR CHANNEL

The monitor channel is used to transfer the configuration or maintenance information between the upstream and downstream devices. The commands of addressing the internal global/local registers and the Coe-/FSK-RAMs are transferred by the monitor channel.

Using two monitor control bits (MR and MX) per direction, the data is transferred in a complete handshake procedure. The MR and MX bits in the C/I Channel of the GCI frame are used for the handshake procedure of the monitor channel. See Figure 6 for details.

The transmission of the monitor channel is operated on a pseudo-asynchronous basis:

- Data transfer (bits) on the bus is synchronized to the FSC signal;
- Data flow (bytes) are asynchronously controlled by the handshake procedure.

For example, the data is placed onto the DD Monitor Channel by the Monitor Transmitter of the master device (DD MX bit is activated and set to '0'). This data transfer will be repeated within each frame (125 µs rate) until it is acknowledged by the IDT82V1068 Monitor Receiver (if the DU MR bit is set to '0', it means that the receipt has been acknowledged). Thus, the data rate is not 8 kbytes/s.

2.1.5.1 Monitor Handshake

The monitor channel works in 3 states:

I. Idle state: A pair of inactive (set to '1') MR and MX bits during two or more consecutive frames shows an idle state on the monitor channel and the End of Message (EOM);

II. Sending state: the MX bit is set to active state ('0') by the Monitor Transmitter, together with data-bytes (can be changed) on the monitor channel;

III. Acknowledging: the MR bit is set to active state (i.e. '0') by the Monitor Receiver, together with a data byte remaining in the monitor channel.

A start of transmission is initiated by the monitor transmitter by sending out an active MX bit together with the first byte of data to be transmitted in the monitor channel. This state remains until the addressed monitor receiver acknowledges the receipt by sending out an active low MR bit. The data transmission is repeated each 125 µs frame (minimum is one repetition). During this time the Monitor Transmitter keeps evaluating the MR bit.

Flow control, means in the form of transmission delay, can only take place when the transmitters MX and the receivers MR bit are in active state.

Since the receiver is able to receive the monitor data at least twice (in two consecutive frames), it is able to check for data errors. If two different bytes are received the receiver will wait for the receipt of two identical successive bytes (last look function).

A collision resolution mechanism (check if another device is trying to send data during the same time) is implemented in the transmitter. This is done by looking for the inactive ('1') phase of the MX bit and making a per bit collision check on the transmitted monitor data (check if transmitted '1's are on the DU/DD line; the DU/DD line are open drain lines).

Any abort leads to a reset of the IDT82V1068 command stack, the device is ready to receive new commands.

To obtain a maximum speed data transfer, the transmitter anticipates the falling edge of the receivers acknowledgment.

Due to the inherent programming structure, duplex operation is not possible. It is not allowed to send any data to the IDT82V1068, while the transmission is active.

Refer to Figure 7 and Figure 8 for more information about the monitor handshake procedure.

The IDT82V1068 can be controlled very flexibly by commands operating on registers or RAMs via the GCI monitor channel, refer to "Programming Description" on page 25 for further details.

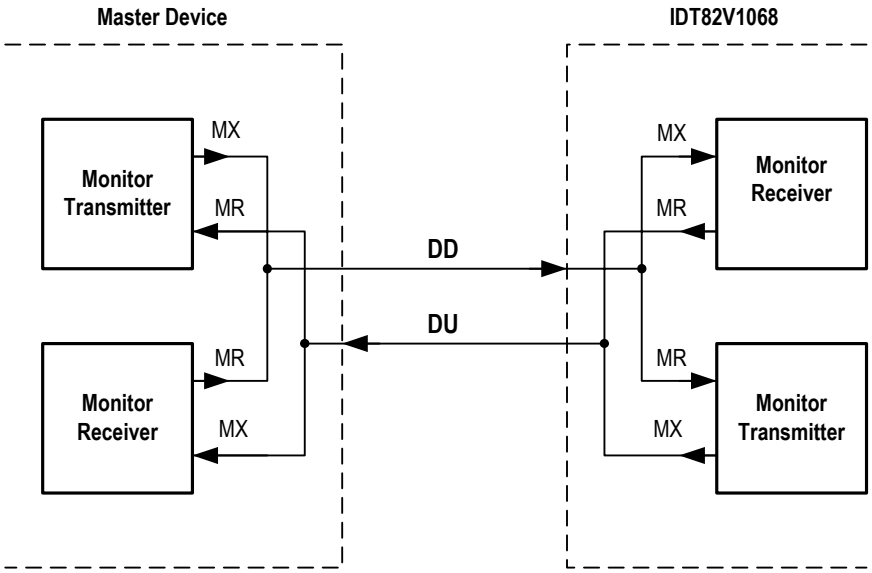
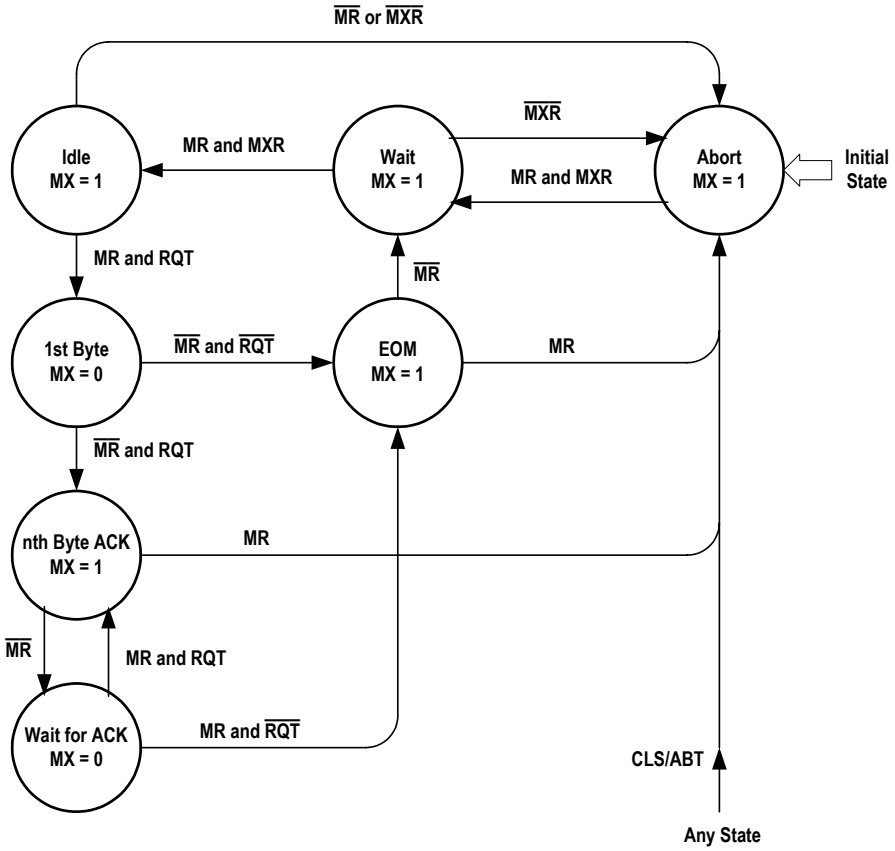
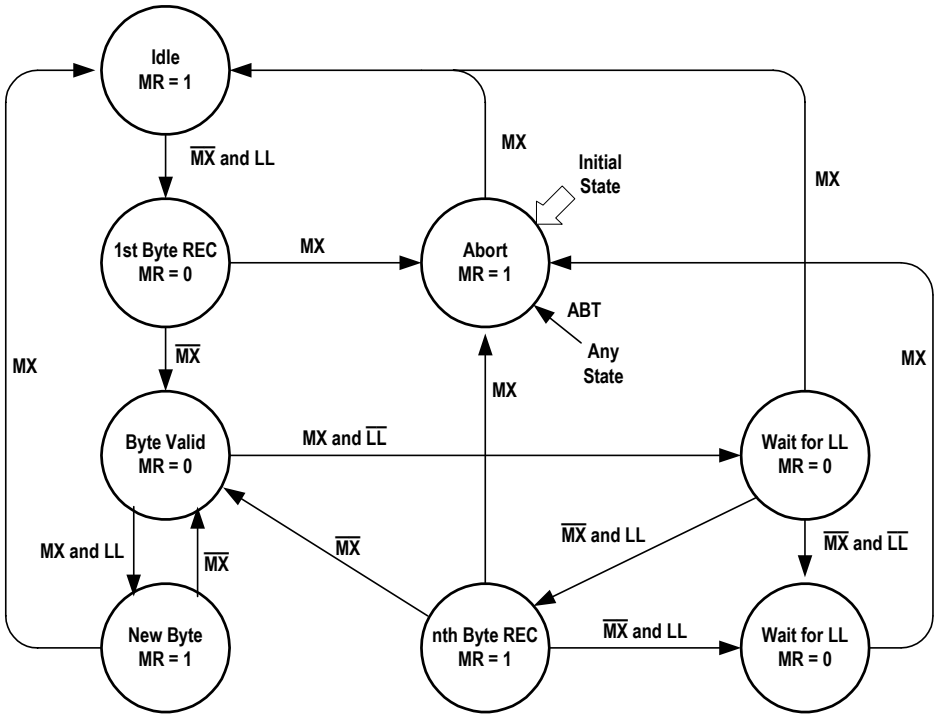


Figure 6 Monitor Channel Operation



MR: MR bit received on DD
MX: MX bit calculated and expected on DU
MXR: MX bit sampled on DU
CLS: Collision within the monitor data byte on DU
RQT: Request for transmission from internal source
ABT: Abort request/indication

Figure 7 State Diagram of the Monitor Transmitter



MR: MR bit calculated and transmitted on DU
MX: MX bit received data downstream (DD)
LL: Last look of monitor byte received on DD
ABT: Abort indication to internal source

Figure 8 State Diagram of the Monitor Receiver

2.2 DSP PROGRAMMING

2.2.1 SIGNAL PROCESSING

Several blocks are programmable for signal processing. This allows to optimize the performance of the IDT82V1068 for the system. Figure 9 shows the signal flow for each channel and indicates the programmable blocks.

The programmable digital filters are used to adjust the transmit/receive gain, realize impedance matching and transhybrid balancing and correct the frequency response. The coefficients of all digital filters can be calculated by a software (Cal48) provided by IDT. If the users provide accurate SLIC model, impedance and gain requirements, the software (Cal48) will then calculate all the coefficients for the relevant filters. When these coefficients are written to the coefficient RAM of the IDT82V1068, the final AC characteristics of the line card (consists of SLIC and CODEC) will meet the ITU-T specifications.

2.2.2 GAIN ADJUSTMENT

The analog gain and digital gain of each channel can be adjusted separately in the IDT82V1068.

For each individual channel, the analog A/D gain of the transmit path can be selected as 0 dB or 6 dB. The selection is done by the A/D Gain bit GAD in Local Command 10. The default analog gain in the transmit path is 0 dB.

For each individual channel, the analog D/A gain of the receive path can be selected as 0 dB or -6 dB. The selection is done by the D/A Gain bit GDA in Local Command 10. The default analog gain in the receive path is 0 dB.

The digital gain of the transmit path (GTX) is programmed from -3 dB to +12 dB with minimum 0.1 dB step. If the CS[5] bit is '0' in Local Command 1, the digital gain of the transmit path is set to the default value. If the CS[5] bit is '1' in Local Command 1, the digital gain of the transmit path is determined by the coefficient in the GTX of the Coe-RAM.

The digital gain of the receive path (GRX) is programmed from -12 dB to +3 dB with minimum 0.1 dB step. If the CS[7] bit is '0' in Local Command 1, the digital gain of the receive path is set to the default value. If the CS[7] bit is '1' in Local Command 1, the digital gain of the receive path is determined by the coefficient in the GRX of the Coe-RAM.

2.2.3 IMPEDANCE MATCHING

Each channel of the IDT82V1068 has a programmable feedback from VIN to VOUT. It synthesizes the two-wire impedance of the SLIC. The Impedance Matching Filter (IMF) and the Gain of Impedance Scaling (GIS) are adjustable and work together to realize impedance matching. If the CS[0] bit in Local Command 1 is '0', the IMF coefficient is set to be default value; if the CS[0] bit is '1', the IMF coefficient is set by the IMF of the Coe-RAM. If the CS[2] bit in Local Command 1 is '0', the GIS coefficient is set to default value; if the CS[2] bit is '1', the GIS coefficient is set by the GIS of the Coe-RAM.

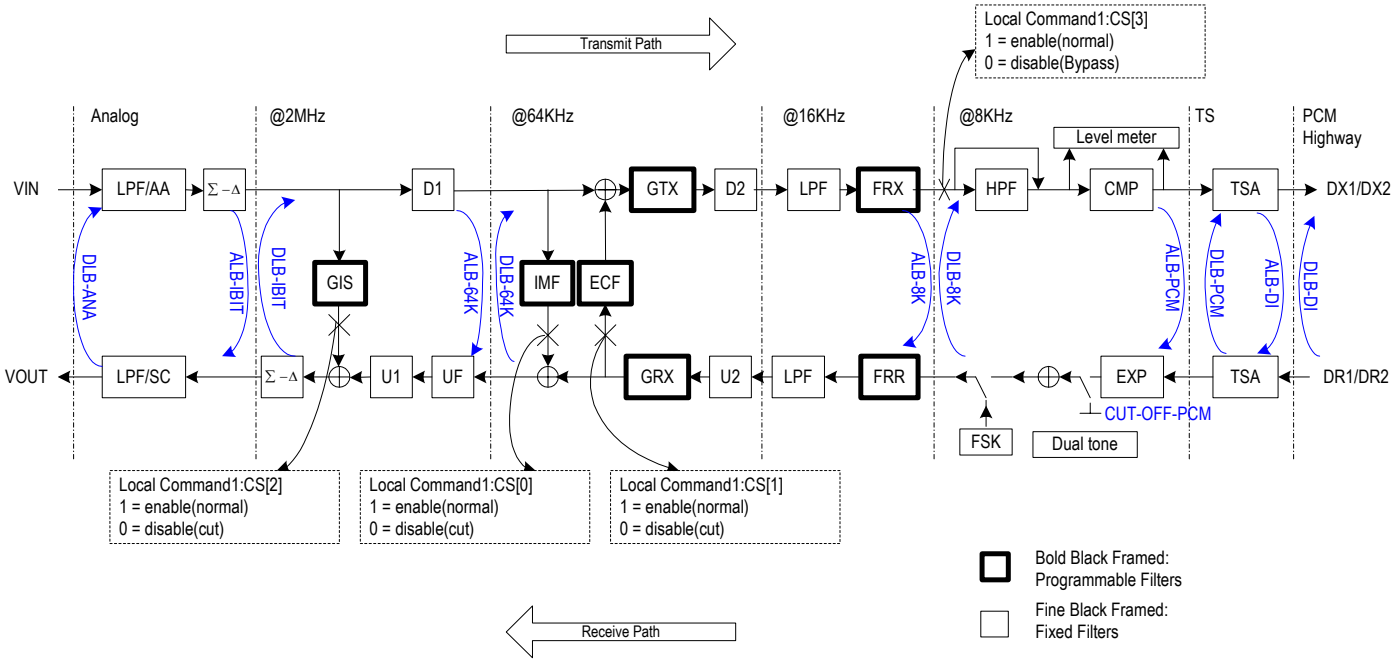
2.2.4 TRANSHYBRID BALANCE

Transhybrid balancing filter is used to adjust transhybrid balance to ensure the echo cancellation meet the ITU-T specifications. The coefficient for Echo Cancellation (ECF) can be programmed. If the CS[1] bit in Local Command 1 is '0', the ECF coefficient is set to default value; if the CS[1] bit is '1', the ECF coefficient is set by the ECF of the Coe-RAM.

2.2.5 FREQUENCY RESPONSE CORRECTION

The IDT82V1068 provides two filters that can be programmed to correct any frequency distortion caused by the impedance matching filter. They are the Frequency Response Correction for Transmit path filter (FRX) and the Frequency Response Correction for Receive path filter (FRR). The coefficients of the FRX filter and the FRR filter are programmable. If the CS[4] bit in Local Command 1 is '0', the FRX coefficient is set to default value; If the CS[4] bit is '1', the FRX coefficient is set by the FRX of the Coe-RAM. If the CS[6] bit in Local Command 1 is '0', the FRR coefficient is set to default value; If the CS[6] bit is '1', the FRR coefficient is set by the FRR of the Coe-RAM.

Refer to Table 11 on page 54 for the Coe-RAM address allocation.



These loopbacks and receive PCM cutoff are controlled by Global Command 26, Local Command 1 and Local Command 2 as shown in the following. Once its corresponding bit in the command is set to 1, the loopback will be enabled.

	MSB							LSB
Global Command 26	ALB_64k	PLLPD	DLB_64k	DLB_ANA	ALB_8k	DLB_8k	DLB_DI	ALB_DI
	MSB							LSB
Local Command 2	IE[3]	IE[2]	IE[1]	IE[0]	CUTOFF	DLB_PCM	ALB_1BIT	DLB_1BIT
	MSB							LSB
Local Command 3	Reserved							ALB_PCM

Figure 9 Signal Flow for Each Channel

Abbreviation List

LPF/AA: Anti-Alias Low-pass Filter
LPF/SC: Smoothing Low-pass Filter
LPF: Low-pass Filter
HPF: High-pass Filter
GIS: Gain for Impedance Scaling
D1: 1st Down Sample Stage
D2: 2nd Down Sample Stage
U1: 1st Up Sample Stage
U2: 2nd Up Sample Stage
UF: Up Sampling Filter (64k-128k)
IMF: Impedance Matching Filter
ECF: Echo Cancellation Filter
GTX: Gain for Transmit Path
GRX: Gain for Receive Path
FRX: Frequency Response Correction for Transmit
FRR: Frequency Response Correction for Receive
CMP: Compression
EXP: Expansion
TSA: Time slot Assignment

2.3 SLIC CONTROL

The IDT82V1068 provides 7 SLIC signaling pins per channel: 2 inputs SI1 and SI2, 2 I/O ports SB1 and SB2 together with 3 outputs SO1, SO2 and SO3.

2.3.1 SI1 AND SI2

In both MPI and GCI modes, the SLIC inputs SI1 and SI2 of all eight channels can be read by Global Command 9 and Global Command 10 respectively. The eight SIA bits in Global Command 9 represent the eight debounced SI1 signals on the corresponding channels, and the eight SIB bits in Global Command 10 represent the eight debounced SI2 signals on the corresponding channels. In this way, the information on SI1 or SI2 of eight channels can be obtained from the IDT82V1068 by applying a read operation. Both SI1 and SI2 can be assigned to off-hook signal, ring trip signal, ground key signal or other signals. These two Global Commands provide for the microprocessor a more efficient way to obtain time-critical data such as on/off-hook and ring trip information.

In MPI mode, the SI1 and SI2 status of each channel can also be read by Local Command 9.

In GCI mode, the SI1 and SI2 status of each channel can be read via the upstream C/I byte. Refer to "Upstream C/I Channel" on page 15 for further details.

2.3.2 SB1 AND SB2

In both MPI and GCI modes, the SLIC I/O pin SB1 of each channel can be configured as an input or an output separately by Global Command 13 (the default direction is input). Each bit in this command corresponds to one channel's SB1 direction. When a bit in this command is set to 0, the SB1 pin of its corresponding channel is configured as an input; when the bit is set to 1, the SB1 pin of its corresponding channel is configured as an output.

The Global Command 14 determines the I/O direction of the SB2 pin of each channel in the same way.

In MPI mode, if SB1 and SB2 are selected as inputs, they can be read globally by Global Command 11 and Global Command 12 respectively, or locally by Local Command 9. The Global Command reads the SB1 or SB2 status for all eight channels, while the Local Command reads the SB1 and SB2 status for each individual channel.

In MPI mode, if SB1 and SB2 are selected as outputs, data can only be written to them by Global Command 11 and Global Command 12 respectively.

In GCI mode, if SB1 and SB2 are selected as inputs, they can be read by Global Command 11 and Global Command 12 respectively. In addition, the SB1 can also be read via the upstream C/I channel octet.

In GCI mode, if SB1 and SB2 are selected as outputs, data can only be written to them via the downstream C/I channel octet.

2.3.3 SO1, SO2 AND SO3

The SLIC outputs SO1, SO2 and SO3 can only be written individually for each channel.

In MPI mode, these three outputs of each channel is written by Local Command 9. When the Local Command 9 executes a read operation, the bits corresponding to SO1 to SO3 will be read out with the data written by the last write operation.

In GCI mode, data can only be written to SO1, SO2 and SO3 through downstream C/I channel octet.

2.4 HARDWARE RING TRIP

In order to prevent the damage caused by high voltage ring signal, the IDT82V1068 offers a hardware ring trip function to respond to the off-hook signal as fast as possible. This function is enabled by setting the RTE bit in Global Command 15.

The off-hook signal can be input via either the SI1 pin or the SI2 pin, while the ring control signal can be output via any of the SO1, SO2, SO3, SB1 and SB2 pins (provided that SB1 and SB2 are configured as outputs). In Global Command 15, the IS bit determines which input is used and the OS[2:0] bits determine which output is used.

When a valid off-hook signal arrives on SI1 or SI2, the IDT82V1068 will turn off the ring signal by inverting the selected output, regardless of the value in the corresponding SLIC output control register (this value should be changed by users later). This function provides a much faster response to off-hook signals than the software ring trip which turns off the ring signal by changing the value of selected output in the corresponding register.

The IPI bit in Global Command 15 is used to indicate the valid polarity of the input. If the off-hook signal is active low, the IPI bit should be set to 0; if the off-hook signal is active high, the IPI bit should be set to 1.

The OPI bit in Global Command 15 is used to indicate the valid polarity of the output. If the ring control signal is required to be low in normal status and high to activate a ring, the OPI bit should be set to 1; if it is required to be high in normal status and low to activate a ring, the OPI bit should be set to 0.

For example, in a system where the off-hook signal is active low and ring control signal is active high, the IPI bit in Global Command 15 should be set to 0 and the OPI bit should be set to 1. In normal status, the selected input (off-hook signal) is high and the selected output (ring control signal) is low. When the ring is activated by setting the output (ring control signal) high, a low pulse appearing on the input (off-hook signal) will inform the device to invert the output to low and cut off the ring signal.

2.5 INTERRUPT AND INTERRUPT ENABLE

An interrupt mechanism is offered in the IDT82V1068 for reading the SLIC input status. Each of SLIC inputs can generate an interrupt when its state is changed.

Any of SI1, SI2, SB1 and SB2 (provided that SB1 and SB2 are configured as inputs) can be interrupt source. As SI1 and SI2 are debounced signals while SB1 and SB2 are not, users should pay more attention when SB1 and SB2 are selected as interrupt sources.

The IDT82V1068 provides an Interrupt Enable Command (Local Command 2) for each interrupt source to enable its interrupt ability. This command contains 4 bits (IE[3:0]) for each channel. Each bit of the IE[3:0] corresponds to one interrupt source of the specific channel. The device will ignore the interrupt signal if its corresponding bit in Interrupt Enable Command is set to 0 (disable).

Multiple interrupt sources can be enabled at the same time. The interrupt sources can only be cleared by executing a read operation of Local Command 9. When Local Command 9 executes a read operation, all 7 interrupt sources of the corresponding channel will be cleared. In addition, when Global Command 2 (interrupt clear command) executes a write operation, the interrupt sources of all eight channels will be cleared.

2.6 CHOPPER CLOCK

The IDT82V1068 offers two programmable chopper clock outputs (CHCLK1 and CHCLK2) that can be used to drive the power supply switching regulators on the SLICs. Both the CHCLK1 and CHCLK2 are synchronous to the MCLK. The CHCLK1 outputs signal with clock cycle programmable from 2ms to 28 ms. The frequency of CHCLK2 can be any of 256 kHz, 512 kHz and 16.384 MHz. The frequency of the chopper clock is selected by Global Command 8.

2.7 DEBOUNCE FILTERS

The IDT82V1068 provides two debounce filter circuits per channel: Debounced Switch Hook (DSH) Filter for SI1 and Ground Key (GK) Filter for SI2 (see Figure 10). They are used to buffer the input signals on SI1 and SI2 pins before changing the state of the SLIC Debounced Input SI1/SI2 Registers (Global Command 9 and 10), or, before changing the state of the GCI upstream C/I octet. The Frame Sync (FS) signal is necessary for both the DSH and the GK filters.

The debounce time of the SI1 input of each channel is programmed by the DSH debounce bits DSH[3:0] in Local Command 4. The DSH filter is initially clocked at half of the frame sync rate (250 µs), and any data changing at this sample rate resets a programmable counter that clocks at the rate of 2 ms. The value of the counter can be from 0 to 30, programmed by DSH[3:0] bits in Local Command 4. The corresponding SIA bit in the SLIC Debounced Input SI1 Register (accessed by Global Command 9) and the corresponding channel's SI1 bit in GCI upstream C/I octet would not be updated with the SI1 input state until the value of the counter is reached. The SI1 bit usually contains the SLIC switch hook status.

The debounce interval of SI2 input of each channel is programmed by the GK Debounce bits GK[3:0] in Local Command 4. The debounced signal will be output to the SIB bit of SLIC Debounced Input SI2 Register (accessed by Global Command 10) and the corresponding channel's SI2 bit in GCI upstream C/I octet. The GK debounce filter consists of an up/down counter that ranges between 0 and 6. This six-state counter is clocked by the GK timer at the sampling period of 0 to 180 ms, as programmed by Local Command 4. When the sampled value is low, the counter is decremented by each clock pulse. When the sampled value is high, the counter is incremented by each clock pulse. Once the counter increments to 6, it will set a latch whose output is routed to the corresponding SIB bit and the GCI upstream C/I octet SI2 bit. If the counter decrements to 0, this latch will be cleared and the output bit will be set to 0. In other cases, the latch, the SIB status and the SI2 bit in GCI upstream C/I octet remain in their previous state without being changed. In this way, at least six consecutive GK clocks with the debounce input remaining at the same state to reflect the output changes.

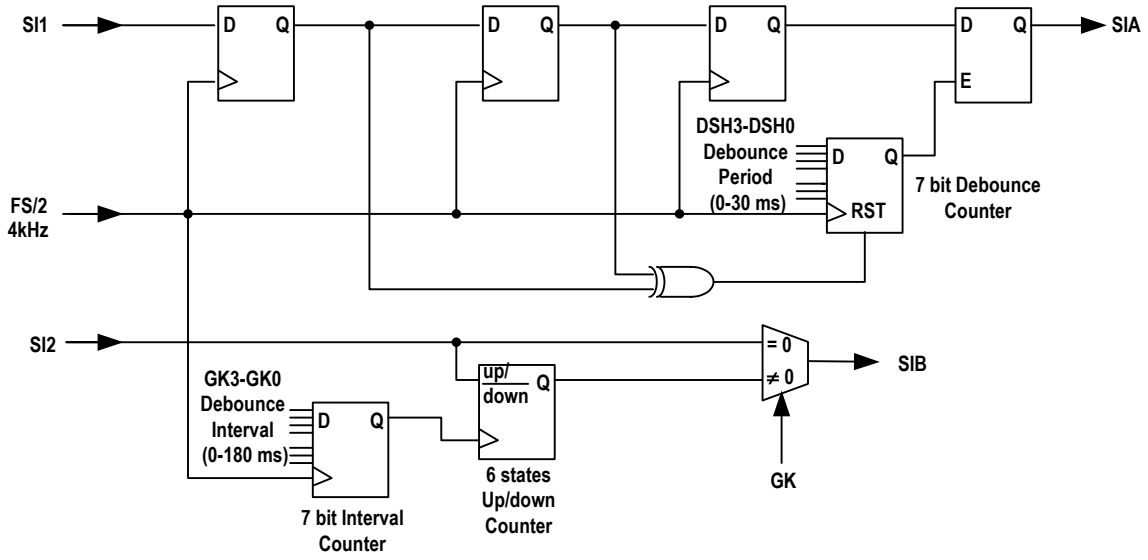


Figure 10 Debounce Filters

2.8 DUAL TONE AND RING GENERATION

Each channel of the IDT82V1068 has two tone generators: Tone 0 and Tone1. The dual tone generators can generate a gain-adjustable dual tone signal and output it to the VOUT pin. The generated dual tone signals can be used as test signals, DTMF, dial tone, busy tone, congestion tone and Caller-ID Alerting Tone etc.

The generators Tone 0 and Tone 1 of each channel can be enabled or disabled independently by the T0E and T1E bits in Local Command 6. The frequency of the tones is programmable from 1 Hz to 4.095 kHz with 4095 steps. Local Command 5 provides 12 bits for each tone generator to set the frequency.

The gain of the generated dual tone signals of each channel is programmed by the TG[5:0] bits in Local Command 6, in the range of -3 dB to -39 dB. The gain of each tone is calculated by the following formula:

$$G = 20 \times \lg (Tg \times 2/256) + 3.14$$

where, Tg is the decimal value of TG[5:0].

The Dual Tone Output Invert bit (TOI) in Global Command 19 is used to invert the output tone signal. When it is 0', it means no inversion; when it is 1', the output tone signal will be inverted.

The ring signal is a special signal generated by the dual tone generators. When only one tone generator is enabled or both tone

generators generate the same tone, and the frequency of the tone is set as the ring signal required (10 Hz to 100 Hz), a ring signal will be output to the VOUT pin.

2.9 FSK SIGNAL GENERATION

The IDT82V1068 has four FSK generators for sending Caller-ID FSK signals. Any FSK generator can be assigned to any one of the eight channels. Before programming the FSK generator, the Global Command 25 must be used first to specify one or more FSK generators to be configured.

2.9.1 CONFIGURE THE FSK GENERATORS

The general procedure of sending a Caller-ID signal is shown in Figure 11.

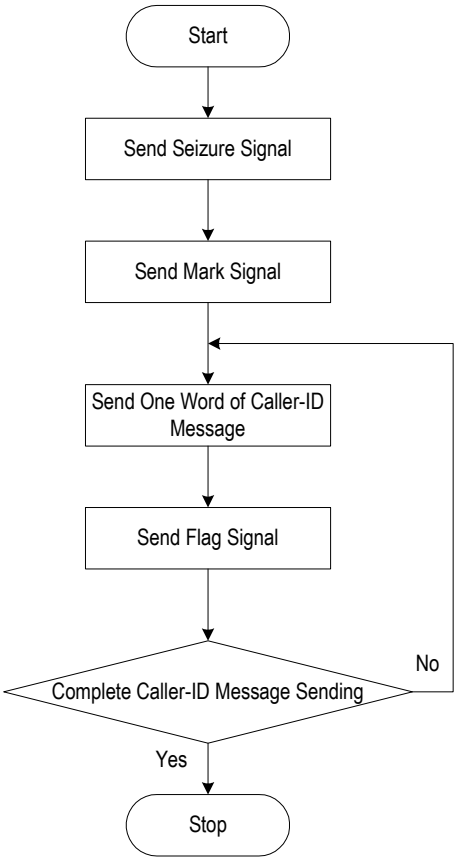


Figure 11 General Procedure of Sending Caller-ID Signal

The Seizure Signal is a series of '01' patterns. The Global Command 22 determines how many '01' patterns will be used as the Seizure Signal. Note that if the Global Command 22 sets 5 (d), the bit length of the Seizure Signal will be 10 (d) bits.

The Mark Signal is a series of '1'. The length of the Mark Signal is determined by the Global Command 23.

One 'Word' of the Caller-ID message consists of 10 bits: one Start Bit at the beginning, one Stop Bit at the end and eight bits of Caller-ID message in the middle. For the IDT82V1068, the eight bits of Caller-ID message are from the FSK-RAM, and the Start Bit/Stop Bit will be added automatically when sending the Caller-ID message.

The Flag Signal is a series of '1'. The length of the Flag Signal is determined by the Global Command 23.

The FMS (FSK Mode Selection) bit in the Global Command 24 determines the specifications of FSK Caller-ID signals. The IDT82V1068 supports both Bellcore 202 and BT standards. Table 3 is the comparison of these two standards.

Table 3 BT/Bellcore Standard of FSK Signal

Item	BT	Bellcore
Mark (1) frequency	1300 Hz ± 1.5%	1300 Hz ± 1.1%
Space (0) frequency	2100 Hz ± 1.1%	2200 Hz ± 1.1%
Transmission rate	1200 baud ± 1%	1200 Hz ± 1%
Word format	1 start bit which is '0', 8 word bits (with least significant bit LSB first), 1 stop bit which is '1'.	1 start bit which is '0', 8 word bits (with least significant bit LSB first), 1 stop bit which is '1'.

The MAS (Mark After Send) bit in the Global Command 24 determines whether to keep on sending a series of '1's after the completion of sending the content in the FSK-RAM. For each FSK generator, the size of the corresponding FSK-RAM is 64 bytes. If the total Caller-ID message is larger than 64 bytes, the MAS bit should be set to '1' to hold the link after the first 64 bytes of Caller-ID message have been sent. So, users can update the FSK-RAM with new data and send the new data without re-sending the Seizure Signal and Mark Signal. This is important to keep the integrity of Caller-ID information.

The FCS[2:0] (FSK Channel Selection) bits in the Global Command 24 are used to select which one of the eight channels will be used to send the FSK signal. The FO bit in the Global Command 24 is used to enable/disable the FSK generator. When all the configurations and FSK-RAM updating have been completed, the FS (FSK Start) bit in the Global Command 24 is used to trigger the sending of FSK signal.

A recommended procedure of programming the FSK generators is shown in the Figure 12.

2.9.2 FSK-RAM

The contents of Caller-ID message are stored in the FSK-RAM. There are four blocks of FSK-RAM, corresponding to the four FSK generators. The size of each block of FSK-RAM is 64 bytes. The address and the programming method of these four FSK-RAM are exactly the same (refer to "Addressing the FSK-RAM" on page 26 for details). So, before programming the FSK-RAM, the Global Command 25 must be used first to determine which one of the four FSK-RAM blocks will be accessed.

2.9.3 BROADCASTING MODE FOR FSK CONFIGURATION

If more than one FSK generators are selected in the Global Command 25, the subsequential FSK commands (FSK generator configuration commands and FSK-RAM programming commands) will be effective for all the selected FSK generators. This is the Broadcasting mode for FSK generator configuration.

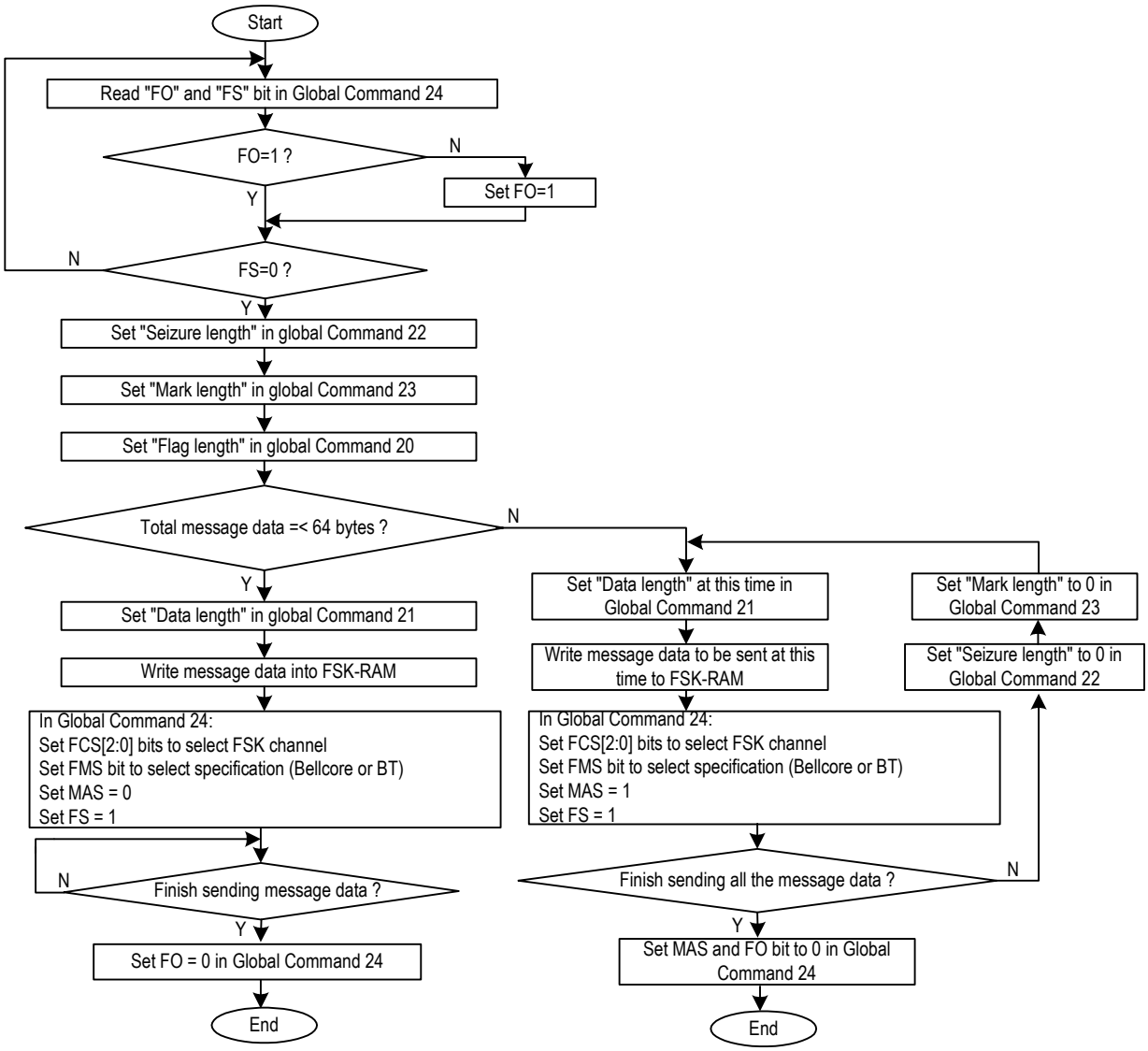


Figure 12 A Recommended Programming Flow Chart for FSK Generator

2.10 LEVEL METERING

The IDT82V1068 has a level meter shared by all 8 signal channels. The level meter is designed to emulate the off-chip PCM test equipment to facilitate the line-card, subscriber line and user telephone set monitoring. The level meter tests the returned signal and reports the measurement result via the MPI/GCI interface. When combined with the dual tone generators and the loopbacks, this allows the microprocessor to test channel integrity. The CS[2:0] bits in Global Command 19 select the channel on which the signal will be metered.

The level metering function is enabled by setting the LMO bit to 1 in Global Command 19. A Level Meter Counter register is provided for this function. It can be accessed by Global Command 18. This register is used to configure the number of time cycles for the sampling PCM data (8 kHz sampling rate). The output of the level metering will be sent to the Level Meter Result Low and Level Meter Result High registers (Global Command 16 and 17). The LMRL register contains the lower 7 bits of the output and a data-ready bit (DRLV), the LMRH register contains the higher 8 bits of the output. An internal accumulator sums the rectified samples until the number configured by Level Meter Counter register is reached. By then, the DRLV bit is set to 1 and accumulation result is latched into the LMRL and LMRH registers simultaneously.

Once the LMRH register is read, the DRLV bit will be reset. The DRLV bit will be set to high again when a new data is available. The contents in LMRL and LMRH will be overwritten by later metering result if they are not read out yet. To read the Level Metering result register, it is highly recommended to read LMRL first.

The L/C bit in Global Command 19 determines the mode of level meter operation. When the L/C bit is 1, the level meter will measure the linear PCM data. If the DRLV bit is 1, the measure result will be output to LMRL and LMRH. When the L/C bit is 0, the compressed PCM will be output transparently to LMRH.

The calculation and method of level metering will be described in Application Note.

2.11 CHANNEL POWER DOWN/STANDBY MODE

Each individual channel of the IDT82V1068 can be powered down independently by Local Command 10. When the channel is powered down (enters standby mode), the PCM data transmission and reception together with the D-to-A and A-to-D conversions are disabled. In this way, the power consumption of the device can be reduced. When the IDT82V1068 is powered up or reset, all eight channels will be powered down. All circuits that contain programmed information retain their data when powered down. In MPI mode, the microprocessor interface is always active so that new command could be received and executed. In GCI mode, the monitor channel of any time slot is always on so that new command could be accepted at any time.

2.12 POWER DOWN PLL/SUSPEND MODE

A suspend mode is offered to the whole chip to save power. In this mode, the PLL block is turned off and the DSP operation is disabled. This mode saves much more power consumption than the standby mode. In this mode, only Global Commands and Local Commands can be executed. The RAM operation is disabled as the internal clock has been turned off. The PLL block is powered down by Global Command 26. The suspend mode can be entered by powering down the PLL blocks and all channels.

3 OPERATING DESCRIPTION

3.1 PROGRAMMING DESCRIPTION

The IDT82V1068 can be programmed very flexibly via the serial control interface (MPI mode) or via the GCI monitor channel (GCI mode). In both MPI and GCI modes, the programming is realized by writing commands to registers or RAMs on the chip. In MPI mode, the command data is transmitted/received via the CI/CO pin. In GCI mode, the command data is sent/received via the DD/DU pin.

3.1.1 BROADCASTING MODE FOR MPI PROGRAMMING

A broadcasting mode is provided in MPI write-operation (not allowed in read operation). Each channel has its own enable bit (CE[0] to CE[7] in Global Register 6) to allow individual channel programming. If more than one Channel Enable bit is high (enable) or all Channel Enable bits are high, all the corresponding channels will be enabled and can receive the programming information. Therefore, a broadcasting mode can be implemented by simply enabling all the channels in the device to receive the programming information. The Broadcasting mode is very useful when initializing the IDT82V1068 (setting coefficients, for example) in a large system.

3.1.2 IDENTIFICATION CODE FOR MPI MODE

In MPI mode, the IDT82V1068 provides an Identification Code to distinguish itself from other device of the system. When being read, the IDT82V1068 first outputs an Identification Code of 81H to indicate that the following data is from the IDT82V1068, then outputs the data bytes. Refer to Table 5 and Table 6 on page 27 for details.

3.1.3 PROGRAM START BYTE FOR GCI MODE

The IDT82V1068 uses the monitor channel to exchange the status or mode information with the high level processors. The messages transmitted in the monitor channel have different data structures. For a complete command operation, the first byte of monitor channel data indicates the address of the device either sending or receiving the data. All monitor channel messages to/from the IDT82V1068 begin with the following Program Start (PS) byte:

b7	b6	b5	b4	b3	b2	b1	b0
1	0	0	$\overline{A}$/B	0	0	0	1

Because one monitor channel is shared by two voice data channels, the $\overline{A}$/B bit is necessary to be used in the PS byte to identify the two channels (named as Channel A and Channel B).

$\overline{A}$/B = 0: means that Channel A is the source (upstream) or destination (downstream) -81H;

$\overline{A}$/B = 1: means that Channel B is the source (upstream) or destination (downstream) -91H.

The Program Start byte is followed by a command (global/local command or RAM command) byte. For Global Commands, the $\overline{A}$/B bit in the PS byte will be ignored. If the command byte specifies a write, there may be 1 to 16 additional data bytes follows (1-4 bytes for registers, 1-16 bytes for RAM). If the command byte specifies a read, additional data bytes may follow. The IDT82V1068 responds to the read command by sending up to 16 data bytes upstream containing the information requested by the upstream controller. Each byte on monitor channel must be transferred at least twice and in two consecutive frames.

3.1.4 IDENTIFICATION COMMAND FOR GCI MODE

In order to distinguish different devices unambiguously by software, a two byte identification command (8000H) is defined for analog lines GCI devices:

1	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0

Each device will then respond with its specific identification code. For the IDT82V1068, this two byte identification code is 8082H:

1	0	0	0	0	0	0	0
1	0	0	0	0	0	1	0

3.1.5 COMMAND TYPE AND FORMAT

The IDT82V1068 provides three types of register/RAM commands for both MPI and GCI modes, they are:

Local Command (LC): used to access the Local Registers. There are 14 Local Registers per channel.

Global Command (GC): used to access the Global Registers. There are total 26 Global Registers shared by all eight channels.

RAM Command (RC): used to access the Coe-RAM and the FSK-RAM. There are 40 words (divided into 5 blocks) Coe-RAM for each channel, each word has 14 valid bits. The IDT82V1068 provides four FSK generators shared by all eight channels. There are 32 words (divided into 4 blocks) FSK-RAM for each FSK generator, each word has 16 bits.

The format of the commands is as the following:

b7	b6	b5	b4	b3	b2	b1	b0
$\overline{R}$/W	CT		Address				

$\overline{R}$/W: Read/Write Command bit
- b7 = 0: Read Command
- b7 = 1: Write Command

CT: Command Type
- b6 b5 = 00: Local Command
- b6 b5 = 01: Global Command
- b6 b5 = 10: Not Allowed
- b6 b5 = 11: RAM Command

Address: The b[4:0] bits specify a register(s) or a RAM location(s) to be addressed.

For both Local Commands and Global Commands, the b[4:0] bits are used to address the Local Registers or Global Registers.

For RAM Commands, the b4 bit is used to specify if the Coe-RAM or the FSK RAM is to be addressed:

b4 = 0: addressing the Coe-RAM

b4 = 1: addressing the FSK-RAM

When addressing the Coe-RAM, the b[3:0] bits are used to specify a block in the Coe-RAM. When addressing the FSK-RAM, the b3 bit is always '0' and the b[2:0] bits are used to specify a block in the FSK-RAM.

3.1.6 ADDRESSING LOCAL REGISTER

In MPI mode, when using Local Commands, the Channel Enable Command (Global Command 6) must be used first to specify which channel will be addressed, then the Local Commands follows. If Global Command 6 enables more than one channel, all the channels enabled will be addressed by one Local Command at one time.

In GCI mode, both the location of the time slot (determined by the TS pin) and the b4 bit in Program Start Byte would indicate which channel to be addressed.

The b[4:0] bits in a Local Command determine which one of the Local Registers of the selected channel(s) will be addressed.

The IDT82V1068 provides a consecutive adjacent addressing method for reading/writing the Local Registers. According to the value of the b[1:0] bits specified in a Local Command, there will be 1 to 4 adjacent local registers that will be read/written automatically with the highest order first. For example, if the b[1:0] bits specified in the Local Command is '11', 4 adjacent registers will be addressed by this Command. If b[1:0] = '10', 3 adjacent registers will be addressed. Refer to Table 4 for details.

Table 4 Consecutive Adjacent Addressing

Address Specified in Local Commands					In/Out Data	Registers to Be Addressed
b4	b3	b2	b1	b0		
X	X	X	1	1 (b1b0 = 11, 4 bytes of data)	Byte 1	XXX11
					Byte 2	XXX10
					Byte 3	XXX01
					Byte 4	XXX00
X	X	X	1	0 (b1b0 = 10, 3 bytes of data)	Byte 1	XXX10
					Byte 2	XXX01
					Byte 3	XXX00
X	X	X	0	1 (b1b0 = 01, 2 bytes of data)	Byte 1	XXX01
					Byte 2	XXX00
X	X	X	0	0 (b1b0 = 00, 1 byte of data)	Byte 1	XXX00

In MPI mode, when the $\overline{CS}$ pin becomes low, the IDT82V1068 treats the first byte on the CI pin as a command byte, and the rest byte(s) as data byte(s). To write another command, the $\overline{CS}$ pin must be changed from low to high to finish the previous command and then changed from high to low to indicate the start of the next command. When a read/write operation is completed, the $\overline{CS}$ pin must be pulled to high in 8-bit time.

In MPI mode, the procedure of the consecutive adjacent addressing can be stopped by the $\overline{CS}$ signal at any time. When the $\overline{CS}$ pin is changed from low to high, the operation on the current register and the next adjacent registers will be aborted. But the results of the previous operation are still remained.

In GCI mode, the procedure of the consecutive adjacent addressing can not be stopped once a command is initiated. For write command, the number of bytes following the command must be as same as the number of registers being written.

3.1.7 ADDRESSING THE GLOBAL REGISTERS

The address of the 27 Global Registers is as the following:
00000 - 11001 (Global Register 1- 26)
11100 (Global Register 27)

It should be noted that the address of Global Register 27 is 11100 and not 11010, because the address space from 11010 to 11011 are reserved.

For the adjacent 26 Global Registers, the IDT82V1068 also provides a consecutive adjacent addressing for read/write operation, as it does for the Local Registers. In MPI mode, the procedure of the consecutive adjacent addressing for Global Registers can also be stopped by the $\overline{CS}$ signal at any time. But in GCI mode, the procedure can not be stopped once a command is initiated. For the 27th Global Register (address is 11100), once a read/write procedure is completed, the $\overline{CS}$ pin must be pulled to high. It should be noted that, in GCI mode, the Global Command for all 8 channels can be transferred via any GCI time slot.

3.1.8 ADDRESSING THE COE-RAM

The IDT82V1068 provides 40 words of Coe-RAM for each channel. They are divided into 5 blocks, each block contains 8 words. The 5 blocks are:

- IMF RAM (Word 0 - Word 7), containing the Impedance Matching Filter coefficient;
- ECF RAM (Word 8 - Word 15), containing the Echo Cancellation Filter coefficient;
- GIS RAM (Word 16 - Word 23), containing the Gain of Impedance Scaling;
- FRX RAM (Word 24 - Word 30) and GTX RAM (Word 31), containing the coefficients for the Frequency Response Correction in Transmit Path and Gain in Transmit Path;
- FRR RAM (Word 32 - Word 38) and GRX RAM (Word 39), containing the coefficients for the Frequency Response Correction in Receive Path and Gain in Receive Path.

Refer to Table 11 on page 54 for the Coe-RAM address allocation.

Each word in the Coe-RAM is 14-bit (b[13:0]) wide. To write a Coe-RAM word, 16 bits (b[15:0]) (or, two 8-bit bytes) are needed to fulfill with MSB first, but the lowest two bits (b[1:0]) will be ignored. When being read, each Coe-RAM word will output 16 bits with MSB first, but the last two bits (b[1:0]) are meaningless.

In MPI mode, when addressing the Coe-RAM, Global Command 6 (Channel Enable) must be used first to specify the channel(s), then the address (b[4:0]) in the following RAM Command will indicate which block of the Coe-RAM of the specified the channel(s) will be addressed.

In GCI mode, both the location of time slot (determined by the TS pin) and the b4 bit in the Program Start Byte will indicate which channel will be addressed.

The address in a Coe-RAM Command locates a block of the Coe-RAM. That is, when executing a Coe-RAM Command, all 8 words in the specified block will be addressed automatically, with the highest order word first.

In MPI mode, when reading/writing a Coe-RAM block, the addressing procedure can be stopped by the $\overline{CS}$ signal at any time. When the $\overline{CS}$ signal is changed from low to high, the operation on the current word and the next adjacent words will be aborted. But the results of the previous operation are still remained.

3.1.9 ADDRESSING THE FSK-RAM

The IDT82V1068 provides four FSK generators shared by all eight channels. Four FSK-RAMs are provided for the four FSK generators respectively. Before accessing the FSK-RAM, the Global Command 25 must be used first to specify one or more FSK generator(s), then the

corresponding FSK-RAM(s) will be addressed.

Each FSK-RAM consists of 4 blocks. Each block has eight 16-bit words. So, one FSK-RAM consists of 64 bytes.

To write a FSK-RAM word, 16 bits (or, two 8-bit bytes) are needed to fulfill with MSB first**.** When being read, each word will output 16 bits with MSB first.

Only the b[2:0] bits in a FSK-RAM Command are needed to specify one of the 4 blocks in FSK-RAM, the b3 bit should always be 0, the b4 bit should always be 1 to indicate the command is for the FSK-RAM.

The way of addressing the FSK-RAM is similar to that of addressing the Coe-RAM. When the address of a FSK-RAM block is specified in a FSK-RAM Command, all 8 words in this block will be read/written automatically, with the highest order word first.

In MPI mode, when reading/writing a FSK-RAM block, the addressing procedure can be stopped by the $\overline{CS}$ signal at any time. When the $\overline{CS}$ pin is changed from low to high, the operation on the current word and the next adjacent words will be aborted. But this will not change the results of the previous operation.

3.1.10 EXAMPLES OF MPI COMMANDS

Examples of the Local Command, Global Command, Coe-RAM Command and FSK-RAM Command in MPI mode are shown in Table 5, Table 6, Table 7 and Table 8 respectively.

Table 5 Local Command Transmission Sequence in MPI Mode

Data Transmitted On the CI Pin	Data Received on the CO Pin
Global Command 6 (Channel Program Enable Byte) Local Command byte, write Data byte 1 . . . Data byte m* Global Command 6 (Channel Program Enable byte) Local Command byte, read	 Identification Code (81H) Data byte 1 . . . Data byte m*

Table 6 Global Command Transmission Sequence in MPI Mode

Data Transmitted On the CI Pin	Data Received on the CO Pin
Global Command byte, write Data byte 1 . . . Data byte m* Global Command byte, read	 Identification Code (81H) Data byte 1 . . . Data byte m*

Table 7 Coe-RAM Command Transmission Sequence in MPI Mode

Data Transmitted On the CI Pin	Data Received on the CO Pin
Global Command 6 (Channel Program Enable Byte) Coe-RAM Command byte, write Data word 1 (high byte, low byte**) Data word 2 (high byte, low byte) . . . Data word 8 (high byte, low byte) Global Command 6 (Channel Program Enable byte) Coe-RAM Command byte, read	 Identification Code (81H) Data word 1 (high byte, low byte**) Data word 2 (high byte, low byte) . . . Data word 8 (high byte, low byte)

Table 8 FSK-RAM Command Transmission Sequence in MPI Mode

Data Transmitted On the CI Pin	Data Received on the CO Pin
FSK-RAM Command byte, write Data word 1 (high byte, low byte**) Data word 2 (high byte, low byte) . . . Data word 8 (high byte, low byte) FSK-RAM Command byte, read	 Identification Code (81H) Data word 1 (high byte, low byte**) Data word 2 (high byte, low byte) . . . Data word 8 (high byte, low byte)

3.1.11 EXAMPLES OF GCI COMMANDS

Examples of the Local/Global Command and Coe-RAM/FSK-RAM Command in GCI mode are shown in Table 9 and Table 10, respectively.

Table 9 Local/Global Command Transmission Sequence in GCI Mode

GCI Monitor Channel	
Downstream	**Upstream**
Program Start byte (81H/91H) Local/Global Command byte, write Data byte 1 . . . Data byte m* Program Start byte (81H/91H) Local/Global Command byte, read	 Program Start byte (81H/91H) Data byte 1 . . . Data byte m*

Table 10 Coe-RAM/FSK-RAM Command Transmission Sequence in GCI Mode

GCI Monitor Channel	
Downstream	**Upstream**
Program Start byte (81H/91H) Coe-RAM/FSK-RAM Command byte, write Data word 1 (high byte, low byte**) Data word 2 (high byte, low byte) . . . Data word 8 (high byte, low byte) Program Start byte (81H/91H) Coe-RAM/FSK-RAM Command byte, read	 Program Start byte (81H/91H) Data word 1 (high byte, low byte**) Data word 2 (high byte, low byte) . . . Data word 8 (high byte, low byte)

Notes:

* The number of the data bytes can be 1, 2, 3 or 4, depending on the two bits 'b1b0' in the Local/Global Command.

** When addressing the Coe-RAM, the data word is 14-bit wide, the lowest two bits in the low byte of each word are ignored. When addressing the FSK-RAM, the data word is 16-bit wide.

3.2 POWER-ON SEQUENCE

To power on the IDT82V1068, users should follow the sequence below:

1. Apply ground first;
2. Apply VCC, finish signal connections and set the $\overline{\text{RESET}}$ pin to low, thus the device goes into the default state;
3. Set the $\overline{\text{RESET}}$ pin to high;
4. Select master clock frequency;
5. Program filter coefficients and other parameters as required.

3.3 DEFAULT STATE AFTER RESET

When the IDT82V1068 is powered on, or reset either by setting the $\overline{\text{RESET}}$ pin to logic low for at least 50 µs or by the GCI/MPI Command, the device will enter the default state as described below:

1. All eight channels are powered down and enter standby mode;
2. All loopbacks and cutoff are disabled;
3. The DX1/DU pin is selected for all channels to transmit data, the DR1/DD pin is selected for all channels to receive data;
4. The master clock frequency is assumed to be 2.048 MHz;
5. For MPI mode, the transmit and receive time slots are set to 0-7 for channel 1-8 respectively. The PCM data rate is as same as the BCLK frequency. Data is transmitted on the rising edges and received on the falling edges of the BCLK signal;
   For GCI mode, the time slots for transmitting and receiving are determined by the TS pin. the data rate is determined by the DOUBLE pin. The DD/DU clocks data on the rising edges of the DCL signal.
6. A-Law is selected;
7. The coefficients of FRX, FRR, GTX and GTR filters are set to default values. The analog gains are set to 0 dB. The IMF, GIS and ECF filters are disabled. The HPF filter is enabled (Refer to Figure 9 for more information about the filters);
8. The SB1 and SB2 pins are configured as inputs;
9. The SI1 and SI2 pins are configured as no debounce pins;
10. All interrupts are disabled, all pending interrupts are cleared;
11. All feature function blocks including FSK generators, dual tone generators, ring trip and level metering are turned off;
12. The CHCLK1 and CHCLK2 outputs are set to high.

The data stored in the RAMs will not be changed by any kind of reset operations. In this way, the RAM data will not be lost unless the device is powered down physically.

3.4 COMMAND LIST

In the following global and local commands lists, it should be noted that:
1. R/W = 0, Read command; R/W = 1, Write command.
2. The reserved bit(s) in the command must be filled in '0' in write operation and will be ignored in read operation.
3. The global or local commands described below are available for both MPI and GCI modes except for those with special statement.

3.4.1 GLOBAL COMMANDS LIST

GC1: Revision Number, Read (20H); No Operation, Write (A0H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	R/W	0	1	0	0	0	0	0

When applying a read operation, the revision number of the IDT82V1068 will be read out by executing this command. The default revision number is 1(d).

When applying a write operation, nothing will be done by this command. But a data byte of FFH must follow the write command to ensure proper operation.

GC2: Interrupt Clear, Write Only (A1H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	1	0	1	0	0	0	0	1
I/O Data	1	1	1	1	1	1	1	1

All interrupts will be cleared by this command. When applying this command, a data byte of FFH must follow to ensure proper operation.

GC3: Software Reset, Write Only (A2H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	1	0	1	0	0	0	1	0
I/O Data	1	1	1	1	1	1	1	1

This command resets all Local Registers, but does not reset the Global Registers and the RAMs. When executing this command, a data byte of FFH must follow to ensure proper operation.

GC4: Hardware Reset, Write Only (A3H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	1	0	1	0	0	0	1	1
I/O Data	1	1	1	1	1	1	1	1

The action of this command is equivalent to pulling the RESET pin to low (Refer to "Default State After Reset" on page 29 for more information about the reset operation).
Note that when executing this command, a data byte of FFH must follow to ensure proper operation.

GC5: MCLK Frequency Selection, Read/Write (24H/A4H) (This command is available for MPI mode only)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	R/W	0	1	0	0	1	0	0
I/O Data	Reserved				Sel[3]	Sel[2]	Sel[1]	Sel[0]

In MPI mode, this command is used to select the master clock (MCLK) frequency. The default frequency is 2.048 MHz.
Sel[3:0] = 0000: 8.192 MHz
Sel[3:0] = 0001: 4.096 MHz
Sel[3:0] = 0010: 2.048 MHz (default)

Sel[3:0] = 0110: 1.536 MHz
Sel[3:0] = 1110: 1.544 MHz
Sel[3:0] = 0101: 3.072 MHz
Sel[3:0] = 1101: 3.088 MHz
Sel[3:0] = 0100: 6.144 MHz
Sel[3:0] = 1100: 6.176 MHz
(In GCI mode, the MCLK frequency as same as the DCL frequency, which is 2.048 MHz or 4.096 MHz, depending on the logic level of the CI/DOUBLE pin. Refer to "Pin Description" on page 7 for further details.)

GC6: Channel Program Enable, Read/Write (25H/A5H). (This command is available for MPI mode only.)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	0	0	1	0	1
I/O Data	CE[7]	CE[6]	CE[5]	CE[4]	CE[3]	CE[2]	CE[1]	CE[0]

The Channel Program Enable command is used to specify the channel(s) before Local Commands or a Coe-RAM Commands are used. This command byte provides one bit per channel to indicate if the corresponding channel will receive Local Commands and Coe-RAM Commands.
CE[0] = 0: Disabled, Channel 1 will not receive Local Commands and Coe-RAM Commands (default);
CE[0] = 1: Enabled, Channel 1 will receive Local Commands and Coe-RAM Commands.
CE[1] = 0: Disabled, Channel 2 will not receive Local Commands and Coe-RAM Commands (default);
CE[1] = 1: Enabled, Channel 2 will receive Local Commands and Coe-RAM Commands.
CE[2] = 0: Disabled, Channel 3 will not receive Local Commands and Coe-RAM Commands (default);
CE[2] = 1: Enabled, Channel 3 will receive Local Commands and Coe-RAM Commands.
CE[3] = 0: Disabled, Channel 4 will not receive Local Commands and Coe-RAM Commands (default);
CE[3] = 1: Enabled, Channel 4 will receive Local Commands and Coe-RAM Commands.
CE[4] = 0: Disabled, Channel 5 will not receive Local Commands and Coe-RAM Commands (default);
CE[4] = 1: Enabled, Channel 5 will receive Local Commands and Coe-RAM Commands.
CE[5] = 0: Disabled, Channel 6 will not receive Local Commands and Coe-RAM Commands (default);
CE[5] = 1: Enabled, Channel 6 will receive Local Commands and Coe-RAM Commands.
CE[6] = 0: Disabled, Channel 7 will not receive Local Commands and Coe-RAM Commands (default);
CE[6] = 1: Enabled, Channel 7 will receive Local Commands and Coe-RAM Commands.
CE[7] = 0: Disabled, Channel 8 will not receive Local Commands and Coe-RAM Commands (default);
CE[7] = 1: Enabled, Channel 8 will receive Local Commands and Coe-RAM Commands.

GC7: PCM Data Offset, PCM Clock Slope, Data Mode Select, and A/μ-Law Select, Read/Write (26H/A6H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	0	0	1	1	0
I/O Data	LS	DMS	CS[2]	CS[1]	CS[0]	DO[2]	DO[1]	DO[0]

The PCM Data Offset bits (DO[2:0]) determine the PCM data transmit/receive time slots will be offset from the Frame Synchronous (FS) signal by how many BCLK periods. (For MPI mode only)
DO[2:0] = 000: offset from the FS signal by 0 BCLK period (default);
DO[2:0] = 001: offset from the FS signal by 1 BCLK period;
DO[2:0] = 010: offset from the FS signal by 2 BCLK periods;
DO[2:0] = 011: offset from the FS signal by 3 BCLK periods;
DO[2:0] = 100: offset from the FS signal by 4 BCLK periods;
DO[2:0] = 101: offset from the FS signal by 5 BCLK periods;
DO[2:0] = 110: offset from the FS signal by 6 BCLK periods;
DO[2:0] = 111: offset from the FS signal by 7 BCLK periods.

The CS[2] bit is used to select the clock mode (single or double). If single clock is selected, the data rate will be as same as the BCLK frequency. If double clock is selected, the data rate will be half of the BCLK frequency. (For MPI mode only)
CS[2] = 0: single clock is selected (default);
CS[2] = 1: double clock is selected;

The PCM Clock Slope (CS[1:0]) bits determine the PCM data will be transmitted and received on which edges of the BCLK signal. (For MPI mode only)

CS[1:0] = 00: The PCM data is transmitted on the rising edges of BCLK and received on the falling edges of BCLK (default);
CS[1:0] = 01: The PCM data is transmitted on the rising edges of BCLK and received on the rising edges of BCLK;
CS[1:0] = 10: The PCM data is transmitted on the falling edges of BCLK and received on the falling edges of BCLK;
CS[1:0] = 11: The PCM data is transmitted on the falling edges of BCLK and received on the rising edges of BCLK.

The Data Mode Select bit (DMS) determines the coding format of the voice data. (For both MPI and GCI modes)

DMS = 0: compressed code (default);
DMS = 1: linear code.

A/μ-law Select bit (LS) selects A-law or μ-law. (For both MPI and GCI modes)

LS = 0: A-law (default);
LS = 1: μ-law.

GC8: Chopper Clock Selection, Read/Write (27H/A7H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	0	0	1	1	1
I/O Data	Reserved		CHCLK2_SEL[1]	CHCLK2_SEL[0]	CHCLK1_SEL[3]	CHCLK1_SEL[2]	CHCLK1_SEL[1]	CHCLK1_SEL[0]

The CHCLK1_SEL[3:0] bits configure the programmable output pin CHCLK1.
CHCLK1_SEL[3:0] = 0000: CHCLK1 outputs 1 permanently (default);
CHCLK1_SEL[3:0] = 0001: CHCLK1 outputs a digital signal at the frequency of 1000/2 Hz;
CHCLK1_SEL[3:0] = 0010: CHCLK 1 outputs a digital signal at the frequency of 1000/4 Hz;
CHCLK1_SEL[3:0] = 0011: CHCLK1 outputs a digital signal at the frequency of 1000/6 Hz;
CHCLK1_SEL[3:0] = 0100: CHCLK1 outputs a digital signal at the frequency of 1000/8 Hz;
CHCLK1_SEL[3:0] = 0101: CHCLK 1 outputs a digital signal at the frequency of 1000/10 Hz;
CHCLK1_SEL[3:0] = 0110: CHCLK1 outputs a digital signal at the frequency of 1000/12 Hz;
CHCLK1_SEL[3:0] = 0111: CHCLK1 outputs a digital signal at the frequency of 1000/14 Hz;
CHCLK1_SEL[3:0] = 1000: CHCLK 1 outputs a digital signal at the frequency of 1000/16 Hz;
CHCLK1_SEL[3:0] = 1001: CHCLK1 outputs a digital signal at the frequency of 1000/18 Hz;
CHCLK1_SEL[3:0] = 1010: CHCLK1 outputs a digital signal at the frequency of 1000/20 Hz;
CHCLK1_SEL[3:0] = 1011: CHCLK 1 outputs a digital signal at the frequency of 1000/22 Hz;
CHCLK1_SEL[3:0] = 1100: CHCLK1 outputs a digital signal at the frequency of 1000/24 Hz;
CHCLK1_SEL[3:0] = 1101: CHCLK1 outputs a digital signal at the frequency of 1000/26 Hz;
CHCLK1_SEL[3:0] = 1110: CHCLK 1 outputs a digital signal at the frequency of 1000/28 Hz;
CHCLK1_SEL[3:0] = 1111: CHCLK1 outputs 0 permanently.

The CHCLK2_SEL[1:0] bits configure the programmable output pin CHCLK2.
CHCLK2_SEL[1:0] = 00: CHCLK2 outputs 1 permanently (default);
CHCLK2_SEL[1:0] = 01: CHCLK2 outputs a digital signal at the frequency of 256 kHz;
CHCLK2_SEL[1:0] = 10: CHCLK2 outputs a digital signal at the frequency of 512 kHz;
CHCLK2_SEL[1:0] = 11: CHCLK2 outputs a digital signal at the frequency of 16.384 MHz.

GC9: SLIC Debounce Input SI1, Read Only (28H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	0	0	1	0	1	0	0	0
I/O Data	SIA[7]	SIA[6]	SIA[5]	SIA[4]	SIA[3]	SIA[2]	SIA[1]	SIA[0]

The SIA[7:0] bits are the debounced versions of the pins SI1_8 to SI1_1. The SIA[7:0] bits contain the SLIC status information received by the SLIC interface pins SI1_8 to SI1_1 respectively. See Figure 10 on page 21 for details.

SIA[0]: debounced data of SI1 on Channel 1 (default value is 0);
SIA[1]: debounced data of SI1 on Channel 2 (default value is 0);
SIA[2]: debounced data of SI1 on Channel 3 (default value is 0);
SIA[3]: debounced data of SI1 on Channel 4 (default value is 0);

SIA[4]: debounced data of SI1 on Channel 5 (default value is 0);
SIA[5]: debounced data of SI1 on Channel 6 (default value is 0);
SIA[6]: debounced data of SI1 on Channel 7 (default value is 0);
SIA[7]: debounced data of SI1 on Channel 8 (default value is 0).

GC10: SLIC Debounce Input SI2, Read Only (29H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	0	0	1	0	1	0	0	1
I/O Data	SIB[7]	SIB[6]	SIB[5]	SIB[4]	SIB[3]	SIB[2]	SIB[1]	SIB[0]

The SIB[7:0] bits are the debounced versions of the pins SI2_8 to SI2_1. The SIB[7:0] bits contain the SLIC ground key status information received by the SLIC interface pins SI2_8 to SI2_1 respectively.
SIB[0]: debounced data of SI2 on Channel 1 (default value is 0);
SIB[1]: debounced data of SI2 on Channel 2 (default value is 0);
SIB[2]: debounced data of SI2 on Channel 3 (default value is 0);
SIB[3]: debounced data of SI2 on Channel 4 (default value is 0);
SIB[4]: debounced data of SI2 on Channel 5 (default value is 0);
SIB[5]: debounced data of SI2 on Channel 6 (default value is 0);
SIB[6]: debounced data of SI2 on Channel 7 (default value is 0);
SIB[7]: debounced data of SI2 on Channel 8 (default value is 0).

GC11: SLIC Real-time SB1 Data, Read/Write (2AH/AAH)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	0	1	0	1	0
I/O Data	SB1[7]	SB1[6]	SB1[5]	SB1[4]	SB1[3]	SB1[2]	SB1[1]	SB1[0]

The SB1[7:0] bits contain the information of the SLIC bidirectional pins SB1_8 to SB1_1 respectively.
SB1[0]: SB1 data on Channel 1 (default value is 0);
SB1[1]: SB1 data on Channel 2 (default value is 0);
SB1[2]: SB1 data on Channel 3 (default value is 0);
SB1[3]: SB1 data on Channel 4 (default value is 0);
SB1[4]: SB1 data on Channel 5 (default value is 0);
SB1[5]: SB1 data on Channel 6 (default value is 0);
SB1[6]: SB1 data on Channel 7 (default value is 0);
SB1[7]: SB1 data on Channel 8 (default value is 0).

GC12: SLIC Real-time SB2 Data, Read/Write (2BH/ABH)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	0	1	0	1	1
I/O Data	SB2[7]	SB2[6]	SB2[5]	SB2[4]	SB2[3]	SB2[2]	SB2[1]	SB2[0]

The SB2[7:0] bits contain the information of the SLIC bidirectional pins SB2_8 to SB2_1 respectively.
SB2[0]: SB2 data on Channel 1 (default value is 0);
SB2[1]: SB2 data on Channel 2 (default value is 0);
SB2[2]: SB2 data on Channel 3 (default value is 0);
SB2[3]: SB2 data on Channel 4 (default value is 0);
SB2[4]: SB2 data on Channel 5 (default value is 0);
SB2[5]: SB2 data on Channel 6 (default value is 0);
SB2[6]: SB2 data on Channel 7 (default value is 0);
SB2[7]: SB2 data on Channel 8 (default value is 0).

GC13: SB1 Direction Selection, Read/Write (2CH/ACH)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	0	1	1	0	0
I/O Data	SB1C[7]	SB1C[6]	SB1C[5]	SB1C[4]	SB1C[3]	SB1C[2]	SB1C[1]	SB1C[0]

The SB1C[7:0] bits configure the directions of the SLIC interface pins SB1_8 to SB1_1 respectively.
SB1C[0] = 0: SB1 pin on Channel 1 is configured as input (default);
SB1C[0] = 1: SB1 pin on Channel 1 is configured as output;
SB1C[1] = 0: SB1 pin on Channel 2 is configured as input (default);
SB1C[1] = 1: SB1 pin on Channel 2 is configured as output;
SB1C[2] = 0: SB1 pin on Channel 3 is configured as input (default);
SB1C[2] = 1: SB1 pin on Channel 3 is configured as output;
SB1C[3] = 0: SB1 pin on Channel 4 is configured as input (default);
SB1C[3] = 1: SB1 pin on Channel 4 is configured as output;
SB1C[4] = 0: SB1 pin on Channel 5 is configured as input (default);
SB1C[4] = 1: SB1 pin on Channel 5 is configured as output;
SB1C[5] = 0: SB1 pin on Channel 6 is configured as input (default);
SB1C[5] = 1: SB1 pin on Channel 6 is configured as output;
SB1C[6] = 0: SB1 pin on Channel 7 is configured as input (default);
SB1C[6] = 1: SB1 pin on Channel 7 is configured as output;
SB1C[7] = 0: SB1 pin on Channel 8 is configured as input (default);
SB1C[7] = 1: SB1 pin on Channel 8 is configured as output.

GC14: SB2 Direction Selection, Read/Write (2DH/ADH)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	0	1	1	0	1
I/O Data	SB2C[7]	SB2C[6]	SB2C[5]	SB2C[4]	SB2C[3]	SB2C[2]	SB2C[1]	SB2C[0]

The SB2C[7:0] bits configure the directions of the SLIC interface pins SB2_8 to SB2_1 respectively.
SB2C[0] = 0: SB2 pin on Channel 1 is configured as input (default);
SB2C[0] = 1: SB2 pin on Channel 1 is configured as output;
SB2C[1] = 0: SB2 pin on Channel 2 is configured as input (default);
SB2C[1] = 1: SB2 pin on Channel 2 is configured as output;
SB2C[2] = 0: SB2 pin on Channel 3 is configured as input (default);
SB2C[2] = 1: SB2 pin on Channel 3 is configured as output;
SB2C[3] = 0: SB2 pin on Channel 4 is configured as input (default);
SB2C[3] = 1: SB2 pin on Channel 4 is configured as output;
SB2C[4] = 0: SB2 pin on Channel 5 is configured as input (default);
SB2C[4] = 1: SB2 pin on Channel 5 is configured as output;
SB2C[5] = 0: SB2 pin on Channel 6 is configured as input (default);
SB2C[5] = 1: SB2 pin on Channel 6 is configured as output;
SB2C[6] = 0: SB2 pin on Channel 7 is configured as input (default);
SB2C[6] = 1: SB2 pin on Channel 7 is configured as output;
SB2C[7] = 0: SB2 pin on Channel 8 is configured as input (default);
SB2C[7] = 1: SB2 pin on Channel 8 is configured as output;

GC15: SLIC Ring Trip Setting, Read/Write (2EH/AEH)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	0	1	1	1	0
I/O Data	OPI	Reserved	IPI	IS	RTE	OS[2]	OS[1]	OS[0]

The Output Selection bits OS[2:0] determine which output pin will be selected as the ring control signal source.
OS[2:0] = 000 - 010: not defined;
OS[2:0] = 011: SB1 is selected (when SB1 is configured as an output);

OS[2:0] = 100: SB2 is selected (when SB2 is configured as an output);
OS[2:0] = 101: SO1 is selected;
OS[2:0] = 110: SO2 is selected;
OS[2:0] = 111: SO3 is selected.

The Ring Trip Enable bit RTE enables or disables the ring trip function block.
RTE = 0: the ring trip function block is disabled (default);
RTE = 1: the ring trip function block is enabled.

The Input Selection bit IS determines which input will be selected as the off-hook indication signal source.
IS = 0: SI1 is selected (default);
IS = 1: SI2 is selected.

The Input Polarity Indicator bit IPI indicates the valid polarity of input.
IPI = 0: active low (default);
IPI = 1: active high.

The Output Polarity Indicator bit OPI indicates the valid polarity of output.
OPI = 0: the selected output pin changing from high to low will activate the ring (default);
OPI = 1: the selected output pin changing from low to high will activate the ring.

GC16: Level Meter Result Low Register, Read Only (30H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	0	0	1	1	0	0	0	0
I/O Data	LMRL[7]	LMRL[6]	LMRL[5]	LMRL[4]	LMRL[3]	LMRL[2]	LMRL[1]	DRLV

This register contains the lower 8 bits of the level meter result with the default value of '0000-0000'. The DRLV bit is the active high data_ready bit. To read the level meter result, users should read the low register first, then read the high register (LMRH[7:0]). Once the high register is read, the DRLV bit will be cleared immediately.

GC17: Level Meter Result High Register, Read Only (31H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	0	0	1	1	0	0	0	1
I/O Data	LMRH[7]	LMRH6]	LMRH[5]	LMRH[4]	LMRH[3]	LMRH[2]	LMRH[1]	LMRH[0]

This register contains the higher 8 bits of the level meter result. The default value of this register is 0(d).

GC18: Level Meter Counter, Read/Write (32H/B2H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	1	0	0	1	0
I/O Data	CN[7]	CN[6]	CN[5]	CN[4]	CN[3]	CN[2]	CN[1]	CN[0]

The level meter counter register is used to configure the number of time cycles for sampling the PCM data.
CN[7:0] = 0 (d): the linear or compressed PCM data is output to registers LMRH and LMRL directly (default);
CN[7:0] = N: The PCM data is sampled for N * 125 µS (N from 1 to 255).

GC19: Level Meter Channel Select, Level Meter Mode Select, Level Meter On/off and Dual Tone Output Invert, Read/Write (33H/B3H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	1	0	0	1	1
I/O Data	Reserved	TOI	Reserved	LMO	L/C	CS[2]	CS[1]	CS[0]

The level meter Channel Select bits (CS[2:0]) are used to select a channel, data on which will be level metered.
CS[2:0] = 000: Channel 0 is selected (default);

CS[2:0] = 001: Channel 1 is selected;
CS[2:0] = 010: Channel 2 is selected;
CS[2:0] = 011: Channel 3 is selected;
CS[2:0] = 100: Channel 4 is selected;
CS[2:0] = 101: Channel 5 is selected;
CS[2:0] = 110: Channel 6 is selected;
CS[2:0] = 111: Channel 7 is selected.

The level meter Mode Select bit (L/C) determines the mode of level meter operation.
L/C = 0: Message mode is selected. The compressed PCM data will be output to the level meter result register LMRH transparently (default);
L/C = 1: Meter mode is selected. The linear PCM data will be metered and output to the level meter result registers LMRH and LMRL when the data_ready bit DRLV is '1'.

The level meter On/off bit (LMO) enables the level meter.
LMO = 0: Level meter is disabled (default);
LMO = 1: Level meter is enabled.

The Dual Tone Output Invert bit (TOI) determines whether the output tone signal will be inverted or not.
TOI = 0: The output tone signal will not be inverted (default);
TOI = 1: The output tone signal will be inverted.

GC20: FSK Flag Length, Read/Write (34H/B4H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	1	0	1	0	0
I/O Data	FL[7]	FL[6]	FL[5]	FL[4]	FL[3]	FL[2]	FL[1]	FL[0]

The Flag Length bits (FL[7:0]) determine the number of the flag bits '1' that will be transmitted between the transmission of the message bytes. The value of FL[7:0] is valid from 0 to 255(d). The default value is 0(d). If 0(d) is selected, no flag signal will be sent.

GC21: FSK Data Length, Read/Write (35H/B5H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	1	0	1	0	1
I/O Data	WL[7]	WL[6]	WL[5]	WL[4]	WL[3]	WL[2]	WL[1]	WL[0]

Data Length bits (WL[7:0]) determine the number of all the data bytes that will be transmitted except the flag signal. The value is valid from 0 to 64(d). Any value larger than 64(d) will be taken as 64(d).
The default value of this register is 0(d). When 0(d) is selected, none of the word data will be sent out. When the Mark After Send bit MAS in Global Command 24 is set to 1, the mark signal will be sent after the data bytes in the FSK-RAM have been sent out. When the MAS bit is set to 0, the mark signal will not be sent after the data bytes in the FSK-RAM have been sent out.

GC22: FSK Seizure Length, Read/Write (36H/B6H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	1	0	1	1	0
I/O Data	SL[7]	SL[6]	SL[5]	SL[4]	SL[3]	SL[2]	SL[1]	SL[0]

The Seizure Length bits (SL[7:0]) determine the number of '01' pairs that represent the seizure phase. The Seizure Length is two times of the value set in the SL[7:0] bits. The value of the SL[7:0] bits is valid from 0 to 255(d), corresponding to the Seizure Length of 0 to 510(d). The default value is 0(d). When 0(d) is selected, no seizure signal will be sent.

GC23: FSK Mark Length, Read/Write (37H/B7H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	1	0	1	1	1
I/O Data	ML[7]	ML[6]	ML[5]	ML[4]	ML[3]	ML[2]	ML[1]	ML[0]

The Mark Length bits (ML[7:0]) determine the number of the mark bits '1' that will be transmitted in the initial flag phase. The value of the ML[7:0] bits is valid from 0 to 255(d). The default value is 0(d). When 0(d) is selected, no mark signal will be sent.

GC24: FSK Start, Mark After Send, FSK Mode Select, FSK Channel Select and FSK On/Off, Read/Write (38H/B8H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	1	1	0	0	0
I/O Data	FO	FSC[2]	FCS[1]	FCS[0]	Reserved	FMS	MAS	FS

The FSK Start bit (FS) is used to initiate the FSK signal transmission. It will be cleared to the default value of '0' after the data bytes in the FSK-RAM have been sent out. If the Seizure Length, Mark Length together with the Data Length are set to 0(d), the FSK Start bit will be reset to 0 immediately after it is set to 1.

The Mark After Send bit (MAS) determine the FSK block operation after the data bytes in the FSK-RAM have been sent out.
MAS = 0: The output will be muted after sending out all data bytes in the FSK-RAM (default);
MAS = 1: After sending out all data bytes in the FSK-RAM, the IDT82V1068 keeps sending a series of '1' until the MAS bit is set to 0 and the FS bit is set to 1.

The FSK Mode Select bit (FMS) is used to select the FSK modulation specification.
FMS = 0: Bellcore specification is selected (default);
FMS = 1: BT specification is selected.

The FSK Channel Select bits (FCS[2:0]) selects a channel on which the FSK operation will be implemented. Channel 1 to Channel 4 are the default selections for the FSK generator 1 to generator 4 respectively.
FCS[2:0] = 000: Channel 0 is selected (default);
FCS[2:0] = 001: Channel 1 is selected;
FCS[2:0] = 010: Channel 2 is selected;
FCS[2:0] = 011: Channel 3 is selected;
FCS[2:0] = 100: Channel 4 is selected;
FCS[2:0] = 101: Channel 5 is selected;
FCS[2:0] = 110: Channel 6 is selected;
FCS[2:0] = 111: Channel 7 is selected.

The FSK On/Off (FO) enables or disables the whole FSK function block.
FO = 0: The FSK function block is disabled (default);
FO = 1: The FSK function block is enabled.

GC25: FSK Generator Selection, Read/Write (39H/B9H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	1	1	0	0	1
I/O Data	Reserved				FSK_G4	FSK_G3	FSK_G2	FSK_G1

The FSK Generator Selection bits (FSK_G1 to FSK_G4) determine which FSK generator(s) will be programmed.
FSK_G1 = 0: FSK generator 1 is not selected;
FSK_G1 = 1: FSK generator 1 is selected (default).
FSK_G2 = 0: FSK generator 2 is not selected (default);
FSK_G2 = 1: FSK generator 2 is selected.
FSK_G3 = 0: FSK generator 3 is not selected (default);
FSK_G3 = 1: FSK generator 3 is selected.
FSK_G4 = 0: FSK generator 4 is not selected (default);

FSK_G4 = 1: FSK generator 4 is selected.

The IDT82V1068 provides four FSK generators shared by all eight channels. Before configuring the FSK generator(s) (e.g., setting the Flag Length/Data Length/Seizure Length/Mark Length, selecting the FSK channel and programming the FSK-RAM), this command must be used first to specify one or more FSK generators to be configured, the FSK configuration registers and FSK-RAM will then be accessed accordingly. The FSK Generator 1 (FSK_G1) is selected by default.

GC26: Loopback Control and PLL Power Down, Read/Write (3CH/BCH)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	1	1	1	0	0
I/O Data	ALB_64k	PLLPD	DLB_64k	DLB_ANA	ALB_8k	DLB_8k	DLB_DI	ALB_DI

The loopback control bits (ALB_DI, DLB_DI, DLB_8k, ALB_8k, DLB_ANA, DLB_64k and ALB_64k) determine the loopback status. Figure 9 on page 19 shows all the loopbacks and cutoff in the IDT82V1068.

ALB_DI = 0: The analog loopback via DX to DR is disabled (default);
ALB_DI = 1: The analog loopback via DX to DR is enabled;

DLB_DI = 0: The digital loopback via DR to DX is disabled (default);
DLB_DI = 1: The digital loopback via DR to DX is enabled;

DLB_8k = 0: The digital loopback via 8 kHz interface is disabled (default);
DLB_8k = 1: The digital loopback via 8 kHz interface is enabled;

ALB_8k = 0: The analog loopback via 8 kHz interface is disabled (default);
ALB_8k = 1: The analog loopback via 8 kHz interface is enabled;

DLB_ANA = 0: The digital loopback via analog interface is disabled (default);
DLB_ANA = 1: The digital loopback via analog interface is enabled.

DLB_64k = 0: The digital loopback via 64 kHz interface is disabled (default);
DLB_64k = 1: The digital loopback via 64 kHz interface is enabled;

ALB_64k = 0: The analog loopback via 64 kHz interface is disabled (default);
ALB_64k = 1: The analog loopback via 64 kHz interface is enabled;

The PLL Power Down Bit (PLLPD) controls the status of the Phase Lock Loop.
PLLPD = 0: The device is in normal operation (default);
PLLPD = 1: The Phase Lock Loop is powered down. The device works in Power-Saving mode. All clocks stop running.

3.4.2 LOCAL COMMANDS LIST

LC1: Coefficient Selection, Read/Write (00H/80H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	0	0	0	0	0	0
I/O Data	CS[7]	CS[6]	CS[5]	CS[4]	CS[3]	CS[2]	CS[1]	CS[0]

The Coefficient Selection bits (CS[7:0]) are used to control the digital filters and function blocks on the corresponding channel such as the Impedance Matching Filter, Echo Cancellation Filter, High-Pass Filter, Gain for Impedance Scaling, Gain in Transmit/Receive Path and Frequency Response Correction in Transmit/Receive Path. See Figure 9 on page 19 for details.
It should be noted that the Impedance Matching Filter and the Gain for Impedance Scaling are working together to adjust the impedance. That is to say, The CS[0] and CS[2] bits should be set to the same value to ensure the correct operation.

CS[0] = 0: The Impedance Matching Filter is disabled (default);
CS[0] = 1: The Impedance Matching Filter coefficient is set by IMF RAM;

CS[1] = 0: The Echo Cancellation Filter is disabled (default);
CS[1] = 1: The Echo Cancellation Filter coefficient is set by ECF RAM;

CS[2] = 0: The Gain for Impedance Scaling is disabled (default);
CS[2] = 1: The Gain for Impedance Scaling coefficient is set by GIS RAM;

CS[3] = 0: The High-Pass Filter is bypassed/disabled;
CS[3] = 1: The High-Pass Filter is enabled (default);

CS[4] = 0: The Frequency Response Correction in Transmit Path is bypassed (default);
CS[4] = 1: The Frequency Response Correction in Transmit Path coefficient is set by FRX RAM;

CS[5] = 0: The Gain in Transmit Path is 0 dB (default);
CS[5] = 1: The Gain in Transmit Path coefficient is set by GTX RAM;

CS[6] = 0: The Frequency Response Correction in Receive Path is bypassed (default);
CS[6] = 1: The Frequency Response Correction in Receive Path coefficient is set by FRR RAM;

CS[7] = 0: The Gain in Receive Path is 0 dB (default);
CS[7] = 1: The Gain in Receive Path coefficient is set by GRX RAM.

Refer to Figure 18 on page 53 for the Coe-RAM address mapping.

LC2: Loopback Control, PCM Receive Path Cutoff and SLIC Input Interrupt Enable, Read/Write (01H/81H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	0	0	0	0	0	1
I/O Data	IE[3]	IE[2]	IE[1]	IE[0]	CUTOFF	DLB_PCM	ALB_1BIT	DLB_1BIT

The loopback control bits (DLB_1BIT, ALB_1BIT and DLB_PCM) determine the loopback status on the corresponding channel. See Figure 9 on page 19 for details.

DLB_1BIT = 0: The digital loopback via Onebit on the corresponding channel is disabled (default);
DLB_1BIT = 1: The digital loopback via Onebit on the corresponding channel is enabled;

ALB_1BIT = 0: The analog loopback via Onebit on the corresponding channel is disabled (default);
ALB_1BIT = 1: The analog loopback via Onebit on the corresponding channel is enabled;

DLB_PCM = 0: The digital loopback via the PCM interface on the corresponding channel is disabled (default);
DLB_PCM = 1: The digital loopback via the PCM interface on the corresponding channel is enabled. In this loopback mode, the digital data received from the DR1/2 pin will be switched by the time slot setting and then transmitted out from the DX1/2 pin.

The PCM receive path cutoff bit (CUTOFF) is used to cut off the PCM receive path.
CUTOFF = 0: The PCM receive path in normal operation;
CUTOFF = 1: The PCM receive path is cut off.

The SLIC Input Interrupt Enable bits (IE[3:0]) enable or disable the interrupt signal on the corresponding channel.
IE[0] = 0: Interrupt disable. The interrupt signal generated by the SB2 pin of the corresponding channel (when the SB1 pin is configured as an input) will be ignored (default);
IE[0] = 1: Interrupt enable. The interrupt signal generated by the SB2 pin of the corresponding channel (when the SB1 pin is configured as an input) will be recognized;

IE[1] = 0: Interrupt disable. The interrupt signal generated by the SB1 pin of the corresponding channel (when the SB1 is configured as an input) will be ignored (default);
IE[1] = 1: Interrupt enable. The interrupt signal generated by the SB1 pin of the corresponding channel (when the SB1 pin is configured as an input) will be recognized;

IE[2] = 0: Interrupt disable. The interrupt signal generated by the SI2 pin of the corresponding channel will be ignored (default);
IE[2] = 1: Interrupt enable. The interrupt signal generated by the SI2 pin of the corresponding channel will be recognized;

IE[3] = 0: Interrupt disable. The interrupt signal generated by the SI1 pin of the corresponding channel will be ignored (default);
IE[3] = 1: Interrupt enable. The interrupt signal generated by the SI1 pin of the corresponding channel will be recognized;

LC3: Loopback Control, Read/Write (02H/82H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	0	0	0	0	1	0
I/O Data	Reserved							ALB_PCM

The loopback control bit ALB_PCM determines the status of the loopback ALB_PCM on the corresponding channel.
ALB_PCM = 0: The analog loopback via the PCM interface on the corresponding channel is disabled (default);
ALB_PCM = 1: The analog loopback via the PCM interface on the corresponding channel is enabled.

LC4: DSH Debounce and GK Debounce Configurations, Read/Write (03H/83H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	0	0	0	0	1	1
I/O Data	GK[3]	GK[2]	GK[1]	GK[0]	DSH[3]	DSH[2]	DSH[1]	DSH[0]

The DSH Debounce bits (DSH[3:0]) is used to set the debounce time for the SI1 input of the corresponding channel. The debounce time for SI1 is programmable from 0 to 30 ms in step of 2 ms.
DSH[3:0] = 0000: 0 ms (default);
DSH[3:0] = 0001: 2 ms;
DSH[3:0] = 0010: 4 ms;
DSH[3:0] = 0011: 6 ms;
DSH[3:0] = 0100: 8 ms;
DSH[3:0] = 0101: 10 ms;
DSH[3:0] = 0110: 12 ms;
DSH[3:0] = 0111: 14 ms;
DSH[3:0] = 1000: 16 ms;
DSH[3:0] = 1001: 18 ms;
DSH[3:0] = 1010: 20 ms;
DSH[3:0] = 1011: 22 ms;
DSH[3:0] = 1100: 24 ms;
DSH[3:0] = 1101: 26 ms;
DSH[3:0] = 1110: 28 ms;
DSH[3:0] = 1111: 30 ms.

The GK Debounce bits (GK[3:0]) is used to set the debounce interval for the SI2 input of the corresponding channel. The debounce time

for SI2 is programmable from 0 to 180 ms in step of 12 ms.
GK[3:0] = 0000: 0 ms (default);
GK[3:0] = 0001: 12 ms;
GK[3:0] = 0010: 24 ms;
GK[3:0] = 0011: 36 ms;
GK[3:0] = 0100: 48 ms;
GK[3:0] = 0101: 60 ms;
GK[3:0] = 0110: 72 ms;
GK[3:0] = 0111: 84 ms;
GK[3:0] = 1000: 96 ms;
GK[3:0] = 1001: 108 ms;
GK[3:0] = 1010: 120 ms;
GK[3:0] = 1011: 132 ms;
GK[3:0] = 1100: 144 ms;
GK[3:0] = 1101: 156 ms;
GK[3:0] = 1110: 168 ms;
GK[3:0] = 1111: 180 ms.

LC5: Dual Tone Frequency Setting, Read/Write (04H, 05H, 06H/84H, 85H, 86H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	0	0	0	1	0	0
I/O Data	T0[7]	T0[6]	T0[5]	T0[4]	T0[3]	T0[2]	T0[1]	T0[0]

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	0	0	0	1	0	1
I/O Data	T1[3]	T1[2]	T1[1]	T1[0]	T0[11]	T0[10]	T0[9]	T0[8]

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	0	0	0	1	1	0
I/O Data	T1[11]	T1[10]	T1[9]	T1[8]	T1[7]	T1[6]	T1[5]	T1[4]

The decimal value of Dual Tone Frequency Setting bits (T0[11:0]) is the frequency of the Tone 0 on the corresponding channel. The decimal value of T1[11:0] bits is the Tone 1 frequency on the corresponding channel.

LC6: Tone Generator Enable and Tone Gain Setting, Read/Write (07H/87H)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	0	0	0	1	1	1
I/O Data	T1E	T0E	TG[5]	TG[4]	TG[3]	TG[2]	TG[1]	TG[0]

The Tone Gain bits (TG[5:0]) are used to set the gain of the dual tone signal on the corresponding channel.
$G = 20 \times lg (Tg \times 2/256) + 3.14$
where: G is the desired tone gain, Tg is the decimal value of the TG[5:0] bits.

The tone generator enable bits T1E and T0E are used to activate the corresponding channel's tone generators Tone 1 and Tone 0, respectively.
T1E = 0: Tone 1 is disabled at the peak value in phase 90 degree (default);
T1E = 1: Tone 1 is enabled at zero-crossing;
T0E = 0: Tone 0 is disabled at the peak value in phase 90 degree (default);
T0E = 1: Tone 0 is enabled at zero-crossing.

LC7: Transmit Timeslot and Transmit Highway Selection, Read/Write (08H/88H) (For MPI mode only)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	0	0	1	0	0	0
I/O Data	THS	TT[6]	TT[5]	TT[4]	TT[3]	TT[2]	TT[1]	TT[0]

The Transmit Timeslot selection bits (TT[6:0]) determine which time slot will be used to transmit the data of the corresponding channel. The valid value of TT[6:0] is 0d - 127d, corresponding to Time slot 0 to Time slot 127. The default value is 0d.

The Transmit Highway Selection bit (THS) selects a PCM highway for the corresponding channel to transmit the voice data.
THS = 0: DX1 is selected (default);
THS = 1: DX2 is selected.

LC8: Receive Timeslot and Highway Selection, Read/Write (09H/89H) (For MPI mode only)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	0	0	1	0	0	1
I/O Data	RHS	RT[6]	RT[5]	RT[4]	RT[3]	RT[2]	RT[1]	RT[0]

The Receive Timeslot selection bits RT[6:0] determine which time slot will be used for the corresponding channel to receive the data. The valid value of RT[6:0] is 0d - 127d, corresponding to Time slot 0 to Time slot 127. The default value is 0d.

The Receive Highway Selection bit RHS selects a PCM highway for the corresponding channel to receive the voice data.
RHS = 0: DR1 is selected (default);
RHS = 1: DR2 is selected.

LC9: SLIC I/O Data, Read/Write (0AH/8AH) (For MPI mode only)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	0	0	1	0	1	0
I/O Data	Reserved	SO3	SO2	SO1	SI1	SI2	SB1	SB2

The SLIC I/O Data register contains the information of the SLIC I/O pins SI1, SI2, SB1, SB2, SO1, SO2 and SO3 on the corresponding channel. The default value of this register is 0d. It should be noted that the SI1, SI2, SB1 and SB2 bits in this register are read only.

LC10: D/A Gain and A/D Gain Setting, Channel Power Down, Read/Write (0CH/8CH)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	0	0	1	1	0	0
I/O Data	PD	GAD	GDA	Reserved				

The GDA bit is used to set the analog gain of D/A for the corresponding channel.
GDA = 0: 0 dB (default);
GDA = 1: -6 dB.

The GAD bit is used to set the analog gain of A/D for the corresponding channel.
GAD = 0: 0 dB (default);
GAD = 1: +6 dB.

The Channel Power Down bit (PD) disables or enables the corresponding channel.
PD = 0: The corresponding channel is in normal operation;
PD = 1: The corresponding channel is powered down (default).

LC11: PCM Data Low Byte, Read Only (0EH) (For MPI mode only)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	0	0	0	0	1	1	1	0
I/O Data	PCM[7]	PCM[6]	PCM[5]	PCM[4]	PCM[3]	PCM[2]	PCM[1]	PCM[0]

This command is used for the MCU to monitor the transmit (A to D) PCM data.
For linear Code, the low 8 bits of the PCM data will be output at the CO pin, at the same time, the transmit data will be output to the PCM bus without any interference.
For compressed code (A/μ-Law), the total 8 bit PCM data will be output at the CO pin.

LC12: PCM Data High Byte, Read Only (0FH) (For MPI mode only)

	b7	b6	b5	b4	b3	b2	b1	b0
Command	0	0	0	0	1	1	1	1
I/O Data	PCM[15]	PCM[14	PCM[13]	PCM[12]	PCM[11]	PCM[10]	PCM[9]	PCM[8]

This command is used for the MCU to monitor the transmit (A to D) PCM data.
For linear Code, the high 8 bits of the PCM data will be output at the CO pin, at the same time, the transmit data will be output to the PCM bus without any interference.
For compressed code (A/μ-Law), this command is not used.

4 ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	Com'l & Ind'l	Unit
Power supply voltage	4.5	V
Voltage on any pin with respect to the ground	-0.5 to 4.5	V
Package power dissipation	1	W
Storage temperature	-65 to 150	°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

5 RECOMMENDED DC OPERATING CONDITIONS

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature	-40		+85	°C
Power supply voltage	3.135		3.465	V

6 DC ELECTRICAL CHARACTERISTICS

6.1 DIGITAL INTERFACE

Parameter	Description	Min.	Typ.	Max.	Units	Test Conditions
V_{IL}	Input low voltage			1.2	V	All digital inputs
V_{IH}	Input high voltage	1.8			V	All digital inputs
V_{OL}	Output low voltage			0.3	V	DX, I_L = 6 mA; All other digital outputs, I_L = 3.6 mA.
V_{OH}	Output high voltage	VDD – 0.3			V	DX, I_L = -6 mA; All other digital outputs, I_L = -3.6 mA.
I_I	Input current	–10		10	µA	All digital inputs, GND<VIN<VDD
I_{OZ}	Output current in high-impedance state	–10		10	µA	DX
C_I	Input capacitance			5	pF	

6.2 POWER DISSIPATION

Parameter	Description	Min.	Typ.	Max.	Units	Test Conditions
I_{DD1}	Operating current		110		mA	All channels are active.
I_{DD0}	Standby current			5	mA	All channels and PLL are powered down.

6.3 ANALOG INTERFACE

Parameter	Description	Min.	Typ.	Max.	Units	Test Conditions
V_{OUT1}	Output voltage, VOUT		1.5		V	Alternating ±zero μ-law PCM code applied to DR
V_{OUT2}	Output voltage swing, VOUT	2.1			Vp-p	R_L = 300 Ω
R_I	Input resistance, VIN	40	50	60	kΩ	0.25 V < VIN < 4.75 V
R_O	Output resistance, VOUT			20	Ω	0 dBm0, 1020 Hz PCM code applied to DR
R_L	Load resistance, VOUT	300			Ω	External loading
I_I	Input leakage current, VIN	–1.0		1.0	μA	0.25 V < VIN < VDD – 0.25 V
I_Z	Output leakage current, VOUT	–10		10	μA	Power down
CL	Load capacitance, VOUT			100	pF	External loading

7 AC ELECTRICAL CHARACTERISTICS

0 dBm0 is defined as 0.5026 Vrms for A-law and 0.4987 Vrms for μ-law, both for 600 Ω load. Unless otherwise noted, the analog input is a 0 dBm0, 1020 Hz sine wave; the input amplifier is set for unity gain. The digital input is a PCM bit stream equivalent to that obtained by passing a 0 dBm0, 1020 Hz sine wave through an ideal encoder. The output level is sin(x)/x-corrected. Typical values are for V_{DD} = 3.3 V and T_A = 25 °C.

7.1 ABSOLUTE GAIN

Parameter	Description	Min.	Typ.	Max.	Units	Test Conditions
G_{XA}	Transmit gain, absolute 0 °C to 85 °C –40 °C	 –0.05 –0.1		 0.45 0.5	dB	Signal input of 0 dBm0, μ-law or A-law
G_{RA}	Receive gain, absolute 0 °C to 85 °C –40 °C	 –0.45 –0.5		 0.05 0.1	dB	Measured relative to 0 dBm0, μ-law or A-law, PCM input of 0 dBm0, 1020Hz. R_L = 10 kΩ

7.2 GAIN TRACKING

Parameter	Description	Min.	Typ.	Max.	Units	Test Conditions
GT_X	Transmit gain tracking +3 dBm0 to –37 dBm0 (exclude –37 dBm0) –37 dBm0 to –50 dBm0 (exclude –50 dBm0) –50 dBm0 to –55 dBm0	 –0.25 –0.50 –1.40		 0.25 0.50 1.40	dB	Tested by sinusoidal method, A-law or μ-law
GT_R	Receive gain tracking +3 dBm0 to –40 dBm0 (exclude –40 dBm0) –40 dBm0 to –50 dBm0 (exclude –50 dBm0) –50 dBm0 to –55 dBm0	 –0.10 –0.25 –0.50		 0.10 0.50 0.50	dB	Tested by sinusoidal method, A-law or μ-law

7.3 FREQUENCY RESPONSE

Parameter	Description	Min.	Typ.	Max.	Units	Test Conditions
G_{XR}	Transmit gain, relative to G_{XA} f = 50 Hz f = 60 Hz f = 300 Hz to 3000 Hz f = 3000 Hz to 3400 Hz f = 3600 Hz f ≥ 4600 Hz	 –0.15 –0.4 		 –30 –30 0.15 0.15 –0.1 –35	dB	High-pass filter is enabled.
G_{RR}	Receive gain, relative to G_{RA} f < 300 Hz f = 300 Hz to 3000 Hz f = 3000 Hz to 3400 Hz f = 3600 Hz f ≥ 4600 Hz	 –0.15 –0.4 		 0 0.15 0.15 –0.2 –35	dB	

7.4 GROUP DELAY

Parameter	Description	Min.	Typ.	Max.	Units	Test Conditions
D_{XR}	Transmit delay, relative to 1800 Hz f = 500 Hz to 600 Hz f = 600 Hz to 1000 Hz f = 1000 Hz to 2600 Hz f = 2600 Hz to 2800 Hz			 280 150 80 280	µs	
D_{RR}	Receive delay, relative to 1800 Hz f = 500 Hz to 600 Hz f = 600 Hz to 1000 Hz f = 1000 Hz to 2600 Hz f = 2600 Hz to 2800 Hz			 50 80 120 150	µs	

7.5 DISTORTION

Parameter	Description	Min.	Typ.	Max.	Units	Test Conditions
STD_X	Transmit signal to total distortion ratio A-law: input level = 0 dBm0 input level = –30 dBm0 input level = –40 dBm0 input level = –45 dBm0 µ-law: input level = 0 dBm0 input level = –30 dBm0 input level = –40 dBm0 input level = –45 dBm0	 36 36 30 24 36 36 31 27			dB	ITU-T O.132 Sine wave method, psophometric weighted for A-law; Sine wave method, C message weighted for µ-law.
STD_R	Receive signal to total distortion ratio A-law: input level = 0 dBm0 input level = –30 dBm0 input level = –40 dBm0 input level = –45 dBm0 µ-law: input level = 0 dBm0 input level = –30 dBm0 input level = –40 dBm0 input level = –45 dBm0	 36 36 30 24 36 36 31 27			dB	ITU-T O.132 Sine wave method, psophometric weighted for A-law; Sine wave method, C message weighted for µ-law.
SFD_X	Single frequency distortion, transmit			–42	dBm0	200 Hz to 3400 Hz, 0 dBm0 input, output any other single frequency ≤ 3400 Hz
SFD_R	Single frequency distortion, receive			–42	dBm0	200 Hz to 3400 Hz, 0 dBm0 input, output any other single frequency ≤ 3400 Hz
IMD	Intermodulation distortion			–42	dBm0	Transmit or receive, two frequencies in the range (300 Hz – 3400 Hz) at –6 dBm0.

7.6 NOISE

Parameter	Description	Min.	Typ.	Max.	Units	Test Conditions
N_{XC}	Transmit noise, C message weighted for μ-law			18	dBrnC0	
N_{XP}	Transmit noise, psophometrically weighted for A-law			–68	dBm0p	
N_{RC}	Receive noise, C message weighted for μ-law			12	dBrnC0	
N_{RP}	Receive noise, psophometrically weighted for A-law			–78	dBm0p	
N_{RS}	Noise, single frequency f = 0 kHz to 100 kHz			–53	dBm0	VIN = 0 Vrms, tested at VOUT.
PSR_X	Power supply rejection, transmit f = 300 Hz to 3.4 kHz f = 3.4 kHz to 20 kHz	 40 25			dB	VDD = 3.3 VDC+100 mVrms
PSR_R	Power supply rejection, receive f = 300 Hz to 3.4 kHz f = 3.4 kHz to 20 kHz	 40 25			dB	The PCM code is positive one LSB, VDD = 3.3 VDC+100 mVrms,
SOS	Spurious out-of-band signals at VOUT, relative to input PCM code applied: f = 4.6 kHz to 20 kHz f = 20 kHz to 50 kHz			 –40 –30	dB	0dBm0, 300 Hz to 3400 Hz input

7.7 INTERCHANNEL CROSSTALK

Parameter	Description	Min.	Typ.	Max.	Units	Test Conditions
XT_{X-R}	Transmit to receive crosstalk		–85	–78	dB	300 Hz to 3400 Hz, 0 dBm0 signal into the VIN pin of the interfering channel. Idle PCM code into the channel under test.
XT_{R-X}	Receive to transmit crosstalk		–85	–80	dB	300 Hz to 3400 Hz, 0 dBm0 PCM code into the interfering channel. VIN = 0 Vrms for the channel under test.
XT_{X-X}	Transmit to transmit crosstalk		–85	–78	dB	300 Hz to 3400 Hz, 0 dBm0 signal into the VIN pin of the interfering channel. VIN = 0 Vrms for the channel under test
XT_{R-R}	Receive to receive crosstalk		–85	–80	dB	300 Hz to 3400 Hz, 0 dBm0 PCM code into the interfering channel. Idle PCM code into the channel under test

8 TIMING CHARACTERISTICS

8.1 CLOCK

Symbol	Description	Min.	Typ.	Max.	Units	Test Conditions
t1	CCLK period	122		100 k	ns	
t2	CCLK pulse width	48			ns	
t3	CCLK rise and fall time			25	ns	
t4	BCLK period	122			ns	
t5	BCLK pulse width	48			ns	
t6	BCLK rise and fall time			15	ns	
t7	MCLK pulse width	48			ns	
t8	MCLK rise and fall time			15	ns	
t9	DCL period f = 2.048 kHz f = 4.096 kHz		488 244		ns	
t10	DCL rise and fall time			60	ns	
t11	DCL pulse width	90			ns	

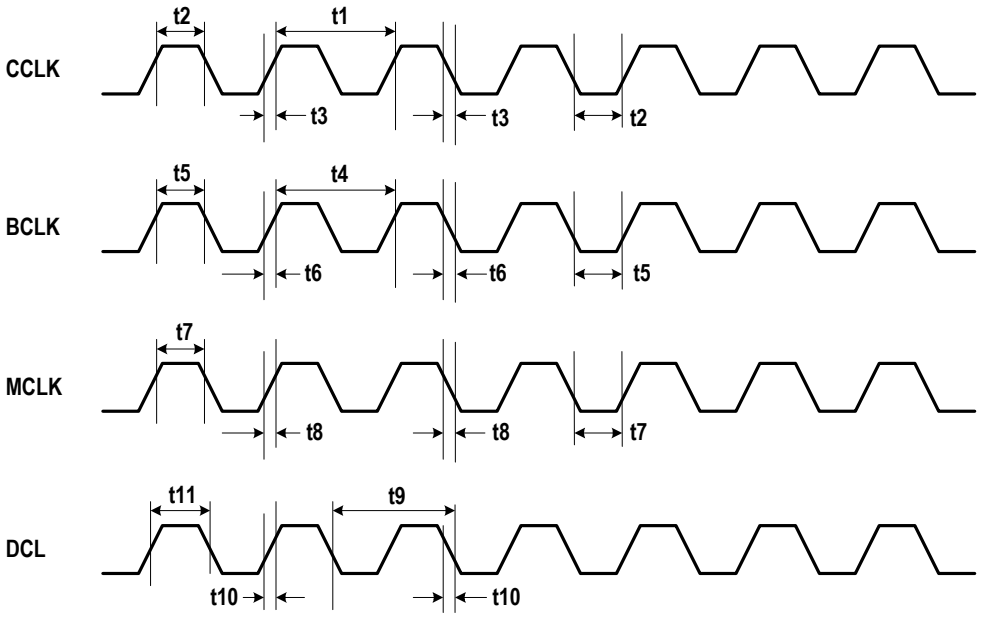


Figure 13 Clock Timing

8.2 MICROPROCESSOR INTERFACE

Symbol	Description	Min.	Typ.	Max.	Units	Test Conditions
t12	$\overline{CS}$ setup time	15			ns	
t13	$\overline{CS}$ pulse width		8 * n * t1 (n ≥ 2)		ns	
t14	$\overline{CS}$ off time	250			ns	
t15	Input data setup time	30			ns	
t16	Input data hold time	30			ns	
t17	SLIC output latch valid			1000	ns	
t18	Output data turn on delay			50	ns	
t19	Output data hold time	0			ns	
t20	Output data turn off delay			50	ns	
t21	output data valid	0		50	ns	

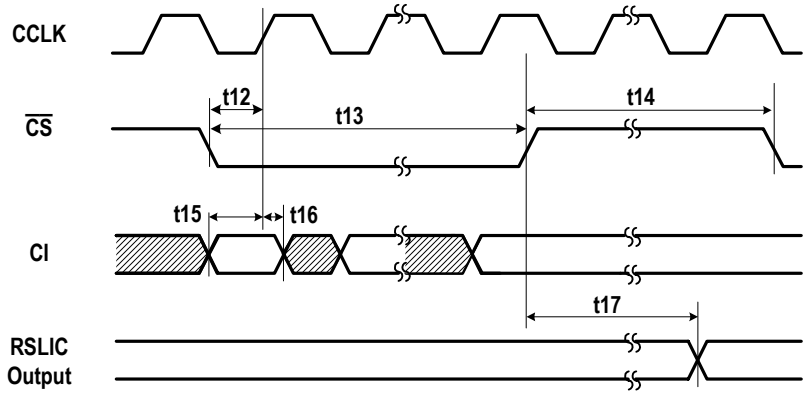


Figure 14 MPI Input Timing

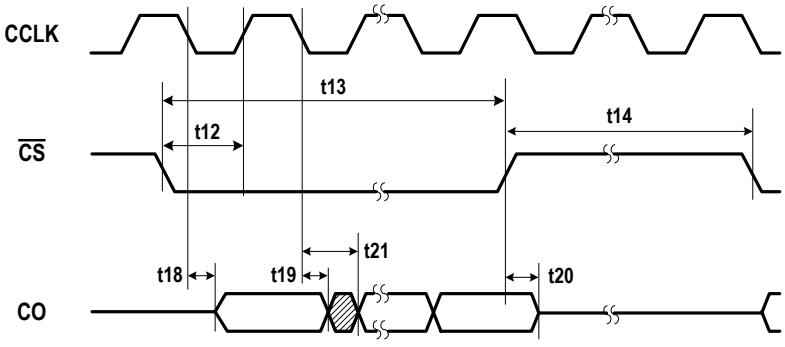


Figure 15 MPI Output Timing

8.3 PCM INTERFACE

Symbol	Description	Min.	Typ.	Max.	Units	Test Conditions
t22	Data enable delay time	5		70	ns	
t23	Data delay time from BCLK	5		70	ns	
t24	Data float delay time	5		70	ns	
t25	Frame sync setup time	25		t4 – 50	ns	
t26	Frame sync hold time	50			ns	
t27	$\overline{TSX1}$/$\overline{TSX2}$ enable delay time	5		80	ns	
t28	$\overline{TSX1}$/$\overline{TSX2}$ disable delay time	5		80	ns	
t29	Receive data setup time	25			ns	
t30	Receive data hold time	5			ns	

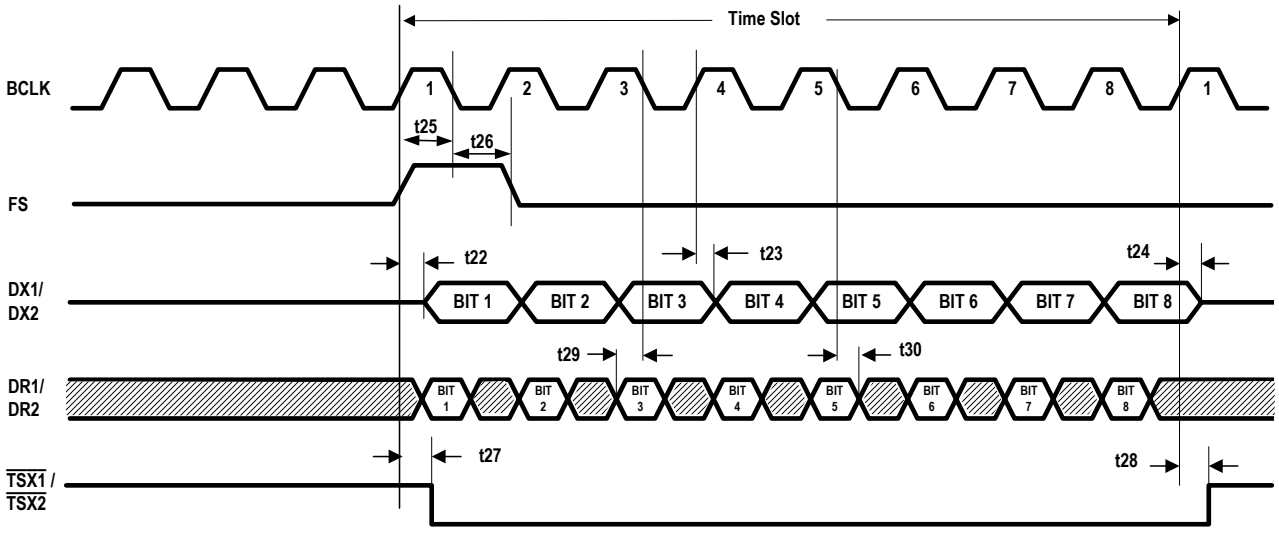


Figure 16 PCM Interface Timing

8.4 GCI INTERFACE

Symbol	Description	Min.	Typ.	Max.	Units	Test Conditions
t31	FSC rise and fall time			60	ns	
t32	FSC setup time	70		t9 – 50	ns	
t33	FSC hold time	50			ns	
t34	FSC high pulse width	130			ns	
t35	DU data delay time			100	ns	
t36	DD data delay time	110			ns	
t37	DD data hold time	50			ns	

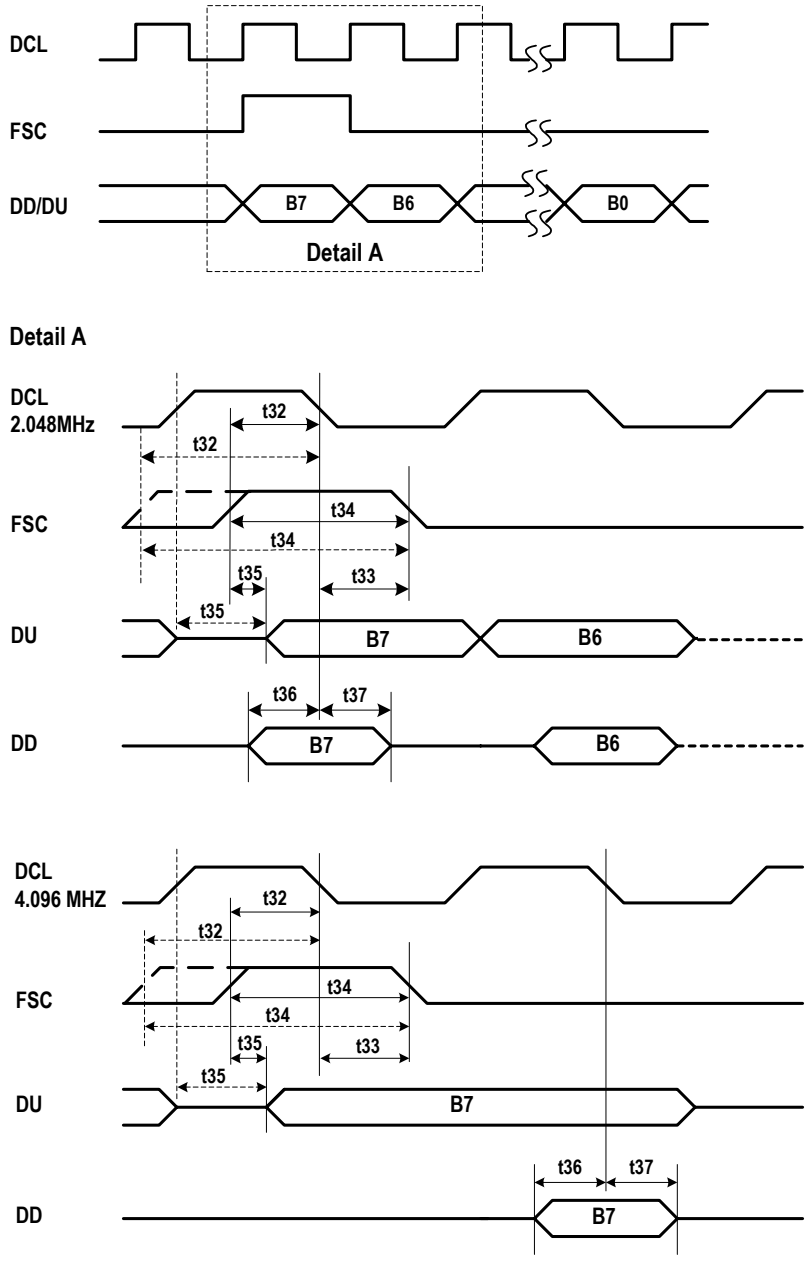


Figure 17 GCI Interface Timing

9 APPENDIX: IDT82V1068 COE-RAM MAPPING

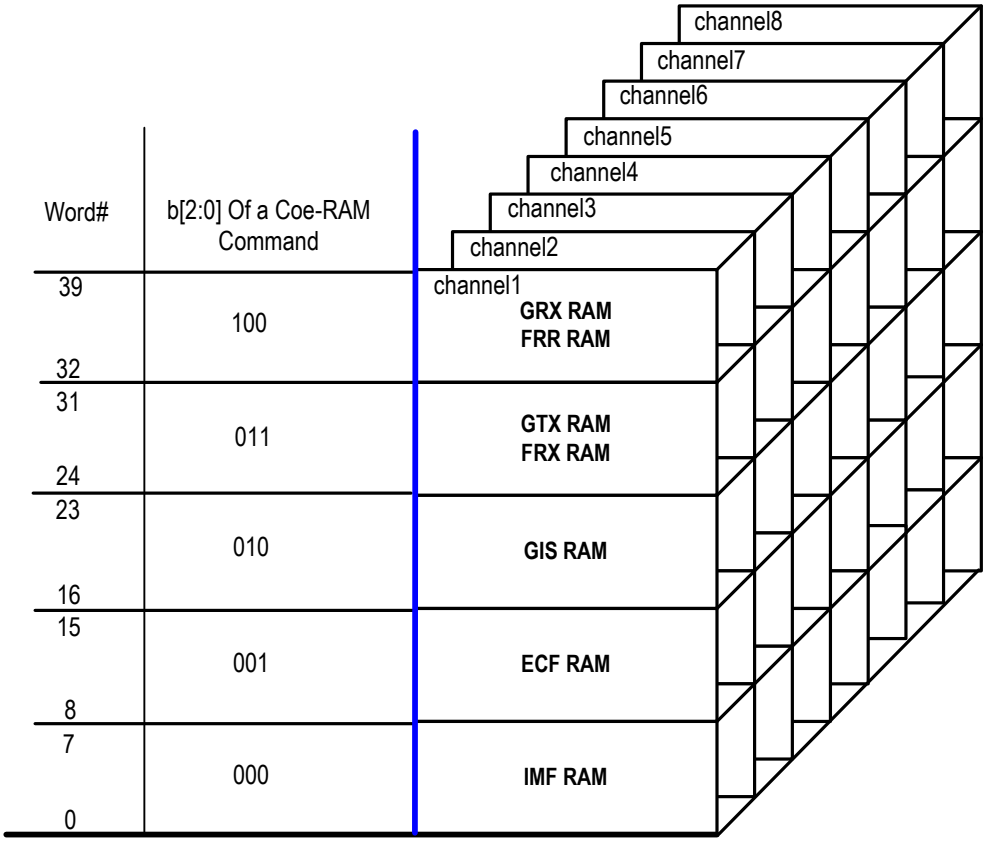


Figure 18 Coe-RAM Address Mapping

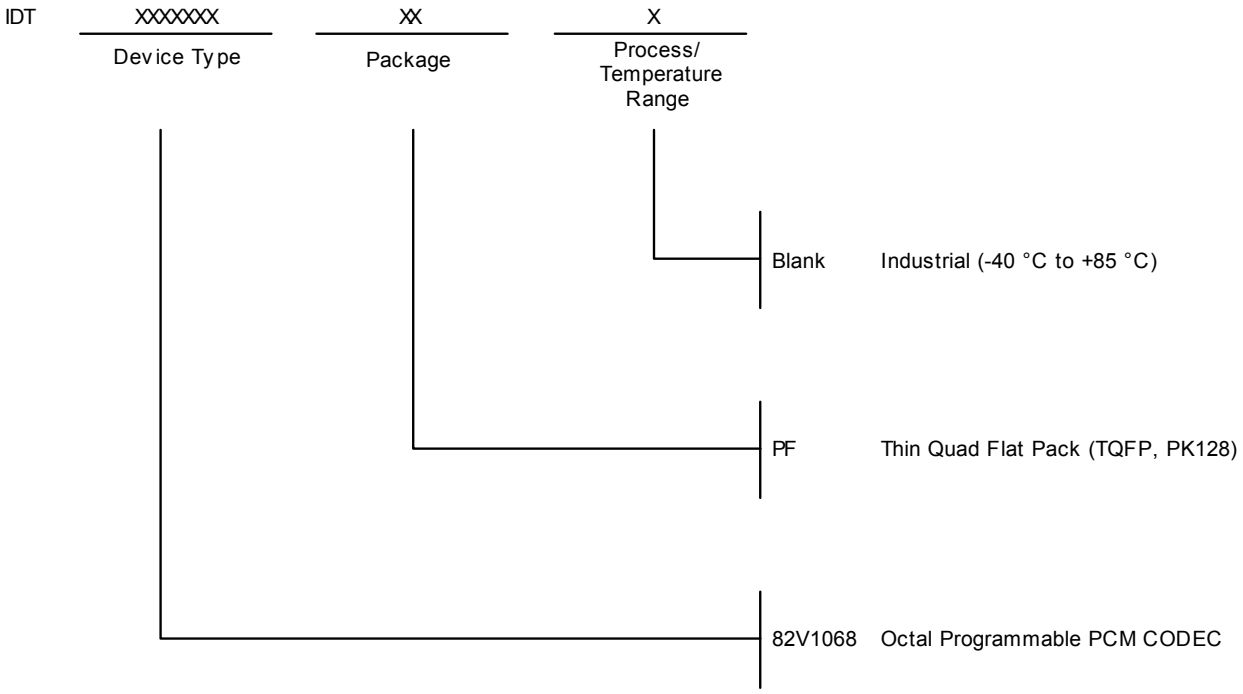
Generally, 6 bits of address are needed to locate each word of the 40 Coe-RAM words. The 40 words of Coe-RAM are divided into 5 blocks with 8 words per block in the IDT82V1068. So, only 3 bits of address are needed to locate each of the block. When the address of a Coe-RAM block (b[2:0]) is specified in a Coe-RAM Command, all 8 words of this block will be addressed automatically, with the highest order word first (The IDT82V1068 will count down from '111' to '000' so that it accesses the 8 words successively). Refer to “Addressing the Coe-RAM” on page 26 for more information.

The address assignment for the 40 words Coe-RAM is shown in Table 11. The number in the “Address” column is the actual hexadecimal address of the Coe-RAM word. As the IDT82V1068 handles the lower 3 bits automatically, only the higher 3 bits (in bold style) are needed for a Coe-RAM Command. It should be noted that, when addressing the GRX RAM, the FRR RAM will be addressed at the same time.

Table 11 Coe-RAM Address Allocation

Block #	Word #	Address	Function
5	39	100,111	GRX RAM
	38	100,110	FRR RAM
	37	100,101	
	36	100,100	
	35	100,011	
	34	100,010	
	33	100,001	
	32	100,000	
4	31	011,111	GTX RAM
	30	011,110	FRX RAM
	29	011,101	
	28	011,100	
	27	011,011	
	26	011,010	
	25	011,001	
	24	011,000	
3	23	010,111	GIS RAM
	22	010,110	
	21	010,101	
	20	010,100	
	19	010,011	
	18	010,010	
	17	010,001	
	16	010,000	
2	15	001,111	ECF RAM
	14	001,110	
	13	001,101	
	12	001,100	
	11	001,011	
	10	001,010	
	9	001,001	
	8	001,000	
1	7	000,111	IMF RAM
	6	000,110	
	5	000,101	
	4	000,100	
	3	000,011	
	2	000,010	
	1	000,001	
	0	000,000	

10 ORDERING INFORMATION



DATA SHEET DOCUMENT HISTORY

12/05/2002	pgs. 32, 37, 46
01/10/2003	pgs. 44, 55
03/04/2003	pgs. 1, 46

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