27-Line Plug and Play SCSI Terminator

The 27-channel IMP5121 SCSI terminator is part of IMP's family of high-performance SCSI terminators that deliver true UltraSCSI performance. The BiCMOS design offers superior performance over first generation linear regulator / resistor based terminators.

IMP's new architecture employs high-speed adaptive elements for each channel, thereby providing the fastest response possible - typically 35MHz, which is 100 times faster than the older linear regulator terminator approach. The bandwidth of terminators based on the older regulator / resistor terminator architecture is limited to 500kHz since a large output stabilization capacitor is required. The IMP architecture eliminates the external output compensation capacitor and the need for transient output capacitors while maintaining pin compatibility with first generation designs. Reduced component count is inherent with the IMP5121.

The IMP5121 architecture tolerates marginal system designs. A key improvement offered by the IMP5121 lies in its ability to insure reliable, error-free communications even in systems which do not adhere to recommended SCSI hardware design guidelines, such as improper cable lengths and impedance. Frequently, this situation is not controlled by the peripheral or host designer.

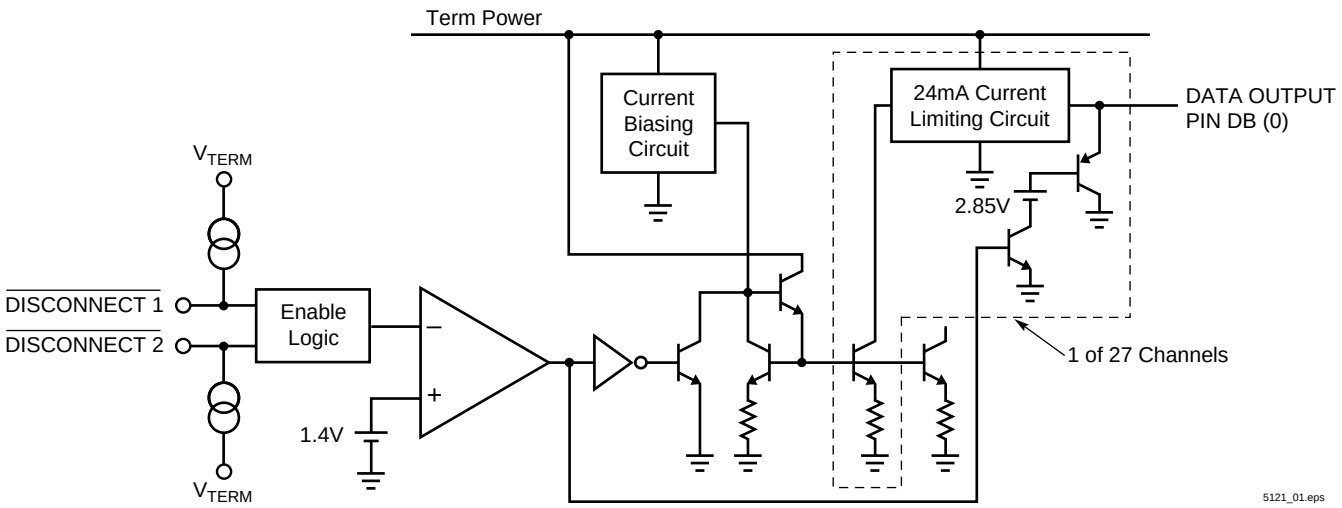
For portable and configurable peripherals, the IMP5121 can be placed in a sleep mode with TTL compatible signals. Quiescent current is less than 150µA when disabled.

Key Features

- SCSI Plug and Play
  — Host bus adapter with 3 SCSI connectors
- Ultra-Fast response for Fast-20 SCSI
- Split disconnect for mixing 16-bit (wide) or 8-bit (narrow) buses
- 35MHz channel bandwidth
- Sleep-mode current less than 150µA
- NO external compensation capacitors
- Compatible with active negation drivers
- Hot swap compatible
- Superior replacement for the LX5121 and UCC5621

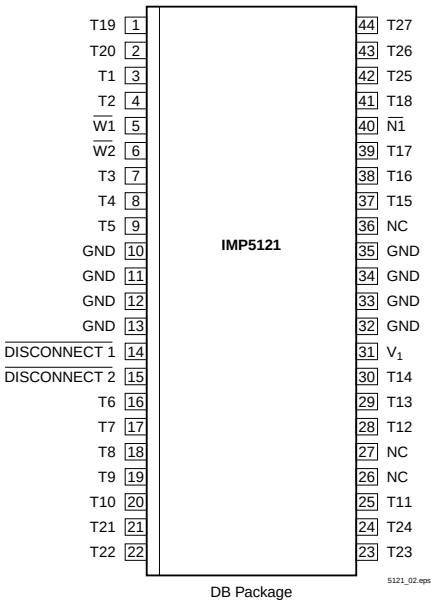
For Host Bus Adapters and three SCSI connectors, the IMP5121 has multiple disable pins for Plug and Play SCSI capability. It also splits the upper nine termination lines for mixing 16-bit (wide) and 8-bit (narrow) buses with minimal board trace capacitance.

Block Diagrams



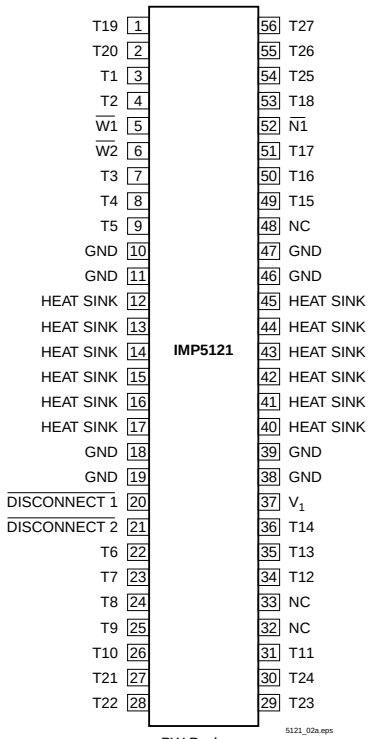
Pin Configuration

SSOP-44



DB Package

TSSOP-56



PW Package

Ordering Information

Part Number	Temperature Range	Package
IMP5121CDB	0°C to 125°C	44-pin Plastic SSOP
IMP5121CPW	0°C to 125°C	56-pin Plastic TSSOP

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Absolute Maximum Ratings[1]

TermPwr Voltage . . . . . +7V
Continuous Output Voltage Range . . . . . 0V to 5.5V
Continuous Disable Voltage Range . . . . . 0V to 5.5V
Operating Junction Temperature . . . . . 150°C
Storage Temperature Range . . . . . –65°C to 150°C
Lead Temperature (Soldering, 10 sec.) . . . . . 300°C

Note: 1. Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.

Thermal Data

PW and DB Package
Thermal Resistance Junction-to-Ambient, θ_{JA} . . . . . 50°C / W

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
The θ_{JA} numbers are guidelines for the thermal performance of the device / pc-board system. All of the ambient airflow is assumed.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Termpwr Voltage	V_{TERM}	4.0		5.5	V
High Level Disable Input Voltage	V_{IH}	2		V_{TERM}	V
Low Level Disable Input Voltage	V_{IL}	0		0.8	V
Operating Junction Temperature Range – IMP5121C		0		125	°C

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Note: 2. Recommended operating conditions indicate the range over which the device is functional.

Electrical Characteristics

Unless otherwise specified, these specifications apply at an ambient operating temperature of T_A = 25°C. TermPwr = 4.75V. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output High Voltage	V_{OUT}		2.65	2.85		V
TermPwr Supply Current	I_{CC}	All data lines = Open		12	20	mA
		All data lines = 0.5V		635	670	
		Disable Pins 1, 2 < 0.8V		50	150	µA
Output Current	I_{OUT}	V_{OUT} = 0.5V	–20	–22	–24	mA
Disconnect Input Current	I_{IN}	$\overline{\text{DISCONNECT}}$ Pins = 0V			–10	µA
Output Leakage Current	I_{OL}	$\overline{\text{DISCONNECT}}$ Pins < 0.8V, V_O = 0.2V			1	µA
Channel Bandwidth	BW			35		MHz
Termination Sink Current, per Channel	I_{SINK}	V_{OUT} = 4V	7			mA

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Application Information

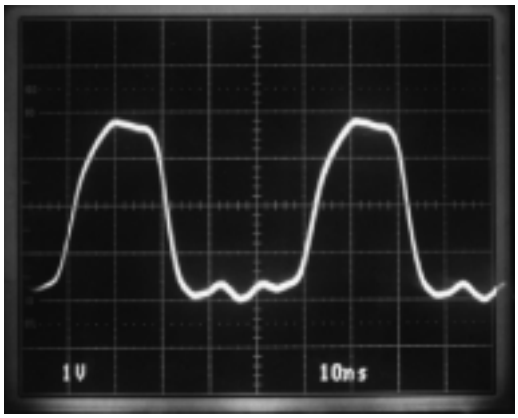

Figure 1. Receiving Waveform – 20MHz

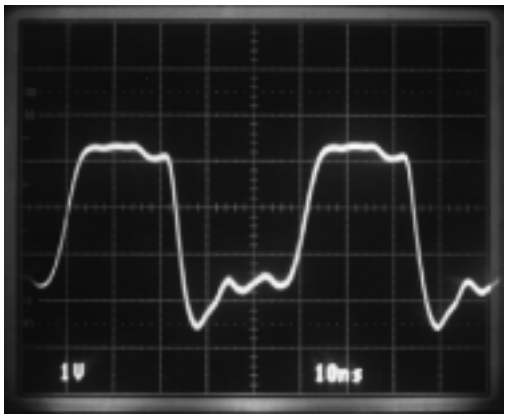

Figure 2. Driving Waveform – 20MHz

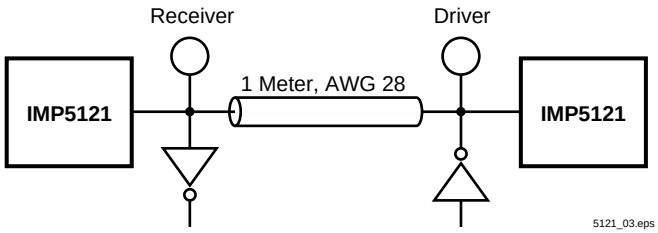

Figure 3.

IMP5121 Maximizes Line Current

Cable transmission theory suggests to optimize signal speed and quality, the termination should act both as an ideal voltage reference when the line is released (deasserted) and as an ideal current source when the line is active (asserted). Common active terminators which consist of linear regulators in series with resistors (typically 110Ω) are a compromise. With coventional linear terminators as the line voltage increases the amount of current decreases linearly by the equation;

$$\frac{(V_{REF} - V_{LINE})}{R} = I.$$

The IMP5121, with its unique new architecture, applies the maximum amount of current regardless of line voltage until the termination high threshold (2.85V) is reached.

Acting as a near ideal line terminator, the IMP5121 closely reproduces the optimum case when the device is enabled. To enable the device the $\overline{DISC1}$ and $\overline{DISC2}$ pins must be driven per *Table 1*. When enabled, quiescent current is 12mA and the device will respond to line demands by delivering 24mA on assertion and by imposing 2.85V on de-assertion.

Disable / Sleep Mode

Disable mode places the device in a sleep state, where quiescent current is reduced to less than 150µA. When disabled, all outputs are in a high impedance state. Sleep mode can be used for power conservation or to remove the terminator from the SCSI chain.

An additional feature of the IMP5121 is its compatibility with active negation drivers.

Table 1. Power Up/ Power Down Function Table

$\overline{\text{DISCONNECT 1}}$	$\overline{\text{DISCONNECT 2}}$	W1	W2	N1	T1-T18	T19-T27
H	L	DC	DC	DC	Enabled	Disabled
L	H	DC	DC	DC	Disabled	Enabled
L	L	DC	DC	DC	Disabled	Disabled
H	H	H	H	H	Enabled	Enabled
H	H	H	H	L	Enabled	Enabled
H	H	H	L	H	Enabled	Enabled
H	H	H	L	L	Disabled	Enabled
H	H	L	H	H	Enabled	Enabled
H	H	L	H	L	Disabled	Enabled
H	H	L	L	H	Disabled	Disabled
H	H	L	L	L	Disabled	Disabled

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For Plug and Play SCSI auto-termination disabling, connect pin 50 of the External Wide SCSI connector to $\overline{\text{W1}}$ of the IMP5121, connect pin 50 of the Internal Wide SCSI connector to $\overline{\text{W2}}$ of the IMP5121, and connect pin 22 of the Internal Narrow connector to $\overline{\text{N1}}$ of the IMP5121.

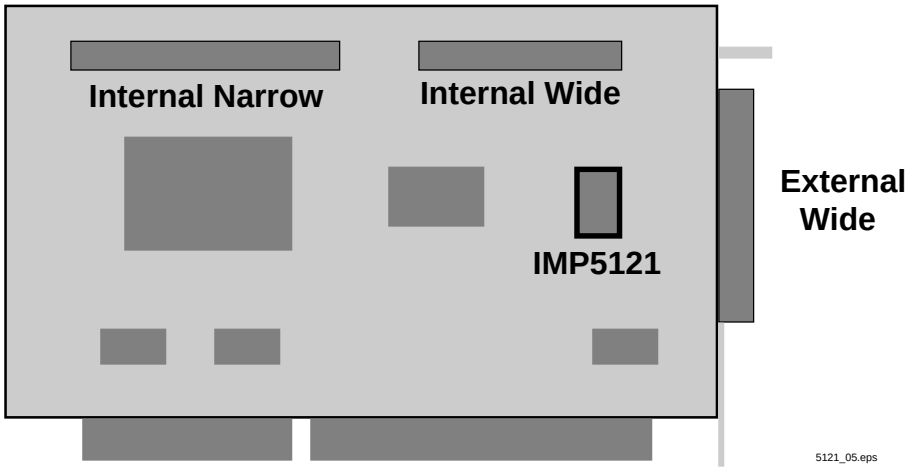
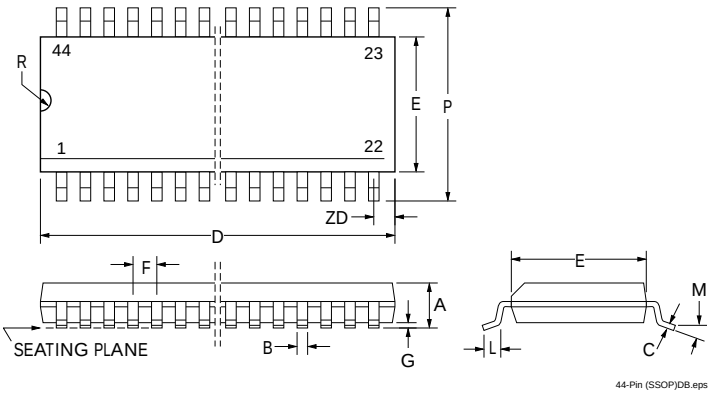


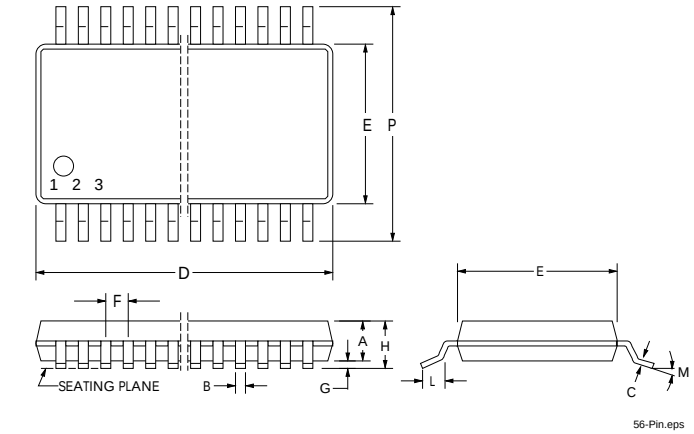
Figure 4. Plug and Play Diagram

Package Dimensions

SSOP (44-Pin)



TSSOP (56-Pin)



	Inches		Millimeters	
	Min	Max	Min	Max
SSOP (44-Pin)				
A	0.096	0.104	2.44	2.64
B	0.011	0.020	0.28	0.51
C	0.0091	0.0125	0.23	0.32
D	0.698	0.706	17.73	17.93
E	0.291	0.299	7.40	7.60
F	0.0315 BSC		0.80 BSC	
G	0.004	0.012	0.10	0.30
L	0.016	0.050	0.40	1.27
M	0°	8°	0°	8°
P	0.396	0.414	10.11	10.51
R	0.025	0.035	0.63	0.89
ZD	0.033 REF		0.51 REF	
LC*	—	0.004	—	0.10
TSSOP (56-Pin)				
A	0.032	0.041	0.80	1.05
B	0.007	0.011	0.17	0.27
C	0.004	0.008	0.09	0.20
D	0.547	0.555	13.90	14.10
E	0.236	0.244	6.0	6.2
F	0.02 BSC		0.50 BSC	
G	0.002	0.005	0.05	0.15
H	—	0.047	—	1.20
L	0.018	0.030	0.45	0.75
M	0°	8°	0°	8°
P	0.32 BSC		8.1 BSC	
LC*	—	0.004	—	0.10

** Lead Coplanarity*

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Publication #: 7005
Revision: C
Issue Date: 08/19/02
Type: Preliminary