IMS T225
transputer

inmos

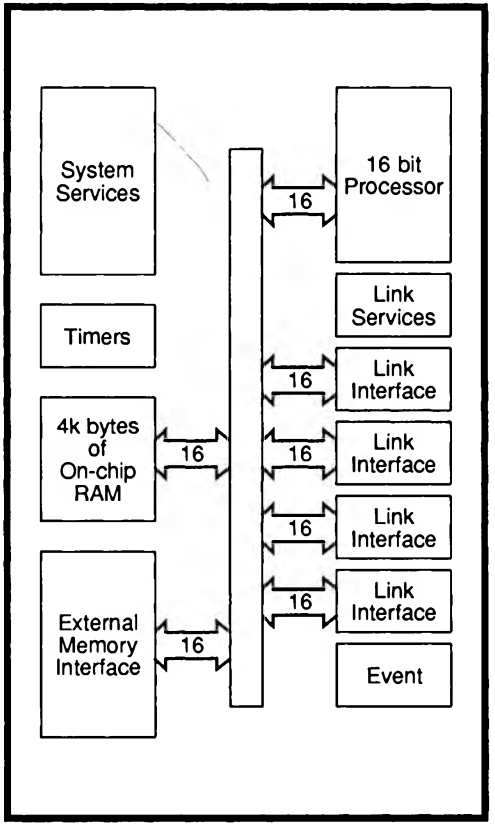
Product Preview

FEATURES

16 bit architecture
33 ns internal cycle time
30 MIPS (peak) instruction rate
IMS T225-20 is pin compatible with IMS T222-20
Debugging support
4 Kbytes on-chip static RAM
60 Mbytes/sec sustained data rate to internal memory
64 Kbytes directly addressable external memory
30 Mbytes/sec sustained data rate to external memory
630 ns response to interrupts
Four INMOS serial links 5/10/20 Mbits/sec
Bi-directional data rate of 2.4 Mbytes/sec per link
Internal timers of 1 μs and 64 μs
Boot from ROM or communication links
Single 5 MHz clock input
Single +5V ±5% power supply
MIL-STD-883C processing will be available

APPLICATIONS

Real time processing
Microprocessor applications
High speed multi processor systems
Industrial control
Robotics
System simulation
Digital signal processing
Telecommunications
Fault tolerant systems
Medical instrumentation



1 Introduction

The IMS T225 transputer is a 16 bit CMOS microcomputer with 4 Kbytes on-chip RAM for high speed processing, an external memory interface and four standard INMOS communication links. The instruction set achieves efficient implementation of high level languages and provides direct support for the occam model of concurrency when using either a single transputer or a network. Procedure calls, process switching and typical interrupt latency are sub-microsecond. A device running at 30 MHz achieves an instruction throughput of 15 MIPS.

For convenience of description, the IMS T225 operation is split into the basic blocks shown in figure 1.1.

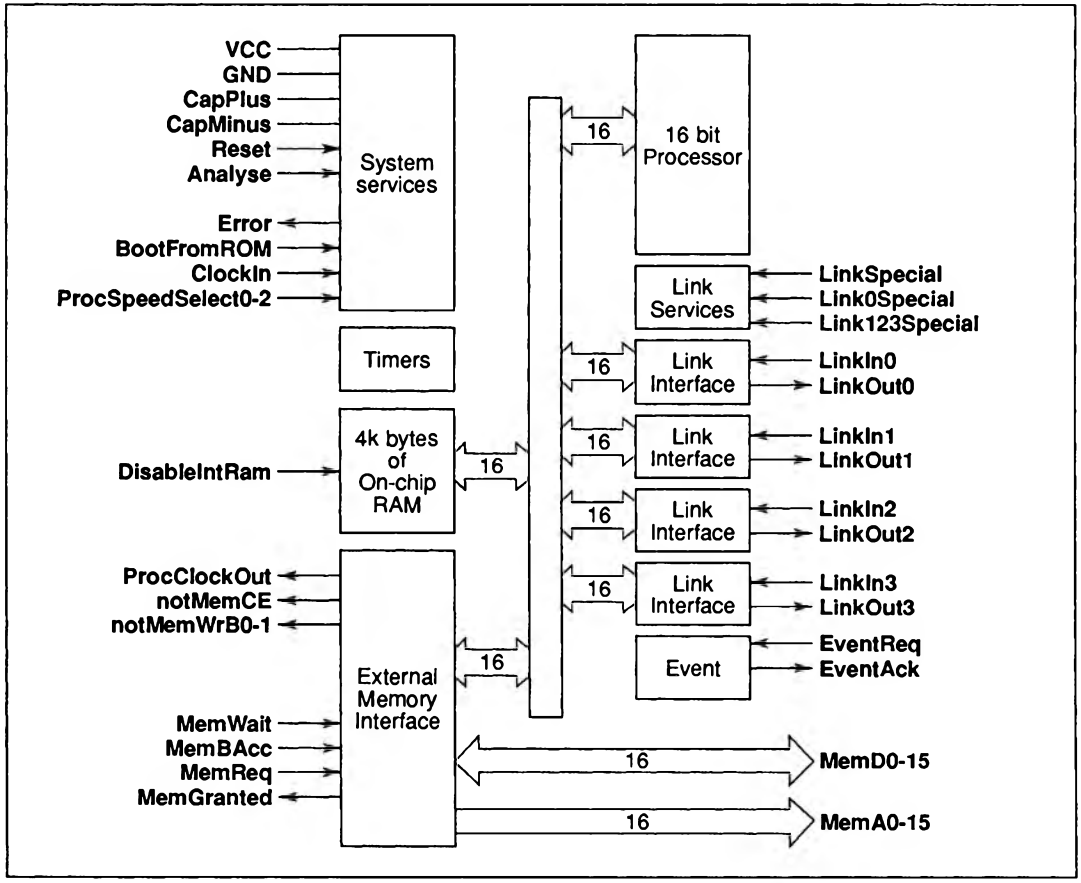


Figure 1.1 IMS T225 block diagram

The IMS T225 is functionally equivalent to the IMS T222 but has the addition of three speed select pins (**ProcSpeedSelect0-2**) and improved links. The IMS T225 is pin compatible with the IMS T222 and is a direct replacement in many applications. The IMS T225 can directly access a linear address space of 64 Kbytes. The 16 bit wide non-multiplexed external memory interface provides a data rate of up to 2 bytes every 100 nanoseconds (20 Mbytes/sec) for a 20 MHz device.

System Services include processor reset and bootstrap control, together with facilities for error analysis.

The INMOS communication links allow networks of transputers to be constructed by direct point to point connections with no external logic. The links support the standard operating speed of 10 Mbits/sec, but also

operate at 5 or 20 Mbits/sec. The links have been improved over those of the IMS T222 and fully support overlapped acknowledge; each IMS T225 link can transfer data bi-directionally at up to 2.4 Mbytes/sec. The link speed settings are the same as those on the IMS T800 (see page 241).

The IMS T225 instruction set contains a number of instructions to facilitate the implementation of breakpoints. For further information concerning breakpointing, refer to *Support for debugging/breakpointing in transputers* (technical note 61).

2 Pin designations

Table 2.1 IMS T225 system services

Pin	In/Out	Function
VCC, GND		Power supply and return
CapPlus, CapMinus		External capacitor for internal clock power supply
ClockIn	in	Input clock
ProcSpeedSelect0-2	in	Processor speed selectors
Reset	in	System reset
Error	out	Error indicator
Analyse	in	Error analysis
BootFromRom	in	Bootstraps from external ROM or from link
DisableIntRAM	in	Disable internal RAM

Table 2.2 IMS T225 external memory interface

Pin	In/Out	Function
ProcClockOut	out	Processor clock
MemA0-15	out	Sixteen address lines
MemD0-15	in/out	Sixteen data lines
notMemWrB0-1	out	Two byte-addressing write strobes
notMemCE	out	Chip enable
MemBAcc	in	Byte access mode selector
MemWait	in	Memory cycle extender
MemReq	in	Direct memory access request
MemGranted	out	Direct memory access granted

Table 2.3 IMS T225 event

Pin	In/Out	Function
EventReq	in	Event request
EventAck	out	Event request acknowledge

Table 2.4 IMS T225 link

Pin	In/Out	Function
LinkIn0-3	in	Four serial data input channels
LinkOut0-3	out	Four serial data output channels
LinkSpecial	in	Select non-standard speed as 5 or 20 Mbits/sec
Link0Special	in	Select special speed for Link 0
Link123Special	in	Select special speed for Links 1,2,3

Signal names are prefixed by **not** if they are active low, otherwise they are active high.
Pinout details for various packages are given on page 459.

3 Instruction set summary

The instruction set of the IMS T225 is the same as that of the IMS T222 with a number of additions. The instructions additional to those of the IMS T222 are listed below.

The load device identity (*lddevid*) instruction (table 3.4) pushes the device type identity into the A register. Each product is allocated a unique group of numbers for use with the *lddevid* instruction. The product identity numbers for the IMS T225 are 40 to 49 inclusive.

Table 3.5 contains a number of instructions to facilitate the implementation of breakpoints. These instructions overload the operation of *j0*. Normally *j0* is a no-op which might cause descheduling. *Setj0break* enables the breakpointing facilities and causes *j0* to act as a breakpointing instruction. When breakpointing is enabled, *j0* swaps the current **Iptr** and **Wptr** with an **Iptr** and **Wptr** stored above MemStart. The breakpoint instruction does not cause descheduling, and preserves the state of the registers. It is possible to single step the processor at machine level using these instructions. Refer to *Support for debugging/breakpointing in transputers* (technical note 61) for more detailed information regarding debugger support.

Table 3.1 IMS T225 arithmetic/logical operation codes

Operation Code	Memory Code	Mnemonic	Processor Cycles	Name	D E
08	F8	prod	**b**+4 **m**+5	product for positive register *A* product for negative register *A*	

Table 3.2 IMS T225 general operation codes

Operation Code	Memory Code	Mnemonic	Processor Cycles	Name	D E
5A	25FA	dup	1	duplicate top of stack	
79	27F9	pop	1	pop processor stack	

Table 3.3 IMS T225 CRC and bit operation codes

Operation Code	Memory Code	Mnemonic	Processor Cycles	Name	D E
74	27F4	crcword	35	calculate crc on word	
75	27F5	crcbyte	11	calculate crc on byte	
76	27F6	bitcnt	**b**+2	count bits set in word	
77	27F7	bitrevword	36	reverse bits in word	
78	27F8	bitrevnbits	**n**+4	reverse bottom n bits in word	

Table 3.4 IMS T225 processor initialisation operation codes

Operation Code	Memory Code	Mnemonic	Processor Cycles	Name	D E
17C	2127FC	lddevid	1	load device identity	
7E	27FE	ldmemstartval	1	load value of memstart address	

Table 3.5 IMS T225 debugger support codes

Operation Code	Memory Code	Mnemonic	Processor Cycles	Name	D E
0	00	jump 0	3	jump 0 (break not enabled)	D
			11	jump 0 (break enabled, high priority)	
			13	jump 0 (break enabled, low priority)	
B1	2BF1	break	9	break (high priority)	
			11	break (low priority)	
B2	2BF2	clrj0break	1	clear jump 0 break enable flag	
B3	2BF3	setj0break	1	set jump 0 break enable flag	
B4	2BF4	testj0break	2	test jump 0 break enable flag set	
7A	27FA	timerdisableh	1	disable high priority timer interrupt	
7B	27FB	timerdisablel	1	disable low priority timer interrupt	
7C	27FC	timerenableh	6	enable high priority timer interrupt	
7D	27FD	timerenablel	6	enable low priority timer interrupt	

4 Package specifications

4.1 68 pin grid array package

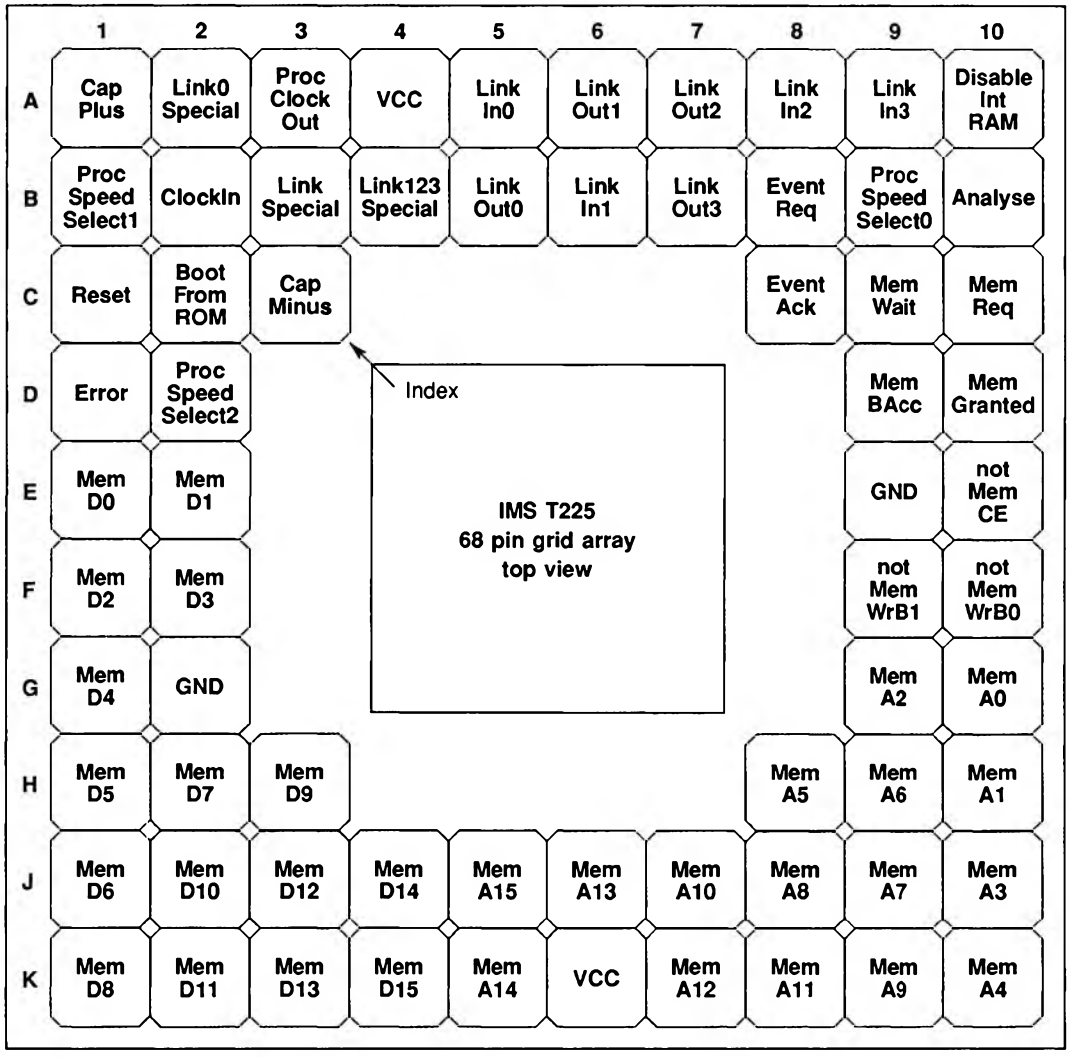


Figure 4.1 IMS T225 68 pin grid array package pinout

Details of the 68 pin grid array package dimensions are given on page 449

4.2 68 pin PLCC J-bend package

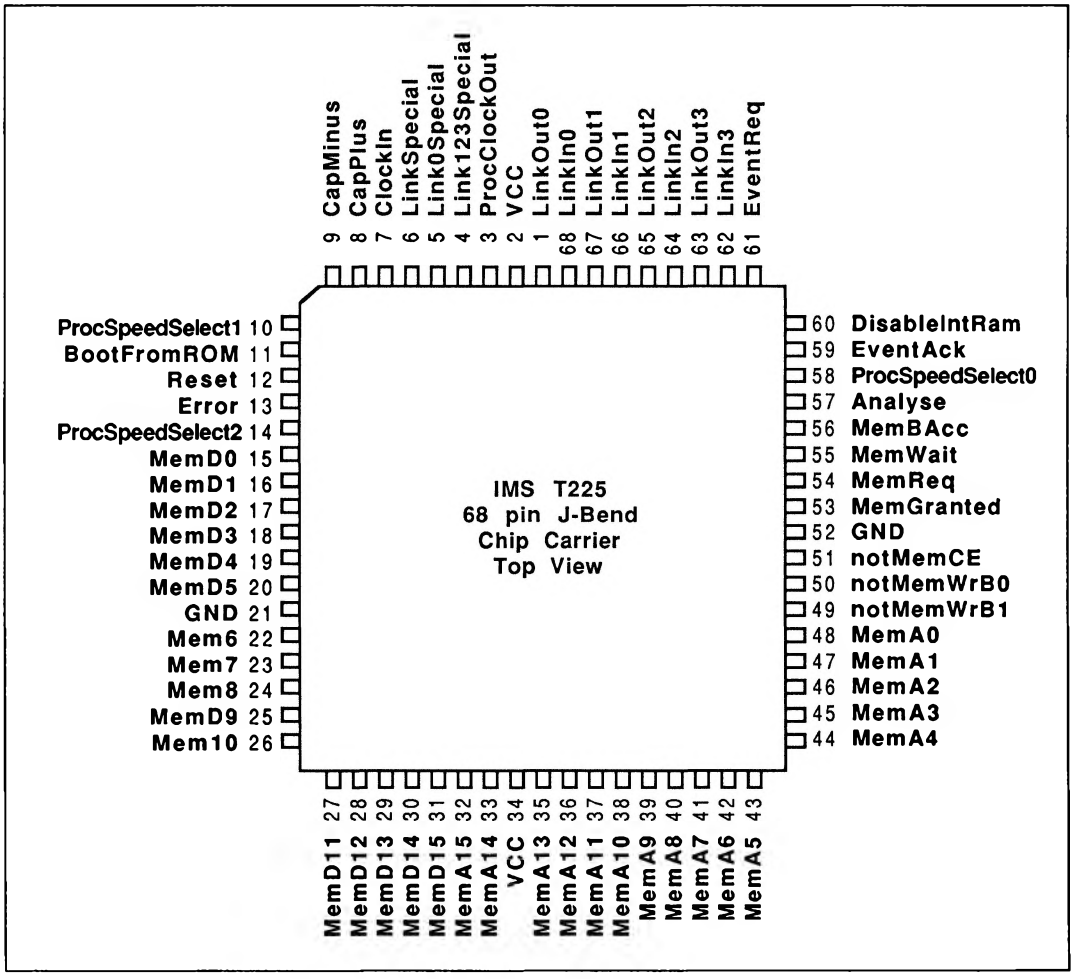


Figure 4.2 IMS T225 68 pin PLCC J-bend package pinout

Details of the 68 pin PLCC J-bend package dimensions are given on page 451.

5 Ordering

This section indicates the designation of speed and package selections for the various devices. Speed of **ClockIn** is 5 MHz for all parts. Transputer processor cycle time is nominal; it can be calculated more exactly using the phase lock loop factor **PLLx**, as detailed in the external memory section.

For availability contact local INMOS sales office or authorised distributor.

Table 5.1 IMS T225 ordering details

INMOS designation	Processor clock speed	Processor cycle time	PLLx	Package
IMS T225-G17S	17.5 MHz	57 ns	3.5	Ceramic Pin Grid
IMS T225-G20S	20.0 MHz	50 ns	4.0	Ceramic Pin Grid
IMS T225-G25S	25.0 MHz	40 ns	5.0	Ceramic Pin Grid
IMS T225-G30S	30.0 MHz	33 ns	6.0	Ceramic Pin Grid
IMS T225-J17S	17.5 MHz	57 ns	3.5	Plastic J-Bend
IMS T225-J20S	20.0 MHz	50 ns	4.0	Plastic J-Bend