IMS1420M
High Performance 4Kx4 Static RAM MIL-STD-883C

FEATURES

- Full Military Temperature Operating Range (-55° C to + 125° C)
- MIL-STD-883C Processing
- 4Kx4 Bit Organisation
- 55 and 70 nsec Access Times
- Fully TTL Compatible
- Common Data Input and Output
- Three-state Output
- Power Down Function
- Single +5V ± 10% Operation
- 20-Pin, 300-mil DIP (JEDEC Std.)
- 20-Pin Ceramic LCC (JEDEC Std.)

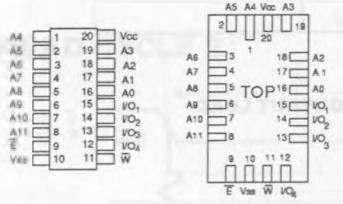
DESCRIPTION

The INMOS IMS1420M is a high performance 4Kx4 Static RAM processed in full compliance to MIL-STD-883C with access times of 55ns and 70ns and a maximum power consumption of 660mW. These characteristics are made possible by the combination of innovative circuit design and INMOS' proprietary NMOS technology.

The IMS1420M features fully static operation requiring no external clocks or timing strobes with equal access and cycle times. Additionally, the IMS1420M provides a Chip Enable (/E) function that can be used to place the device into a low-power standby mode reducing consumption to less than 165mW.

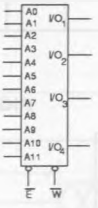
The IMS1420M is a high speed VLSI RAM intended for military applications which demand high performance and reliability.

PIN CONFIGURATION

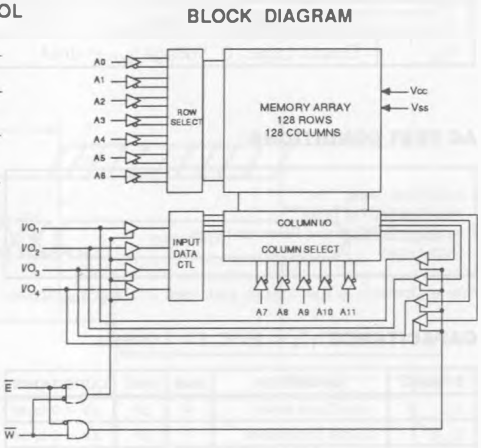


DIP CHIP CARRIER

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0 - A_{11}	ADDRESS INPUTS	Vcc POWER (+5V)
$\overline{W}$	WRITE ENABLE	Vss GROUND
$\overline{E}$	CHIP ENABLE	
I/O	DATA IN/OUT	

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} ..... −3.5 to 7.0V
Temperature Under Bias..... −65°C to 135°C
Storage Temperature (Ambient)..... −65°C to 150°C
Power Dissipation..... 1W
DC Output Current..... 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.4		6.0	V	All Inputs
V_{IL}	Input Logic "0" Voltage	−2.0		0.8	V	All Inputs
T_A	Ambient Operating Temperature	−55		125	°C	400 Linear ft/min transverse air flow

DC ELECTRICAL CHARACTERISTICS ($-55°C \leq T_A \leq 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current AC		120	mA	$t_C = t_C$ min
I_{CC2}	V_{CC} Power Supply Current (Standby)		30	mA	$\overline{E} \geq V_{IH}$ min
I_{IN}	Input Leakage Current (Any Input)	−10	10	μA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off State Output Leakage Current	−50	50	μA	V_{CC} = max $V_{OUT} = V_{SS}$ to V_{CC}
V_{OH}	Output Logic "1" Voltage $I_{OUT} = -4mA$	2.4		V	
V_{OL}	Output Logic "0" Voltage $I_{OUT} = 8mA$		0.4	V	

AC TEST CONDITIONS[a]

Input Pulse Levels	V_{SS} to 3V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Figure 1

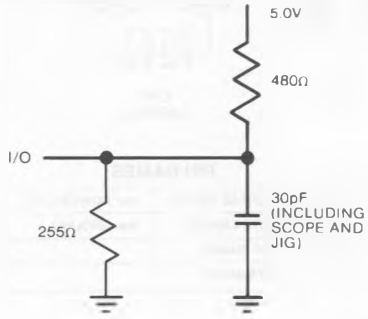
Note a: Operation to specifications guaranteed 2ms after V_{CC} applied

CAPACITANCE[b] ($T_A = 25°C$, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNIT	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V
$C_{\overline{E}}$	$\overline{E}$ Capacitance	6	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested

FIGURE 1. OUTPUT LOAD



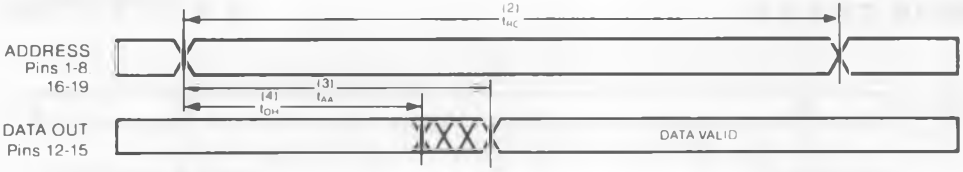
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \leq T_A \leq 125°C$) ($V_{CC}$ = 5.0V ± 10%)

READ CYCLE

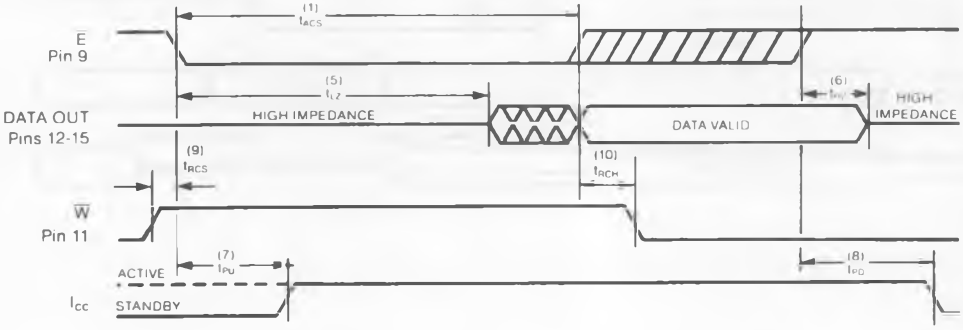
NO.	SYMBOL	PARAMETER	IMS1420M-55		IMS1420M-70		UNITS	NOTES
			MIN	MAX	MIN	MAX		
1	t_{ACS}	Chip Enable Access Time		55		70	ns	
2	t_{RC}	Read Cycle Time	55		70		ns	c
3	t_{AA}	Address Access Time		55		70	ns	d
4	t_{OH}	Output Hold After Address Change	3		3		ns	j
5	t_{LZ}	Chip Enable to Output Active	15		15		ns	j
6	t_{HZ}	Chip Disable to Output Disable		25		30	ns	f
7	t_{PU}	Chip Enable to Power Up	0		0		ns	j
8	t_{PD}	Chip Disable to Power Down	0	55	0	70	ns	j
9	t_{RCS}	Read Command Set-up Time	−5		−5		ns	
10	t_{RCH}	Read Command Hold Time	−5		−5		ns	
	t_T	Input Rise and Fall Times		50		50	ns	e

Note c: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected, $\overline{E}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ±200mV from steady state output voltage.
Note j: Parameter guaranteed but not tested.

READ CYCLE 1 [c, d]



READ CYCLE 2 [c]



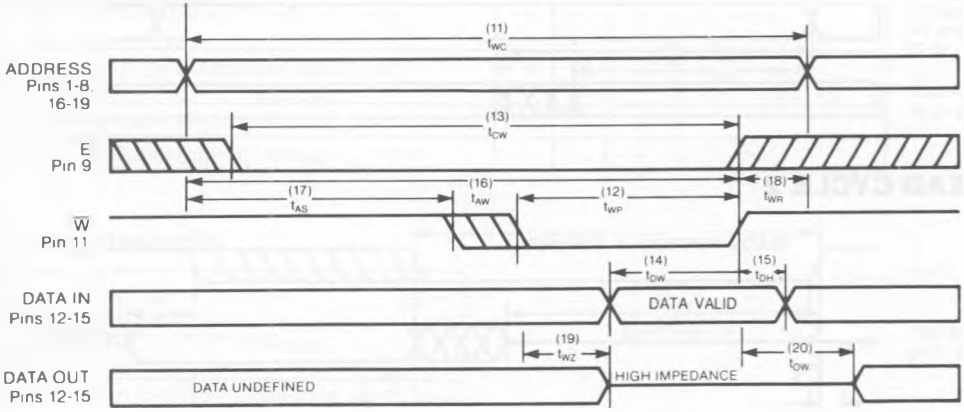
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \leq T_A \leq 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[h]

NO.	SYMBOL	PARAMETER	IMS1420M-55		IMS1420M-70		UNITS	NOTES
			MIN	MAX	MIN	MAX		
11	t_{WC}	Write Cycle Time	55		70		ns	
12	t_{WP}	Write Pulse Width	45		65		ns	
13	t_{CW}	Chip Enable to End of Write	45		65		ns	
14	t_{DW}	Data Set-up to End of Write	25		30		ns	
15	t_{DH}	Data Hold After End of Write	3		5		ns	
16	t_{AW}	Address Set-up to End of Write	45		65		ns	
17	t_{AS}	Address Set-up to Beginning of Write	0		0		ns	
18	t_{WR}	Address Hold After End of Write	5		5		ns	
19	t_{WZ}	Write Enable to Output Disable	0	25	0	30	ns	f
20	t_{OW}	Output Active After End of Write	0		0		ns	g

Note f: Measured ± 200mV from steady state output voltage.
Note g: If $\overline{E}$ goes high with $\overline{W}$ low, Output remains in HIGH impedance state.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.

WRITE CYCLE 1



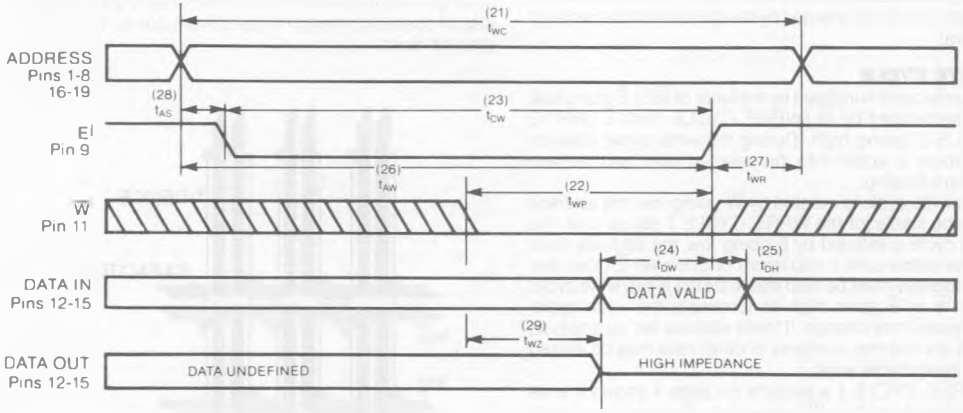
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \leq T_A \leq 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 2: $\overline{E}$ CONTROLLED[h]

NO.	SYMBOL	PARAMETER	IMS1420M-55		IMS1420M-70		UNITS	NOTES
			MIN	MAX	MIN	MAX		
21	t_{WC}	Write Cycle Time	55		70		ns	
22	t_{WP}	Write Pulse Width	45		65		ns	
23	t_{CW}	Chip Enable to End of Write	45		65		ns	
24	t_{DW}	Data Set-up to End of Write	25		30		ns	
25	t_{DH}	Data Hold After End of Write	5		5		ns	
26	t_{AW}	Address Set-up to End of Write	40		60		ns	
27	t_{WR}	Address Hold After End of Write	5		5		ns	
28	t_{AS}	Address Set-up to Beginning of Write	−5		−5		ns	
29	t_{WZ}	Write Enable to Output Disable	0	25	0	30	ns	f

Note f: Measured ± 200mV from steady state output voltage.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.

WRITE CYCLE 2



DEVICE OPERATION

The IMS1420M has two control inputs, Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$), twelve address inputs, and four Data I/O lines.

When V_{CC} is first applied to pin 20, a circuit associated with the $\overline{E}$ input forces the device into the lower power standby mode regardless of the state of the $\overline{E}$ input. After V_{CC} is applied for 2ms the $\overline{E}$ input controls device selection as well as active and standby modes.

With $\overline{E}$ low, the device is selected and the twelve address inputs are decoded to select one 4-bit word out of 4096. READ and WRITE operations on the memory cell are controlled by $\overline{W}$ input. With $\overline{E}$ high, the device is deselected, the output is disabled, and the power consumption is reduced to less than one-third of the active mode power.

READ CYCLE

A read cycle is defined as $\overline{W} \geq V_{IH}$ min with $\overline{E} \leq V_{IL}$ max. Read access time is measured from either $\overline{E}$ going low or from valid address.

The READ CYCLE 1 waveform on page 3 shows a read access that is initiated by a change in the address inputs while $\overline{E}$ is low. The output remains active throughout READ CYCLE 1 and is valid at the specified address access time. The address inputs may change at access time and the output remains valid for a minimum of 3ns. As long as $\overline{E}$ remains low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform on page 3 shows a read access that is initiated by $\overline{E}$ going low. As long as address is stable within 5ns after $\overline{E}$ goes low, valid data is at the output at the specified Chip Enable access time. If address is not valid within 5ns after $\overline{E}$ goes low, the timing is as specified in the READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE

A write cycle is initiated by the latter of $\overline{W}$ or $\overline{E}$ going low, and terminated by $\overline{W}$ (WRITE CYCLE 1) or $\overline{E}$ (WRITE CYCLE 2) going high. During the write cycle, data on the inputs is written into the selected cells, and the outputs are floating.

If a write cycle is initiated by $\overline{W}$ going low, the address must be stable for the WRITE CYCLE 1 set-up time. If a write cycle is initiated by $\overline{E}$ going low, the address need not be stable until a maximum of 5ns after $\overline{E}$ goes low. The address must be held stable for the entire write cycle. After $\overline{W}$ or $\overline{E}$ goes high to terminate the write cycle, addresses may change. If these address set-up and hold times are not met, contents of other cells may be altered in unpredictable ways.

WRITE CYCLE 1 waveform on page 4 shows a write cycle terminated by $\overline{W}$ going high. D_{IN} set-up and hold times are referenced to the rising edge of $\overline{W}$. With $\overline{W}$ high, the outputs become active. When $\overline{W}$ goes high at the end of a write cycle and the outputs of the memory go active, the data from the memory will be the same as the data just written into the memory. Thus, no data bus contention will occur.

WRITE CYCLE 2 waveform on page 5 shows a write cycle terminated by $\overline{E}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{E}$. With $\overline{E}$ high, the outputs remain in the high impedance state.

APPLICATION

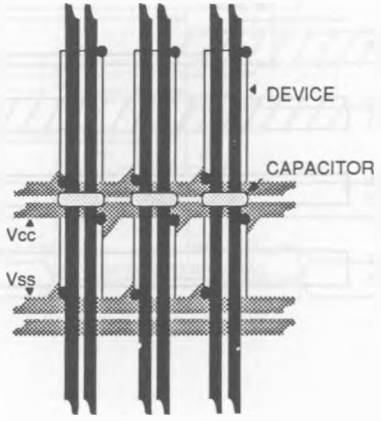
Fundamental rules in regard to memory board layout should be followed to ensure maximum benefit from the features offered by the IMS1420M Static RAM.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the operating margins of the IMS1420M. The impedance in the decoupling path from the power pin (20) through the decoupling capacitor, to the ground pin (10) should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Since the current transients associated with the operation of the high speed IMS1420M are high frequency, the line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor acts as a low impedance power supply located near the memory device. The high frequency decoupling capacitor should have a value of 0.1μF, and be placed between the rows of memory devices in the array (see drawing). A larger tantalum capacitor with a value between 22μF and 47μF should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path.

The ground grid of the memory array should extend to the TTL driver periphery circuit. This will provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.



V_{CC}, V_{SS} GRID SHOWING DECOUPLING CAPACITORS

TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

The recommended technique is to use series termination. The series termination technique has the advantage of drawing no DC current and using a minimum of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The line should be kept short by placing the driver-termination combination close to the memory array.

Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10Ω to 30Ω range will be required.

Proper power distribution techniques, including adequate use of decoupling capacitors, and proper termination of TTL drive outputs, are some of the most important, yet basic guidelines that need to be followed when designing and building a memory board. The guidelines are intended to maintain the operating margins of all devices on the memory board by providing a quiet environment free of noise spikes and signal reflections.

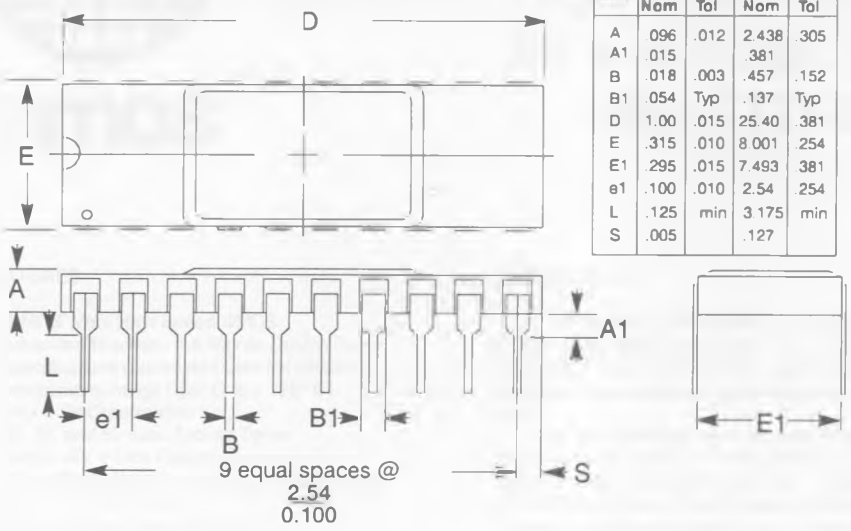
Type	Package	Lead finish
A	Formed flat-pack	gold
B	Formed flat-pack	solder
C	LCC	gold
D	Cerdip	solder
E	Small outline, J-bend	solder
G	PGA	gold
H	Small outline, Gull wing	solder
J	PLCC, J-bend	solder
K	Sidebraze ceramic DIP	solder
N	Ceramic LCC	solder
P	Plastic DIP	solder
S	Sidebraze ceramic DIP	gold
T	(Skinny) Flat-pack	solder
W	Ceramic LCC	gold
Y	(Skinny) Flat-pack	gold

ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS 1420M	55ns	CERAMIC DIP	IMS1420S-55M
	55ns	CERAMIC LCC	IMS1420N-55M
	70ns	CERAMIC DIP	IMS1420S-70M
	70ns	CERAMIC LCC	IMS1420N-70M

PACKAGING INFORMATION

20 Pin Ceramic Dual-In-Line



Dim	Inches		mm	
	Nom	Tol	Nom	Tol
A	.096	.012	2.438	.305
A1	.015		.381	
B	.018	.003	.457	.152
B1	.054	Typ	.137	Typ
D	1.00	.015	25.40	.381
E	.315	.010	8.001	.254
E1	.295	.015	7.493	.381
e1	.100	.010	2.54	.254
L	.125	min	3.175	min
S	.005		.127	

20 Pin Leadless Chip Carrier

Dim	Inches		mm		Notes
	Nom	Tol	Nom	Tol	
A	.071	.007	1.803	.178	
B1	.025	.003	.635	.076	
D	.425	.010	10.795	.254	
E	.290	.010	7.360	.254	
e1	.050	.005	1.270