IMS16X5 series High Performance Memory Products

Advance Information

IMS 1605: 64K x 1
IMS 1625: 16K x 4
IMS 1629: 16K x 4 with Output Enable
IMS 1626/7: 16K x 4 with Separate I/Os
IMS 1635: 8K x 8
IMS 1695: 8K x 9

FEATURES

- INMOS' Very High Speed Double Metal CMOS
- Advanced Process-1.2 Micron Design Rules
- 64K Bit Devices
- 15, 20 and 25 ns Address Access Times
- 15, 20 and 25 ns Chip Enable Access Times
- Fully TTL Compatible
- Single +5V ± 10% Operation
- Battery Backup Operation - 2V Data Retention, 10µA typical at 25°C
- Packages include: DIP, LCC and SOJ
- Military Versions Available

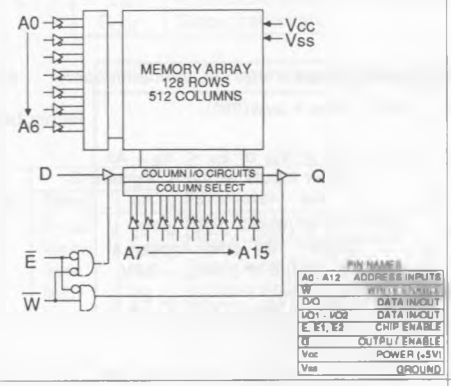
DESCRIPTION

The INMOS IMS16X5 series are high speed advanced 64K double layer metal CMOS Static RAMs.

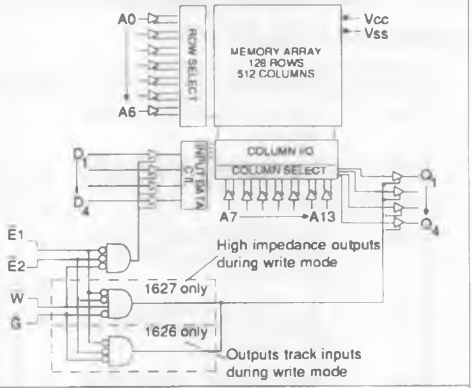
The range features fully static operation requiring no external clocks or timing strobes, with equal access and cycle times. A chip enable function ($\overline{E}$) that can be used to place the device into a low-power standby mode is available on all organisations. The 8K x 8 organisations provide an additional Chip Enable for reduced low-power standby mode. Output Enable ($\overline{G}$) is an enhancement on organisations requiring fast access to data and enhanced bus contention control.

Military versions of the 16X5 are also available.

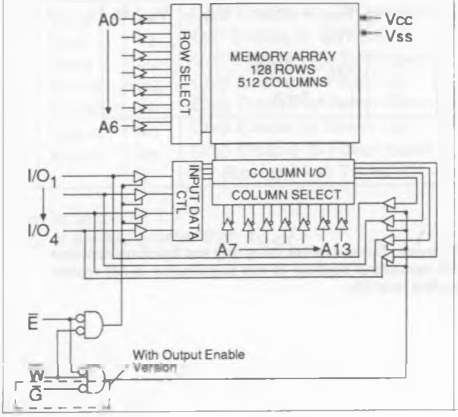
64K x 1



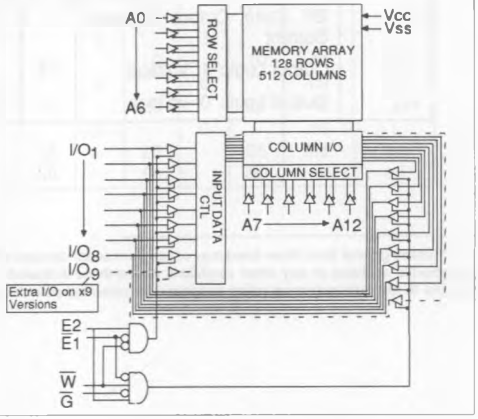
16K x 4 (Separate Inputs and Outputs)



16K x 4 (Without and with Output Enable)



8K x 8 / 8K x 9



2.1 Electrical specifications

2.1.1 Absolute maximum ratings[1]

Symbol	Parameter	Min	Max	Unit	
V_{SS}	Value on relative pin	−2.0	7.0	V	
	Voltage on I/O	−1.0	V_{CC} +0.5	V	
T_A	Temperature under bias	−55	125	°C	(One output at a time, one second duration)
	Storage temperature	−65	150	°C	
	Power dissipation		1	W	
	DC output current		25	mA	

2.1.2 DC operating conditions

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic '1' Voltage	2.0		V_{CC} + 0.5	V	All inputs
V_{IL}	Input Logic '0' Voltage	−0.5*		0.8	V	All inputs
T_A	Ambient Operating Temperature	0		70	°C	400 linear ft/min air flow

*V_{IL} min. = −3.0V for pulse width <10ns, note b

2.1.3 DC electrical characteristics ($0°C \leq T_A \leq 70°C$)($V_{CC} = 5.0V \pm 10\%$)[a]

For suffixes refer to section 2.1.7.

Symbol	Parameter	Min	Max	Units	Notes
I_{CC1}	Average V_{CC} Power Supply Current		100	mA	$t_{AVAV} = t_{AVAV}$(min).
I_{CC2}	V_{CC} Power Supply Current (Standby, Stable TTL Input Levels)		40	mA	$\overline{E}_1 \geq V_{IH}$ or $E_2 \leq V_{IL}$. All other inputs at $V_{IN} \leq V_{IL}$ or $\geq V_{IH}$.
I_{CC3}	V_{CC} Power Supply Current (Standby, Stable CMOS Input Levels)		2	mA	$\overline{E}_1 \geq (V_{CC} - 0.2V)$ or $E_2 \leq 0.2V$. All other inputs at $V_{IN} \leq 0.2$ or $\geq (V_{CC} - 0.2V$.
I_{CC4}	V_{CC} Power Supply Current (Standby, Cycling CMOS Input Levels)		25	mA	$\overline{E}_1 \geq (V_{CC} - 0.2V)$ or $E_2 \leq 0.2V$. Inputs cycling at $V_{IN} \leq 0.2$ or $\geq (V_{CC} - 0.2V$.
I_{ILK}	Input Leakage Current (any input)		±1	μA	V_{CC} = max. $V_{IN} = V_{SS}$ to V_{CC}.
I_{OLK}	Off State Output Leakage Current		±5	μA	V_{CC} = max. $V_{IN} = V_{SS}$ to V_{CC}.
V_{OH}	Output Logic '1' Voltage	2.4		V	$I_{OH} = -4mA$.
V_{OL}	Output Logic '0' Voltage		0.4	V	$I_{OL} = 8mA$.

[1]Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2.1.4 AC test condition

Input pulse levels	V_{SS} to 3.0V
Input rise and fall times	5ns
Input and output timing reference levels	1.5V
Output load	see figure 2.1

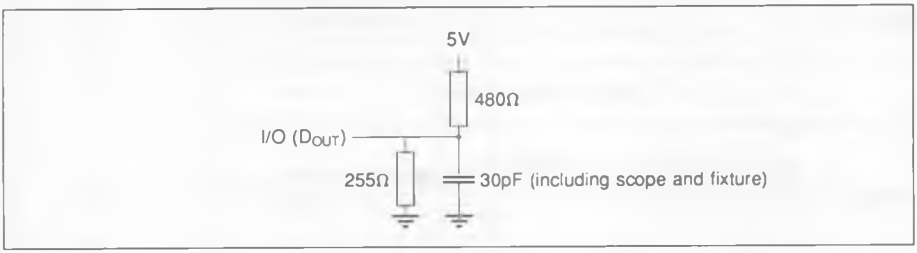


Figure 2.1 Output load

2.1.5 Capacitance[b]

Symbol	Parameter	Min	Max	Units	Conditions
C_{IN}	Input capacitance		5	pF	ΔV = 0 to 3.0V
C_{OUT}	Output capacitance		7	pF	ΔV = 0 to 3.0V

2.1.6 Recommended AC operating conditions ($0°C \leq T_A \leq 70°C$)(V_{CC} = 5.0V ± 10%)

Read cycle[g]

No.	Symbol Stand.	Symbol Alt.	Parameter	16X5-15 min	16X5-15 max	16X5-20 min	16X5-20 max	16X5-25 min	16X5-25 max	Units	Notes*
1	t_{E1LQV}	t_{ACS}	Chip Enable Access Time		15		20		25	ns	
2	t_{E2HQV}	t_{ACS}	Chip Enable Access Time		15		20		25	ns	
3	t_{AVAV}	t_{RC}	Read Cycle Time	15		20		25		ns	c
4	t_{AVQV}	t_{AA}	Address Access Time		15		20		25	ns	d
5	t_{GLQV}	t_{OE}	O/P Enable to Data Valid		8		10		10	ns	
6	t_{AXQX}	t_{OH}	O/P Hold After Add's Ch'ge	3		3		3		ns	
7	t_{E1LQX}[1]	t_{LZ}	Chip Enable to O/P Active	8		8		10		ns	
8	t_{E1HQZ}	t_{HZ}	Chip Disable to O/P inactive		8		10		10	ns	f,j
9	t_{E2HQZ}	t_{LZ}	Chip Enable to O/P Active	8		10		10		ns	
10	t_{E2LQZ}	t_{HZ}	Chip Disable to O/P Inactive		8		10		10	ns	f,j
11	t_{GLQX}	t_{LZ}	O/P Enable to O/P Active	3		3		3		ns	
12	t_{GHQZ}	t_{HZ}	O/P Disable to O/P Inactive		8		10		10	ns	f,j
13	$t_{E1LICCH}$	t_{PU}	Chip Enable to Power Up	0		0		0		ns	j
14	$t_{E1LICCL}$	t_{PD}	Chip Disable to Power Down		15		20		25	ns	j
15	$t_{E2HICCH}$	t_{PU}	Chip Enable to Power Up	0		0		0		ns	j
16	$t_{E2LICCL}$	t_{PD}	Chip Disable to Power down		15		20		25	ns	j
17		t_T	I/P Rise and Fall Times		50		50		50	ns	e,j

* Refer to section 2.1.7.
[1] T_{ELQX} is always greater than T_{EHQZ}

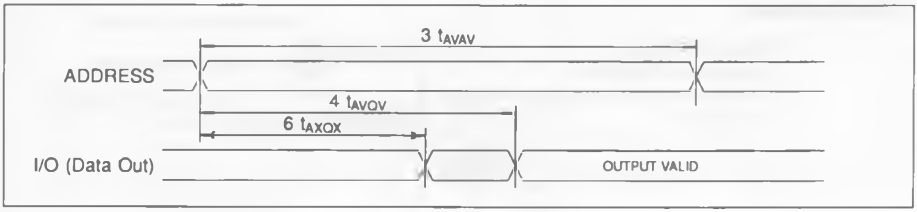


Figure 2.2 Read cycle 1[c,d]

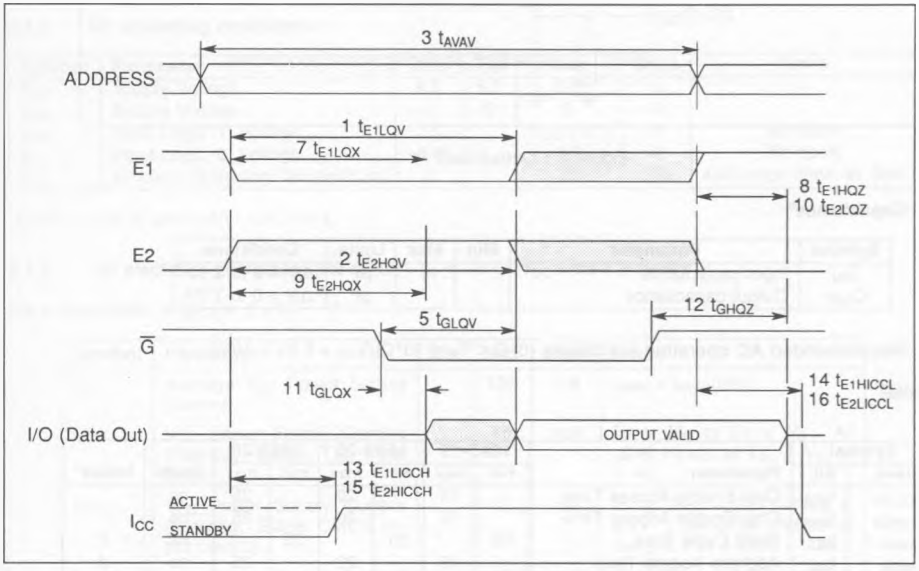


Figure 2.3 Read cycle 2[c]

Write cycle 1: $\overline{W}$ controlled[g,h]

No.	Symbol Stand.	Symbol Alt.	Parameter	16X5-15 min	16X5-15 max	16X5-20 min	16X5-20 max	16X5-25 min	16X5-25 max	Units	Notes*
18	t_{AVAV}	t_{WC}	Write Cycle Time	15		20		25		ns	
19	t_{WLWH}	t_{WP}	Write Pulse Width	12		15		20		ns	
20	t_{E1LWH}	t_{CW}	Chip Enable 1 to End of Write	12		15		20		ns	
21	t_{E2HWH}	t_{CW}	Chip Enable 2 to End of Write	12		15		20		ns	
22	t_{DVWH}	t_{DW}	Data Setup to End of Write	10		12		15		ns	
23	t_{WHDX}	t_{DH}	Data Hold after End of Write	0		0		0		ns	
24	t_{AVWH}	t_{AW}	Address Setup to End of Write	15		15		20		ns	
25	t_{AVWL}	t_{AS}	Address Setup to Start of Write	0		0		0		ns	
26	t_{WHAX}	t_{WR}	Add's Hold After End of Write	0		0		0		ns	
27	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	8	0	10	0	10	ns	f,j
28	t_{WHQX}	t_{OW}	Output Active after End of Write	0		0		0		ns	i,j

Write cycle 2: $\overline{E}1$ or E2 controlled[g,h]

No.	Symbol Stand.	Symbol Alt.	Parameter	16X5-15 min	16X5-15 max	16X5-20 min	16X5-20 max	16X5-25 min	16X5-25 max	Units	Notes*
29	t_{AVAV}	t_{WC}	Write Cycle Time	15		20		25		ns	
30	t_{WLWE1H}	t_{WP}	Write Pulse Width	12		15		20		ns	
31	t_{E1LE1H}	t_{CW}	Chip Enable 1 to End of Write	12		15		20		ns	
32	t_{E2HE2L}	t_{CW}	Chip Enable 2 to End of Write	12		15		20		ns	
33	t_{DVE1H}	t_{DW}	Data Setup to End of Write	10		12		15		ns	
34	t_{E1HDX}	t_{DH}	Data Hold after End of Write	0		0		0		ns	
35	t_{AVE1H}	t_{AW}	Address Setup to End of Write	15		15		20		ns	
36	t_{E1HAX}	t_{WR}	Address Hold after End of Write	0		0		0		ns	
37	t_{AVE1L}	t_{AS}	Address Setup to Start of Write	0		0		0		ns	
38	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	8	0	10	0	10	ns	f,j

* Refer to section 2.1.7.

2.1.7 Notes

Note a: I_{CC} is dependent on output loading and cycle rate, the specified values are obtained with the output unloaded.
Note b: This parameter is sampled and not 100% tested.
Note c: For Read Cycle 1 and 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continually selected, $\overline{E}1$ low $\overline{G}$ low and E2 high.
Note e: Measured between V_{IL} max. and V_{IH} min.
Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}1$, E2, $\overline{G}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}1$ or $\overline{W}$ must be $\geq V_{IH}$ or E2 must be $\leq V_{IL}$ during address transitions.
Note i: If $\overline{W}$ is low when the later of $\overline{E}1$ goes low or E2 goes high, the outputs remain in the high impedance state.
Note j: Parameter guaranteed but not tested.
Note k: Supply recovery rate should not exceed 100mV per 10µs from V_{DR} to V_{CC} min.

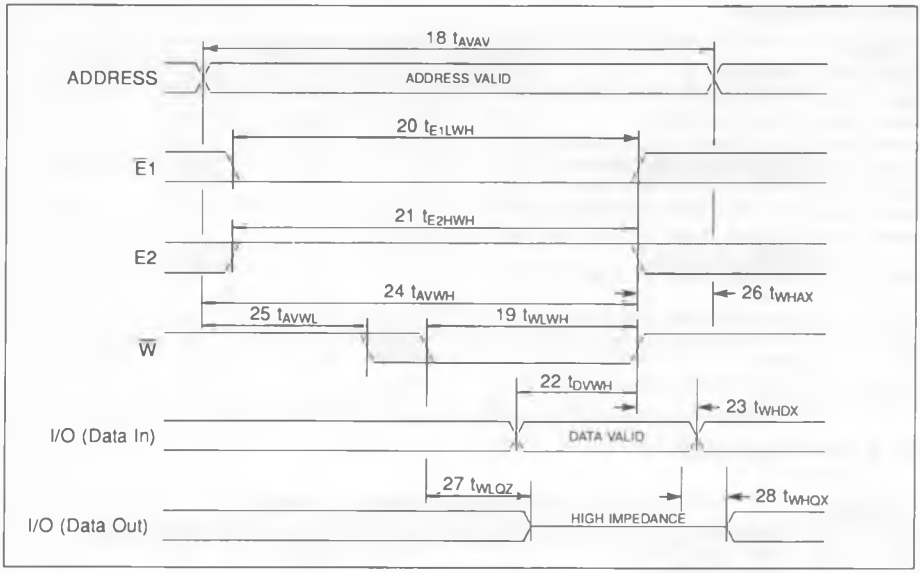


Figure 2.4 WRITE CYCLE 1

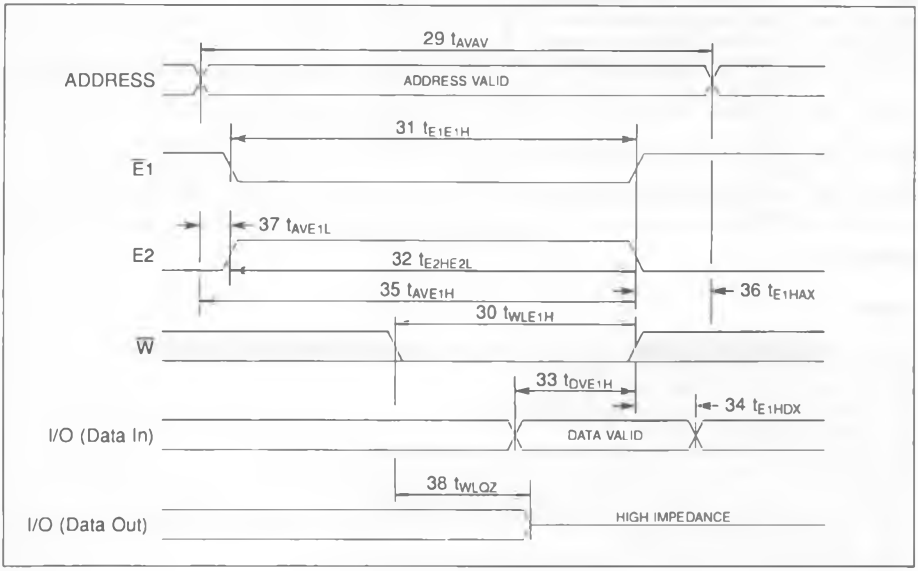


Figure 2.5 WRITE CYCLE 2

2.1.8 Power distribution

Recommended power distribution schemes combine proper power trace layout and placement of decoupling capacitors to maintain the wide operating margins of the IMS 16X5 series. The impedance in the decoupling path from the V_{CC} power pin through the decoupling capacitor to the ground pin should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance/reactance of the decoupling capacitor.

Current transients associated with the operation of high speed memories have very high frequency components, so line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor supplies energy for high frequency current transients and should be located as near the memory as possible, with the shortest lead lengths practical. The high frequency decoupling capacitor should have a minimum value of 0.1μF and be placed between the rows of memory devices in the array. A larger tantalum capacitor for low frquency current transients should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path. The ground grid of the memory array should extend to the TTL driver periphery circuit. This will provide a solid ground reference for the drivers and prevent loss of operating margin due to differential ground noise.

2.1.9 Termination

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the line, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

The recommended series termination technique uses no DC current and a minimum number of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The termination resistor should be placed as close to the driver package as possible. The line should be kept short by placing the driver–termination combination close to the memory array.

Some experimentation will have to be done to find the proper value to use for the series termination to minimise reflections, but generally a series resistor in the 10 to 33Ω range will be required. Because the characteristic impedance of each layout will be different, it is necessary to select the proper value of this resistor by trial and error. A resistor of predetermined value may not properly terminate the transmission line.

Proper power distribution techniques, including adequate use of decoupling capacitors, and proper termination of TTL drive outputs are some of the most important yet basic guidelines that need to be followed when designing and building a memory board. The guidelines are intended to maintain the operating margins of all devices on the memory board by providing a quiet environment free of noise spikes, undershoot, and excessive ringing. It is wise to verify signal fidelity by observation utilizing a wideband oscilloscope and probe.

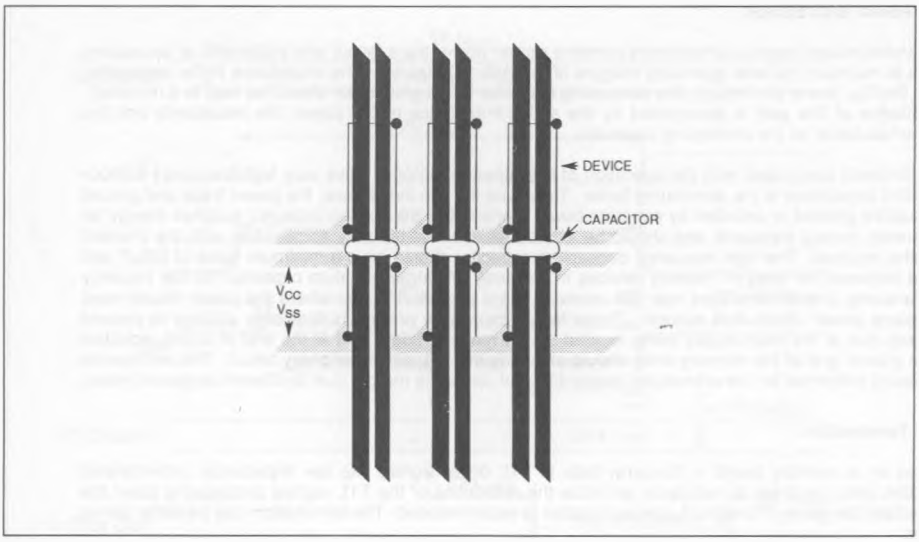


Figure 2.6 Grid showing decoupling capacitors

2.1.10 Data retention (low power versions only)($0°C \leq T_A \leq 70°C$)

Symbol	Parameter	Min	Typ(25°C)	Max	Units	Notes*
V_{DR}	Data Retention Voltage	2.0			V	$V_{IN} \leq 0.2V$ or $\geq (V_{CC}-0.2V)E \geq (V_{CC}-0.2V)$
I_{CCDR1}	Data Retention Current		15	100	µA	$V_{CC} = 3.0V$
I_{CCDR2}	Data Retention Current		10	70	µA	$V_{CC} = 2.0V$
t_{EHVCCL}	Deselect Time (t_{CDR})	0			ns	j,k
t_{VCCHEL}	Recovery Time (t_R)	t_{RC}			ns	j,k (t_{RC} = Read Cycle Time)

* Refer to section 2.1.7.

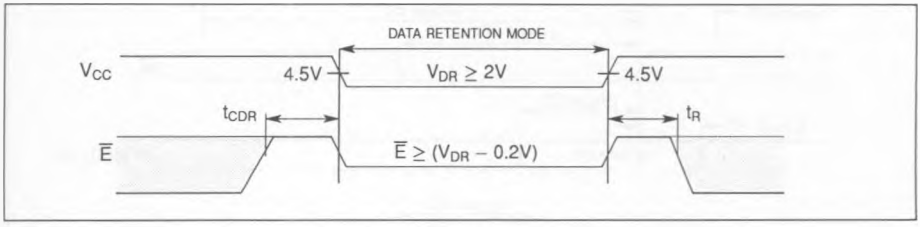


Figure 2.7 Data retention

2.2 Packaging information

2.2.1 Pin-outs and packages

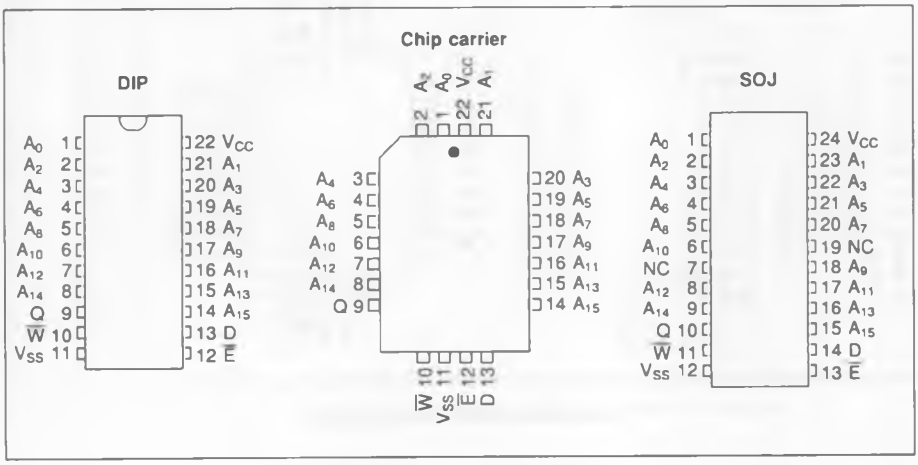


Figure 2.8 64K x 1 pin configuration

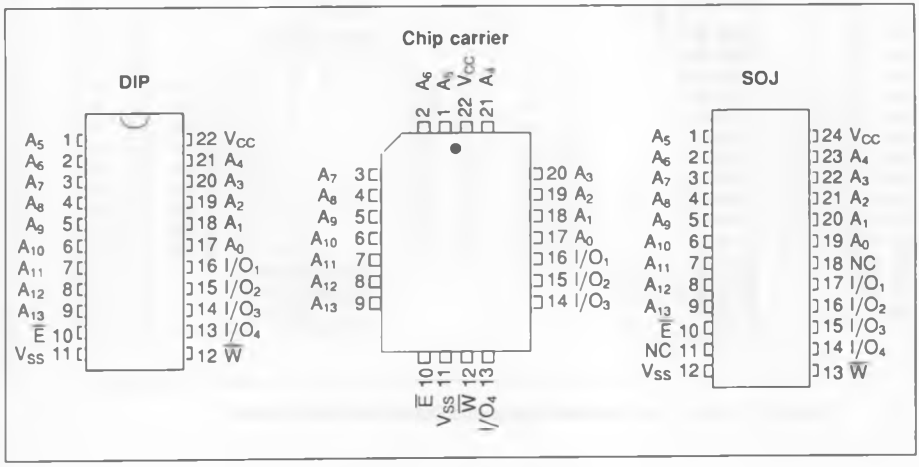


Figure 2.9 16K x 4 pin configuration

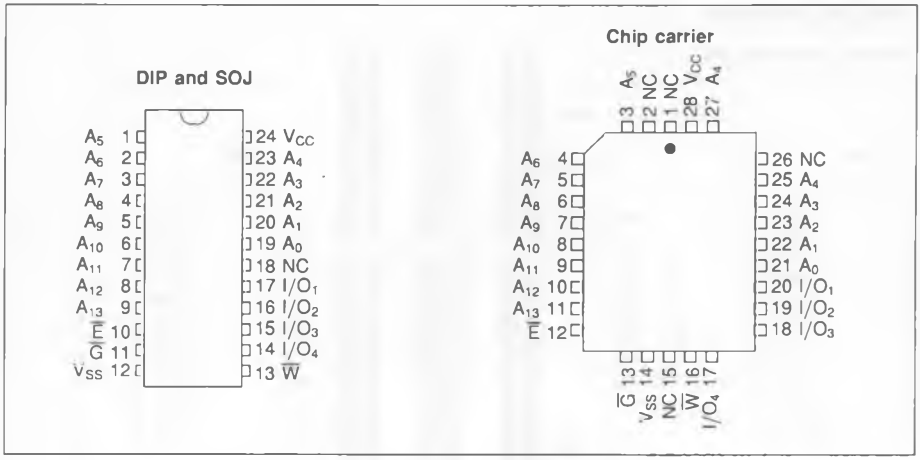


Figure 2.10 16K x 4 (with output enable) pin configuration

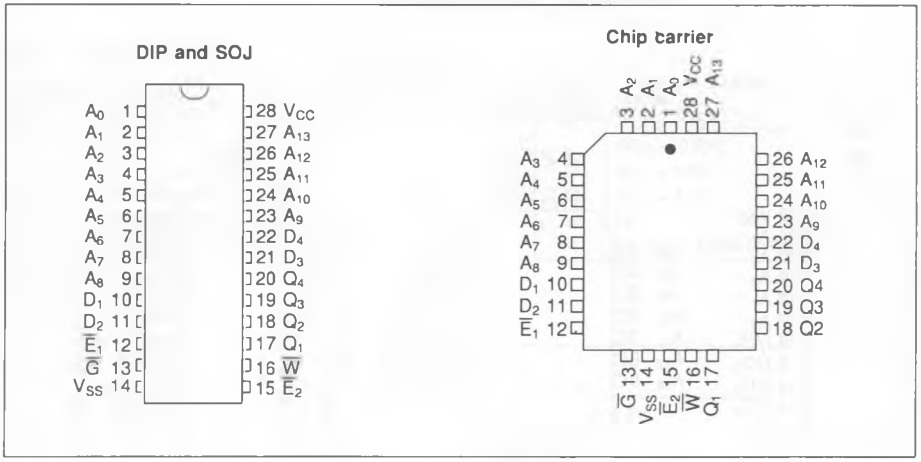


Figure 2.11 16K x 4 (with separate Inputs and Outputs) pin configuration

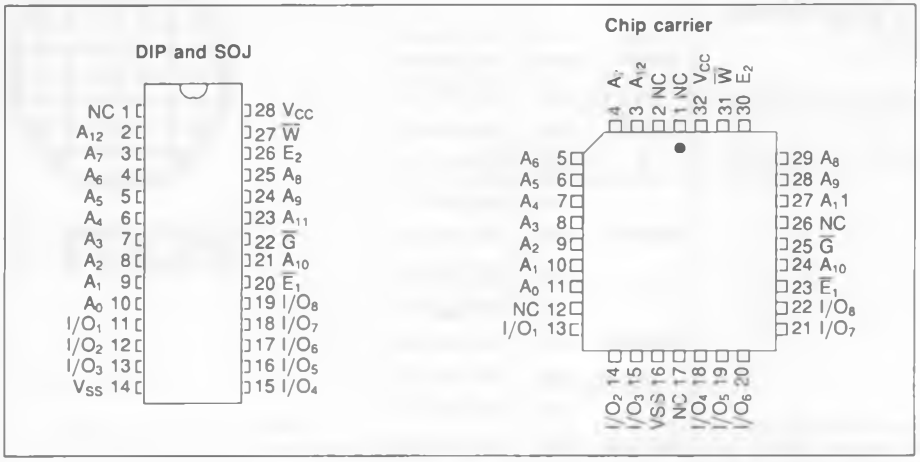


Figure 2.12 8K x 8 pin configuration

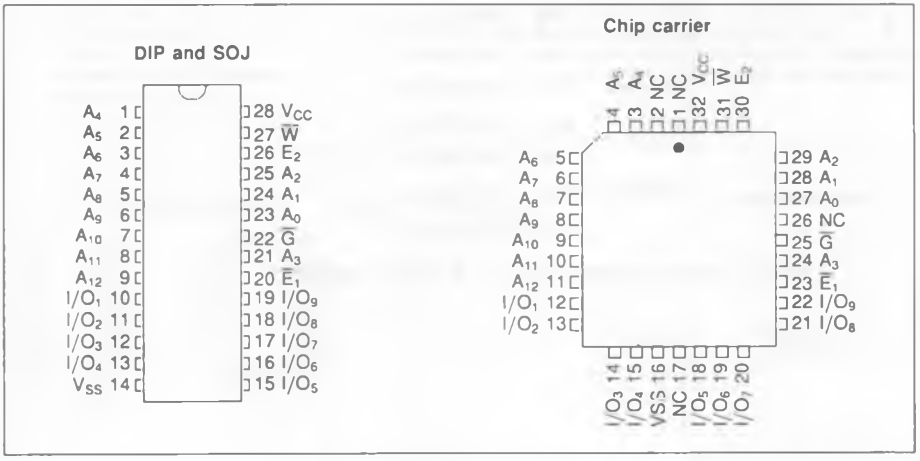


Figure 2.13 8K x 9 pin configuration

2.3 Ordering information

Device	Speed	Part Number
IMS1605	15ns	IMS1605*x*–15
	20ns	IMS1605*x*–20
	25ns	IMS1605*x*–25
IMS1625	15ns	IMS1625*x*–15
	20ns	IMS1625*x*–20
	25ns	IMS1625*x*–25
IMS1629	15ns	IMS1629*x*–15
	20ns	IMS1629*x*–20
	25ns	IMS1629*x*–25
IMS1626	15ns	IMS1626*x*–15
	20ns	IMS1626*x*–20
	25ns	IMS1626*x*–25
IMS1627	15ns	IMS1627*x*–15
	20ns	IMS1627*x*–20
	25ns	IMS1627*x*–25
IMS1635	15ns	IMS1635*x*–15
	20ns	IMS1635*x*–20
	25ns	IMS1635*x*–25
IMS1695	15ns	IMS1695*x*–15
	20ns	IMS1695*x*–20
	25ns	IMS1695*x*–25

Where *x* refers to packages P, S, E, or W. See also Appendix D.