IMS1820
CMOS
High Performance
64K x 4 Static RAM

inmos®

FEATURES

- INMOS' Very High Speed CMOS
- Advanced Process - 1.2 Micron Design Rules
- 64K x 4 Bit Organization
- 25, 30, 35 and 45 ns Address Access Times
- 25, 30, 35 and 45 ns Chip Enable Access Times
- Fully TTL Compatible
- Common Data Input and Outputs
- Three-state Outputs
- 24 Pin 300-mil DIP, SOJ and 28 Pin LCC
- Single +5V ± 10% Operation
- Power Down Function

DESCRIPTION

The INMOS IMS1820 is a high performance 64Kx4 CMOS Static RAM. The IMS1820 allows speed enhancements to existing 64K x 4 applications with the additional benefit of reduced power consumption .

The IMS1820 features fully static operation requiring no external clocks or timing strobes, with equal access and cycle times. Additionally, the IMS1820 provides a Chip Enable function (/E) that can be used to place the device into a low power standby mode.

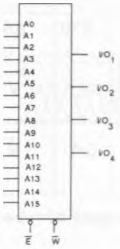
The IMS1820E is an extended temperature version pending military qualification of the IMS1820M.

PIN CONFIGURATION

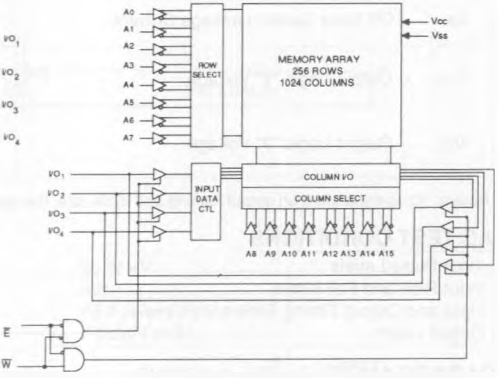
DIP and SOJ

CHIP CARRIER

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0 - A_{15}	ADDRESS INPUTS	Vcc	POWER (+5V)
W	WRITE ENABLE	Vss	GROUND
I/O-I/O	DATA IN/OUT		
E	CHIP ENABLE		

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to Vss.....-2.0 to 7.0V
Voltage on I/O.....-1.0 to (Vcc+0.5V)
Temperature Under Bias.....-55° C to 125°C
Storage Temperature .....-65° C to 150°C
Power Dissipation.....1W
DC Output Current.....25mA
(One output at a time, one second duration)

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		V_{CC} + 0.5	V	All inputs
V_{IL}	Input Logic "0" Voltage	-0.5 *		0.8	V	All inputs
T_A	Ambient Operating Temperature	0		70	°C	400 linear ft/min air flow

* V_{IL} min = -3.0V for pulse width < 10ns, note b

DC ELECTRICAL CHARACTERISTICS ($0°C \le T_A \le 70°C$) ($V_{CC} = 5.0V \pm 10\%$)[a]

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Vcc Power Supply Current		120	mA	tAVAV = tAVAV (min)
I_{CC2}	Vcc Power Supply Current (Standby, Stable TTL Input Levels)		30	mA	E1 ≥ V_{IH} or E2≤V_{IL}. All other inputs at $V_{IN} \le V_{IL}$ or ≥ V_{IH}
I_{CC3}	Vcc Power Supply Current (Standby, Stable CMOS Input Levels)		10	mA	E1 ≥ (Vcc - 0.2V) or E2 ≤ 0.2V. All other inputs at $V_{IN} \le 0.2$ or ≥ (Vcc - 0.2V)
I_{CC4}	Vcc Power Supply Current (Standby, Cycling CMOS Input Levels)		15	mA	E1 ≥ (Vcc - 0.2V) or E2 ≤ 0.2V. Inputs cycling at $V_{IN} \le 0.2$ or ≥ (Vcc - 0.2V)
I_{ILK}	Input Leakage Current (Any Input)		±1	µA	Vcc = max V_{IN} = Vss to Vcc
I_{OLK}	Off State Output Leakage Current		±10	µA	Vcc = max V_{IN} = Vss to Vcc
V_{OH}	Output Logic "1" Voltage	2.4		V	I_{OH} = -4mA
V_{OL}	Output Logic "0" Voltage		0.4	V	I_{OL} = 8mA

Note a: Icc is dependent on output loading and cycle rate, the specified values are obtained with the outputs unloaded.

AC TEST CONDITIONS

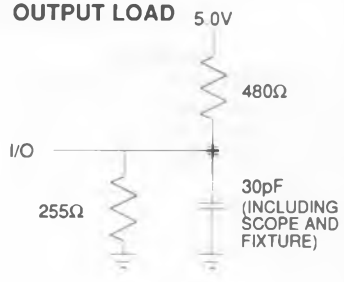
Input Pulse Levels .....Vss to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels..1.5V
Output Load .....See Figure 1

CAPACITANCE[b] (T_A=25°C, f=1.0 MHZ)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	4	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested.

FIGURE 1. OUTPUT LOAD

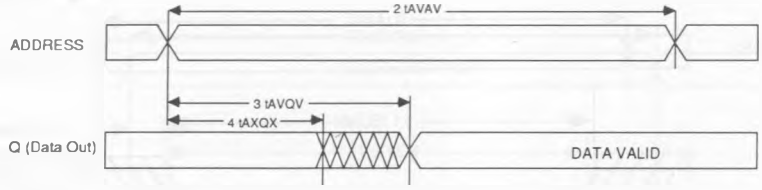


RECOMMENDED AC OPERATING CONDITIONS (0°C ≤ TA ≤ 70°C) (VCC = 5.0V ±10%)
READ CYCLE[g]

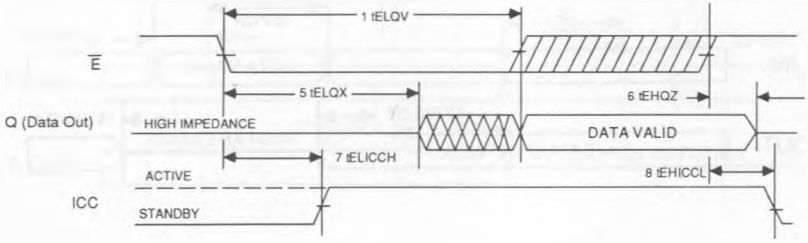
No	SYMBOL Stan'd	SYMBOL Alt.	PARAMETER	IMS 1820-25 MIN	IMS 1820-25 MAX	IMS 1820-30 MIN	IMS 1820-30 MAX	IMS 1820-35 MIN	IMS 1820-35 MAX	IMS 1820-45 MIN	IMS 1820-45 MAX	UNITS	NOTES
1	tELQV	tACS	Chip Enable Access Time		25		30		35		45	ns	
2	tAVAV	tRC	Read Cycle Time	25		30		35		45		ns	c
3	tAVQV	tAA	Address Access Time		25		30		35		45	ns	d
4	tAXQX	tOH	O/P Hold After Addr's Ch'ge	3		3		3		3		ns	
5	tELQX	tLZ	Chip Enable to O/P Active	3		3		3		3		ns	
6	tEHQZ	tHZ	Chip Disable to O/P Inactive	0	12	0	15	0	15	0	20	ns	f,j
7	tELICCH	tPU	Chip Enable to Power Up	0		0		0		0		ns	j
8	tEHICCL	tPD	Chip Enable to Power Down		30		30		30		30	ns	j
		tT	Input Rise and Fall Times		50		50		50		50	ns	e,j

Note c: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected; $\overline{E}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note j: Parameter guaranteed but not tested.

READ CYCLE 1[c,d]



READ CYCLE 2[c]



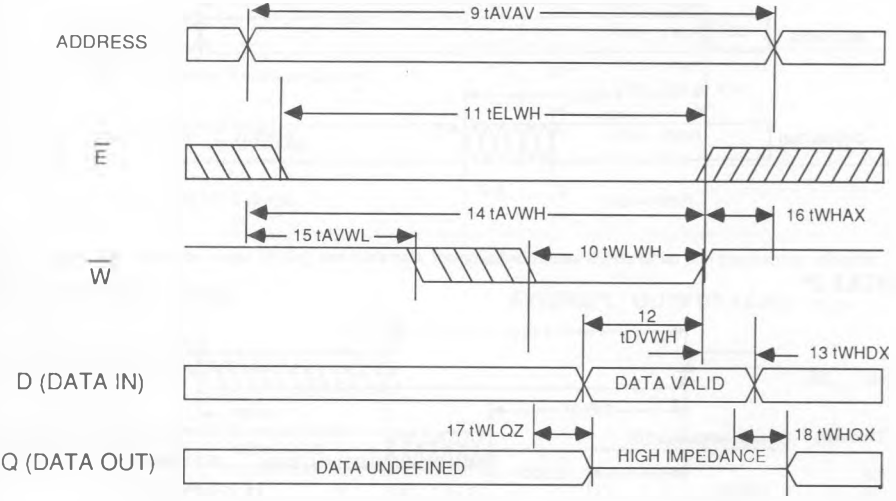
RECOMMENDED AC OPERATING CONDITIONS (0°C ≤ TA ≤ 70°C) (VCC = 5.0V ±10%)

WRITE CYCLE 1: W CONTROLLED[g,h]

No	SYMBOL Stan'd	SYMBOL Alt.	PARAMETER	IMS 1820-25 MIN	IMS 1820-25 MAX	IMS 1820-30 MIN	IMS 1820-30 MAX	IMS 1820-35 MIN	IMS 1820-35 MAX	IMS 1820-45 MIN	IMS 1820-45 MAX	UNITS	NOTES
9	tAVAV	t WC	Write Cycle Time	25		30		35		45		ns	
10	tWLWH	t WP	Write Pulse Width	20		25		30		40		ns	
11	tELWH	t CW	Chip Enable to End of Write	20		25		30		40		ns	
12	tDVWH	t DW	Data Setup to End of Write	10		12		15		20		ns	
13	tWHDX	t DH	Data Hold after End of Write	0		0		0		0		ns	
14	tAVWH	t AW	Address Setup to End of Write	20		25		30		40		ns	
15	tAVWL	t AS	Address Setup to Start of Write	0		0		0		0		ns	
16	tWHAX	t WR	Address Hold after End of Write	2		2		0		0		ns	
17	tWLQZ	t WZ	Write Enable to Output Disable	0	10	0	10	0	15	0	20	ns	f j
18	tWHQX	t OW	Output Active After End of Write	5		5		5		5		ns	i

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: E and W must transition between VIH to VIL or VIL to VIH in a monotonic fashion.
Note h: E, or W must be ≥ VIH during address transitions.
Note i: If W is low when E goes low, the outputs remain in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 1



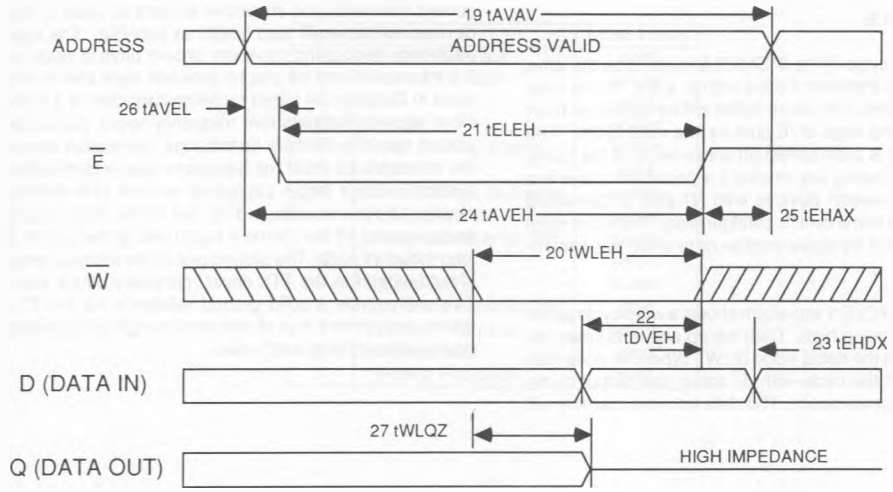
RECOMMENDED AC OPERATING CONDITIONS (0°C < Ta ≤ 70°C) (Vcc = 5.0V ±10%)

WRITE CYCLE 2: E CONTROLLED[g, h]

No	SYMBOL Stan'd	SYMBOL Alt.	PARAMETER	IMS 1820-25 MIN	IMS 1820-25 MAX	IMS 1820-30 MIN	IMS 1820-30 MAX	IMS 1820-35 MIN	IMS 1820-35 MAX	IMS 1820-45 MIN	IMS 1820-45 MAX	UNITS	NOTES
19	tAVAV	t WC	Write Cycle Time	25		30		35		45		ns	
20	tWLEH	t WP	Write Pulse Width	20		25		30		40		ns	
21	tELEH	t CW	Chip Enable to End of Write	20		25		30		40		ns	
22	tDVEH	t DW	Data Setup to End of Write	10		12		15		20		ns	
23	tEHDX	t DH	Data Hold after End of Write	0		0		0		0		ns	
24	tAVEH	t AW	Address Setup to End of Write	20		25		30		40		ns	
25	tEHAX	t WR	Address Hold after End of Write	2		2		0		0		ns	
26	tAVEL	t AS	Address Setup to Start of Write	0		0		0		0		ns	
27	tWLQZ	t WZ	Write Enable to Output Disable	0	10	0	10	0	15	0	20	ns	f,j

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: E and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: E or $\overline{W}$ must be ≥ V_{IH} during address transitions.
Note i: If $\overline{W}$ is low when E goes low, the output remains in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 2



DEVICE OPERATION

The IMS1820 has two control inputs, Chip Enable (/E) and Write Enable (/W), 16 address inputs (A0 -A15), and four data I/O lines.

The /E input controls device selection as well as active and standby modes. With /E low, the device is selected and the 16 address inputs are decoded to select one 4 bit word out of 64K words. Read and Write operations on the memory cell are controlled by the /W input. With /E high, the device is deselected, the output is disabled and the power consumption is reduced to less than one-third of the active mode power with TTL levels and even lower with CMOS levels.

READ CYCLE

A read cycle is defined as /W $\geq$ V_{IH} min with /E $\leq$ V_{IL} max. Read access time is measured from either /E going low or from valid address.

The READ CYCLE 1 waveform shows a read access that is initiated by a change in the address inputs while /E is low. The output remains active throughout READ CYCLE 1 and is valid at the specified address access time. The address inputs may change at access time and long as /E remains low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform shows a read access that is initiated by /E going low. As long as address is stable when /E goes low, valid data is at the output at the specified Chip Enable Access time. If address is not valid when /E goes low, the timing is as specified in READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE

The write cycle of the IMS1820 is initiated by the latter of /E or /W to transition from a high to a low. In the case of /W falling last, the output buffer will be turned on t_{ELQX} after the falling edge of /E (just as in a read cycle). The output buffer is then turned off within t_{WLQZ} of the falling edge of /W. During this interval it is possible to have bus contention between devices with D and Q connected together in a common I/O configuration. Therefore input data should not be active until t_{WLQZ} to aviod bus contention.

WRITE CYCLE 1 waveform shows a write cycle terminated by /W going high. Data set-up and hold times are referenced to the rising edge of /W. When /W goes high at the end of the cycle with /E active, the output of the memory becomes active. The data from the memory will be the same as the input data unless the input data or address changes.

WRITE CYCLE 2 waveform shows a write cycle terminated by /E going high. Data set-up and hold times are referenced to the rising edge of /E. With /E high the output remains in the high impedance state.

APPLICATION

It is imperative when designing with any very high speed memory, such as the IMS1820, that the fundemental rules in regard to memory board layout be followed to ensure proper system operation.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the operating margins of the IMS1820. The impedance in the decoupling path from the power pin through the decoupling capacitor to the ground pin should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Current transients associated with the operation of any high speed device have very high frequency components, so line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor supplies energy for high frequency current transients and should be located as close to the devices with as short lead length as possible. The high frequency decoupling capacitor should have a value of 0.1 microfarad and be placed between each row of devices in the array. A larger tantalum capacitor of a sufficient value to eliminate low frequency ripple, should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path. The ground grid of the memory array should extend to the TTL driver periphery circuit area. This will provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.

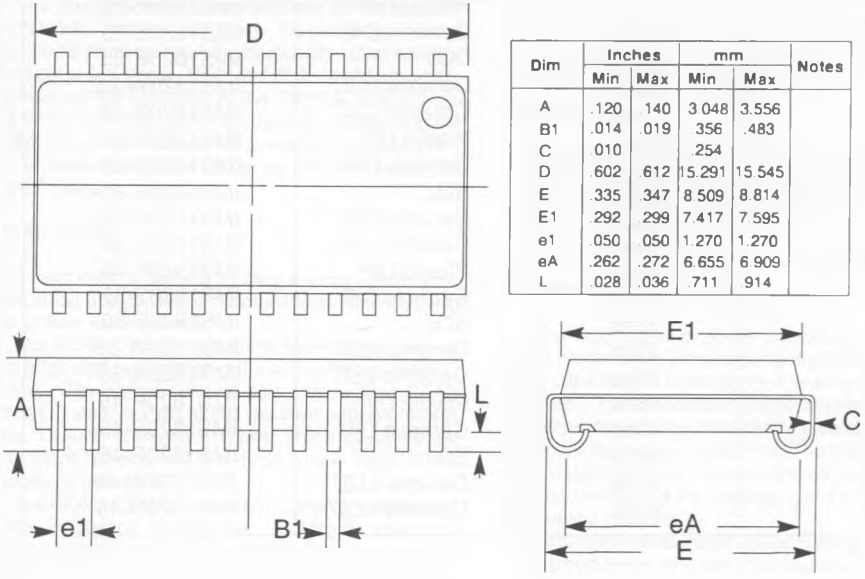
ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS1820	25ns	Plastic DIP	IMS1820P-25
	25ns	Ceramic DIP	IMS1820S-25
	25ns	SOJ	IMS1820E-25
	25ns	Ceramic LCC	IMS1820W-25
	25ns	Ceramic LCC	IMS1820N-25
	30ns	Plastic DIP	IMS1820P-30
	30ns	Ceramic DIP	IMS1820S-30
	30ns	SOJ	IMS1820E-30
	30ns	Ceramic LCC	IMS1820W-30
	30ns	Ceramic LCC	IMS1820N-30
	35ns	Plastic DIP	IMS1820P-35
	35ns	Ceramic DIP	IMS1820S-35
	35ns	SOJ	IMS1820E-35
	35ns	Ceramic LCC	IMS1820W-35
	35ns	Ceramic LCC	IMS1820N-35
	45ns	Plastic DIP	IMS1820P-45
	45ns	Ceramic DIP	IMS1820S-45
	45ns	SOJ	IMS1820E-45
	45ns	Ceramic LCC	IMS1820W-45
	45ns	Ceramic LCC	IMS1820N-45

Type	Package	Lead finish
A	Formed flat-pack	gold
B	Formed flat-pack	solder
C	LCC	gold
D	Cerdip	solder
E	Small outline, J-bend	solder
G	PGA	gold
H	Small outline, Gull wing	solder
J	PLCC, J-bend	solder
K	Sidebraze ceramic DIP	solder
N	Ceramic LCC	solder
P	Plastic DIP	solder
S	Sidebraze ceramic DIP	gold
T	(Skinny) Flat-pack	solder
W	Ceramic LCC	gold
Y	(Skinny) Flat-pack	gold

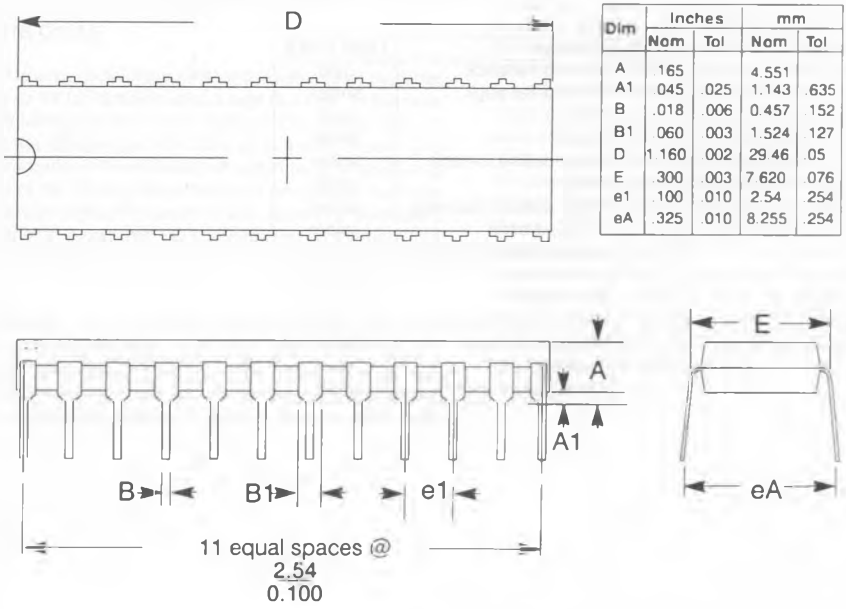
PACKAGING INFORMATION

24 Pin Plastic J Leaded Small Outline



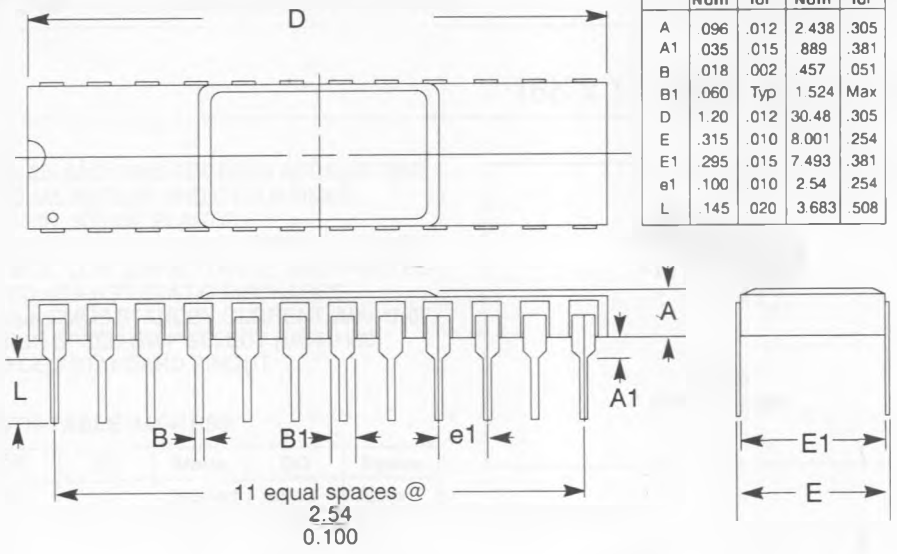
Dim	Inches		mm		Notes
	Min	Max	Min	Max	
A	.120	.140	3.048	3.556	
B1	.014	.019	.356	.483	
C	.010		.254		
D	.602	.612	15.291	15.545	
E	.335	.347	8.509	8.814	
E1	.292	.299	7.417	7.595	
e1	.050	.050	1.270	1.270	
eA	.262	.272	6.655	6.909	
L	.028	.036	.711	.914	

24 Pin Plastic Dual-In-Line



Dim	Inches		mm	
	Nom	Tol	Nom	Tol
A	.165		4.551	
A1	.045	.025	1.143	.635
B	.018	.006	0.457	.152
B1	.060	.003	1.524	.127
D	1.160	.002	29.46	.05
E	.300	.003	7.620	.076
e1	.100	.010	2.54	.254
eA	.325	.010	8.255	.254

24 Pin Ceramic Dual-In-Line



Dim	Inches		mm	
	Nom	Tol	Nom	Tol
A	.096	.012	2.438	.305
A1	.035	.015	.889	.381
B	.018	.002	.457	.051
B1	.060	Typ	1.524	Max
D	1.20	.012	30.48	.305
E	.315	.010	8.001	.254
E1	.295	.015	7.493	.381
e1	.100	010	2.54	.254
L	.145	020	3.683	.508

28 Pin Leadless Chip Carrier

Dim	Inches		mm		Notes
	Nom	Tol	Nom	Tol	
A	.071	.007	1.803	.178	
B1	.025	.003	.635	.076	
D	.550	.010	13.970	.254	
E	.350	.010	8.890	.254	
e1	.050	.002	1.270	.051