±200-V COMMON-MODE VOLTAGE DIFFERENCE AMPLIFIER

Check for Samples: INA148-Q1

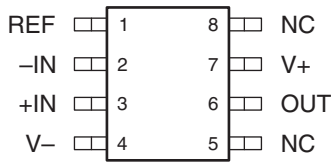
FEATURES

- **Qualified for Automotive Applications**
- **High Common-Mode Voltage**
  - **75 V at V_S = 5 V**
  - **±200 V at V_S = ±15 V**
- **Fixed Differential Gain = 1 V/V**
- **Low Quiescent Current: 260 µA**
- **Wide Supply Range**
  - **Single Supply: 2.7 V to 36 V**
  - **Dual Supplies: ±1.35 V to ±18 V**
- **Low Gain Error: 0.075% Max**
- **Low Nonlinearity: 0.002% Max**
- **High CMR: 86 dB**
- **Surface-Mount SO-8 (D) Package**

APPLICATIONS

- **Current-Shunt Measurements**
- **Differential Sensor Amplifiers**
- **Line Receivers**
- **Battery-Powered Systems**
- **Automotive Instrumentation**
- **Stacked-Cell Monitors**

D PACKAGE
(TOP VIEW)



NC – No internal connection

DESCRIPTION

The INA148 is a precision low-power unity-gain difference amplifier with a high common-mode input voltage range. It consists of a monolithic precision bipolar operational amplifier with a thin-film resistor network.

The on-chip resistors are laser trimmed for an accurate 1-V/V differential gain and high common-mode rejection. Excellent temperature tracking of the resistor network maintains high gain accuracy and common- mode rejection over temperature. The INA148 operates on single or dual supplies.

The INA148 is available in a small SO-8 surface-mount package, and it is specified for operation over the temperature range of –40°C to 125°C.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOIC – D	Reel of 2500	INA148QDRQ1	148Q1

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

V_S	Supply voltage, V+ to V–		36 V
V_{IN}	Input voltage	Continuous	±200 V
		Peak (0.1 second)	±500 V
t_{SS}	Short circuit to ground duration		Continuous
θ_{JA}	Package thermal impedance, junction to free air		97.1°C/W
T_A	Operating free-air temperature range		–40°C to 125°C
T_J	Maximum operating virtual-junction temperature		150°C
T_{stg}	Storage temperature range		–65°C to 150°C
T_{lead}	Lead temperature range (soldering, 10 seconds)		300°C
ESD	Electrostatic discharge rating	Human-Body Model (HBM)	1500 V
		Machine Model (MM)	150 V
		Charged-Device Model (CDM)	2000 V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_S	Supply voltage	Single supply	2.7	36	V
		Dual supply	±1.35	±18	
T_A	Operating free-air temperature		–40	125	°C

ELECTRICAL CHARACTERISTICS

V_S = ±5 V to ±15 V (dual supply), R_L = 10 kΩ to ground, V_{REF} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OS}	Input offset voltage(1) (2)	V_{CM} = 0 V	V_S = ±15 V		±1	±5	mV
			V_S = ±5 V		±1	±5	
$\Delta V_{OS}/\Delta T$	Input offset voltage drift(1)	T_A = –40°C to 125°C			±10		µV/°C
PSRR	Power supply ripple rejection(1)	V_S = ±1.35 V to ±18 V, V_{CM} = 0 V			±50	±400	µV/V
V_{CM}	Common-mode voltage range	$V_{+IN} – V_{–IN}$ = 0	V_S = ±15 V	–200		200	V
			V_S = ±5 V	–100		80	
CMRR	Common-mode rejection ratio	V_S = ±15 V, V_{CM} = –200 V to 200 V, R_S = 0 Ω		70	86		dB
		V_S = ±5 V, V_{CM} = –100 V to 80 V, R_S = 0 Ω		70	86		
	Differential input impedance				2		MΩ
	Common-mode input impedance				1		MΩ
V_n	Voltage noise(1) (3)	f = 0.1 Hz to 10 Hz			17		μV_{p-p}
	Voltage noise density(1) (3)	f = 1 kHz			880		$nV/\sqrt{Hz}$
	Initial gain(1)				1		V/V
	Gain error	V_O = (V– + 0.5) to (V+ – 1.5)			±0.01	±0.075	%
	Gain error over temperature				±3	±10	ppm/°C
	Gain nonlinearity	V_O = (V– + 0.5) to (V+ – 1.5)	V_S = ±15 V		±0.001	±0.002	%FSR
			V_S = ±5 V		±0.001		%FSR
	Small signal bandwidth frequency response				100		kHz
SR	Slew rate				1		V/µs
t_s	Settling time	V_S = ±15 V, 10-V step	0.1%		21		µs
			0.01%		25		
		V_S = ±5 V, 6-V step	0.1%		21		
			0.01%		25		
	Overload recovery	50% input overload			24		µs
V_O	Output voltage	R_L = 100 kΩ		V– + 0.25		V+ – 1	V
		R_L = 10 kΩ		V– + 0.5		V+ – 1.5	
I_O	Output current	Short-circuit current, continuous to common			±13		mA
C_L	Load capacitance	Stable operation			10		nF
I_S	Supply current	V_{IN} = 0, I_O = 0			±260	±300	µA

(1) Overall difference amplifier configuration. Referred to input pins (V_{+IN} and $V_{–IN}$), gain = 1 V/V.
(2) Includes effects of amplifier's input bias and offset currents.
(3) Includes effects of input current noise and thermal noise contribution of resistor network.

ELECTRICAL CHARACTERISTICS

V_S = 5 V (single supply), R_L = 10 kΩ to V_S/2, V_{REF} = V_S/2, T_A = 25°C (unless otherwise noted)

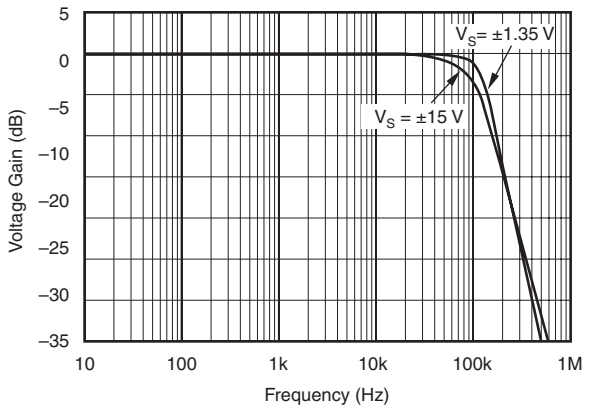
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OS}	Input offset voltage(1) (2)	V_{CM} = V_S/2			±1	±5	mV
$\Delta V_{OS}/\Delta T$	Input offset voltage drift(1)	T_A = –40°C to 125°C			±10		µV/°C
PSRR	Power supply ripple rejection(1)	V_S = 2.7 V to 36 V, V_{CM} = V_S/2			±50	±400	µV/V
V_{CM}	Common-mode voltage range	V_{+IN} – $V_{–IN}$ = 0	V_{REF} = 0.25 V	–4		75	V
			V_{REF} = V_S/2	–47.5		32.5	
CMRR	Common-mode rejection ratio	V_{CM} = –47.5 V to 32.5 V, R_S = 0 Ω		70	86		dB
	Differential input impedance				2		MΩ
	Common-mode input impedance				1		MΩ
V_n	Voltage noise(1) (3)	f = 0.1 Hz to 10 Hz			17		μV_{p-p}
	Voltage noise density(1) (3)	f = 1 kHz			880		nV/√Hz
	Initial gain(1)				1		V/V
	Gain error	V_O = 0.5 V to 3.5 V			±0.01	±0.075	%
	Gain error over temperature				±3	±10	ppm/°C
	Gain nonlinearity	V_O = 0.5 V to 3.5 V			±0.001		%FSR
	Small signal bandwidth				100		kHz
SR	Slew rate				1		V/µs
t_s	Settling time	V_S = 5 V, 3-V step	0.1%		21		µs
			0.01%		25		
	Overload recovery	50% input overload			13		µs
V_O	Output voltage	R_L = 100 kΩ		V– + 0.25		V+ – 1	V
		R_L = 10 kΩ		V– + 0.5		V+ – 1.5	
I_O	Output current	Short-circuit current, continuous to common			±8		mA
C_L	Load capacitance	Stable operation			10		nF
I_Q	Quiescent current	V_{IN} = 0, I_O = 0			260	300	µA

(1) Overall difference amplifier configuration. Referred to input pins (V_{+IN} and $V_{–IN}$), gain = 1 V/V.
(2) Includes effects of amplifier's input bias and offset currents.
(3) Includes effects of input current noise and thermal noise contribution of resistor network.

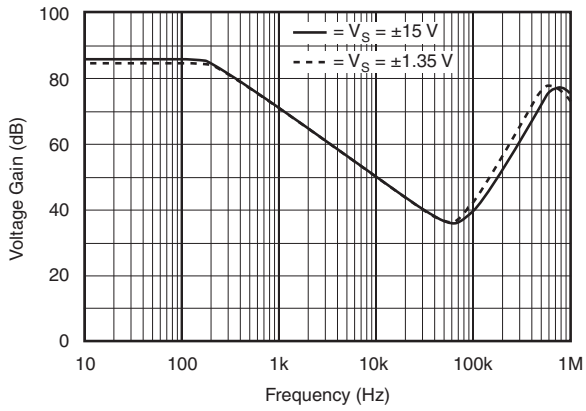
TYPICAL CHARACTERISTICS

V_S = ±15 V, R_L = 10 kΩ to common, V_{REF} = 0 V, T_A = 25°C (unless otherwise noted)

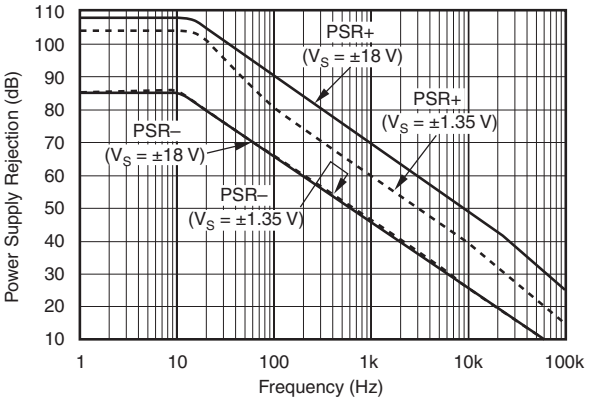
GAIN vs FREQUENCY



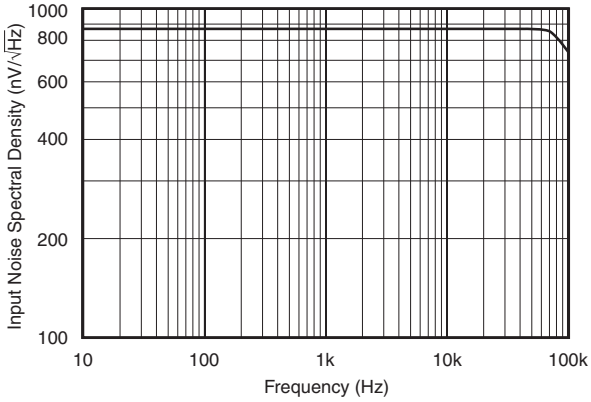
COMMON-MODE REJECTION vs FREQUENCY



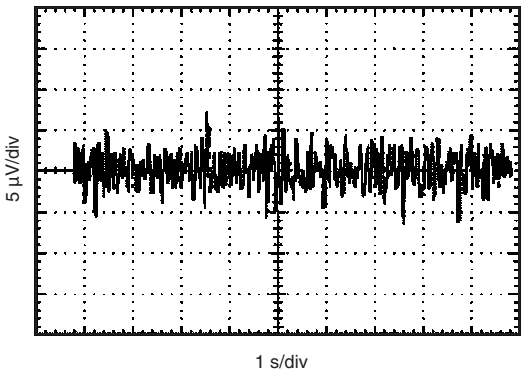
POWER SUPPLY REJECTION vs FREQUENCY



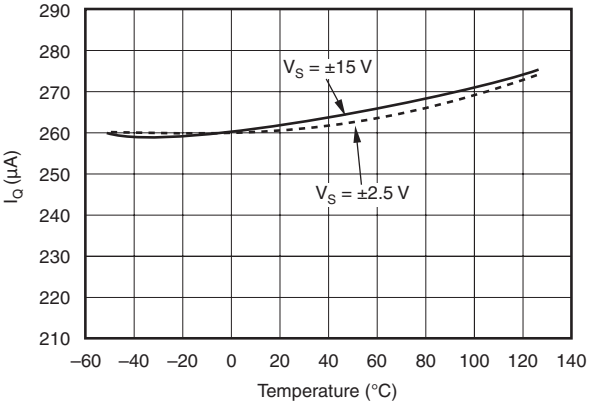
INPUT VOLTAGE NOISE SPECTRAL DENSITY



VOLTAGE NOISE (RTI)
0.1 Hz to 10 Hz



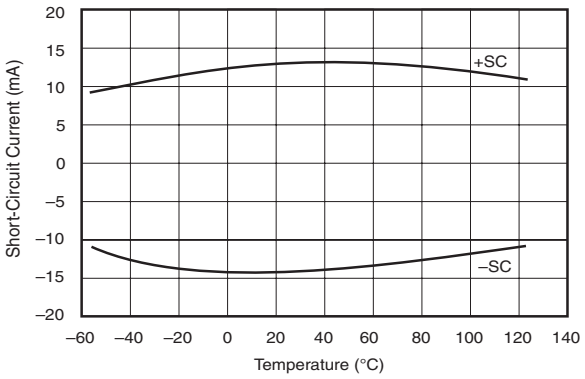
QUIESCENT CURRENT vs TEMPERATURE



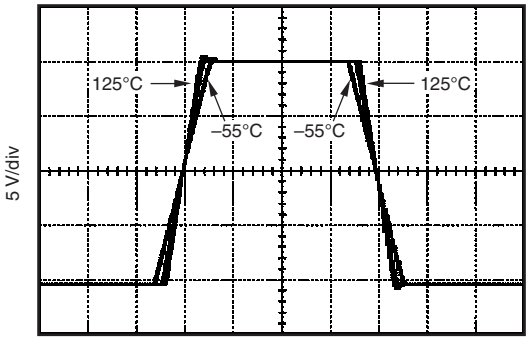
TYPICAL CHARACTERISTICS (continued)

V_S = ±15 V, R_L = 10 kΩ to common, V_{REF} = 0 V, T_A = 25°C (unless otherwise noted)

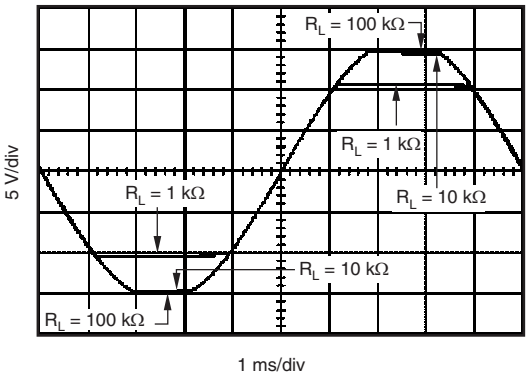
SHORT-CIRCUIT CURRENT vs TEMPERATURE



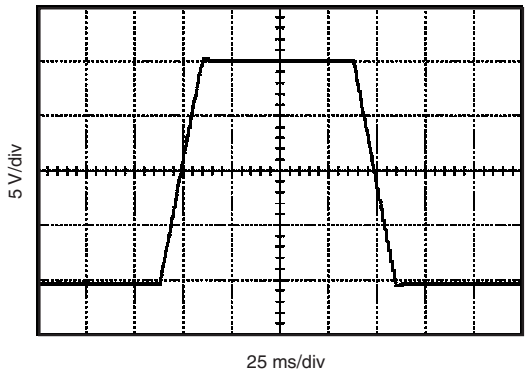
LARGE-SIGNAL STEP RESPONSE vs TEMPERATURE



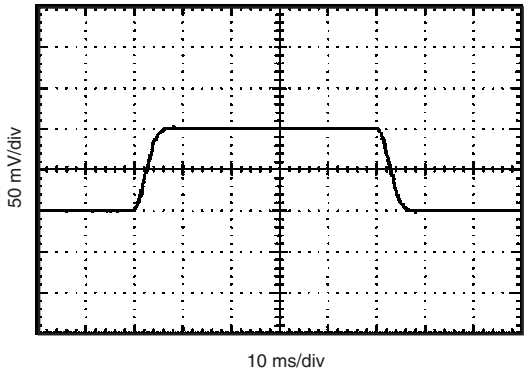
OUTPUT VOLTAGE SWING vs R_L



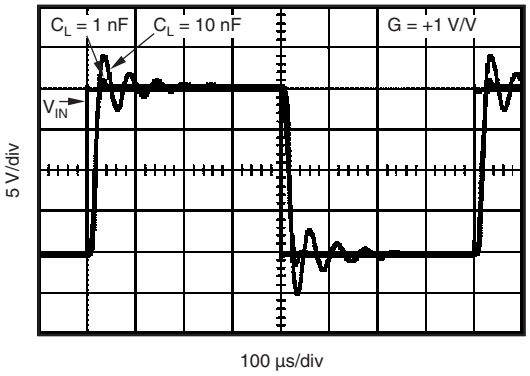
LARGE-SIGNAL STEP RESPONSE (R_L = 10 kΩ, C_L = 10 pF)



SMALL-SIGNAL STEP RESPONSE (R_L = 10 kΩ, C_L = 10 pF)



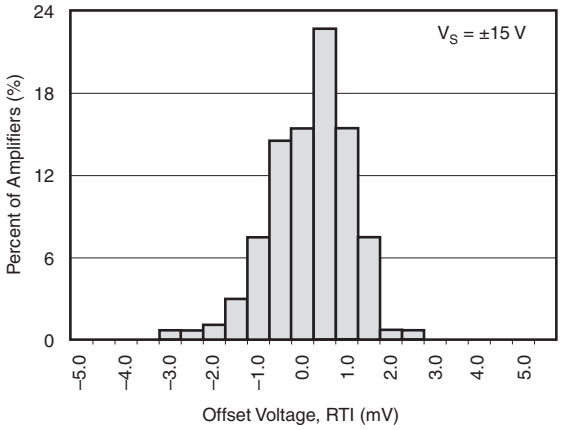
LARGE-SIGNAL CAPACITIVE LOAD RESPONSE (C_L = 1 nF and 10 nF)



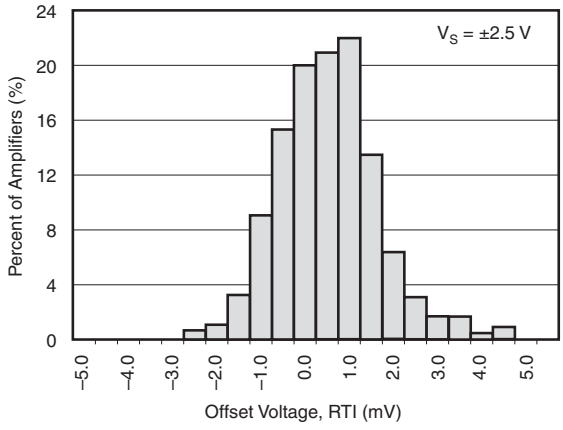
TYPICAL CHARACTERISTICS (continued)

V_S = ±15 V, R_L = 10 kΩ to common, V_{REF} = 0 V, T_A = 25°C (unless otherwise noted)

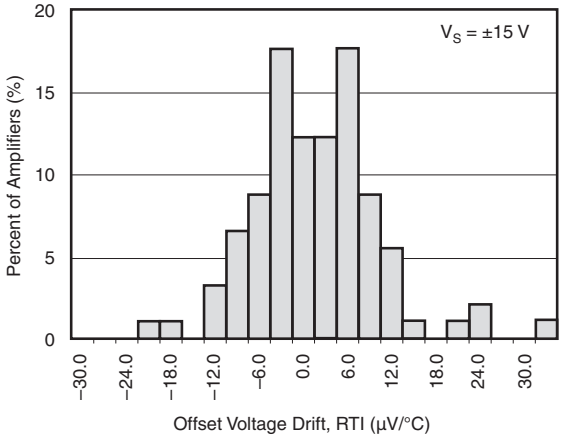
OFFSET VOLTAGE PRODUCTION DISTRIBUTION



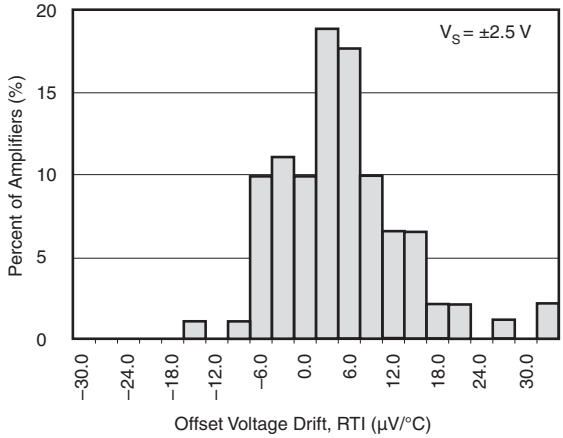
OFFSET VOLTAGE PRODUCTION DISTRIBUTION



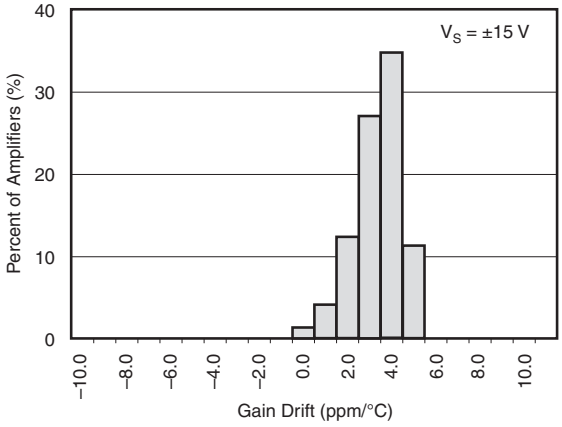
OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION



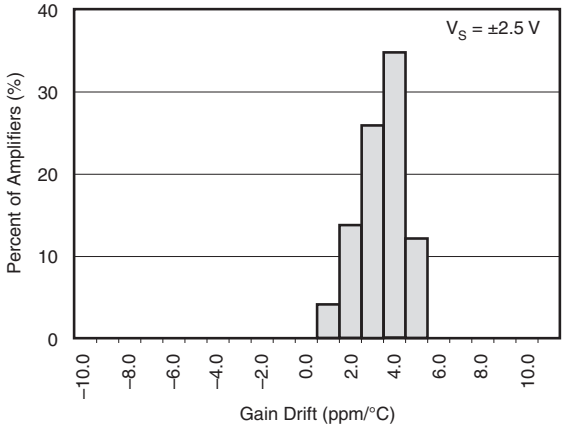
OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION



GAIN DRIFT PRODUCTION DISTRIBUTION



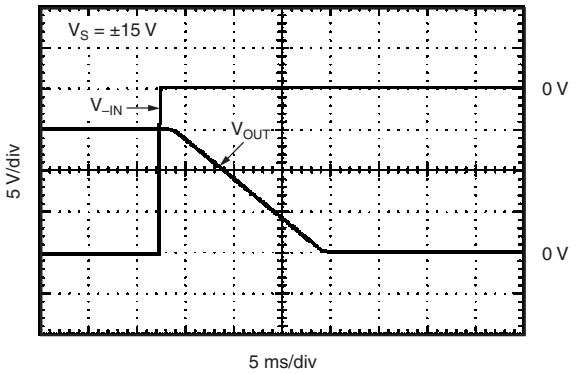
GAIN DRIFT PRODUCTION DISTRIBUTION



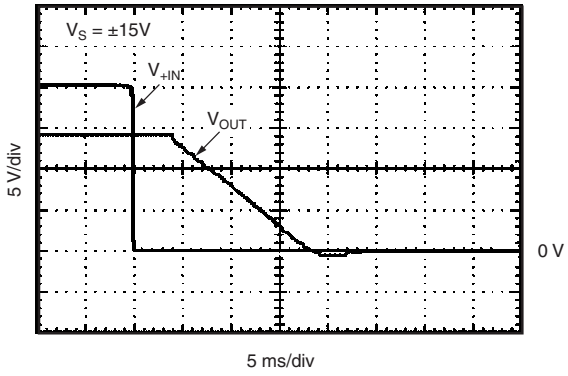
TYPICAL CHARACTERISTICS (continued)

V_S = ±15 V, R_L = 10 kΩ to common, V_{REF} = 0 V, T_A = 25°C (unless otherwise noted)

INVERTING INPUT
50% OVERLOAD RECOVERY TIME



NON-INVERTING INPUT
50% OVERLOAD RECOVERY TIME



APPLICATION INFORMATION

The INA148 is a unity-gain difference amplifier with a high common-mode input voltage range. A basic diagram of the circuit and pin connections is shown in Figure 1.

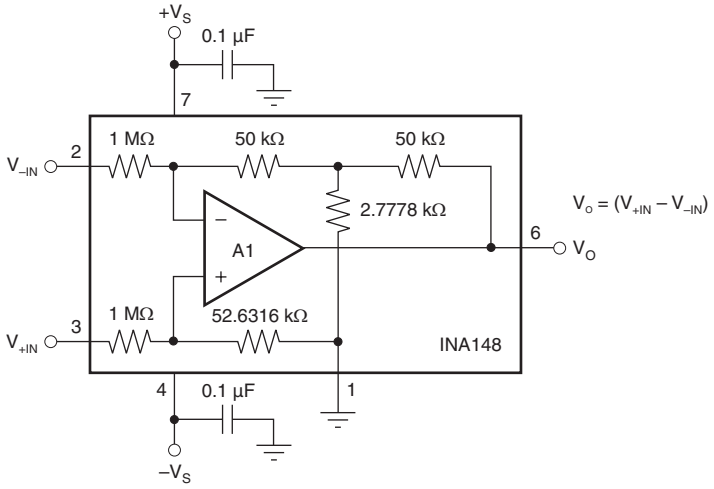


Figure 1. Basic Circuit Connections

To achieve its high common-mode voltage range, the INA148 features a precision laser-trimmed thin-film resistor network with a 20:1 input voltage divider ratio. High input voltages are thereby reduced in amplitude, allowing the internal operational amplifier (op amp) to "see" input voltages that are within its linear operating range. A "Tee" network in the op amp feedback network places the amplifier in a gain of 20 V/V, thus restoring the circuit's overall gain to unity (1 V/V).

External voltages can be summed into the amplifier's output by using the REF pin, making the differential amplifier a highly versatile design tool. Voltages on the REF pin also influence the INA148's common-mode voltage range.

In accordance with good engineering practice for linear integrated circuits, the INA148's power-supply bypass capacitors should be connected as close to pins 4 and 7 as practicable. Ceramic or tantalum types are recommended for use as bypass capacitors.

The input impedances are unusually high for a difference amplifier and this should be considered when routing input signal traces on a PC board. Avoid placing digital signal traces near the difference amplifier's input traces to minimize noise pickup.

Operating Voltage

The INA148 is specified for ±15-V and ±5-V dual supplies and 5-V single supplies. The INA148 can be operated with single or dual supplies with excellent performance.

The INA148 is fully characterized for supply voltages from ±1.35 V to ±18 V and over temperatures of –40°C to 125°C. Parameters that vary significantly with operating voltage, load conditions, or temperature are shown in the *Typical Characteristics* section.

Gain Equation

An internal on-chip resistor network sets the overall differential gain of the INA148 to precisely 1 V/V. Output is accordance with Equation 1.

$$V_{OUT} = (V_{+IN} - V_{-IN}) + V_{REF} \quad (1)$$ (1)

Common-Mode Range

The 20:1 input resistor ratio of the INA148 provides an input common-mode range that extends well beyond its power supply rails.

The exact input voltage range depends on the amplifier's power-supply voltage and the voltage applied to the REF terminal (pin 1). Typical input voltage ranges at different power supply voltages can be found in the applications circuits section.

Offset Trim

The INA148 is laser-trimmed for low offset voltage and drift. Most applications require no external offset adjustment.

Because a voltage applied to the reference (REF) pin (pin 1) is summed directly into the amplifier's output signal, this technique can be used to null the amplifier's input offset voltage. Figure 2 shows an optional circuit for trimming the offset voltage.

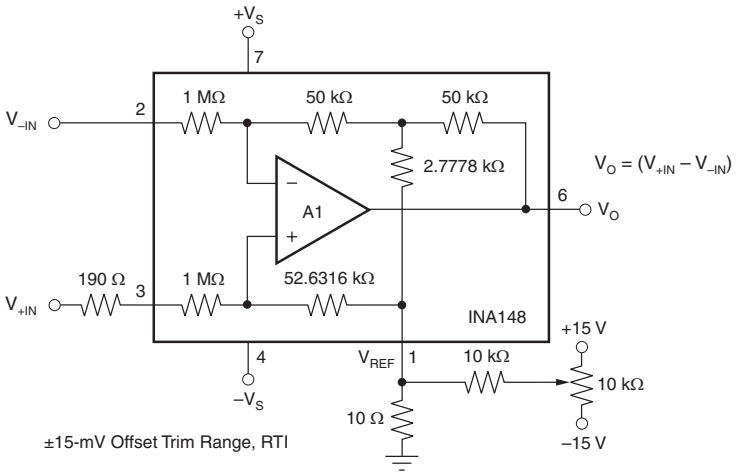


Figure 2. Optional Offset Trim Circuit

To maintain high common-mode rejection (CMR), the source impedance of any signal applied to the REF terminal should be very low (≤5 Ω).

A source impedance of only 10 Ω at the REF pin reduces the INA148's CMR to approximately 74 dB. High CMR can be restored if a resistor is added in series with the amplifier's positive input terminal (pin 3). This resistor should be 19 times the source impedance that drives the REF pin. For example, if the REF pin sees a source impedance of 10 Ω, a resistor of 190 Ω should be added in series with pin 3.

Preferably, the offset trim voltage applied to the REF pin should be buffered with an amplifier such as an OPA237 (see Figure 3). In this case, the op amp output impedance is low enough that no external resistor is needed to maintain the INA148's excellent CMR.

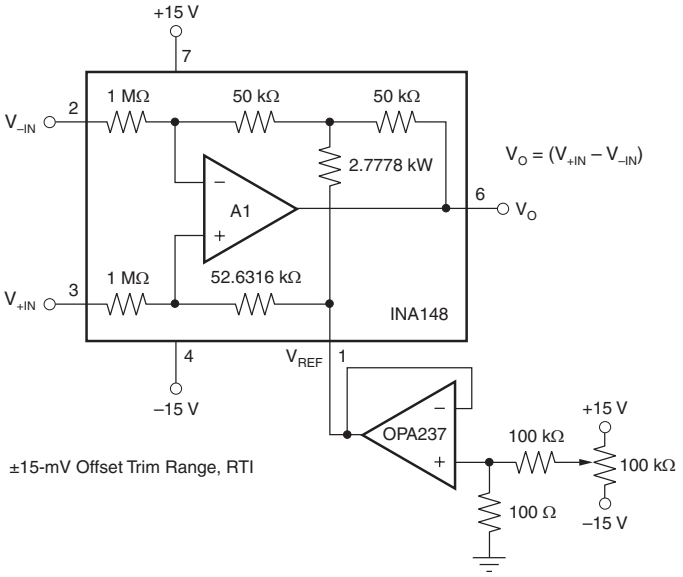


Figure 3. Preferred Offset Trim Circuit

Input Impedance

The input resistor network determines the impedance of each of the INA148 inputs. It is approximately 1 MΩ. Unlike an instrumentation amplifier, signal source impedances at the two input terminals must be nearly equal to maintain good common-mode rejection.

A mismatch between the two inputs' source impedances causes a differential amplifier's common-mode rejection to be degraded. With a source impedance imbalance of only 500 Ω, CMR can fall to approximately 66 dB.

Figure 4 shows a common application—measuring power supply current through a shunt resistor (R_S). A shunt resistor creates an unbalanced source resistance condition that can degrade a differential amplifier's common mode rejection.

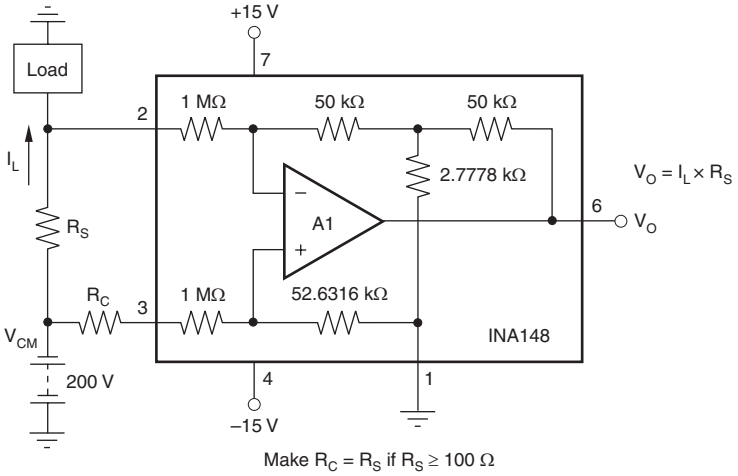


Figure 4. Shunt-Resistor Current Measurement Circuit

Unless the shunt resistor is less than approximately 100 Ω, an additional equal compensating resistor (RC) is recommended to maintain input balance and high CMR.

Source impedances (or shunts) greater than 5 kΩ are not recommended, even if they are "perfectly" compensated. This is because the internal resistor network is laser-trimmed for accurate voltage divider ratios, but not necessarily to absolute values. Input resistors are shown as 1 MΩ, however, this is only their nominal value.

In practice, the input resistors' absolute values may vary by as much as 30%. The two input resistors match to about 5%, so adding compensating resistors greater than 5 kΩ can cause a serious mismatch in the resulting resistor network voltage divider ratios, thus degrading CMR.

Attempts to extend the INA148 input voltage range by adding external resistors is not recommended for the reasons described in the previous paragraph. CMR suffers serious degradation unless the resistors are carefully trimmed for CMR and gain. This is an iterative adjustment and can be tedious and time consuming.

Typical Application Circuits

Figure 5 through Figure 9 show typical application circuits for the INA148.

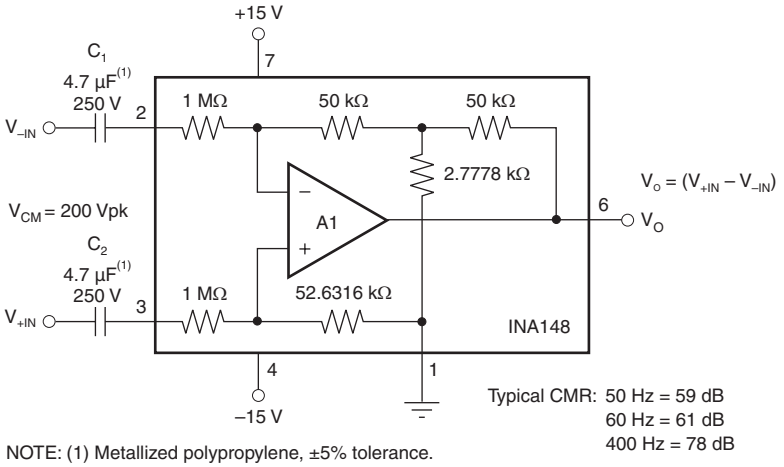


Figure 5. AC-Coupled Difference Amplifier

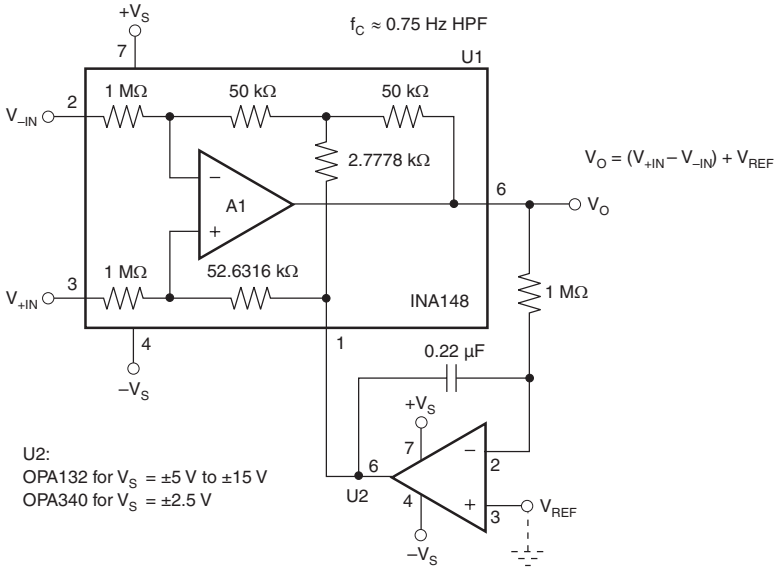


Figure 6. Quasi-AC-Coupled Differential Amplifier

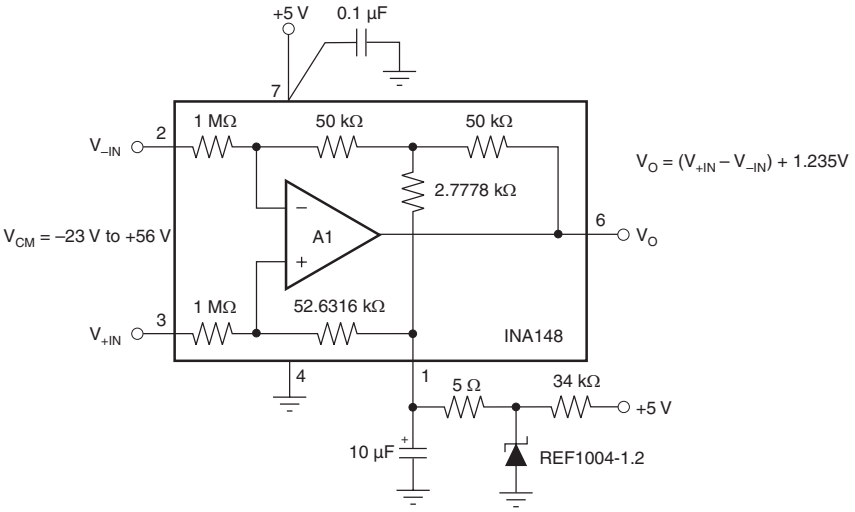


Figure 7. Single-Supply Differential Amplifier

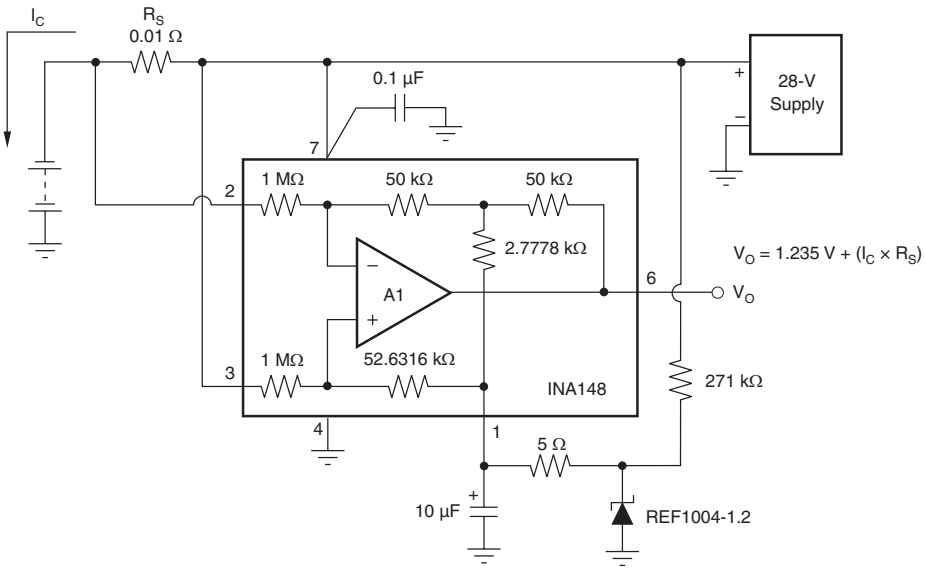


Figure 8. Battery Monitor Circuit

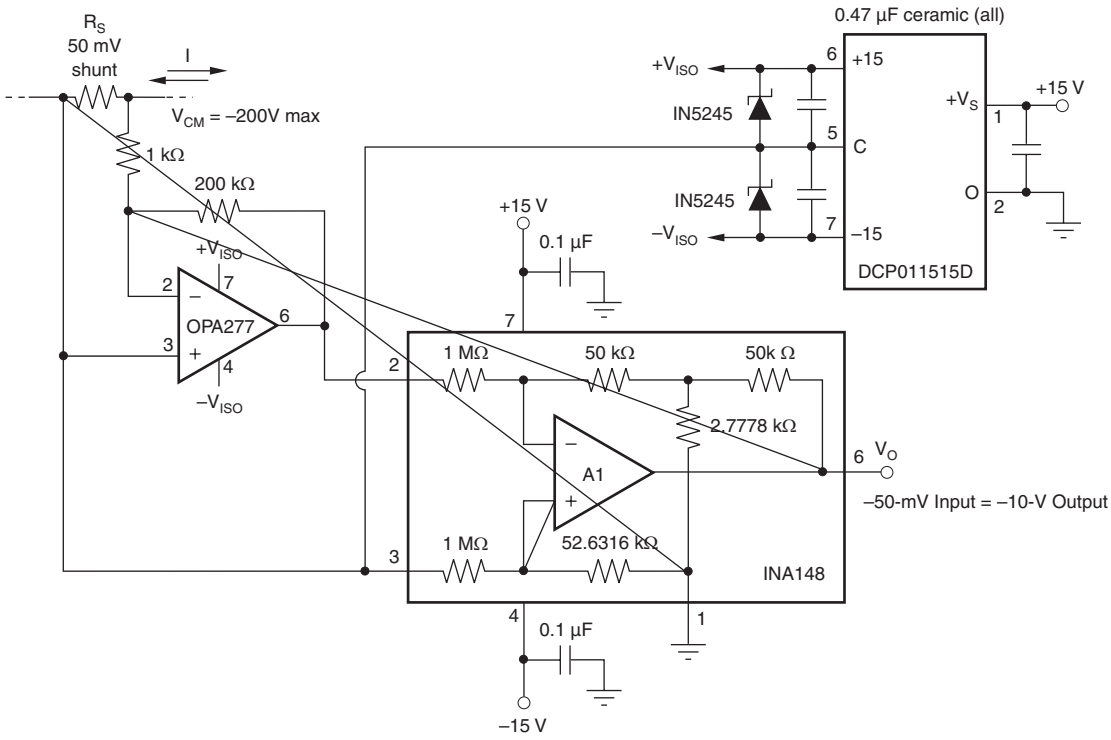


Figure 9. 50-mV Current-Shunt Amplifier with ±200-V Common-Mode Voltage Range

REVISION HISTORY

Changes from Original (March 2009) to Revision A	Page
• Features Bullet From: Low Quiescent Current: 260 mA To: Low Quiescent Current: 260 µA	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
INA148QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		148Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

OTHER QUALIFIED VERSIONS OF INA148-Q1 :

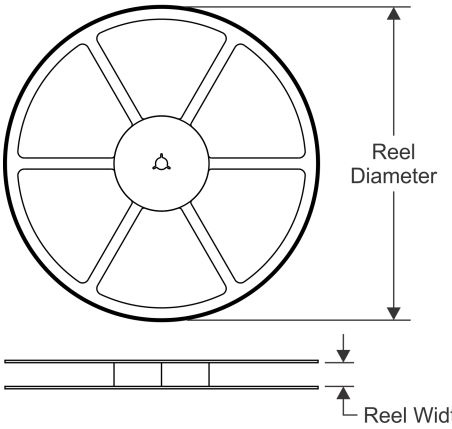
- Catalog: INA148

NOTE: Qualified Version Definitions:

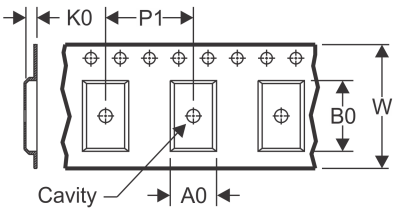
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

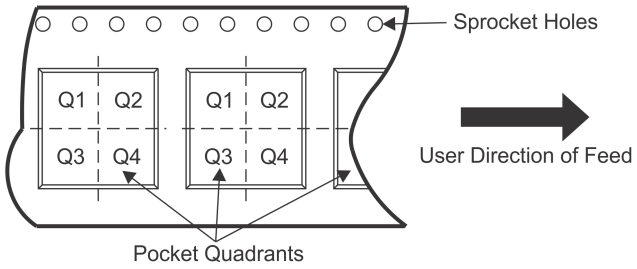


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

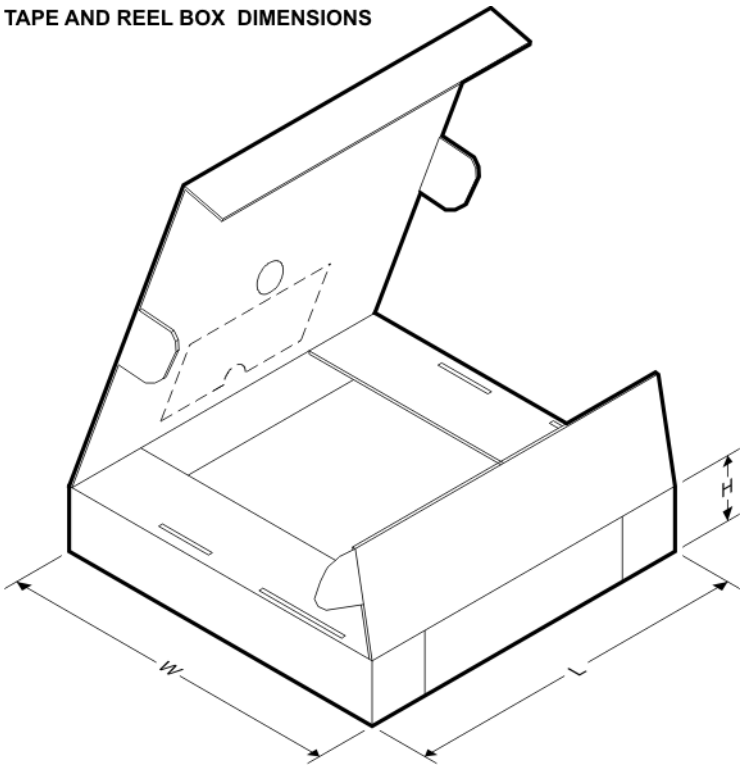
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA148QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

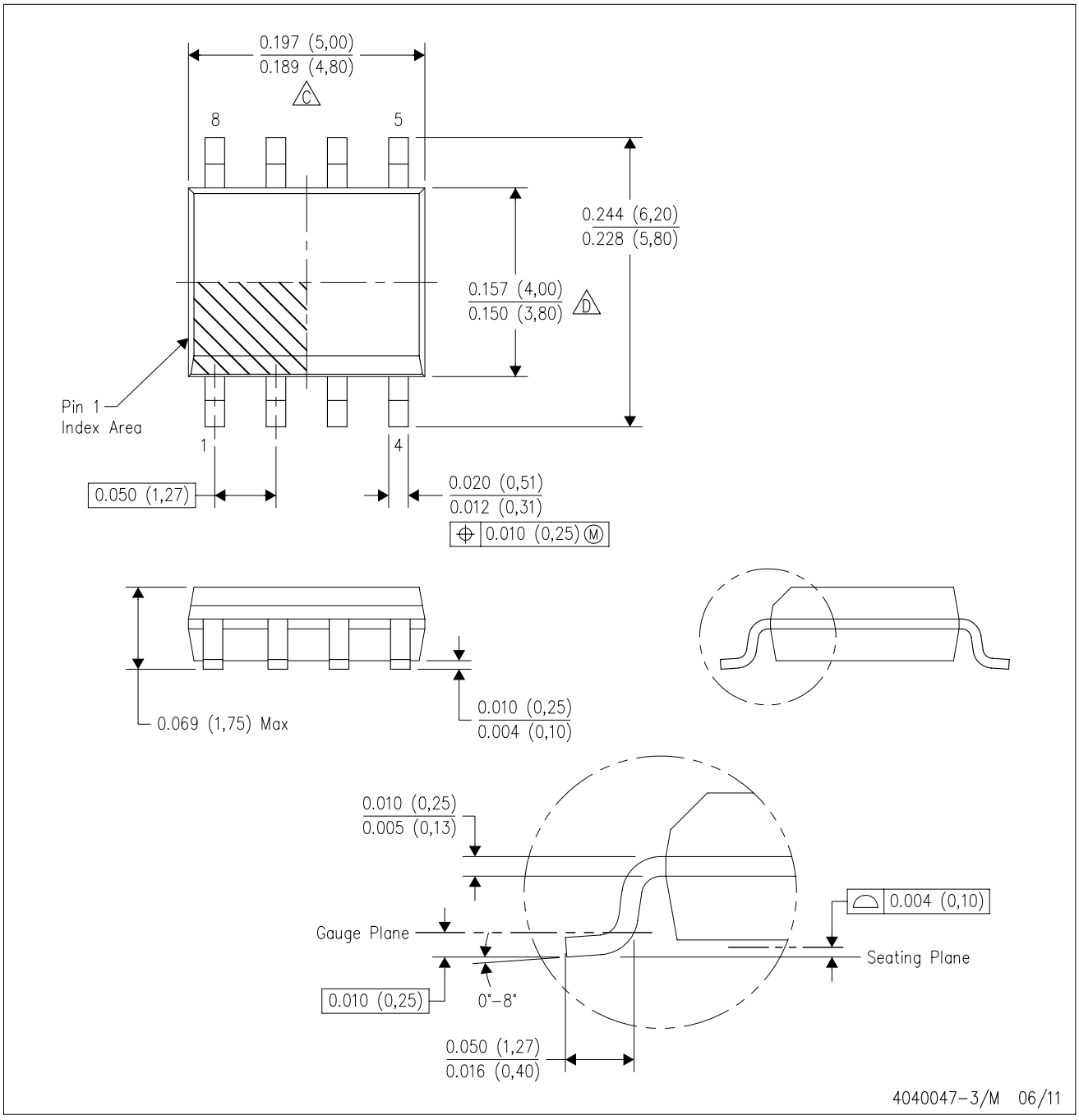
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

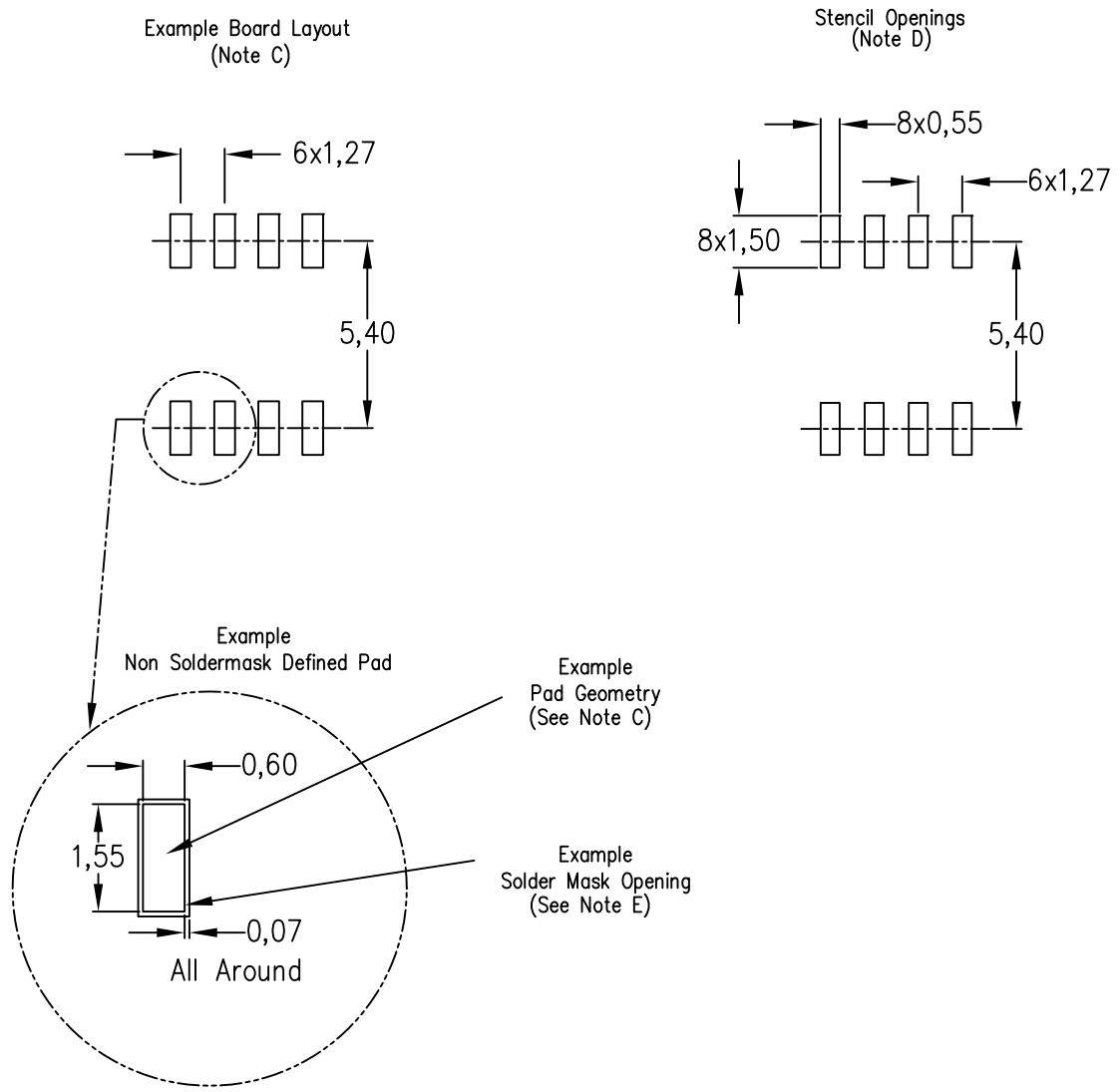
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA148QDRQ1	SOIC	D	8	2500	367.0	367.0	35.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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