VOLTAGE-OUTPUT UNIDIRECTIONAL-MEASUREMENT CURRENT-SHUNT MONITORS

Check for Samples: INA270-Q1, INA271-Q1

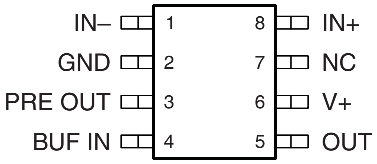
FEATURES

- **Qualified for Automotive Applications**
- **Wide Common-Mode Range: –16 V to 80 V**
- **CMRR: 120 dB**
- **Accuracy:**
  - **±2.5-mV Offset (Max)**
  - **±1% Gain Error (Max)**
  - **20-µV/°C Offset Drift (Max)**
  - **55-ppm/°C Gain Drift (Max)**
- **Bandwidth: Up to 130 kHz**
- **Two Transfer Functions Available:**
  - **14 V/V (INA270)**
  - **20 V/V (INA271)**
- **Quiescent Current: 900 µA (Max)**
- **Power Supply: 2.7 V to 18 V**
- **Provision for Filtering**

APPLICATIONS

- **Power Management**
- **Automotive**
- **Telecom Equipment**
- **Notebook Computers**
- **Battery Chargers**
- **Cell Phones**
- **Welding Equipment**

D PACKAGE
(TOP VIEW)



NC – No internal connection

DESCRIPTION/ORDERING INFORMATION

The INA270 and INA271 family of current-shunt monitors with voltage output can sense voltage drops across current shunts at common-mode voltages from –16 V to 80 V, independent of the supply voltage. The INA270 and INA271 pinouts readily enable filtering.

The INA270 and INA271 are available with two output voltage scales: 14 V/V and 20 V/V. The 130-kHz bandwidth simplifies use in current-control loops.

The INA270 and INA271 operate from a single 2.7-V to 18-V supply, drawing a maximum of 900 µA of supply current. They are specified over the extended operating temperature range of –40°C to 125°C and are offered in an SO-8 package.

ORDERING INFORMATION(1)

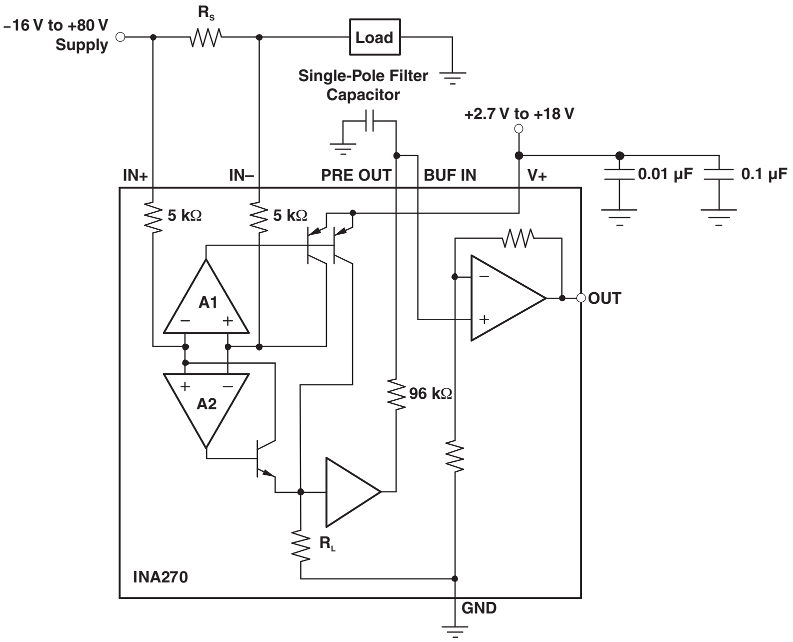
T_A	GAIN	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	14	SOIC – D	Reel of 2500	INA270AQDRQ1	INA270
	20			INA271AQDRQ1	INA271

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

			VALUE
V_S	Supply voltage		18 V
	Differential analog input voltage range ($V_{IN+} – V_{IN–}$)		–18 V to 18 V
	Common-mode analog input voltage range		–16 V to 80 V
V_O	Analog output voltage range (OUT and PRE OUT)		(GND – 0.3) V to (V+ + 0.3) V
I_I	Input current (any pin)		5 mA
θ_{JA}	Package thermal impedance[2] [3]		97.1°C/W
T_J	Maximum junction temperature		150°C
T_A	Operating free-air temperature range		–40 to 125°C
T_{stg}	Storage temperature range		–65 to 150°C
ESD	Electrostatic discharge rating	Human-Body Model HBM)	2000 V
		Machine Model (MM)	100 V
		Charged-Device Model (CDM)	1000 V

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[1] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[2] Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

[3] The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_S	Supply voltage	2.7	18	V
T_A	Operating free-air temperature	–40	125	°C

ELECTRICAL CHARACTERISTICS

$V_S = 5$ V, $V_{CM} = 12$ V, $V_{SENSE} = 100$ mV, PRE OUT connected to BUF IN (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A (1)	MIN	TYP	MAX	UNIT
Input							
V_{SENSE}	Full-scale input voltage	$V_{SENSE} = V_{IN+} + V_{IN–}$	25°C		0.15	$(V_S – 0.2)$/ Gain	V
V_{CM}	Common-mode input voltage		Full range	–16		80	V
CMRR	Common-mode rejection	$V_{IN+} = –16$ V to 80 V	25°C	80	120		dB
		$V_{IN+} = 12$ V to 80 V	Full range	100	120		
V_{OS}	Offset voltage, RTI (2)		25°C		±0.5	2.5	mV
			Full range			±3	
$ΔV_{OS}/ΔT$	Input offset voltage temperature coefficient		Full range		2.5	20	μV/°C
PSR	Offset voltage power-supply rejection	$V_S = 2.7$ V to 18 V, $V_{CM} = 18$ V	Full range		5	100	μV/V
I_{IB}	Input bias current	IN– pin	Full range		±8	±16	μA
Z_O	Output impedance (3)	PRE OUT pin	25°C		96		kΩ
	Buffer input bias current		25°C		–50		nA
	Buffer input bias current temperature coefficient		25°C		±0.3		nA/°C
Output (V_{SENSE} ≥ 20 mV) (4)							
G	Gain	INA270	25°C		14		V/V
		INA271			20		
G_{BUF}	Output buffer gain		25°C		2		V/V
	Total gain error	$V_{SENSE} = 20$ mV to 100 mV	25°C		±0.2	±1	%
			Full range			±2	
	Total gain error temperature coefficient		Full range			50	ppm/°C
	Total output error (5)		25°C		±0.75	±2.2	%
			Full range		±1	±3	
	Nonlinearity error	$V_{SENSE} = 20$ mV to 100 mV	25°C		±0.002		%
Z_O	Output impedance	OUT pin	25°C		1.5		Ω
	Maximum capacitive load	No sustained oscillation	25°C		10		nF
Voltage Output (6)							
	Swing to V+ power-supply rail	$R_L = 10$ kΩ to GND	Full range		V+ – 0.05	V+ – 0.2	V
	Swing to GND	$R_L = 10$ kΩ to GND	Full range		V_{GND} + 0.003	V_{GND} + 0.05	V

(1) Full range is –40°C to 125°C.
(2) RTI = referred to input
(3) Initial resistor variation is ±30% with an additional –2200-ppm/°C temperature coefficient.
(4) For output behavior when $V_{SENSE} < 20$ mV, see Application Information
(5) Total output error includes effects of gain error and V_{OS}.
(6) See Typical Characteristics curve Output Swing vs Output Current and Accuracy Variations as a Result of VSENSE and Common-Mode Voltage in the Application Information section.

ELECTRICAL CHARACTERISTICS (continued)

V_S = 5 V, V_{CM} = 12 V, V_{SENSE} = 100 mV, PRE OUT connected to BUF IN (unless otherwise noted)

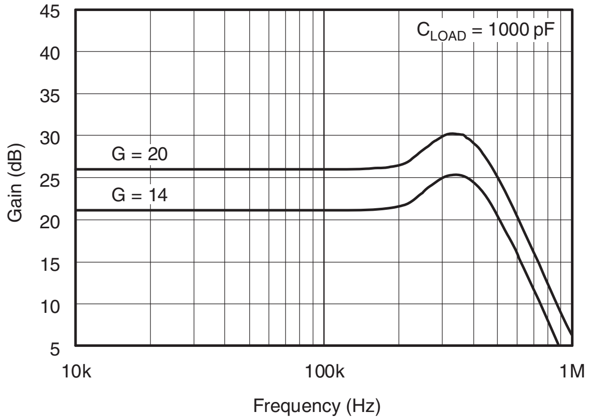
PARAMETER		TEST CONDITIONS	T_A (1)	MIN	TYP	MAX	UNIT
Frequency Response							
BW	Bandwidth	C_L = 5 pF	25°C		130		kHz
ϕ_m	Phase margin	C_L < 10 nF	25°C		40		°
SR	Slew rate		25°C		1		V/µs
t_s	Settling time (1%)	V_{SENSE} = 10 mV to 100 mV, C_L = 5 pF	25°C		2		µs
Noise, RTI (7)							
V_n	Voltage noise density		25°C		40		nV/√Hz
Power Supply							
I_Q	Quiescent current	V_{OUT} = 2 V	25°C		700	900	µA
		V_{SENSE} = 0 V	Full range		350	950	

(7) RTI = referred to input

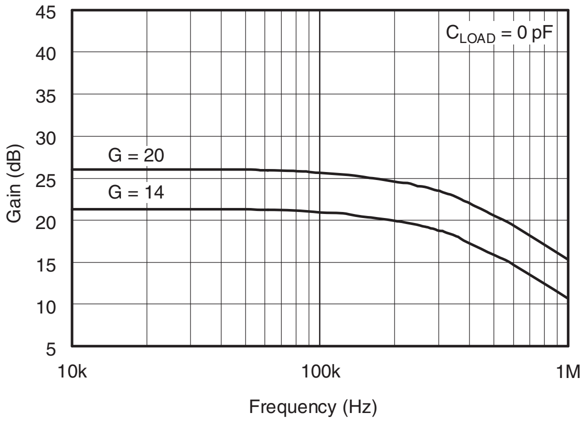
TYPICAL CHARACTERISTICS

T_A = 25°C, V_S = 12 V, V_{CM} = 12 V, V_{SENSE} = 100 mV (unless otherwise noted)

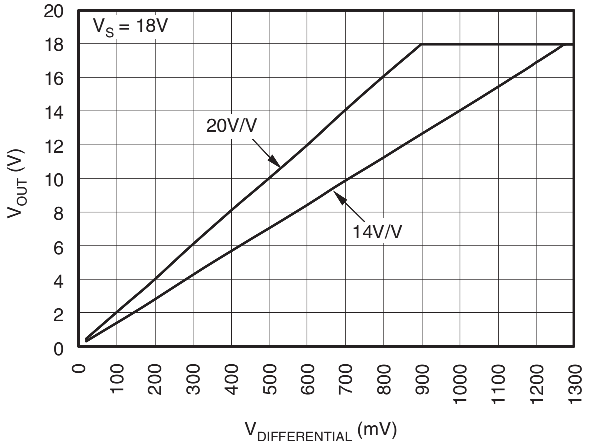
GAIN vs FREQUENCY



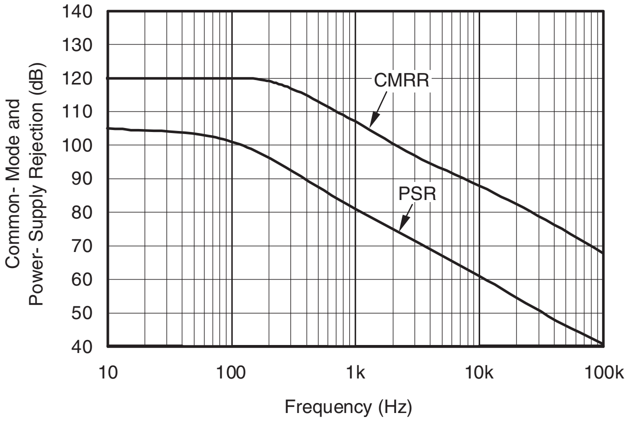
GAIN vs FREQUENCY



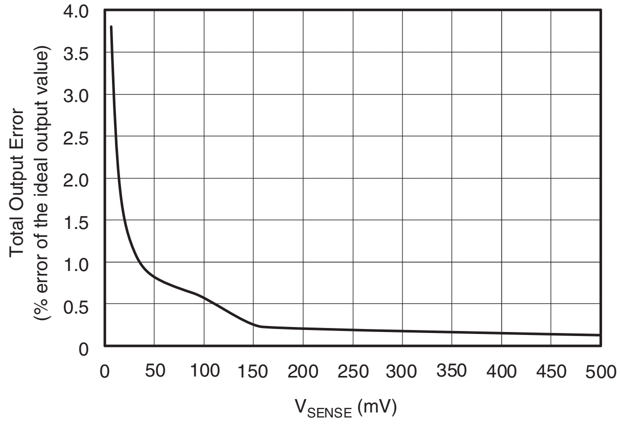
GAIN PLOT



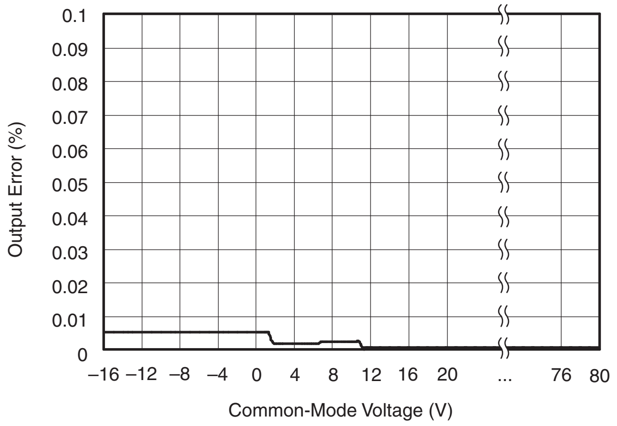
COMMON-MODE AND POWER-SUPPLY REJECTION vs FREQUENCY



TOTAL OUTPUT ERROR vs V_{SENSE}



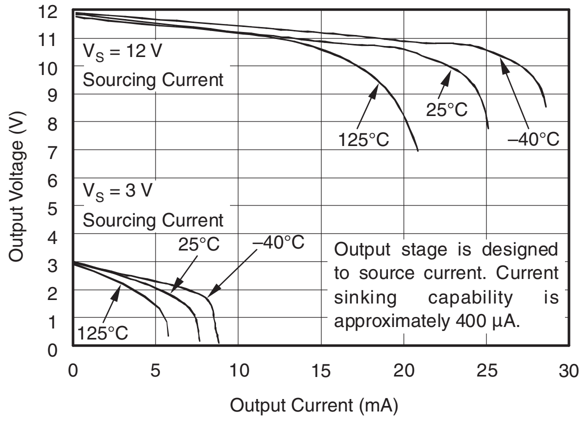
OUTPUT ERROR vs COMMON-MODE VOLTAGE



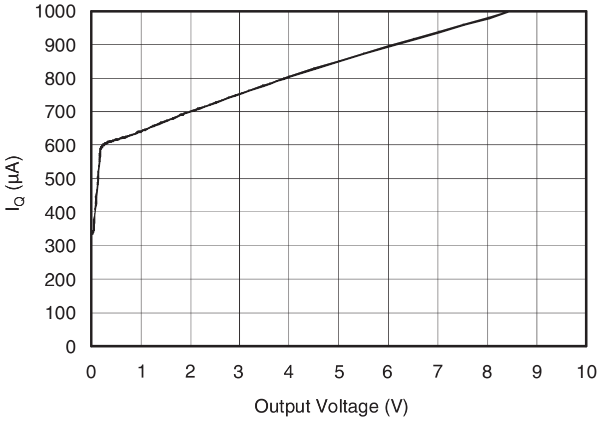
TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, V_S = 12 V, V_{CM} = 12 V, V_{SENSE} = 100 mV (unless otherwise noted)

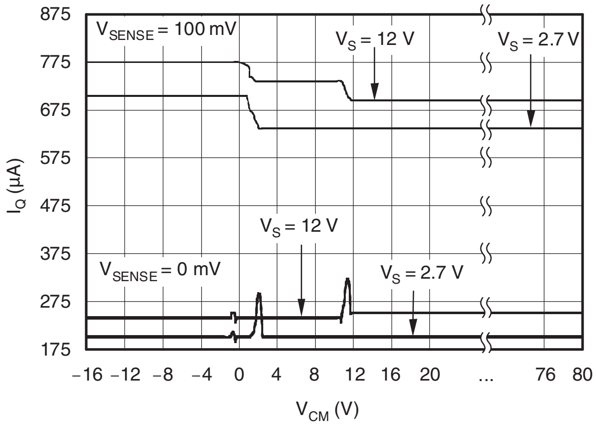
POSITIVE OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



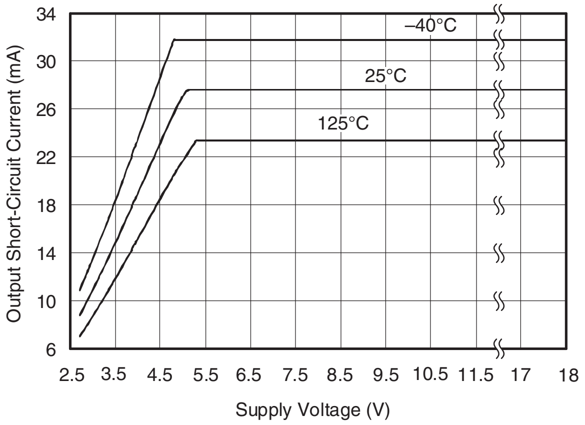
QUIESCENT CURRENT vs OUTPUT VOLTAGE



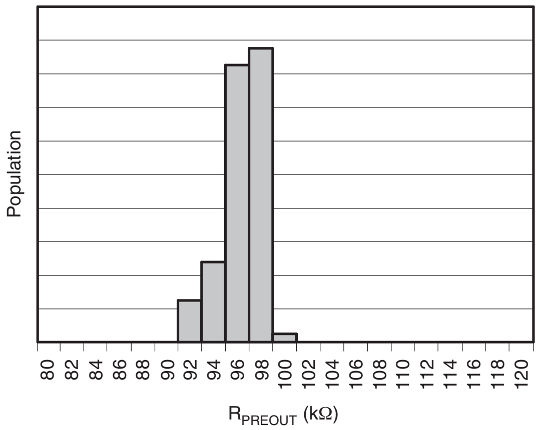
QUIESCENT CURRENT vs COMMON-MODE VOLTAGE



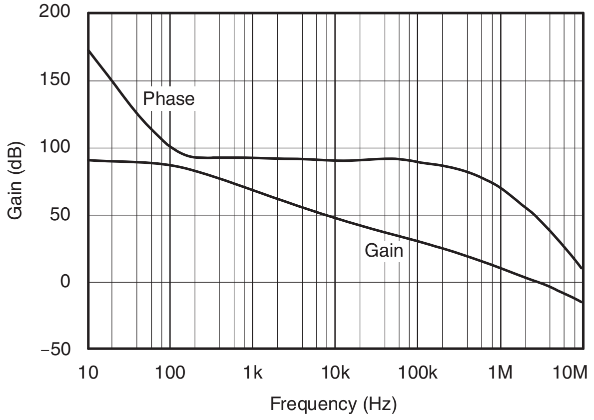
OUTPUT SHORT-CIRCUIT CURRENT vs SUPPLY VOLTAGE



PREOUT OUTPUT RESISTANCE PRODUCTION DISTRIBUTION



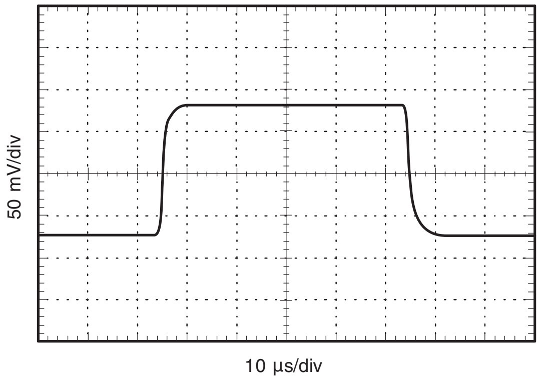
BUFFER GAIN vs FREQUENCY



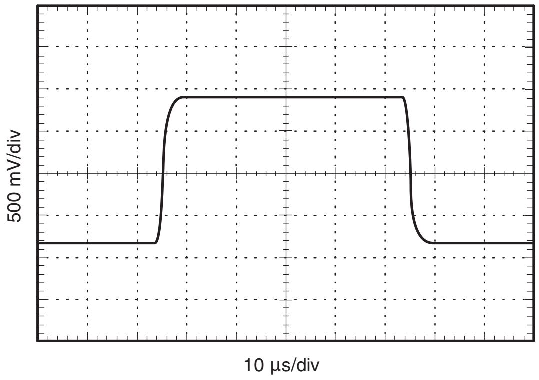
TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, V_S = 12 V, V_{CM} = 12 V, V_{SENSE} = 100 mV (unless otherwise noted)

SMALL-SIGNAL STEP RESPONSE
10-mV TO 20-mV INPUT



LARGE-SIGNAL STEP RESPONSE
10-mV TO 100-mV INPUT



APPLICATION INFORMATION

Basic Connection

Figure 1 illustrates the basic connection of the INA270 and INA271. The input pins, IN+ and IN–, should be connected as closely as possible to the shunt resistor to minimize any resistance in series with the shunt resistance. Power-supply bypass capacitors are required for stability. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise. Minimum bypass capacitors of 0.01 µF and 0.1 µF in value should be placed close to the supply pins. Although not mandatory, an additional 10-mF electrolytic capacitor placed in parallel with the other bypass capacitors may be useful in applications with particularly noisy supplies.

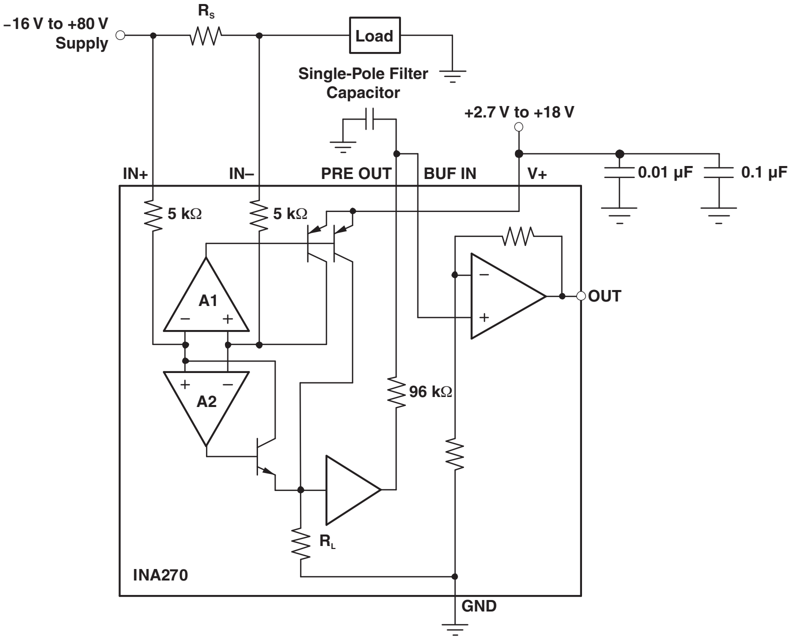


Figure 1. INA270 Basic Connections

Power Supply

The input circuitry of the INA270 and INA271 can accurately measure beyond its power-supply voltage, V+. For example, the V+ power supply can be 5 V, whereas the load power-supply voltage is up to 80 V. The output voltage range of the OUT terminal, however, is limited by the voltages on the power-supply pin.

Selecting R_S

The value chosen for the shunt resistor, R_S, depends on the application and is a compromise between small-signal accuracy and maximum permissible voltage loss in the measurement line. High values of R_S provide better accuracy at lower currents by minimizing the effects of offset, while low values of R_S minimize voltage loss in the supply line. For most applications, best performance is attained with an R_S value that provides a full-scale shunt voltage range of 50 mV to 100 mV. Maximum input voltage for accurate measurements is (V_S – 0.2)/Gain.

Transient Protection

The –16-V to 80-V common-mode range of the INA270 and INA271 is ideal for withstanding automotive fault conditions ranging from 12-V battery reversal up to 80-V transients, since no additional protective components are needed up to those levels. In the event that the INA270 and INA271 are exposed to transients on the inputs in excess of their ratings, external transient absorption with semiconductor transient absorbers (zeners or Transzorbs) are necessary.

Use of MOVs or VDRs is not recommended except when they are used in addition to a semiconductor transient absorber. Select the transient absorber such that it will never allow the INA270 and INA271 to be exposed to transients greater than 80 V (that is, allow for transient absorber tolerance, as well as additional voltage because of transient absorber dynamic impedance).

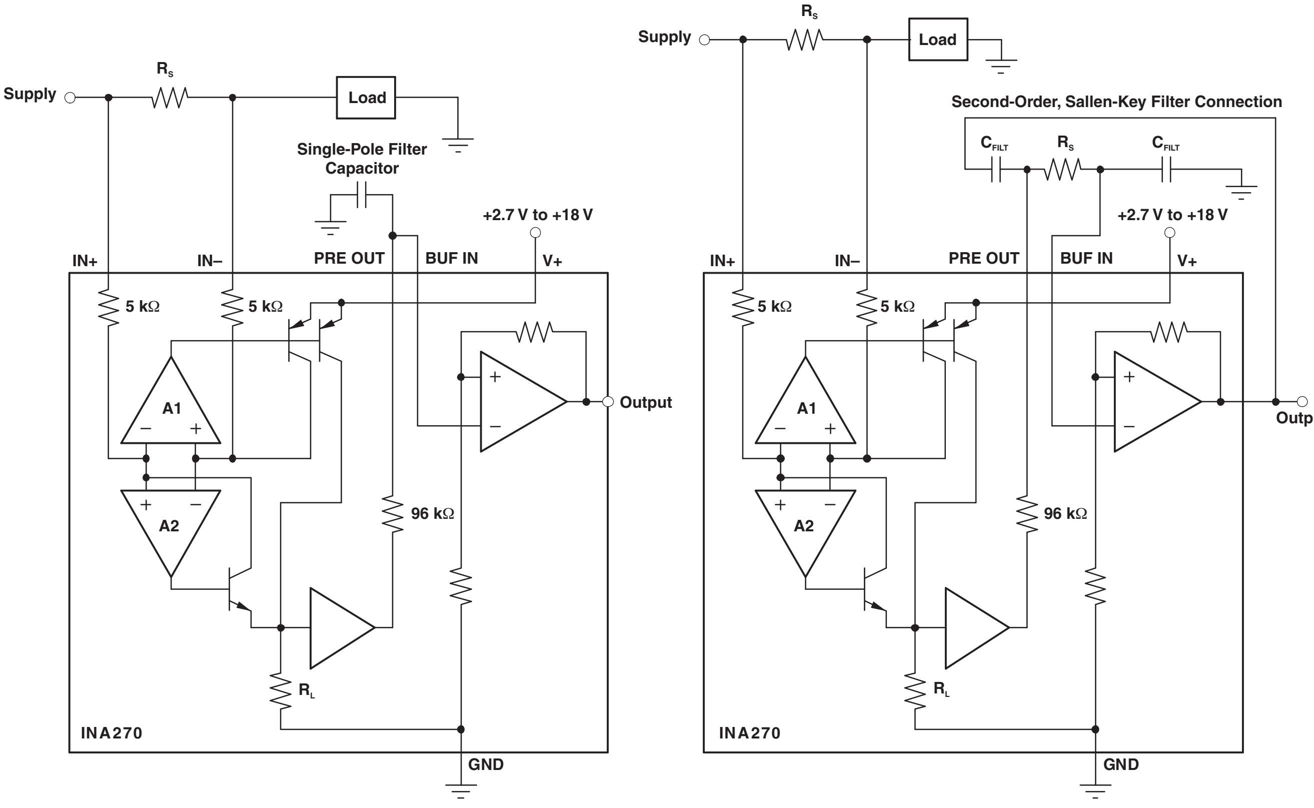
Despite the use of internal zener-type ESD protection, the INA270 and INA271 are not suited to using external resistors in series with the inputs, since the internal gain resistors can vary up to ±30%, but the internal resistors are tightly matched. If gain accuracy is not important, then resistors can be added in series with the INA270 and INA271 inputs, with two equal resistors on each input.

Output Voltage Range

The output of the INA270 and INA271 is accurate within the output voltage swing range set by the power-supply pin, V+.

The INA270 and INA271 readily enable the inclusion of filtering between the preamp output and buffer input. Single-pole filtering can be accomplished with a single capacitor because of the 96-kΩ output impedance at PRE OUT on pin 3 (see Figure 2a).

The INA270 and INA271 readily lend themselves to second-order Sallen-Key configurations (see Figure 2b). When designing these configurations consider that the PRE OUT 96-kΩ output impedance exhibits an initial variation of ±30% with the addition of a –2200-ppm/°C temperature coefficient.



a) Single-Pole Filter b) Second-Order, Sallen-Key Filter

A. The INA270 and INA271 can be easily connected for first-order or second-order filtering. Remember to use the appropriate buffer gain (INA270 = 1.4, INA271 = 2) when designing Sallen-Key configurations.

Figure 2. First-Order or Second-Order Filtering

Accuracy Variations as a Result of V_{SENSE} and Common-Mode Voltage

The accuracy of the INA270 and INA271 current-shunt monitors is a function of two main variables: V_{SENSE} ($V_{IN+} – V_{IN–}$) and common-mode voltage, V_{CM}, relative to the supply voltage, V_S. V_{CM} is expressed as ($V_{IN+} + V_{IN–}$)/2; however, in practice, V_{CM} is seen as the voltage at V_{IN+} because the voltage drop across V_{SENSE} is usually small.

This section addresses the accuracy of these specific operating regions:

Normal Case 1: $V_{SENSE} \geq 20$ mV, $V_{CM} \geq V_S$
Normal Case 2: $V_{SENSE} \geq 20$ mV, $V_{CM} < V_S$
Low V_{SENSE} Case 1: $V_{SENSE} < 20$ mV, $–16\text{ V} \leq V_{CM} < 0$
Low V_{SENSE} Case 2: $V_{SENSE} < 20$ mV, $0\text{ V} \leq V_{CM} \leq V_S$
Low V_{SENSE} Case 3: $V_{SENSE} < 20$ mV, $V_S < V_{CM} \leq 80$ V

Normal Case 1: $V_{SENSE} \geq 20$ mV, $V_{CM} \geq V_S$

This region of operation provides the highest accuracy. Here, the input offset voltage is characterized and measured using a two-step method. First, the gain is determined by Equation 1.

$$G = \frac{V_{OUT1} - V_{OUT2}}{100\text{ mV} - 20\text{ mV}} \tag{1}$$

Where:

V_{OUT1} = Output voltage with V_{SENSE} = 100 mV
V_{OUT2} = Output voltage with V_{SENSE} = 20 mV

Then the offset voltage is measured at V_{SENSE} = 100 mV and referred to the input (RTI) of the current-shunt monitor, as shown in Equation 2.

$$V_{OS}\text{RTI (referred to input)} = \left(\frac{V_{OUT1}}{G}\right) - 100\text{ mV} \tag{2}$$

In Typical Characteristics, the Output Error vs Common-Mode Voltage curve shows the highest accuracy for the this region of operation. In this plot, V_S = 12 V; for $V_{CM} \geq 12$ V, the output error is at its minimum. This case is also used to create the $V_{SENSE} \geq 20$ mV output specifications in Electrical Characteristics.

Low V_{SENSE} Case 1: $V_{SENSE} < 20$ mV, $–16\text{ V} \leq V_{CM} < 0$; and Low V_{SENSE} Case 3: $V_{SENSE} < 20$ mV, $V_S < V_{CM} \leq 80$ V

Although the INA270 family of devices are not designed for accurate operation in either of these regions, some applications are exposed to these conditions. For example, when monitoring power supplies that are switched on and off while V_S is still applied to the INA270 or INA271, it is important to know what the behavior of the devices is in these regions.

As V_{SENSE} approaches 0 mV, in these V_{CM} regions, the device output accuracy degrades. A larger-than-normal offset can appear at the current-shunt monitor output with a typical maximum value of V_{OUT} = 60 mV for V_{SENSE} = 0 mV. As V_{SENSE} approaches 20 mV, V_{OUT} returns to the expected output value with accuracy as specified in Electrical Characteristics. Figure 3 illustrates this effect using the INA271 (Gain = 20).

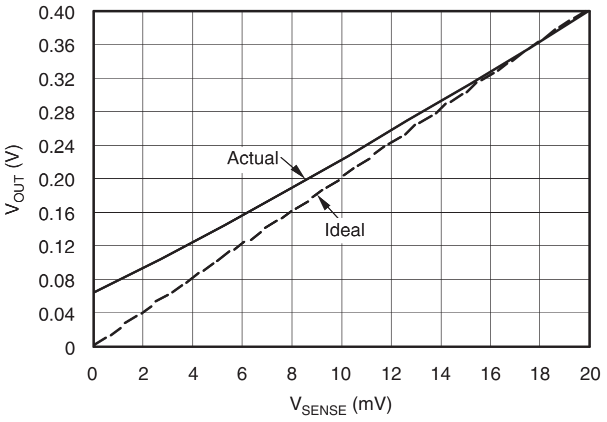


Figure 3. Example for Low V_{SENSE} Cases 1 and 3 (INA271, Gain = 20)

Low V_{SENSE} Case 2: $V_{SENSE} < 20$ mV, $0 V \leq V_{CM} \leq V_S$

This region of operation is the least accurate for the INA270 family. To achieve the wide input common-mode voltage range, these devices use two operational amplifier (op amp) front ends in parallel. One op amp front end operates in the positive input common-mode voltage range, and the other in the negative input region. For this case, neither of these two internal amplifiers dominates and overall loop gain is very low. Within this region, V_{OUT} approaches voltages close to linear operation levels for Normal Case 2.

This deviation from linear operation becomes greatest the closer V_{SENSE} approaches 0 V. Within this region, as V_{SENSE} approaches 20 mV, device operation is closer to that described by Normal Case 2. Figure 4 illustrates this behavior for the INA271. The V_{OUT} maximum peak for this case is determined by maintaining a constant V_S, setting V_{SENSE} = 0 mV and sweeping V_{CM} from 0 V to V_S. The exact V_{CM} at which V_{OUT} peaks during this case varies from part to part. The maximum peak voltage for the INA270 is 0.28 V; for the INA271, the maximum peak voltage is 0.4 V.

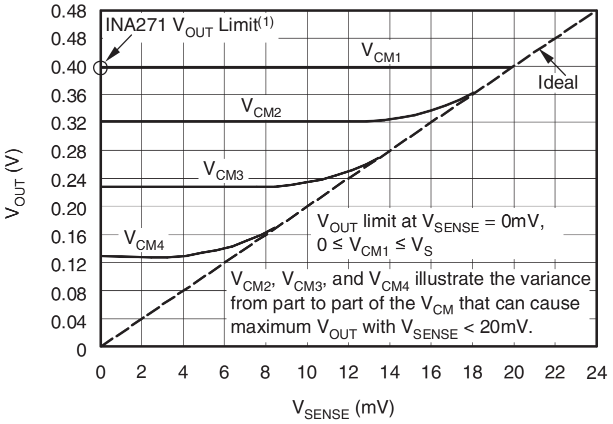


Figure 4. Example for Low V_{SENSE} Case 2 (INA271, Gain = 20)

Shutdown

The INA270 and INA271 do not provide a shutdown pin; however, because they consume a quiescent current less than 1 mA, they can be powered by either the output of logic gates or by transistor switches to supply power. Driving the gate low shuts down the INA270/INA271. Use a totem-pole output buffer or gate that can provide sufficient drive along with 0.1-µF bypass capacitor, preferably ceramic with good high-frequency characteristics. This gate should have a supply voltage of 3 V or greater, because the INA270 and INA271 require a minimum supply greater than 2.7 V. In addition to eliminating quiescent current, this gate also turns off the 10-µA bias current present at each of the inputs. Note that the IN+ and IN– inputs are able to withstand full common-mode voltage under all powered and under-powered conditions. An example shutdown circuit is shown in Figure 5.

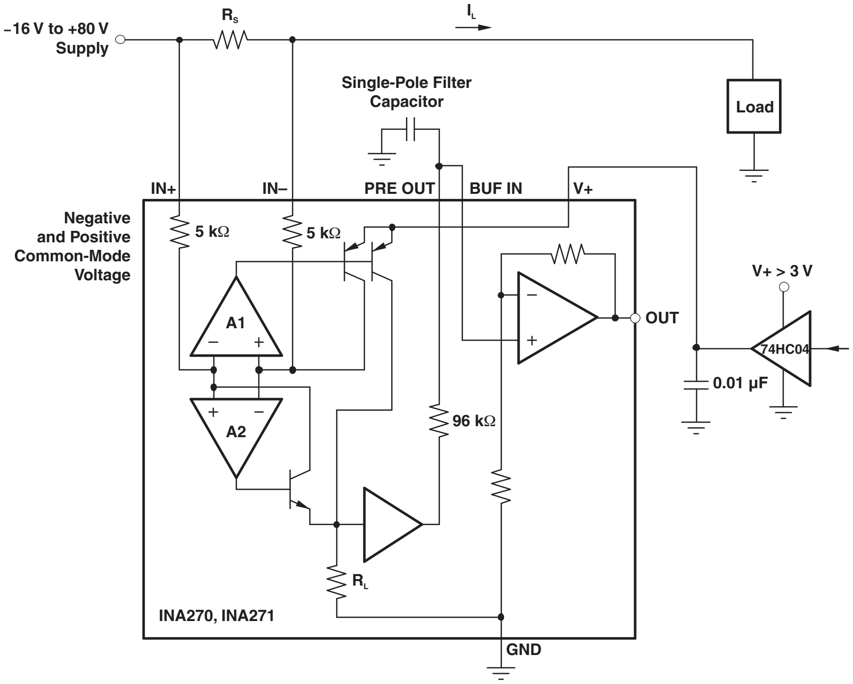


Figure 5. INA270/INA271 Example Shutdown Circuit

RFI/EMI

Attention to good layout practices is always recommended. Keep traces short and, when possible, use a printed circuit board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Small ceramic capacitors placed directly across amplifier inputs can reduce RFI/EMI sensitivity. PCB layout should locate the amplifier as far away as possible from RFI sources. Sources can include other components in the same system as the amplifier itself, such as inductors (particularly switched inductors handling a lot of current and at high frequencies). RFI can generally be identified as a variation in offset voltage or dc signal levels with changes in the interfering RF signal. If the amplifier cannot be located away from sources of radiation, shielding may be needed. Twisting wire input leads makes them more resistant to RF fields. The difference in input pin location of the INA270 and INA271 versus the INA193 through INA198 may provide different EMI performance.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
INA270AQDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples
INA271AQDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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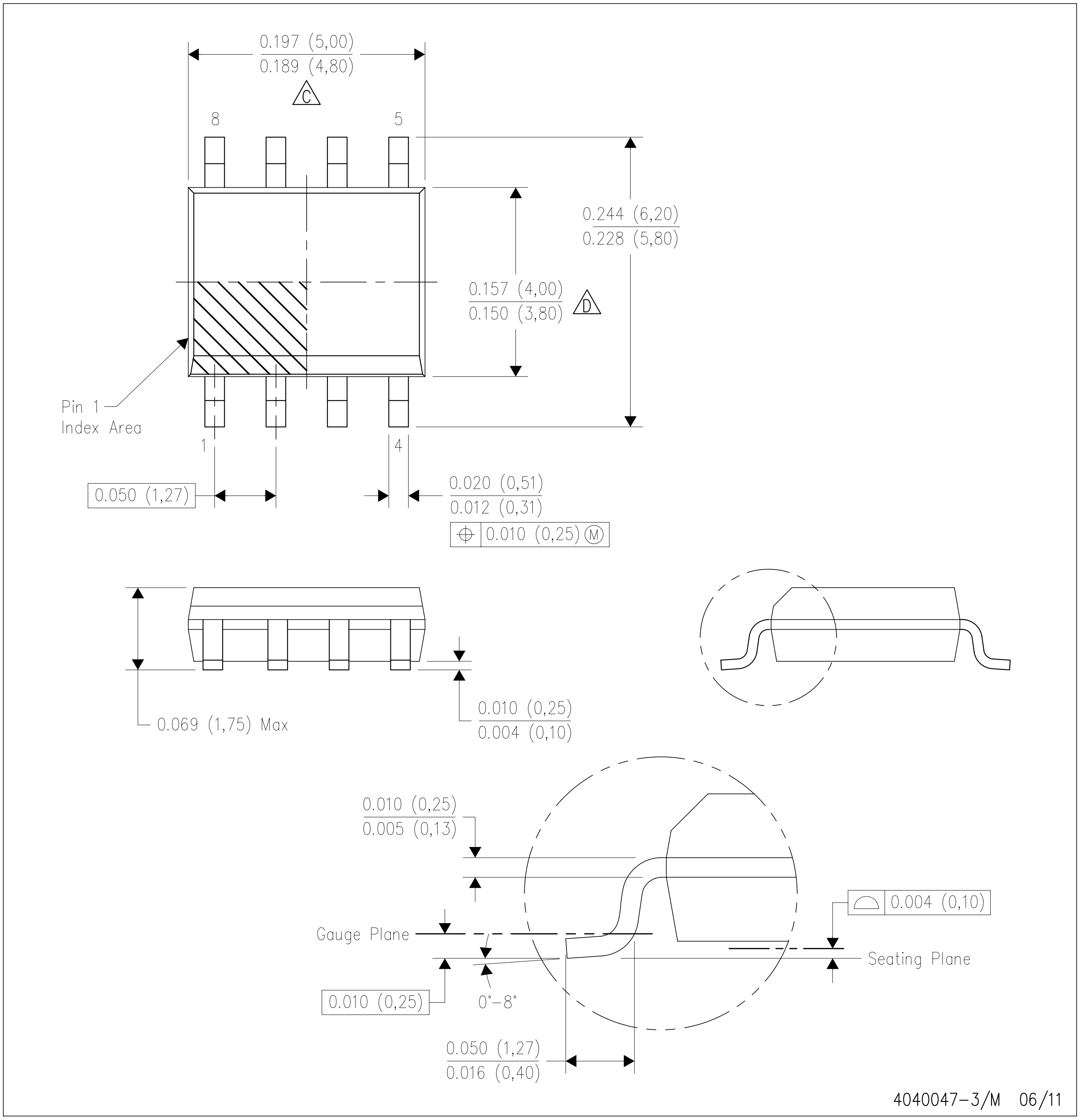
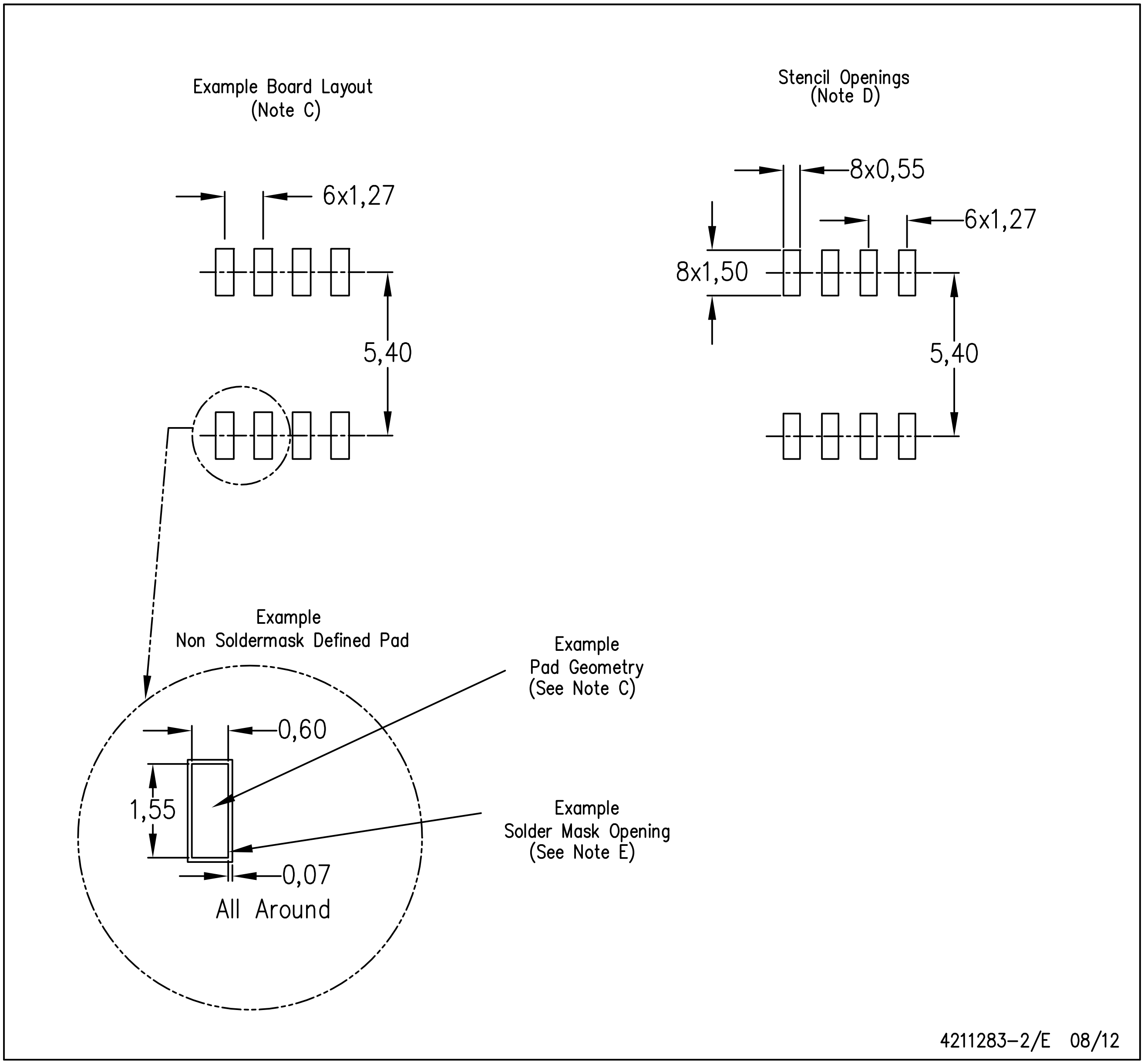
D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS–012 variation AA.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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