High-Accuracy, Wide Common-Mode Range, Bi-Directional CURRENT SHUNT MONITOR Zerø-Drift Series

Check for Samples: INA282, INA283, INA284, INA285, INA286

FEATURES

- **WIDE COMMON-MODE RANGE: –14V to 80V**
- **OFFSET VOLTAGE: ±20µV**
- **CMRR: 140dB**
- **ACCURACY:**
  - **±1.4% Gain Error (Max)**
  - **0.3µV/°C Offset Drift**
  - **0.005%/°C Gain Drift (Max)**
- **AVAILABLE GAINS:**
  - **50V/V: INA282**
  - **100V/V: INA286**
  - **200V/V: INA283**
  - **500V/V: INA284**
  - **1000V/V: INA285**
- **QUIESCENT CURRENT: 900µA (Max)**

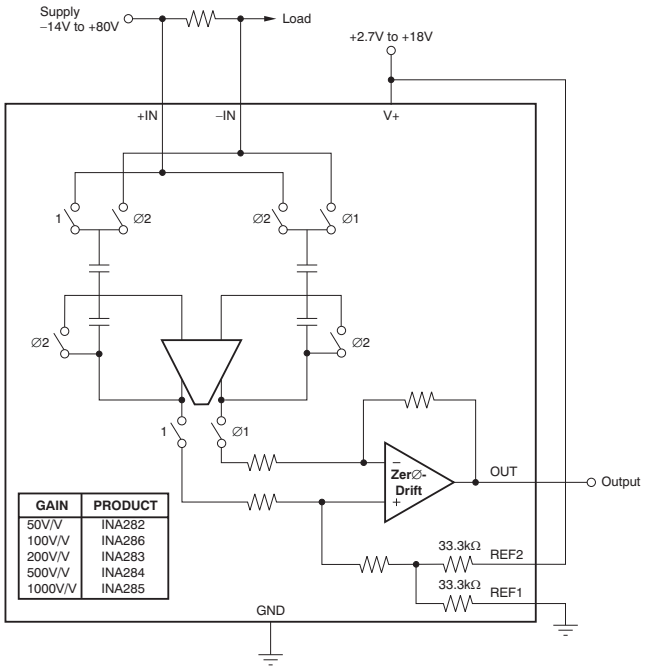
APPLICATIONS

- **TELECOM EQUIPMENT**
- **AUTOMOTIVE**
- **POWER MANAGEMENT**
- **SOLAR INVERTERS**

DESCRIPTION

The INA282 family, which includes the INA282, INA283, INA284, INA285, and INA286 devices, are voltage output current shunt monitors that can sense drops across shunts at common-mode voltages from –14V to +80V, independent of the supply voltage. The low offset of the Zerø-Drift architecture enables current sensing with maximum drops across the shunt as low as 10mV full-scale.

These current shunt monitors operate from a single +2.7V to +18V supply, drawing a maximum of 900µA of supply current. They are specified over the extended operating temperature range of –40°C to +125°C, and offered in an SOIC-8 package.



GAIN	PRODUCT
50V/V	INA282
100V/V	INA286
200V/V	INA283
500V/V	INA284
1000V/V	INA285

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	GAIN	PACKAGE	PACKAGE DESIGNATOR	PACKAGE MARKING
INA282	50V/V	SOIC-8	D	I282A
INA283	200V/V	SOIC-8	D	I283A
INA284	500V/V	SOIC-8	D	I284A
INA285	1000V/V	SOIC-8	D	I285A
INA286	100V/V	SOIC-8	D	I286A

(1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet, or refer to the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		INA282, INA283, INA284, INA285, INA286	UNIT
Supply Voltage		+18	V
Analog Inputs, V_{+IN}, V_{-IN} (2)	Differential (V_{+IN}) – (V_{-IN})(3)	–5 to +5	V
	Common-Mode	–14 to +80	V
Ref1, Ref2, Out		GND–0.3 to (V+) + 0.3	V
Input Current into Any Pin		5	mA
Storage Temperature		–65 to +150	°C
Junction Temperature		+150	°C
ESD Ratings:	Human Body Model (HBM)	3000	V
	Charged-Device Model (CDM)	1000	V
	Machine Model (MM)	200	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) V_{+IN} and V_{-IN} are the voltages at the +IN and –IN pins, respectively.
(3) Input voltages must not exceed common-mode rating.

THERMAL INFORMATION

THERMAL METRIC(1)		INA282AID, INA283AID, INA284AID, INA285AID, INA286AID	UNITS
		D	
		8	
θ_{JA}	Junction-to-ambient thermal resistance	134.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	72.9	
θ_{JB}	Junction-to-board thermal resistance	61.3	
ψ_{JT}	Junction-to-top characterization parameter	18.9	
ψ_{JB}	Junction-to-board characterization parameter	54.3	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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ELECTRICAL CHARACTERISTICS

Boldface limits apply over the specified temperature range, **T_A = –40°C to +125°C.**
At T_A = +25°C, V+ = 5V, V_{+IN} = 12V, V_{REF1} = V_{REF2} = 2.048V referenced to GND, and V_{SENSE} = V_{+IN} – $V_{–IN}$, unless otherwise noted.

PARAMETER		CONDITIONS	INA282, INA283, INA284, INA285, INA286 MIN	TYP	MAX	UNIT
INPUT						
Offset Voltage, RTI(1)	V_{OS}	V_{SENSE} = 0mV		±20	±70	µV
vs Temperature	**dV_{OS}/dT**			**±0.3**	**±1.5**	**µV/°C**
vs Power Supply	PSRR	V_S = +2.7V to +18V, V_{SENSE} = 0mV		3		µV/V
Common-Mode Input Range	**V_{CM}**		**–14**		**80**	**V**
Common-Mode Rejection	**CMRR**	**V_{+IN} = –14V to +80V, V_{SENSE} = 0mV**	**120**	**140**		**dB**
Input Bias Current per Pin(2)	I_B	V_{SENSE} = 0mV		25		µA
Input Offset Current	I_{OS}	V_{SENSE} = 0mV		1		µA
Differential Input Impedance				6		kΩ
REFERENCE INPUTS						
Reference Input Gain				1		V/V
Reference Input Voltage Range(3)			0		V_{GND} + 9	V
Divider Accuracy(4)				±0.2	±0.5	%
Reference Voltage Rejection Ratio		$V_{REF}1$ = $V_{REF}2$ = 40mV to 9V, V+ = 18V				
INA282				±25	±75	µV/V
vs Temperature				**0.055**		**µV/V/°C**
INA283				±13	±30	µV/V
vs Temperature				**0.040**		**µV/V/°C**
INA284				±6	±25	µV/V
vs Temperature				**0.015**		**µV/V/°C**
INA285				±4	±10	µV/V
vs Temperature				**0.010**		**µV/V/°C**
INA286				±17	±45	µV/V
vs Temperature				**0.040**		**µV/V/°C**
GAIN(5)		GND + 0.5V ≤ V_{OUT} ≤ (V+) – 0.5V; V_{REF1} = V_{REF2} = (V+)/2 for all devices				
Gain	G					
INA282		V+ = +5V		50		V/V
INA283		V+ = +5V		200		V/V
INA284		V+ = +12V		500		V/V
INA285		V+ = +12V		1000		V/V
INA286		V+ = +5V		100		V/V
Gain Error						
INA282, INA283, INA286				±0.4	±1.4	%
INA284, INA285				±0.4	±1.6	%
vs Temperature				**0.0008**	**0.005**	**%/°C**
OUTPUT						
Nonlinearity Error				±0.01		%
Output Impedance				1.5		Ω
Maximum Capacitive Load		No sustained oscillation		1		nF

(1) RTI = referred-to-input.
(2) See typical characteristic graph Figure 20 .
(3) The average of the voltage on pins REF1 and REF2 must be between V_{GND} and the lesser of (V_{GND}+9V) and V+.
(4) Reference divider accuracy specifies the match between the reference divider resistors using the configuration in Figure 37.
(5) See typical characteristic graph Figure 25.

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ELECTRICAL CHARACTERISTICS (continued)

Boldface limits apply over the specified temperature range, **T_A = –40°C to +125°C.**
At T_A = +25°C, V+ = 5V, V_{+IN} = 12V, V_{REF1} = V_{REF2} = 2.048V referenced to GND, and V_{SENSE} = V_{+IN} – $V_{–IN}$, unless otherwise noted.

PARAMETER	CONDITIONS	INA282, INA283, INA284, INA285, INA286 MIN	TYP	MAX	UNIT
VOLTAGE OUTPUT(6)	**R_L = 10kΩ to GND**				
Swing to V+ Power-Supply Rail	V+ = 5V		**(V+)–0.17**	**(V+)–0.4**	**V**
Swing to GND			**GND+0.015**	**GND+0.04**	**V**
FREQUENCY RESPONSE					
Effective Bandwidth(7) BW					
INA282			10		kHz
INA283			10		kHz
INA284			4		kHz
INA285			2		kHz
INA286			10		kHz
NOISE, RTI(8)					
Voltage Noise Density	1kHz		110		nV/√Hz
POWER SUPPLY					
Specified Voltage Range V_S		**+2.7**		**+18**	**V**
Quiescent Current I_Q			600	900	µA
TEMPERATURE RANGE					
Specified Range		–40		+125	°C

(6) See typical characteristic graphs Figure 29 through Figure 31.
(7) See typical characteristic graph Figure 15 and the *Effective Bandwidth* section in the Applications Information.
(8) RTI = referred-to-input.

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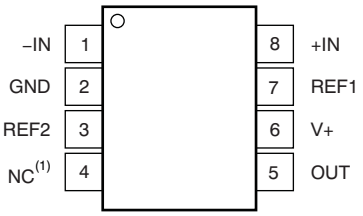
PIN CONFIGURATION

D PACKAGE
SOIC-8
(TOP VIEW)



(1) NC: This pin is not internally connected. The NC pin should either be left floating or connected to GND.

PIN DESCRIPTIONS

SOIC-8		DESCRIPTION
PIN NO.	NAME	
1	–IN	Connection to negative side of shunt resistor.
2	GND	Ground
3	REF2	Reference voltage connection - See application section for connection options.
4	NC	This pin is not internally connected. The NC pin should either be left floating or connected to GND.
5	OUT	Output voltage
6	V+	Power supply
7	REF1	Reference voltage connection - See application section for connection options.
8	+IN	Connection to positive side of shunt resistor.

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TYPICAL CHARACTERISTICS

At T_A = +25°C, V+ = 5V, V_{+IN} = 12V, V_{REF1} = V_{REF2} = 2.048V referenced to GND, and V_{SENSE} = V_{+IN} – $V_{–IN}$, unless otherwise noted.

START-UP TRANSIENT RESPONSE

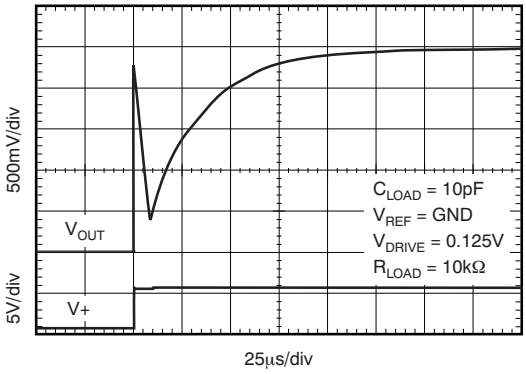

Figure 1.

START-UP TRANSIENT RESPONSE

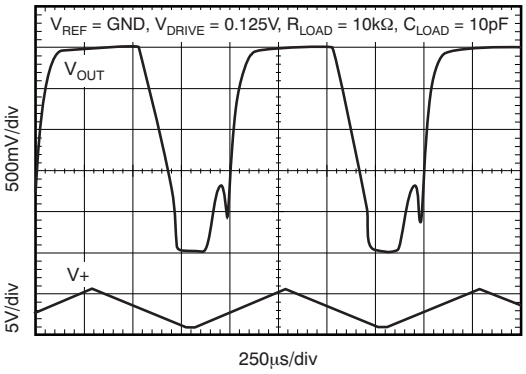

Figure 2.

12V COMMON-MODE STEP RESPONSE

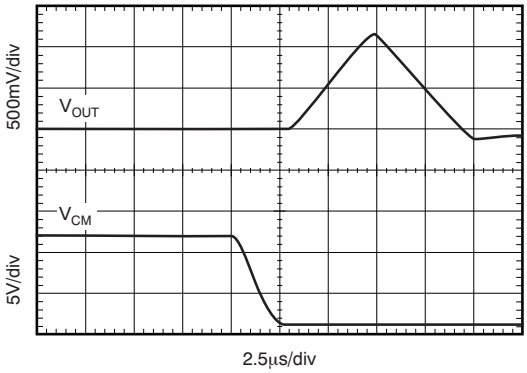

Figure 3.

12V COMMON-MODE STEP RESPONSE

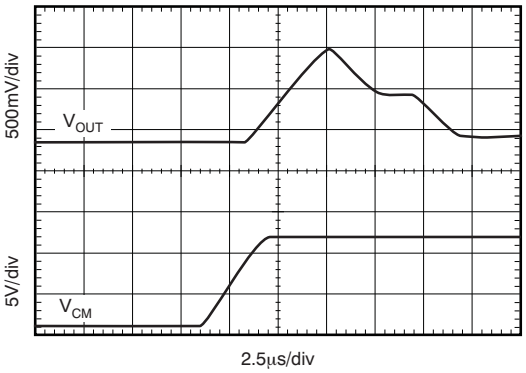

Figure 4.

12V COMMON-MODE STEP RESPONSE

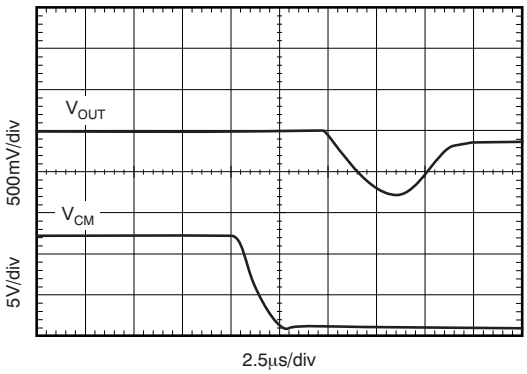

Figure 5.

12V COMMON-MODE STEP RESPONSE

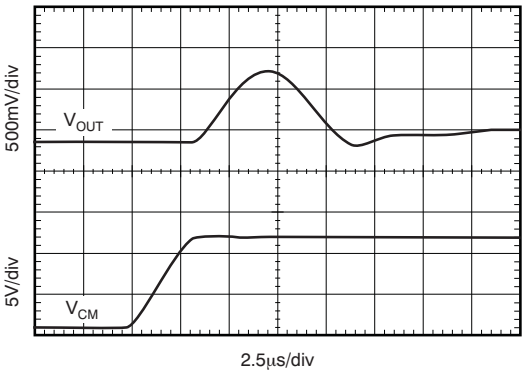

Figure 6.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V+ = 5V, V_{+IN} = 12V, V_{REF1} = V_{REF2} = 2.048V referenced to GND, and V_{SENSE} = V_{+IN} – $V_{–IN}$, unless otherwise noted.

50V COMMON-MODE STEP RESPONSE

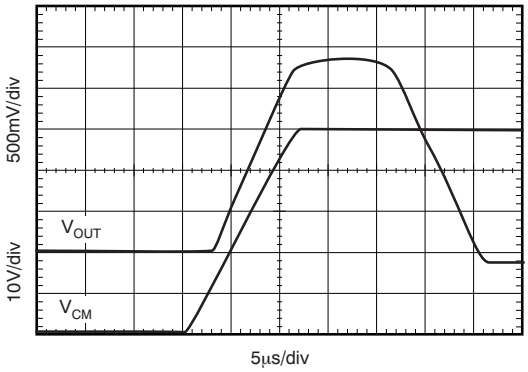

Figure 7.

50V COMMON-MODE STEP RESPONSE

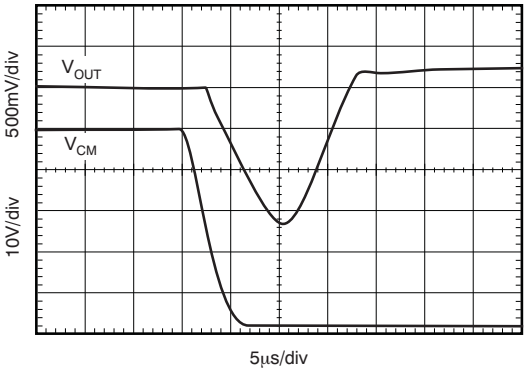

Figure 8.

100mV STEP RESPONSE

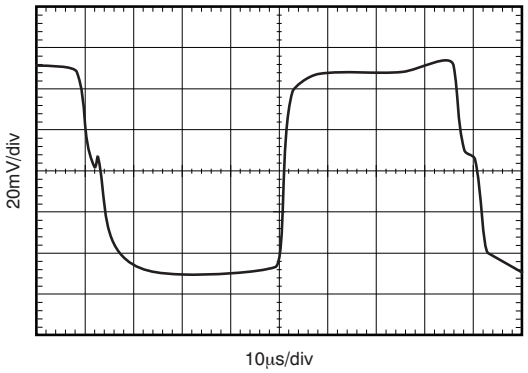

Figure 9.

500mV STEP RESPONSE

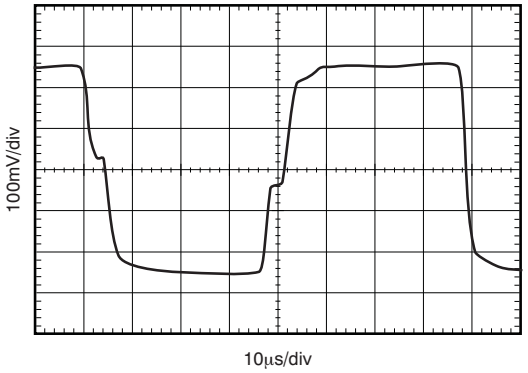

Figure 10.

4V STEP RESPONSE

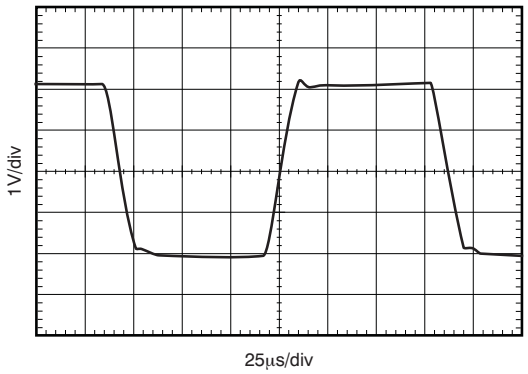

Figure 11.

17V STEP RESPONSE

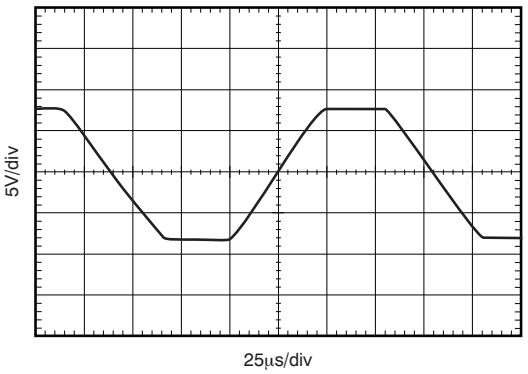

Figure 12.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V+ = 5V, V_{+IN} = 12V, V_{REF1} = V_{REF2} = 2.048V referenced to GND, and V_{SENSE} = V_{+IN} – $V_{–IN}$, unless otherwise noted.

INPUT OVERLOAD

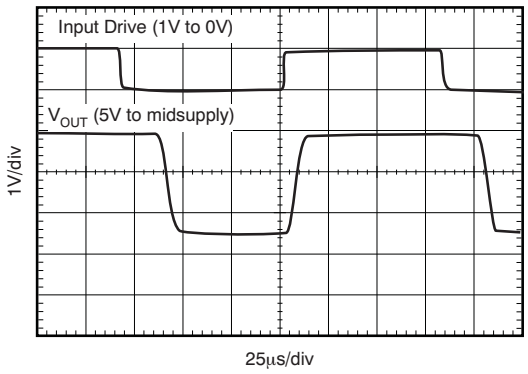

Figure 13.

INA282 PSRR (RTI) vs FREQUENCY

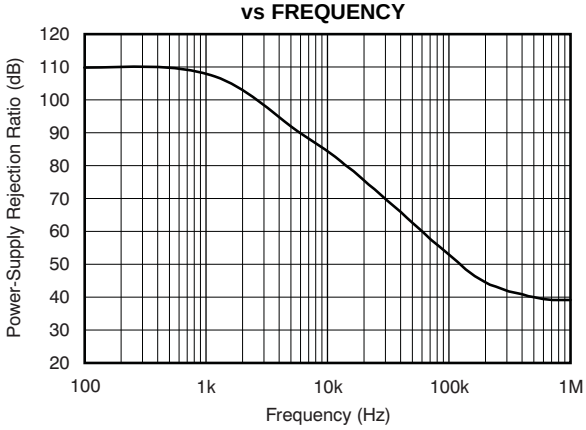

Figure 14.

GAIN vs FREQUENCY

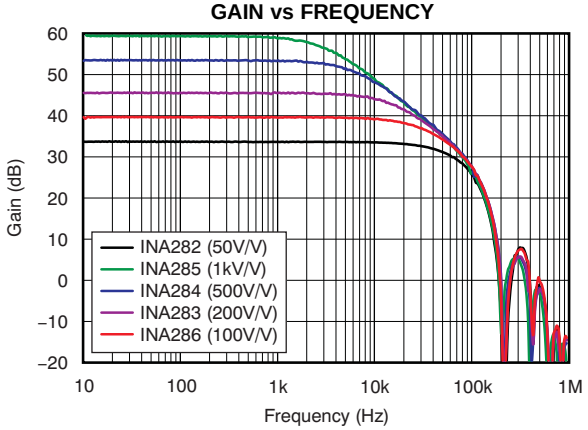

Figure 15.

INA284 COMMON-MODE REJECTION RATIO (RTI)

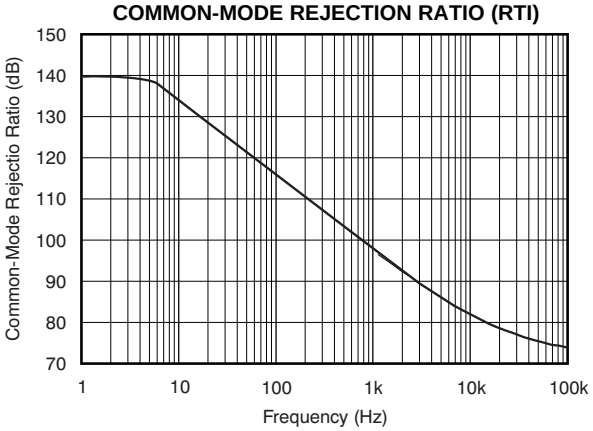

Figure 16.

INA282 COMMON-MODE SLEW RATE INDUCED OFFSET

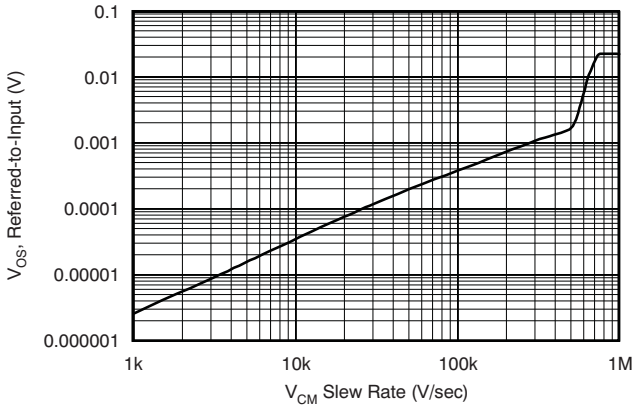

Figure 17.

INA286 OUTPUT IMPEDANCE vs FREQUENCY

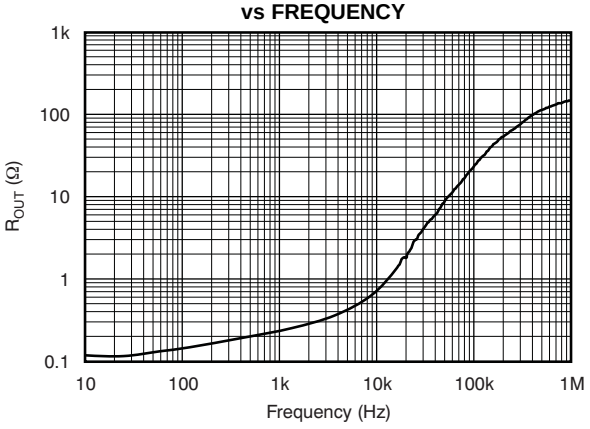

Figure 18.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V+ = 5V, V_{+IN} = 12V, V_{REF1} = V_{REF2} = 2.048V referenced to GND, and V_{SENSE} = V_{+IN} – $V_{–IN}$, unless otherwise noted.

INA282 TYPICAL NONLINEARITY vs OUTPUT VOLTAGE

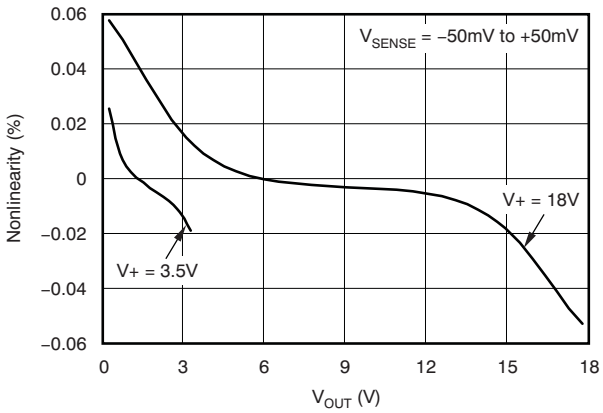

Figure 19.

INA283 +IN BIAS CURRENT vs COMMON-MODE VOLTAGE

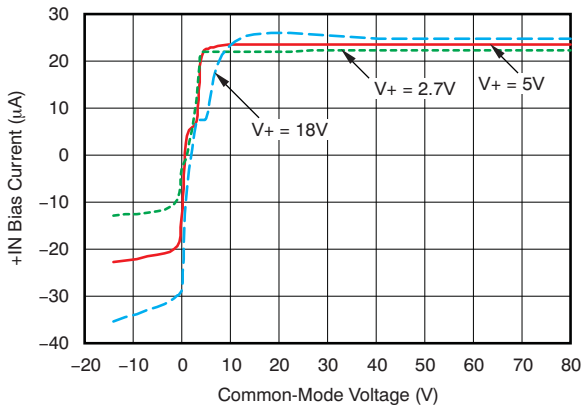

Figure 20.

INA283 QUIESCENT CURRENT vs COMMON-MODE VOLTAGE

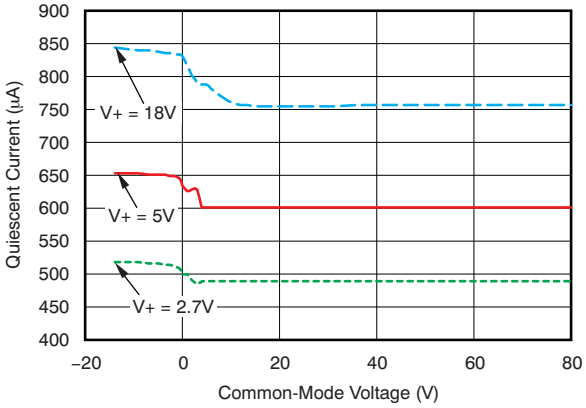

Figure 21.

QUIESCENT CURRENT vs SUPPLY VOLTAGE

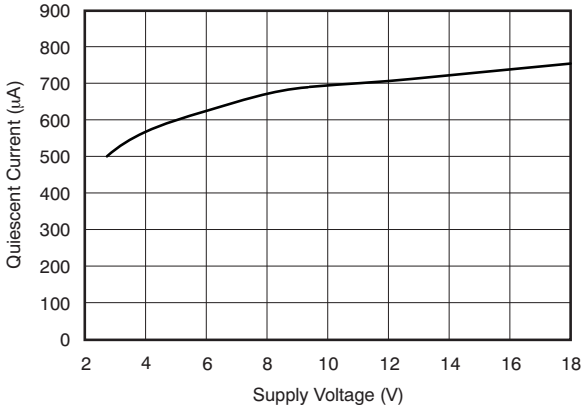

Figure 22.

COMMON-MODE REJECTION RATIO vs TEMPERATURE

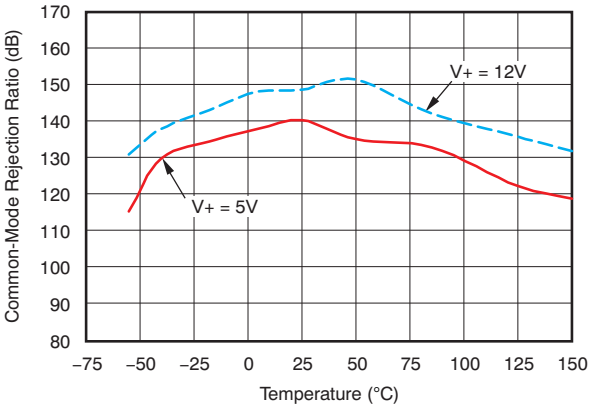

Figure 23.

QUIESCENT CURRENT vs TEMPERATURE

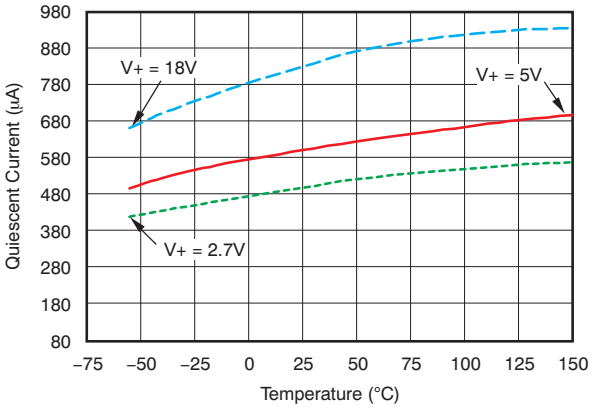

Figure 24.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V+ = 5V, V_{+IN} = 12V, V_{REF1} = V_{REF2} = 2.048V referenced to GND, and V_{SENSE} = V_{+IN} – $V_{–IN}$, unless otherwise noted.

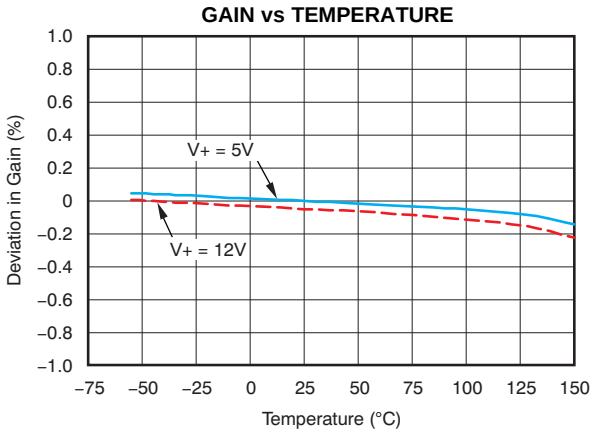

Figure 25.

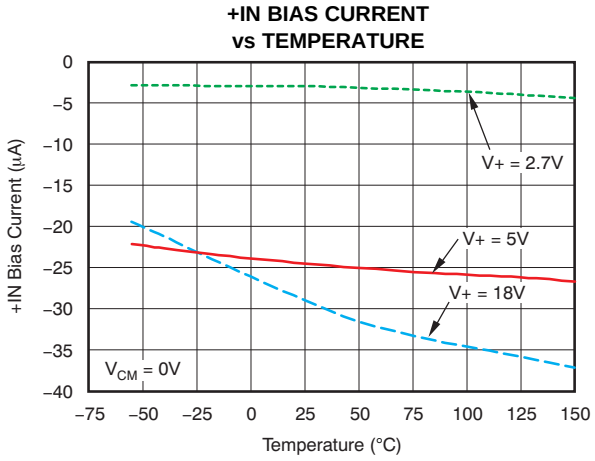

Figure 26.

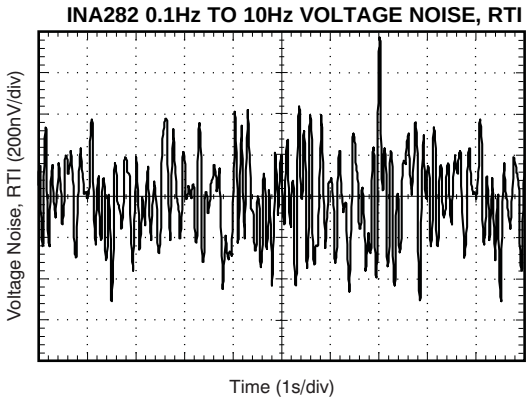

Figure 27.

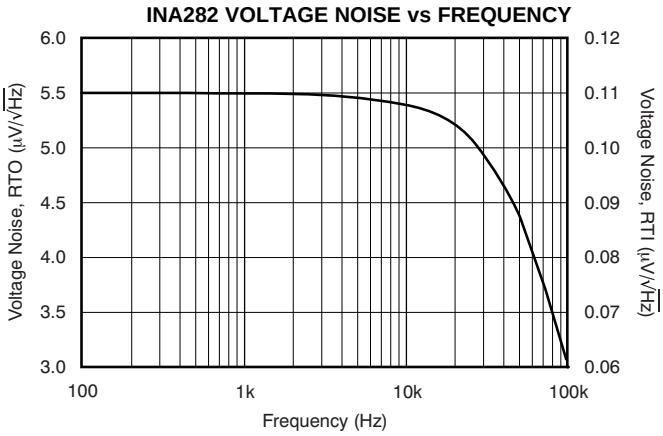

Figure 28.

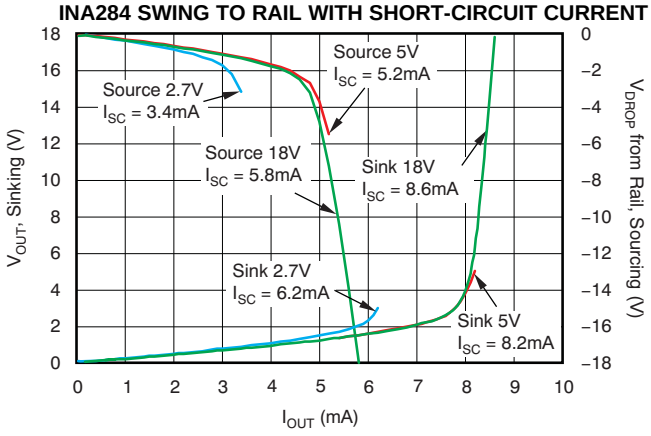

Figure 29.

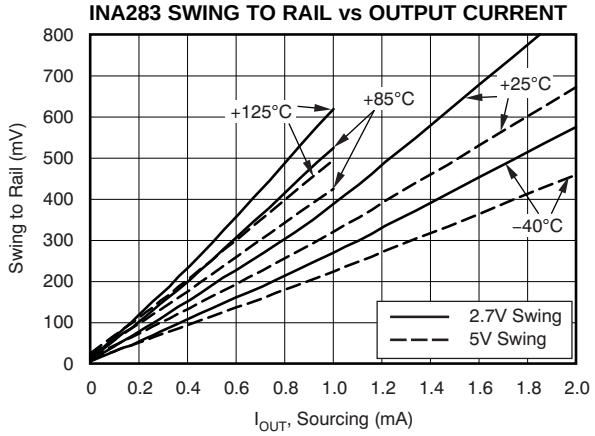

Figure 30.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V+ = 5V, V_{+IN} = 12V, V_{REF1} = V_{REF2} = 2.048V referenced to GND, and V_{SENSE} = V_{+IN} – $V_{–IN}$, unless otherwise noted.

INA283 SWING TO GROUND vs OUTPUT CURRENT

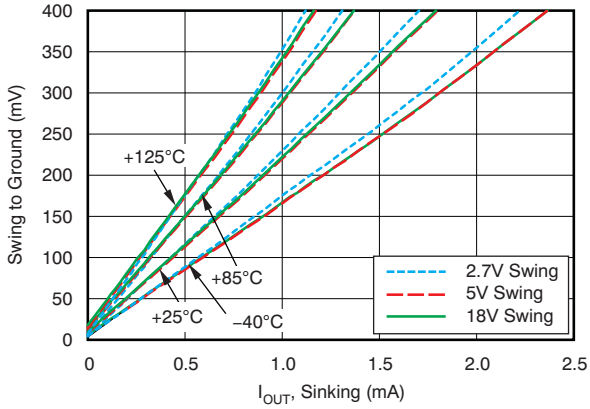

Figure 31.

APPLICATIONS INFORMATION

GENERAL INFORMATION

The INA282 family voltage output current shunt monitors feature a common-mode range that extends 14V below the negative supply rail, as well as up to 80V, which allows use for either low-side or high-side current sensing.

BASIC CONNECTIONS

Figure 32 shows the basic connection of an INA282 family device. The input pins, +IN and –IN, should be connected as closely as possible to the shunt resistor to minimize any resistance in series with the shunt resistance.

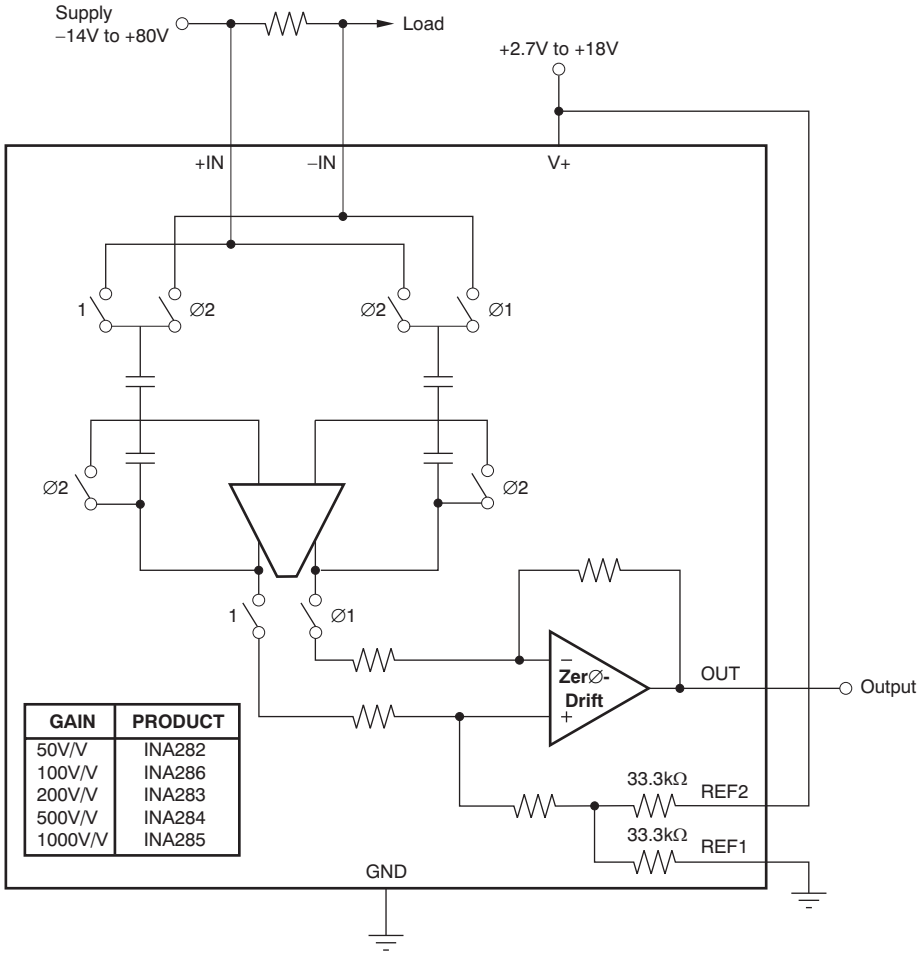

Figure 32. Typical Application

Power-supply bypass capacitors are required for stability. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise. Connect bypass capacitors close to the device pins.

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POWER SUPPLY

The INA282 family can make accurate measurements well outside of its own power-supply voltage, V+, because its inputs (+IN and –IN) may operate anywhere between –14V and +80V independent of V+. For example, the V+ power supply can be 5V while the common-mode voltage being monitored by the shunt may be as high as +80V. Of course, the output voltage range of the INA282 family is constrained by the supply voltage that powers it on V+. Note that when the power to the INA282 family is off (that is, no voltage is supplied to the V+ pin), the input pins (+IN and –IN) are high impedance with respect to ground and typically leak less than ±1μA over the full common-mode range of –14V to +80V

SELECTING R_S

The Zerø-Drift architecture of the INA282 family enables use with full-scale range shunt voltages as low as 10mV.

EFFECTIVE BANDWIDTH

The extremely high dc CMRR of the INA282 family results from the switched capacitor input structure. Because of this architecture, the INA28x exhibits discrete time system behaviors as illustrated in the gain versus frequency graph of Figure 16 and the step response curves of Figure 3 through Figure 10. The response to a step input depends somewhat on the phase of the internal INA28x clock when the input step occurs. It is possible to overload the input amplifier with a rapid change in input common-mode voltage (see Figure 17). Errors as a result of common-mode voltage steps and/or overload situations typically disappear within 15μs after the disturbance is removed.

TRANSIENT PROTECTION

The –14V to +80V common-mode range of the INA282 family is ideal for withstanding automotive fault conditions that range from 12V battery reversal up to +80V transients; no additional protective components are needed up to those levels. In the event that the INA282 family is exposed to transients on the inputs in excess of its ratings, then external transient absorption with semiconductor transient absorbers (Zener or *Transzorbs*) will be necessary. Use of MOVs or VDRs is not recommended except when they are used in addition to a semiconductor transient absorber. Select the transient absorber such that it cannot allow the INA282 family to be exposed to transients greater than 80V (that is, allow for transient absorber tolerance, as well as additional voltage as a result of transient absorber dynamic impedance). Despite the use of internal zener-type electrostatic discharge (ESD) protection, the INA282 family does not lend itself to using external resistors in series with the inputs without degrading gain accuracy.

SHUTDOWN

While the INA282 family does not provide a shutdown pin, the quiescent current of 600μA enables it to be powered from the output of a logic gate. Take the gate low to shut down the INA282 family devices.

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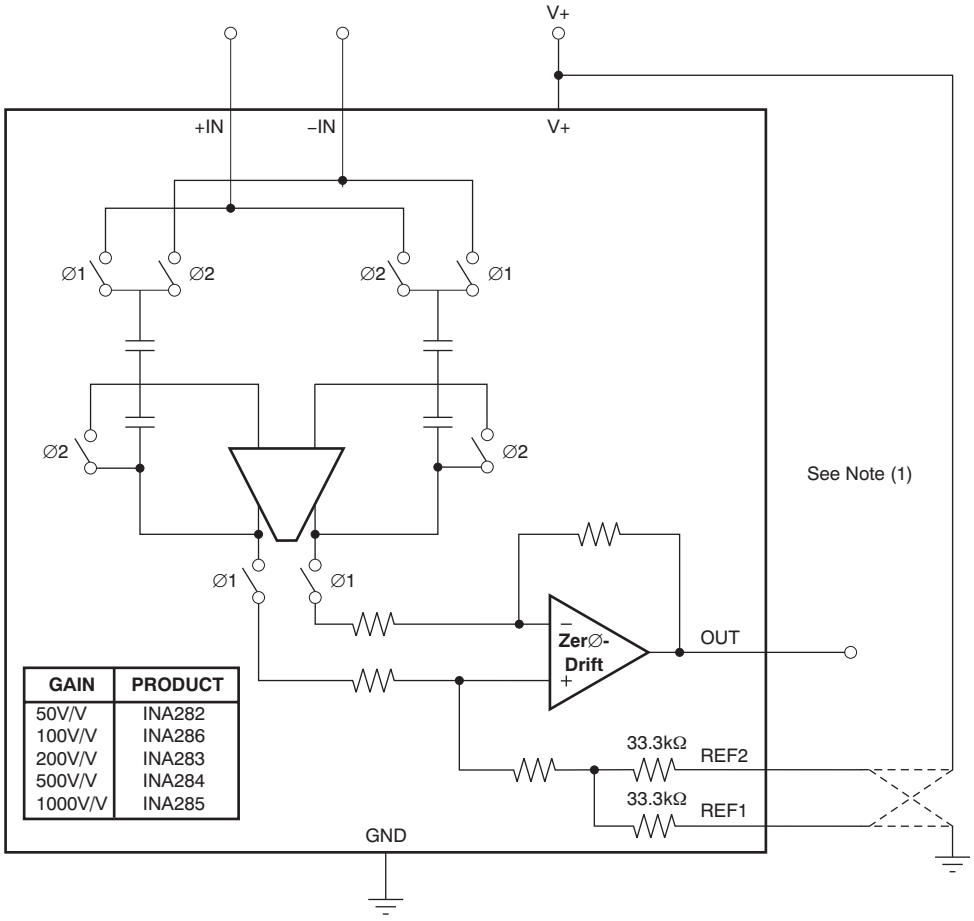
REFERENCE PIN CONNECTION OPTIONS

Figure 33 illustrates a test circuit for reference divider accuracy. The output of the INA282 family can be connected for unidirectional or bidirectional operation. Note that neither the REF1 pin nor the REF2 pin may be connected to any voltage source lower than GND or higher than V+, and that the effective reference voltage (REF1 + REF2)/2 must be 9V or less. This parameter means that the V+ reference output connection shown in Figure 35 is not allowed for V+ greater than 9V. However, the split-supply reference connection shown in Figure 37 is allowed for all values of V+ up to 18V.



(1) Reference divider accuracy is determined by measuring the output with the reference voltage applied to alternate reference resistors, and calculating a result such that the amplifier offset is cancelled in the final measurement.

Figure 33. Test Circuit for Reference Divider Accuracy

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UNIDIRECTIONAL OPERATION

Unidirectional operation allows the INA282 family to measure currents through a resistive shunt in one direction. In the case of unidirectional operation, the output could be set at the negative rail (near ground, and the most common connection) or at the positive rail (near V+) when the differential input is 0V. The output moves to the opposite rail when a correct polarity differential input voltage is applied.

The required polarity of the differential input depends on the output voltage setting. If the output is set at the positive rail, the input polarity must be negative to move the output down. If the output is set at ground, the polarity is positive to move the output up.

The following sections describe how to configure the output for unidirectional operation.

Ground Referenced Output

When using the INA282 family in this mode, both reference inputs are connected to ground; this configuration takes the output to the negative rail when there is 0V differential at the input (as Figure 34 shows).

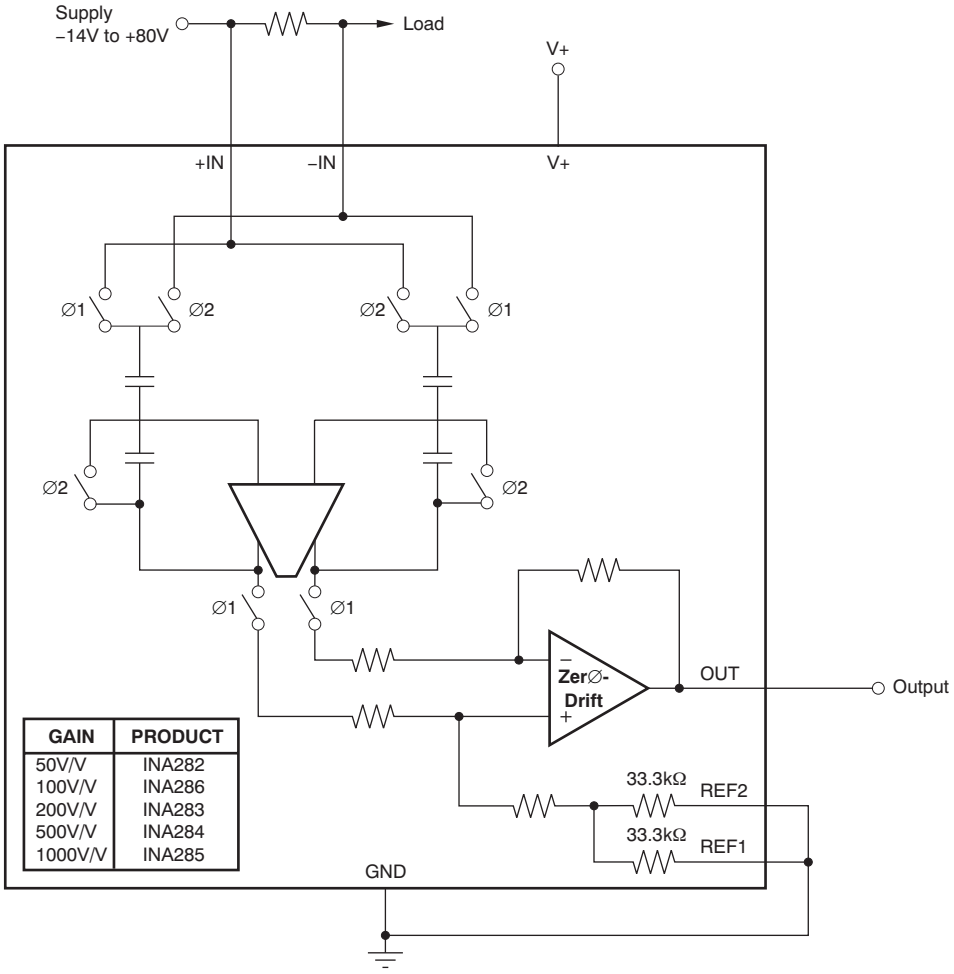

Figure 34. Ground Referenced Output

V+ Referenced Output

This mode is set when both reference pins are connected to the positive supply. It is typically used when a diagnostic scheme requires detection of the amplifier and the wiring before power is applied to the load (as shown in Figure 35).

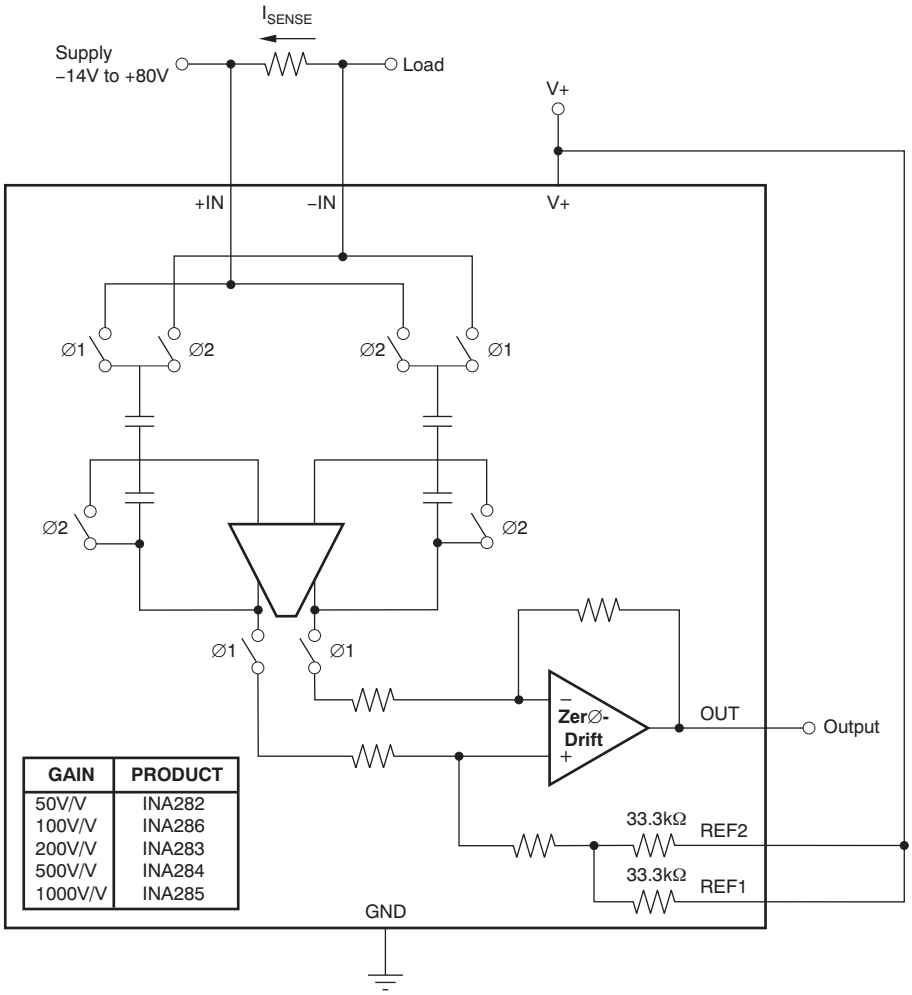

Figure 35. V+ Referenced Output

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BIDIRECTIONAL OPERATION

Bidirectional operation allows the INA282 family to measure currents through a resistive shunt in two directions. In this case, the output can be set anywhere within the limits of what the reference inputs allow (that is, between 0V to 9V, but never to exceed the supply voltage). Typically, it is set at half-scale for equal range in both directions. In some cases, however, it is set at a voltage other than half-scale when the bidirectional current is nonsymmetrical.

The quiescent output voltage is set by applying voltage(s) to the reference inputs. REF1 and REF2 are connected to internal resistors that connect to an internal offset node. There is no operational difference between the pins.

External Reference Output

Connecting both pins together and to a reference produces an output at the reference voltage when there is no differential input; this configuration is illustrated in Figure 36. The output moves down from the reference voltage when the input is negative relative to the –IN pin and up when the input is positive relative to the –IN pin. Note that this technique is the most accurate way to bias the output to a precise voltage.

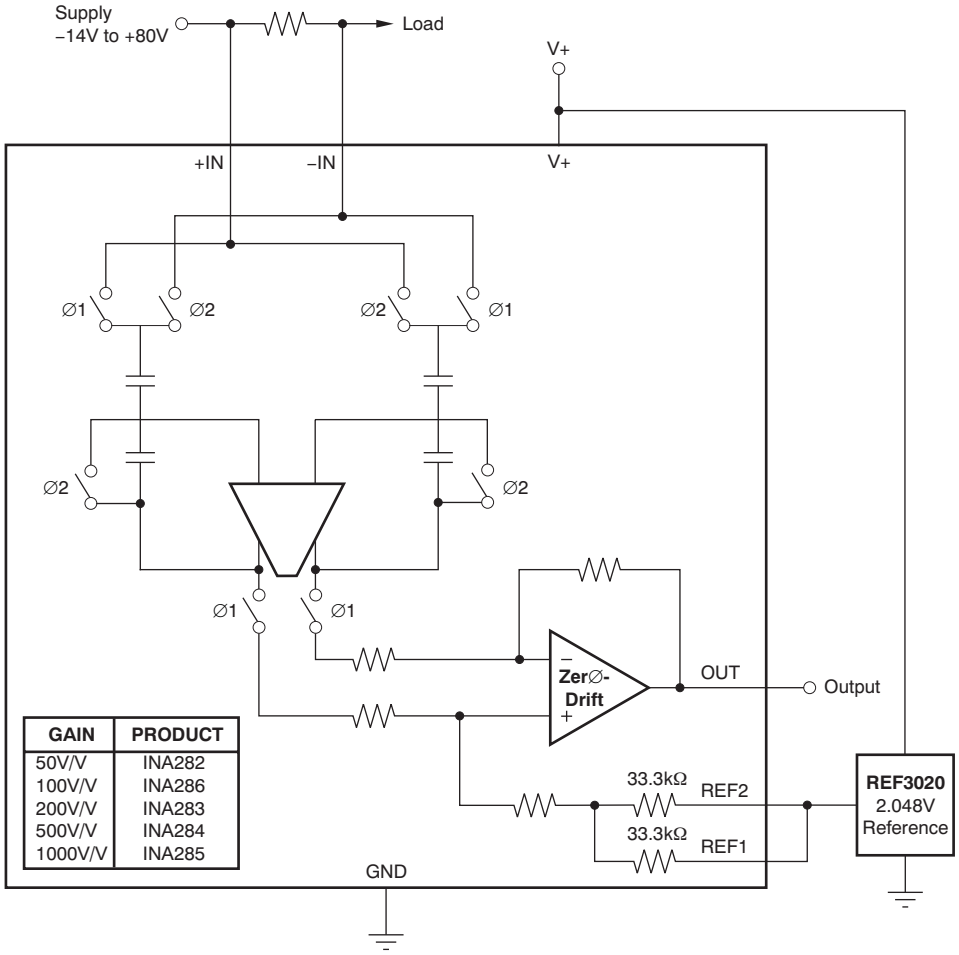

Figure 36. External Reference Output

Splitting the Supply

By connecting one reference pin to V+ and the other to the ground pin, the output is set at half of the supply when there is no differential input, as shown in Figure 37. This method creates a midscale offset that is ratiometric to the supply voltage; thus, if the supply increases or decreases, the output remains at half the supply.

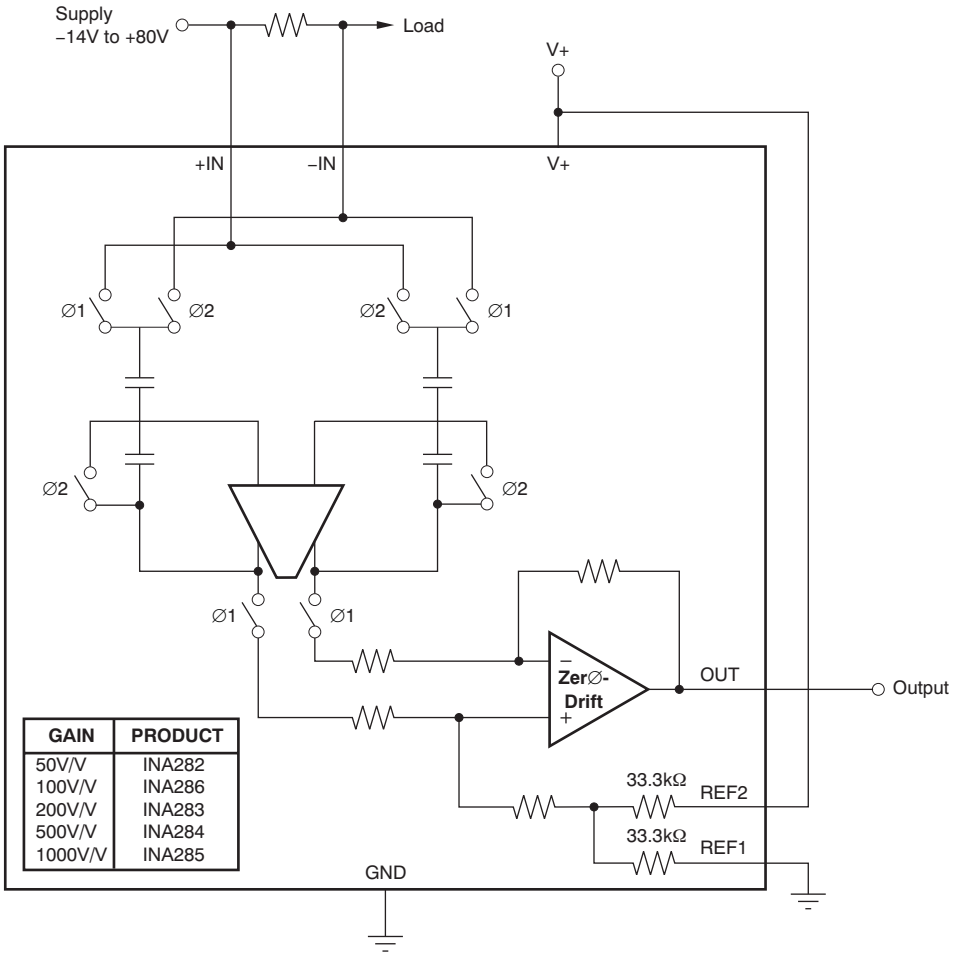

Figure 37. Split-Supply Output

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Splitting an External Reference

In this case, an external reference is divided by 2 with an accuracy of approximately 0.5% by connecting one REF pin to ground and the other REF pin to the reference (as Figure 38 illustrates).

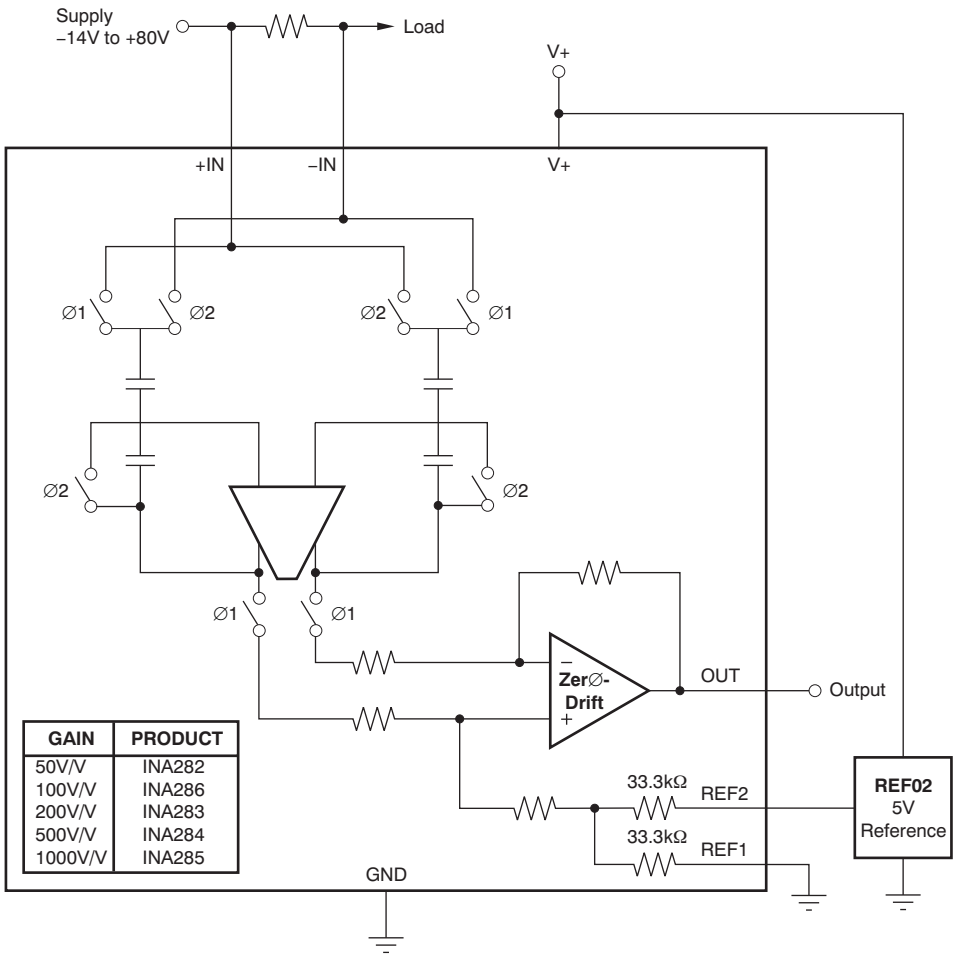
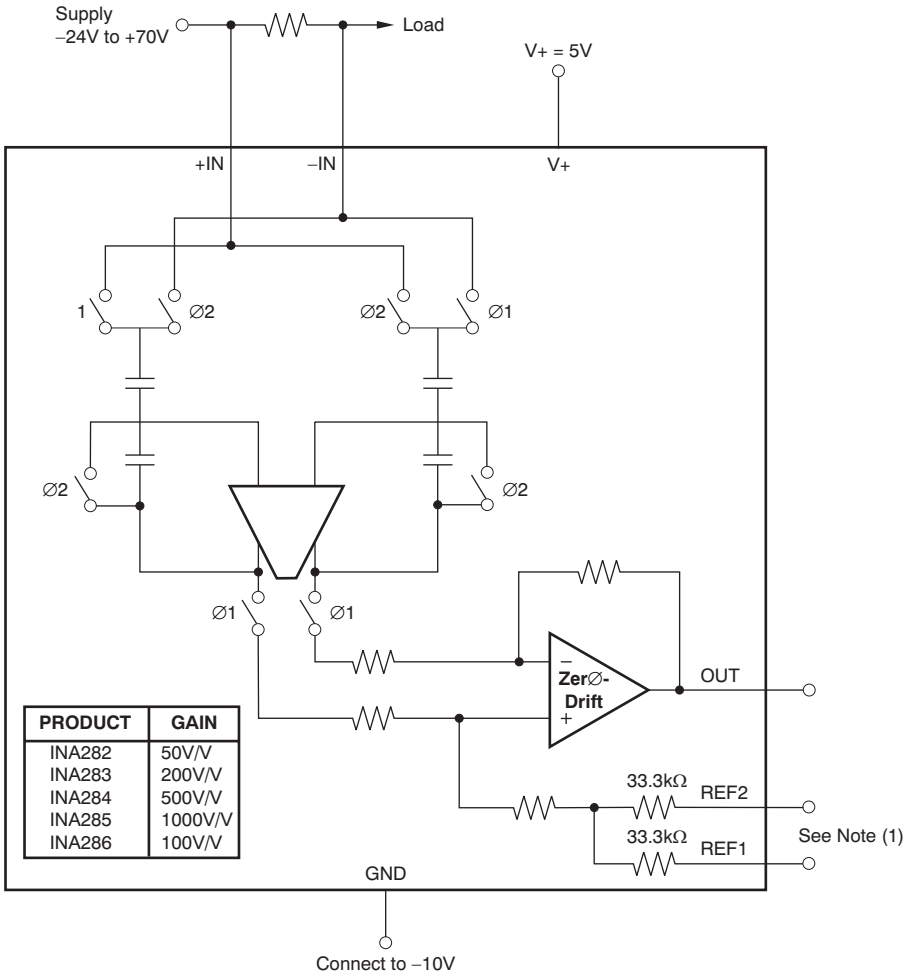


Figure 38. Split Reference Output

EXTENDED NEGATIVE COMMON-MODE RANGE

Using a negative power supply can extend the common-mode range 14V more negative than the supply used. For instance, a –10V supply allows up to –24V negative common-mode. Remember to keep the total voltage between the GND pin and V+ pin to less than 18V. The positive common-mode decreases by the same amount.

The reference input simplifies this type of operation because the output quiescent bias point is always based on the reference connections. Figure 39 shows a circuit configuration for common-mode ranges from –24V to +70V.



(1) Connect the REF pins as desired; however, they cannot exceed 9V above the GND pin voltage.

Figure 39. Circuit Configuration for Common-Mode Ranges from –24V to +70V

CALCULATING TOTAL ERROR

The electrical specifications for the INA282-286 family of devices include the typical individual errors terms such as gain error, offset error, and nonlinearity error. Total error including all of these individual error components is not specified in the Electrical Characteristics table. In order to accurately calculate the error that can be expected from the device, we must first know the operating conditions to which the device is subjected. Some current shunt monitors specify a total error in the product data sheet. However, this total error term is accurate under only one particular set of operating conditions. Specifying the total error at this one point has little practical value because any deviation from these specific operating conditions no longer yields the same total error value. This section discusses the individual error sources, with information on how to apply them in order to calculate the total error value for the device under any normal operating conditions.

The typical error sources that have the largest impact on the total error of the device are input offset voltage, common-mode voltage rejection, gain error and nonlinearity error. For the INA282-286, an additional error source referred to as *Reference Common-Mode Rejection* is also included in the total error value.

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The nonlinearity error of the INA282-286 is relatively low compared to the gain error specification, which results in a gain error that can be expected to be relatively constant throughout the linear input range of the device. While the gain error remains constant across the linear input range of the device, the error associated with the input offset voltage does not. As the differential input voltage developed across a shunt resistor at the input of the INA282-286 decreases, the inherent input offset voltage of the device becomes a larger percentage of the measured input signal resulting in an increase in error in the measurement. This varying error is present among all current shunt monitors, given the input offset voltage ratio to the voltage being sensed by the device. The relatively low input offset voltages present in the INA282-286 devices limit the amount of contribution the offset voltage has on the total error term.

The term *Reference Common-Mode Rejection* refers to the amount of error induced by applying a reference voltage to the INA282-286 device that deviates from the inherent bias voltage present at the output of the first stage of the device. The output of the switched-capacitor network and first-stage amplifier has an inherent bias voltage of approximately 2.048V. Applying a reference voltage of 2.048V to the INA282-286 reference pins results in no additional error term contribution. Applying a voltage to the reference pins that differs from 2.048V creates a voltage potential in the internal difference amplifier, resulting in additional current flowing through the resistor network. As a result of resistor tolerances, this additional current flow causes additional error at the output because of resistor mismatches. Additionally, as a result of resistor tolerances, this additional current flow causes additional error at the output based on the common-mode rejection ratio of the output stage amplifier. This error term is referred back to the input of the device as additional input offset voltage. Increasing the difference between the 2.048V internal bias and the external reference voltage results in a higher input offset voltage. Also, as the error at the output is referred back to the input, there is a larger impact on the input-referred offset, V_{OS}, for the lower-gain versions of the device.

Two examples are provided that detail how different operating conditions can affect the total error calculations. Typical and maximum calculations are shown as well to provide the user more information on how much error variance could be present from device to device.

Example 1

INA282; V_S = 5V; V_{CM} = 12V; V_{REF} = 2.048V; V_{SENSE} = 10mV

Table 1. Example 1

TERM	SYMBOL	EQUATION	TYPICAL VALUE	MAXIMUM VALUE
Initial Input Offset Voltage	V_{OS}	—	20µV	70µV
Added Input Offset Voltage Because of Common-Mode Voltage	V_{OS_CM}	$\frac{1}{10^{\left(\frac{CMRR_dB}{20}\right)}} \times (V_{CM} - 12V)$	0µV	0µV
Added Input Offset Voltage Because of Reference Voltage	V_{OS_REF}	$R_{CMR} \times (2.048V - V_{REF})$	0µV	0µV
Total Input Offset Voltage	V_{OS_Total}	$\sqrt{(V_{OS})^2 + (V_{OS_CM})^2 + (V_{OS_REF})^2}$	20µV	70µV
Error from Input Offset Voltage	Error_V_{OS}	$\frac{V_{OS_Total}}{V_{SENSE}} \times 100$	0.20%	0.70%
Gain Error	Error_Gain	—	0.40%	1.40%
Nonlinearity Error	Error_Lin	—	0.01%	0.01%
Total Error	—	$\sqrt{(Error_V_{OS})^2 + (Error_Gain)^2 + (Error_Lin)^2}$	0.45%	1.56%

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Example 2

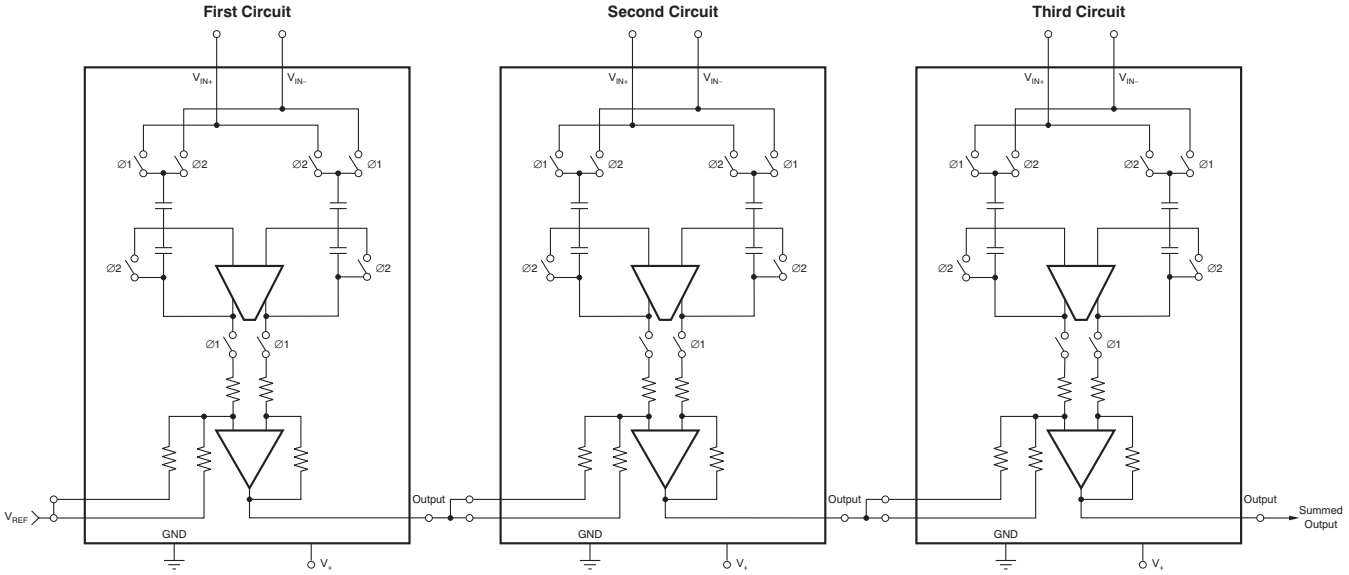
INA286; V_S = 5V; V_{CM} = 24V; V_{REF} = 0V; V_{SENSE} = 10mV

Table 2. Example 2

TERM	SYMBOL	EQUATION	TYPICAL VALUE	MAXIMUM VALUE
Initial Input Offset Voltage	V_{OS}	—	20µV	70µV
Added Input Offset Voltage Because of Common-Mode Voltage	V_{OS_CM}	$\frac{1}{10^{\left(\frac{CMRR_dB}{20}\right)}} \times (V_{CM} - 12V)$	1.2µV	12µV
Added Input Offset Voltage Because of Reference Voltage	V_{OS_REF}	$R_{CMR} \times (2.048V - V_{REF})$	34.8µV	92.2µV
Total Input Offset Voltage	V_{OS_Total}	$\sqrt{(V_{OS})^2 + (V_{OS_CM})^2 + (V_{OS_REF})^2}$	40.2µV	116.4µV
Error from Input Offset Voltage	Error_V_{OS}	$\frac{V_{OS_Total}}{V_{SENSE}} \times 100$	0.40%	1.16%
Gain Error	Error_Gain	—	0.40%	1.40%
Nonlinearity Error	Error_Lin	—	0.01%	0.01%
Total Error	—	$\sqrt{(Error_V_{OS})^2 + (Error_Gain)^2 + (Error_Lin)^2}$	0.57%	1.82%

SUMMING CURRENTS AND PARALLELING

The outputs of multiple INA282 family devices are easily summed by connecting the output of one INA282 family device to the reference input of a second INA282 family device. Summing beyond two devices is possible by repeating this connection, and is shown for three devices in Figure 40. The reference input of the first INA282 family device sets the output quiescent level for all the devices in the string.



NOTE: The voltage applied to the reference inputs cannot exceed 9V.

Figure 40. Summing the Outputs of Multiple INA282 Family Devices

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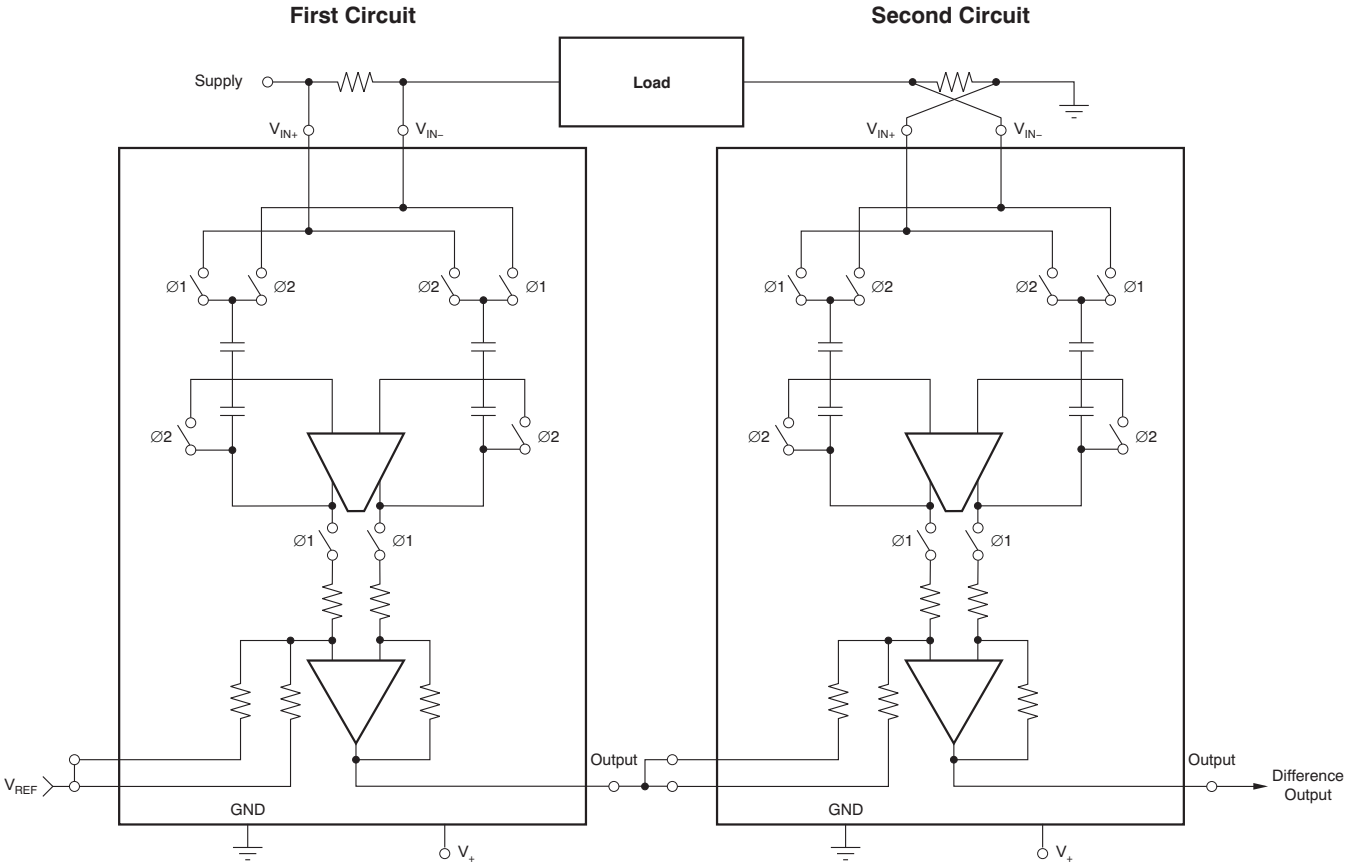
CURRENT DIFFERENCING

Occasionally, the need arises to confirm that the current into a load is identical to the current out of a load, usually as part of diagnostic testing or fault detection. This situation requires precision current differencing, which is the same as summing except that the two amplifiers have the inputs connected opposite of each other. Under normal operating conditions, the final output is very close to the reference value and proportional to any current difference. Figure 41 is an example of the connections required for current differencing.

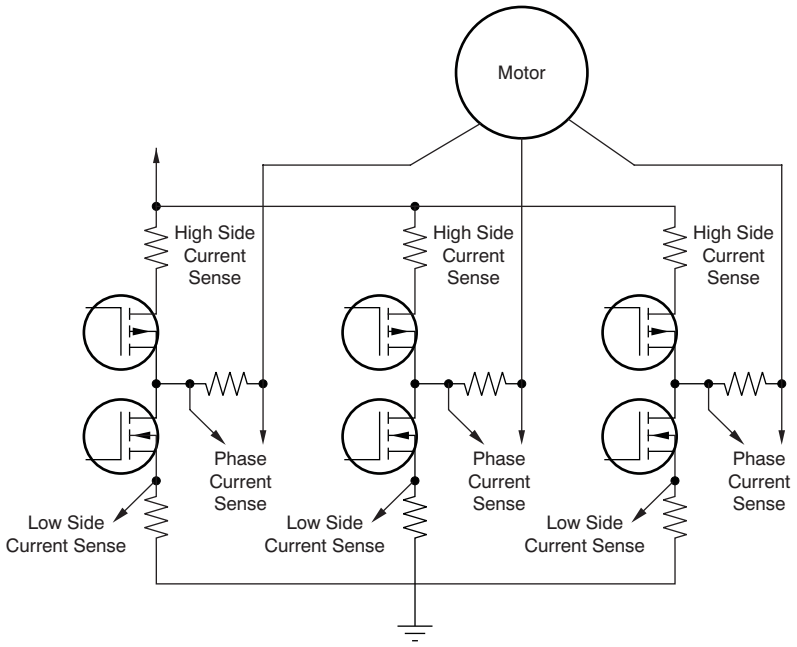


NOTE: This example is identical to the current summing example, except that the two shunt inputs are reversed in polarity, this current differencing circuit is useful in detecting when current into and out of a load do not match.

Figure 41. Current Differencing Using an INA282 Family Device

COMMON-MODE DYNAMICS AND CURRENT DIFFERENCING

Current sensing is frequently used on totem-pole output stages, such as those of bridge-type motor drives. We can sense current in one of three locations on a totem-pole output: on the ground side (low-side sensing); on the power-supply side (high-side sensing); or on the output (phase sensing). Only the output line reports the exact load current. Obviously, the ground and supply-side sensing report only the current in the individual respective phases. Figure 42 depicts these various methods on a three-phase motor driver.



NOTE: Motor drive current sensing can be done on the low side, phase side, or high side. Only the phase output gives complete information regarding current in the motor, but is subject to common-mode transients that even the best amplifiers do not reject completely.

Figure 42. Motor Drive Current Sensing

However, sensing on the output is subject to large common-mode voltage steps that result in feedthrough in even the best amplifiers. The ground and supply-side sensing configurations are free of this problem, thanks to the static common-mode environments. Sensing either ground or supply alone only provides partial information regarding motor current, but sense them individually and sum them and we have the same information provided by phase sensing, with an added advantage of not being subject to transient common-mode artifacts. See Figure 43 for an illustration of two INA282 family devices connected in this manner. Technically, this configuration is current differencing, though, because we want the upper sense to report a positive-going excursion in the overall output, and the negative sense to report a negative-going excursion.

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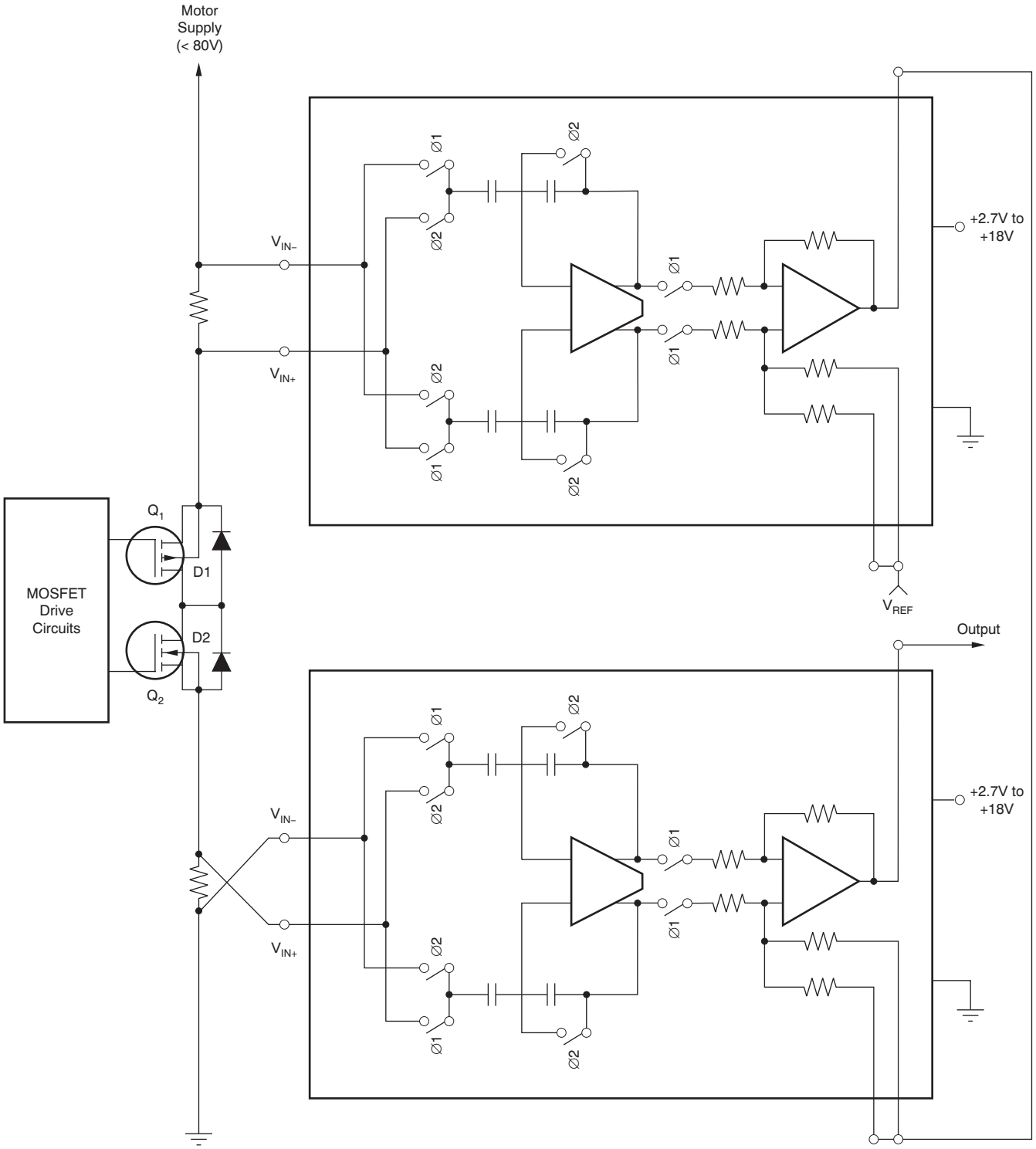

NOTE: By sensing totem-pole current on both the positive and negative rail and summing, dynamic common-mode issues can be avoided entirely. Note that IC_2 is connected with inverting inputs because it should report current with an opposite polarity to that of IC_1.

Figure 43. Sensing and Summing Totem Pole Current

Changes from Revision A (July 2010) to Revision B **Page**

- Changed devices from product preview to production data. 1

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
INA282AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	I282A	Samples
INA282AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	I282A	Samples
INA283AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	I283A	Samples
INA283AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	I283A	Samples
INA284AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	I284A	Samples
INA284AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I284A	Samples
INA285AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	I285A	Samples
INA285AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	I285A	Samples
INA286AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	I286A	Samples
INA286AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	I286A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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OTHER QUALIFIED VERSIONS OF INA282 :

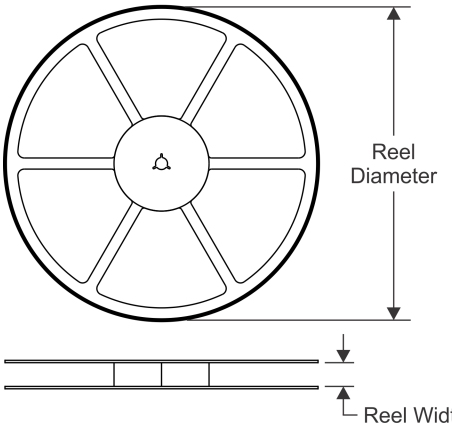
- Automotive: INA282-Q1

NOTE: Qualified Version Definitions:

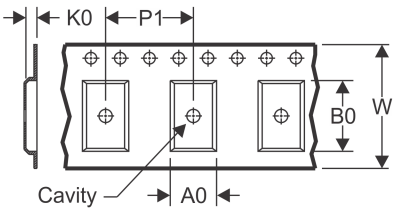
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

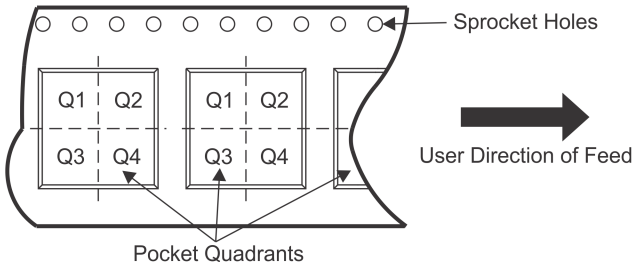


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

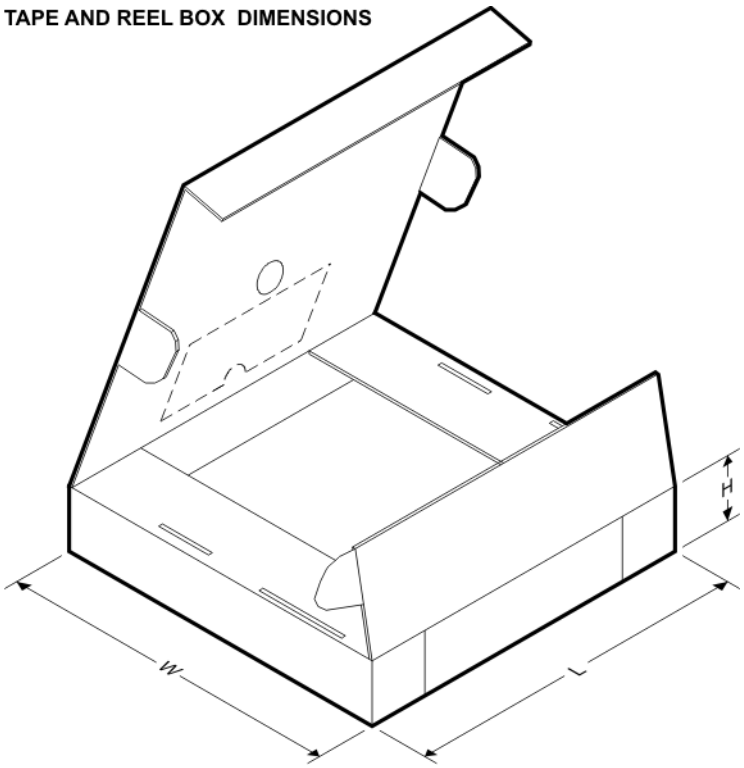
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA282AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA283AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA285AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

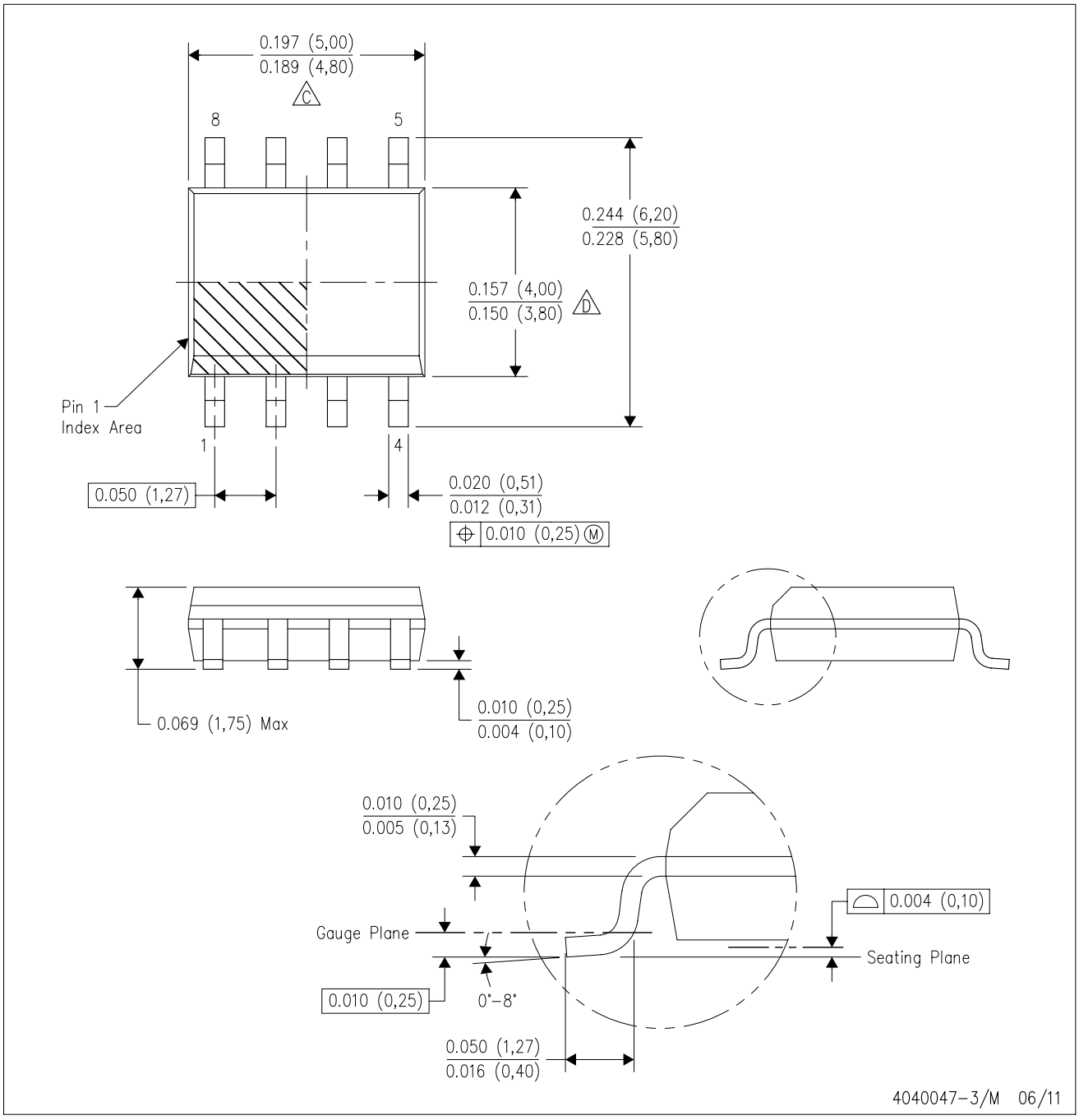
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

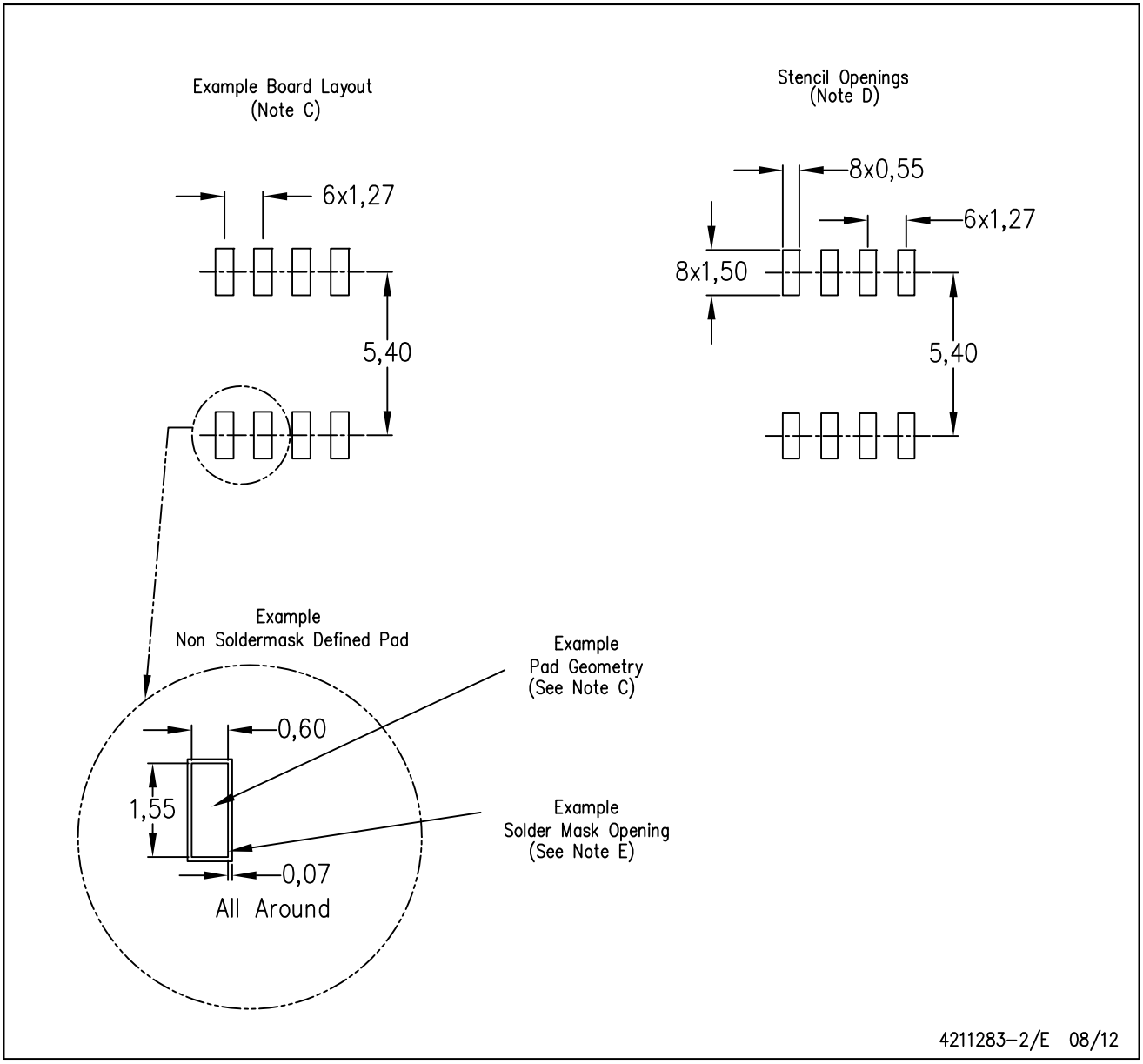
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA282AIDR	SOIC	D	8	2500	367.0	367.0	35.0
INA283AIDR	SOIC	D	8	2500	367.0	367.0	35.0
INA285AIDR	SOIC	D	8	2500	367.0	367.0	35.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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