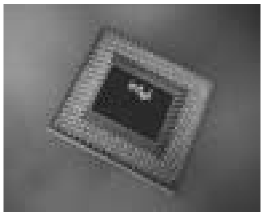
Intel® Celeron™ Processor up to 1.10 GHz

Datasheet

- Available at 1.10 GHz, 1 GHz, 950 MHz, 900 MHz, 850 MHz, 800 MHz, 766 MHz, 733 MHz, 700 MHz, 667 MHz, 633 MHz, 600 MHz, 566 MHz, 533 MHz, 533A MHz, 500 MHz, 466 MHz, 433 MHz, 400 MHz, 366 MHz, 333 MHz, and 300A MHz core frequencies with 128 KB level-two cache (on die); 300 MHz and 266 MHz core frequencies without level-two cache.
- Intel's latest Celeron™ processors in the FC-PGA package are manufactured using the advanced 0.18 micron technology.
- Binary compatible with applications running on previous members of the Intel microprocessor line.
- Dynamic execution microarchitecture.
- Operates on a 100/66 MHz, transaction-oriented system bus.
- Specifically designed for uni-processor based Value PC systems, with the capabilities of MMX™ technology.
- Power Management capabilities.
- Optimized for 32-bit applications running on advanced 32-bit operating systems.
- Uses cost-effective packaging technology.
  - —Single Edge Processor (S.E.P.) Package to maintain compatibility with SC242 (processor core frequencies (MHz): 266, 300, 300A, 333, 366, 400, 433).
  - —Plastic Pin Grid Array (PPGA) Package (processor core frequencies (MHz): 300A, 333, 366, 400, 433, 466, 500, 533).
  - —Flip-Chip Pin Grid Array (FC-PGA) Package (processor core frequencies (MHz); 533A, 566, 600, 633, 667, 700, 733, 766, 800, 850, 900, 950); (GHz); 1, 1.10
- Integrated high-performance 32 KB instruction and data, nonblocking, level-one cache: separate 16 KB instruction and 16 KB data caches.
- Integrated thermal diode.

The Intel® Celeron™ processor is designed for uni-processor based Value PC desktops and is binary compatible with previous generation Intel architecture processors. The Celeron processor provides good performance for applications running on advanced operating systems such as Microsoft* Windows* 95, Windows*98, Windows NT*, and UNIX*. This is achieved by integrating the best attributes of Intel processors—the dynamic execution performance of the P6 microarchitecture plus the capabilities of MMX™ technology—bringing a balanced level of performance to the Value PC market segment. The Celeron processor offers the dependability you would expect from Intel at an exceptional value. Systems based on Celeron processors also include the latest features to simplify system management and lower the cost of ownership for small business and home environments.



PPGA Package

FC-PGA Package

S.E.P. Package

Document Number: 243658-019
August 2001

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1.0 Introduction

The Intel® Celeron™ processor is based on the P6 microarchitecture and is optimized for the Value PC market segment. The Intel Celeron processor, like the Pentium® II processor, features a Dynamic Execution microarchitecture and executes MMX™ technology instructions for enhanced media and communication performance. The Intel Celeron processor also utilizes multiple low-power states such as AutoHALT, Stop-Grant, Sleep, and Deep Sleep to conserve power during idle times.

The Intel Celeron processor is capable of running today's most common PC applications with up to 4 GB of cacheable memory space. As this processor is intended for Value PC systems, it does not provide multiprocessor support. The Pentium II and Pentium® III processors should be used for multiprocessor system designs.

To be cost-effective at both the processor and system level, the Intel Celeron processor utilizes cost-effective packaging technologies. They are the S.E.P. (Single-Edge Processor) package, the PPGA (Plastic Pin Grid Array) package, and the FC-PGA (Flip-Chip Pin Grid Array) package. Refer to the *Intel® Celeron™ Processor Specification Update* for the latest packaging and frequency support information (Order Number 243337).

Note: This datasheet describes the Intel Celeron processor for the PPGA package, FC-PGA package, and the S.E.P. Package versions. Unless otherwise specified, the information in this document applies to all versions and information on PGA packages, refer to both PPGA and FC-PGA packages.

1.1 Terminology

In this document, a '#' symbol after a signal name refers to an active low signal. This means that a signal is in the active state (based on the name of the signal) when driven to a low level. For example, when FLUSH# is low, a flush has been requested. When NMI is high, a nonmaskable interrupt has occurred. In the case of signals where the name does not imply an active state but describes part of a binary sequence (such as *address* or *data*), the '#' symbol implies that the signal is inverted. For example, D[3:0] = 'HLHL' refers to a hex 'A', and D[3:0]# = 'LHLH' also refers to a hex 'A' (H= High logic level, L= Low logic level).

The term "system bus" refers to the interface between the processor, system core logic (a.k.a. the AGPset components), and other bus agents. The system bus is an interface to the processor, memory, and I/O.

1.1.1 Package Terminology

The following terms are used often in this document and are explained here for clarification:

- **Processor substrate**—The structure on which passive components (resistors and capacitors) are mounted.
- **Processor core**—The processor's execution engine.
- **S.E.P. Package**—Single-Edge Processor Package, which consists of a processor substrate, processor core, and passive components. This package differs from the S.E.C. Cartridge as this processor has no external plastic cover, thermal plate, or latch arms.
- **PPGA package—**Plastic Pin Grid Array package. The package is a pinned laminated printed circuit board structure.
- **FC-PGA** - Flip-Chip Pin Grid Array. The FC-PGA uses the same 370-pin zero insertion force socket (PGA370) as the PPGA. Thermal solutions are attached directly to the back of the processor core package without the use of a thermal plate or heat spreader.
- **Keepout zone** - The area on or near a FC-PGA packaged processor that system designs can not utilize.
- **Keep-in zone** - The area of a FC-PGA packaged processor that thermal solutions may utilize.

Additional terms referred to in this and other related documentation:

- **SC242**—242-contact slot connector. A processor in the S.E.P. Package uses this connector to interface with a system board.
- **370-pin socket (PGA370)—**The zero insertion force (ZIF) socket in which a processor in the PPGA package will use to interface with a system board.
- **Retention mechanism**—A mechanical assembly which holds the package in the SC242 connector.

1.1.2 Processor Naming Convention

A letter(s) is added to certain processors (e.g., 533A MHz) when the core frequency alone may not uniquely identify the processor. Below is a summary of what each letter means as well as a table listing all the FC-PGA processors for the PGA370 socket.

Table 1. Processor Identification

Processor	Core Frequency	System Bus Frequency (MHz)	CPUID[1]
300 MHz	300 MHz	66	065xh
300A MHz	300 MHz	66	066xh
366 MHz	366 MHz	66	066xh
400 MHz	400 MHz	66	066xh
433 MHz	433 MHz	66	066xh
466 MHz	466 MHz	66	066xh
500 MHz	500 MHz	66	066xh
533 MHz	533 MHz	66	066xh
533A MHz	533 MHz	66	068xh
566 MHz	566 MHz	66	068xh
600 MHz	600 MHz	66	068xh
633 MHz	633 MHz	66	068xh
667 MHz	667 MHz	66	068xh
700 MHz	700 MHz	66	068xh
733 MHz	733 MHz	66	068xh
766 MHz	766 MHz	66	068xh
800 MHz	800 MHz	100	068xh
850 MHz	850 MHz	100	068xh
900 MHz	900 MHz	100	068xh
950 MHz	950 MHz	100	068xh
1 GHz	1 GHz	100	068xh
1.10 GHz	1.10 MHz	100	068xh

NOTES:
1. Refer to the *Intel® Celeron™ Processor Specification Update* for the exact CPUID for each processor.

1.2 References

The reader of this specification should also be familiar with material and concepts presented in the following documents:

- AP-485, *Intel® Processor Identification and the CPUID Instruction* (Order Number 241618)[1]
- AP-589, *Design for EMI* (Order Number 243334)[1]
- AP-900, *Identifying Support for Streaming SIMD Extensions in the Processor and Operating System*[1]
- AP-905, *Pentium® III Processor Thermal Design Guidelines*[1]
- AP-907, *Pentium® III Processor Power Distribution Guidelines*[1]
- *Intel® Pentium® III Processor for the PGA370 Socket at 500 MHz to 933 MHz* Datasheet (Order Number 245264)
- *Intel® Pentium® III Processor Thermal Metrology for CPUID 068h Family*[1]
- *Intel® Pentium® III Processor Software Application Development Application Notes*[1]
- *Intel®* Celeron™ Processor Specification Update (Order Number 243748)
- *370-Pin Socket (PGA370) Design Guidelines* (Order Number 244410)
- *Intel® Architecture Software Developer's Manual* (Order Number 243193)
  - *Volume I: Basic Architecture* (Order Number 243190)
  - *Volume II: Instruction Set Reference* (Order Number 243191)
  - *Volume III: System Programming Guide* (Order Number 243192)
- *Intel® 440EX AGPset Design Guide* (Order Number 290637)
- *Intel® Celeron™ Processor with the Intel® 440LX AGPset Design Guide* (Order Number 245088)
- *Intel® 440BX AGPset Design Guide* (Order Number 290634)
- *Intel® Celeron™ Processor with the Intel® 440ZX-66 AGPset Design Guide* (Order Number 245126)
- *Intel® Celeron™ Processor (PPGA) at 466 MHz Thermal Solutions Guidelines* (Order Number 245156)

Notes:

1. This reference material can be found on the Intel Developer’s Web site located at http://developer.intel.com.
2. For a complete listing of the Intel® Celeron™ processor reference material, refer to the Intel Developer’s Web site when this processor is formally launched. The Web site is located at http://developer.intel.com/design/celeron/.

2.0 Electrical Specifications

2.1 System Bus and VREF

Celeron processor signals use a variation of the low voltage Gunning Transceiver Logic (GTL) signaling technology. The Intel Celeron processor system bus specification is similar to the GTL specification, but has been enhanced to provide larger noise margins and reduced ringing. The improvements are accomplished by increasing the termination voltage level and controlling the edge rates. Because this specification is different from the standard GTL specification, it is referred to as Assisted Gunning Transceiver Logic (AGTL+) in this document.

The Celeron processor varies from the Pentium Pro processor in its output buffer implementation. The buffers that drive the system bus signals on the Celeron processor are actively driven to $V_{CC_{CORE}}$ for one clock cycle during the low-to-high transition. This improves rise times and reduces overshoot. These signals should still be considered open-drain and require termination to a supply that provides the logic-high signal level.

The AGTL+ inputs use differential receivers which require a reference signal (VREF). VREF is used by the receivers to determine if a signal is a logic-high or a logic-low, and is provided to the processor core by either the processor substrate (S.E.P. Package) or the motherboard (PGA370 socket). Local VREF copies should be generated on the motherboard for all other devices on the AGTL+ system bus.

Termination is used to pull the bus up to the high voltage level and to control reflections on the transmission line. The processor may contain termination resistors (S.E.P. Package and FC-PGA Package) that provide termination for one end of the Intel Celeron processor system bus. Otherwise, this termination must exist on the motherboard.

Solutions exist for single-ended termination as well, though this implementation changes system design and eliminate backwards compatibility for Celeron processors in the PPGA package. Single-ended termination designs must still provide an AGTL+ termination resistor on the motherboard for the RESET# signal.

The AGTL+ bus depends on incident wave switching. Therefore timing calculations for AGTL+ signals are based on motherboard **flight time** as opposed to capacitive deratings. Analog signal simulation of the Intel Celeron processor system bus, including trace lengths, is highly recommended when designing a system. See the *Pentium® II Processor AGTL+ Layout Guidelines* and the *Pentium® II Processor I/O Buffer Models, Quad Format* (Electronic Form) for details.

2.2 Clock Control and Low Power States

Celeron processors allow the use of AutoHALT, Stop-Grant, Sleep, and Deep Sleep states to reduce power consumption by stopping the clock to internal sections of the processor, depending on each particular state. See Figure 1 for a visual representation of the Intel Celeron processor low power states.

For the processor to fully realize the low current consumption of the Stop-Grant, Sleep, and Deep Sleep states, a Model Specific Register (MSR) bit must be set. For the MSR at 02Ah (hex), bit 26 must be set to a ‘1’ (this is the power on default setting) for the processor to stop all internal clocks during these modes. For more information, see the *Pentium® II Processor Developer's Manual* (Order Number 243502).

2.2.1 Normal State—State 1

This is the normal operating state for the processor.

2.2.2 AutoHALT Power Down State—State 2

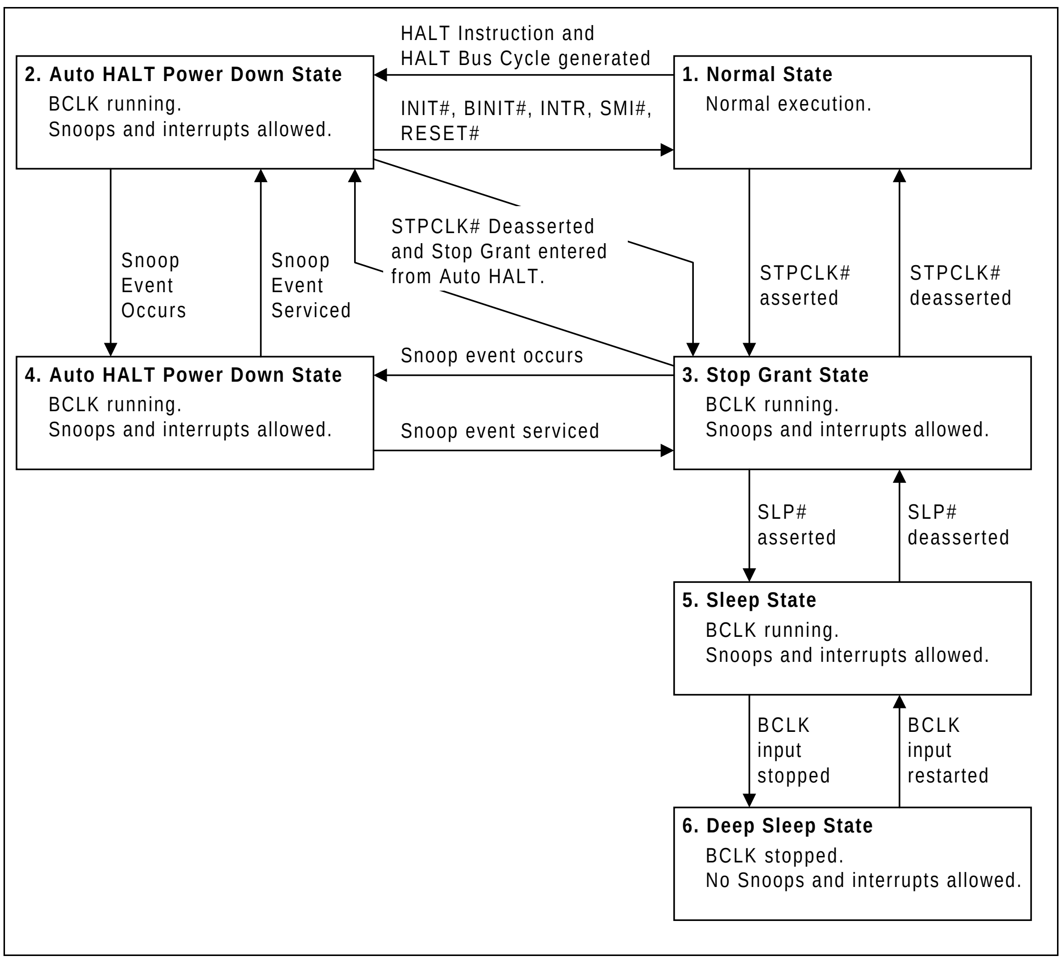
AutoHALT is a low power state entered when the processor executes the HALT instruction. The processor will transition to the Normal state upon the occurrence of SMI#, BINIT#, INIT#, or LINT[1:0] (NMI, INTR). RESET# will cause the processor to immediately initialize itself.

The return from a System Management Interrupt (SMI) handler can be to either Normal Mode or the AutoHALT Power Down state. See the *Intel Architecture Software Developer's Manual, Volume III: System Programmer's Guide* (Order Number 243192) for more information.

FLUSH# will be serviced during the AutoHALT state, and the processor will return to the AutoHALT state.

The system can generate a STPCLK# while the processor is in the AutoHALT Power Down state. When the system deasserts the STPCLK# interrupt, the processor will return execution to the HALT state.

Figure 1. Clock Control State Machine



2.2.3 Stop-Grant State—State 3

The Stop-Grant state on the processor is entered when the STPCLK# signal is asserted.

Since the AGTL+ signal pins receive power from the system bus, these pins should not be driven (allowing the level to return to V_{TT}) for minimum power drawn by the termination resistors in this state. In addition, all other input pins on the system bus should be driven to the inactive state.

BINIT# will not be serviced while the processor is in Stop-Grant state. The event will be latched and can be serviced by software upon exit from Stop-Grant state.

FLUSH# will not be serviced during Stop-Grant state.

RESET# will cause the processor to immediately initialize itself, but the processor will stay in Stop-Grant state. A transition back to the Normal state will occur with the deassertion of the STPCLK# signal.

A transition to the HALT/Grant Snoop state will occur when the processor detects a snoop on the system bus (see Section 2.2.4). A transition to the Sleep state (see Section 2.2.5) will occur with the assertion of the SLP# signal.

While in the Stop-Grant State, SMI#, INIT#, and LINT[1:0] will be latched by the processor, and only serviced when the processor returns to the Normal State. Only one occurrence of each event will be recognized upon return to the Normal state.

2.2.4 HALT/Grant Snoop State—State 4

The processor will respond to snoop transactions on the Celeron processor system bus while in Stop-Grant state or in AutoHALT Power Down state. During a snoop transaction, the processor enters the HALT/Grant Snoop state. The processor will stay in this state until the snoop on the Intel Celeron processor system bus has been serviced (whether by the processor or another agent on the Intel Celeron processor system bus). After the snoop is serviced, the processor will return to the Stop-Grant state or AutoHALT Power Down state, as appropriate.

2.2.5 Sleep State—State 5

The Sleep state is a very low power state in which the processor maintains its context, maintains the phase-locked loop (PLL), and has stopped all internal clocks. The Sleep state can only be entered from Stop-Grant state. Once in the Stop-Grant state, the SLP# pin can be asserted, causing the processor to enter the Sleep state. The SLP# pin is not recognized in the Normal or AutoHALT states.

Snoop events that occur while in Sleep State or during a transition into or out of Sleep state will cause unpredictable behavior.

In the Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions or assertions of signals (with the exception of SLP# or RESET#) are allowed on the system bus while the processor is in Sleep state. Any transition on an input signal before the processor has returned to Stop-Grant state will result in unpredictable behavior.

If RESET# is driven active while the processor is in the Sleep state, and held active as specified in the RESET# pin specification, then the processor will reset itself, ignoring the transition through Stop-Grant State. If RESET# is driven active while the processor is in the Sleep State, the SLP# and STPCLK# signals should be deasserted immediately after RESET# is asserted to ensure the processor correctly executes the Reset sequence.

While in the Sleep state, the processor is capable of entering its lowest power state, the Deep Sleep state, by stopping the BCLK input. (See Section 2.2.6.) Once in the Sleep state, the SLP# pin can be deasserted if another asynchronous system bus event occurs. The SLP# pin has a minimum assertion of one BCLK period.

2.2.6 Deep Sleep State—State 6

The Deep Sleep state is the lowest power state the processor can enter while maintaining context. The Deep Sleep state is entered by stopping the BCLK input (after the Sleep state was entered from the assertion of the SLP# pin). The processor is in Deep Sleep state immediately after BLCK is stopped. It is recommended that the BLCK input be held low during the Deep Sleep State. Stopping of the BCLK input lowers the overall current consumption to leakage levels.

To re-enter the Sleep state, the BCLK input must be restarted. A period of 1 ms (to allow for PLL stabilization) must occur before the processor can be considered to be in the Sleep State. Once in the Sleep state, the SLP# pin can be deasserted to re-enter the Stop-Grant state.

While in Deep Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions or assertions of signals are allowed on the system bus while the processor is in Deep Sleep state. Any transition on an input signal before the processor has returned to Stop-Grant state will result in unpredictable behavior.

2.2.7 Clock Control

BCLK provides the clock signal for the processor and on die L2 cache. During AutoHALT Power Down and Stop-Grant states, the processor processes a system bus snoop. The processor does not stop the clock to the L2 cache during AutoHALT Power Down or Stop-Grant states. Entrance into the Halt/Grant Snoop state allows the L2 cache to be snooped, similar to the Normal state.

When the processor is in the Sleep or Deep Sleep states, it does not respond to interrupts or snoop transactions. During the Sleep state, the internal clock to the L2 cache is not stopped. During the Deep Sleep state, the internal clock to the L2 cache is stopped. The internal clock to the L2 cache will be restarted only after the internal clocking mechanism for the processor is stable (i.e., the processor has re-entered Sleep state).

PICCLK should not be removed during the AutoHALT Power Down or Stop-Grant states. PICCLK can be removed during the Sleep or Deep Sleep states. When transitioning from the Deep Sleep state to the Sleep state, PICCLK must be restarted with BCLK.

2.3 Power and Ground Pins

There are five pins defined on the S.E.P. Package for voltage identification (VID) and four pins on the PPGA and FC-PGA packages. These pins specify the voltage required by the processor core. These have been added to cleanly support voltage specification variations on current and future Celeron processors.

For clean on-chip power distribution, Intel Celeron processors in the S.E.P. Package have 27 VCC (power) and 30 VSS (ground) inputs. The 27 VCC pins are further divided to provide the different voltage levels to the components. VCC_{CORE} inputs for the processor core account for 19 of the VCC pins, while 4 VTT inputs (1.5 V) are used to provide a AGTL+ termination voltage to the processor. For only the S.E.P. Package, one VCC_5 pin is provided for Voltage Transient Tools. VCC_5 and VCC_{CORE} must remain electrically separated from each other.

The PPGA package has more power (88) and ground (80) pins than the S.E.P. Package. Of the power pins, 77 are used for the processor core ($V_{CC_{CORE}}$) and 8 are used as a AGTL+ reference voltage (VREF). The other 3 power pins are $V_{CC_{1.5}}$, $V_{CC_{2.5}}$ and $V_{CC_{CMOS}}$ and are used for future processor compatibility.

FC-PGA package has 77 $V_{CC_{CORE}}$, 77 ground pins, eight VREF, one $V_{CC_{1.5}}$, one $V_{CC_{2.5}}$, and one $V_{CC_{CMOS}}$. $V_{CC_{CORE}}$ inputs supply the processor core, including the on-die L2 cache. The VREF inputs are used as the AGTL+ reference voltage for the processor.

The $V_{CC_{CMOS}}$ pin is provided as a feature for future processor support in a flexible design. In such a design, the $V_{CC_{CMOS}}$ pin is used to provide the CMOS voltage for use by the platform. Additionally, 2.5 V must be provided to the $V_{CC_{2.5}}$ input and 1.5 V must be provided to the $Vcc_{1.5}$ input. The processor routes the CMOS voltage level through the package that it is compatible with. For example, processors requiring 1.5 V CMOS voltage levels route 1.5 V to the $V_{CC_{CMOS}}$ output.

Each power signal, regardless of package, must meet the specifications stated in Table 4. In addition, all $V_{CC_{CORE}}$ pins must be connected to a voltage island while all VSS pins have to connect to a system ground plane. In addition, the motherboard must implement the VTT pins as a voltage island or large trace. Similarly, all VSS pins must be connected to a system ground plane.

2.3.1 Phase Lock Loop (PLL) Power

It is highly critical that phase lock loop power delivery to the processor meets Intel's requirements. A low pass filter is required for power delivery to pins PLL1 and PLL2. This serves as an isolated, decoupled power source for the internal PLL.

2.4 Processor Decoupling

Due to the large number of transistors and high internal clock speeds, the processor is capable of generating large average current swings between low and full power states. This causes voltages on power planes to sag below their nominal values if bulk decoupling is not adequate. Care must be taken in the board design to ensure that the voltage provided to the processor remains within the specifications listed in Table 5. Failure to do so can result in timing violations or a reduced lifetime of the component.

2.4.1 System Bus AGTL+ Decoupling

The S.E.P. Package and FC-PGA package contain high frequency decoupling capacitance on the processor substrate, where the PPGA package does not. Therefore, Celeron processors in the PGA packages require high frequency decoupling on the system motherboard. Bulk decoupling must be provided on the motherboard for proper AGTL+ bus operation for all packages. See AP-585, *Pentium® II Processor AGTL+ Guidelines* (Order Number 243330), AP-587, *Pentium® II Processor Power Distribution Guidelines* (Order Number 243332), and the *Pentium® II Processor Developer's Manual* (Order Number 243502) for more information.

2.5 Voltage Identification

The processor's voltage identification (VID) pins can be used to automatically select the $V_{CC_{CORE}}$ voltage from a compatible voltage regulator. There are five VID pins (VID[4:0]) on the S.E.P. Package, while there are only four (VID[3:0]) on the PGA packages. This is because there are no Celeron processors in the PGA package that require more than 2.05 V (see Table 2).

VID pins are not signals, but rather are an open or short circuit to V_{SS} on the processor. The combination of opens and shorts defines the processor core's required voltage. The VID pins also allow for compatibility with current and future Intel Celeron processors.

Note that the '11111' (all opens) ID can be used to detect the absence of a processor core in a given slot (S.E.P. Package only), as long as the power supply used does not affect the VID signals. Detection logic and pull-ups should not affect VID inputs at the power source (see Section 7.0).

External logic monitoring the VID signals or the voltage regulator may require the VID pins to be pulled-up. If this is the case, the VID pins should be pulled up to a TTL-compatible level with external resistors to the power source of the regulator.

The power source chosen must be guaranteed to be stable whenever the voltage regulator's supply is stable. This will prevent the possibility of the processor supply going above the specified $V_{CC_{CORE}}$ in the event of a failure in the supply for the VID lines. In the case of a DC-to-DC converter, this can be accomplished by using the input voltage to the converter for the VID line pull-ups. In addition, the power supply must supply the requested voltage or disable itself.

Table 2. Voltage Identification Definition

VID4 (S.E.P.P. only)	VID3	VID2	VID1	VID0	$V_{CC_{CORE}}$
0	1	1	1	1	1.30
0	1	1	1	0	1.35
0	1	1	0	1	1.40
0	1	1	0	0	1.45
0	1	0	1	1	1.50
0	1	0	1	0	1.55
0	1	0	0	1	1.60
0	1	0	0	0	1.65
0	0	1	1	1	1.70
0	0	1	1	0	1.75
0	0	1	0	1	1.80
0	0	1	0	0	1.85
0	0	0	1	1	1.90
0	0	0	1	0	1.95
0	0	0	0	1	2.00
0	0	0	0	0	2.05
1	1	1	1	1	No Core[4]
1	1	1	1	0	2.1[4]

NOTES:
1. 0 = Processor pin connected to V_{SS}.
2. 1 = Open on processor; may be pulled up to TTL V_{IH} on motherboard.
3. The Celeron processor core uses a 2.0 V power source.
4. VID4 applies only to the S.E.P. Package. VID[3:0] applies to both S.E.P. and PGA packages.

2.6 System Bus Unused Pins

All RESERVED pins must remain unconnected. Connection of these pins to $V_{CC_{CORE}}$, V_{SS}, or to any other signal (including each other) can result in component malfunction or incompatibility with future Celeron processor products. See Section 5.0 for a pin listing of the processor and the location of each RESERVED pin.

For Intel Celeron processors in the S.E.P. Package, the TESTHI pin must be at a logic-high level when the core power supply comes up. For more information, please refer to erratum C26 of the *Intel® Celeron™ Processor Specification Update* (Order Number 243748). Also note that the TESTHI signal is not available on Intel Celeron processors in the PGA package.

PICCLK must be driven with a valid clock input and the PICD[1:0] lines must be pulled-up to 2.5 V even when the APIC will not be used. A separate pull-up resistor must be provided for each PICD line.

For reliable operation, always connect unused inputs or bi-directional signals to their deasserted signal level. The pull-up or pull-down resistor value is system dependent and should be chosen such that the logic-high (V_{IH}) and logic-low (V_{IL}) requirements are met.

For the S.E.P. Package, unused AGTL+ inputs should not be connected as the package substrate has termination resistors. On the other hand, the PGA packages do not have AGTL+ termination in their package and must have any unused AGTL+ inputs terminated through a pull-up resistor. For designs that intend to only support the FC-PGA processor, unused AGTL+ inputs will be terminated by the processor’s on-die termination resistors and, thus, do not need to be terminated on the motherboard. However, the reset pin should always be terminated on the motherboard.

For unused CMOS inputs, active-low signals should be connected through a pull-up resistor to meet V_{IH} requirements and active-high signals should be connected through a pull-down resistor to meet V_{IL} requirements. Unused CMOS outputs can be left unconnected. A resistor must be used when tying bi-directional signals to power or ground. For any signal pulled to either power or ground, a resistor will allow for system testability.

2.7 Processor System Bus Signal Groups

To simplify the following discussion, the Celeron processor system bus signals have been combined into groups by buffer type. **All Celeron processor system bus outputs are open drain** and require a high-level source provided externally by the termination or pull-up resistor.

AGTL+ input signals have differential input buffers, which use V_{REF} as a reference signal. AGTL+ output signals require termination to 1.5 V. In this document, the term "AGTL+ Input" refers to the AGTL+ input group as well as the AGTL+ I/O group when receiving. Similarly, "AGTL+ Output" refers to the AGTL+ output group as well as the AGTL+ I/O group when driving.

EMI pins (S.E.P. Package only) should be connected to motherboard ground and/or to chassis ground through zero ohm (0 Ω) resistors. The zero ohm resistors should be placed in close proximity to the SC242 connector. The path to chassis ground should be short in length and have a low impedance.

The PWRGOOD, BCLK, and PICCLK inputs can each be driven from ground to 2.5 V. Other CMOS inputs (A20M#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PREQ#, SMI, SLP#, and STPCLK#) must be pulled up to $V_{CC_{CMOS}}$. In addition, the CMOS, APIC, and TAP outputs are open drain and should be pulled high to $V_{CC_{CMOS}}$. This ensures not only correct operation for current Intel Celeron processors, but compatibility for future Intel Celeron processor products as well.

The groups and the signals contained within each group are shown in Table 3. Refer to Section 7.0 for descriptions of these signals.

Table 3. Intel® Celeron™ Processor System Bus Signal Groups

Group Name	Signals
AGTL+ Input	BPRI#, DEFER#, RESET#[11], RS[2:0]#, TRDY#
AGTL+ Output	PRDY#
AGTL+ I/O	A[31:3]#, ADS#, BNR#, BP[3:2]#, BPM[1:0]#, BR0#[8], D[63:0]#, DBSY#, DRDY#, HIT#, HITM#, LOCK#, REQ[4:0]#,
CMOS Input[4]	A20M#, FLUSH#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PREQ#, SMI#, SLP#[2], STPCLK#
CMOS Input	PWRGOOD[1,9]
CMOS Output[4]	FERR#, IERR#, THERMTRIP#[3]
System Bus Clock	BCLK[9]
APIC Clock	PICCLK[9]
APIC I/O[4]	PICD[1:0]
TAP Input[4]	TCK, TDI, TMS, TRST#
TAP Output[4]	TDO
Power/Other[5]	CPUPRES#[7], EDGCTRL[7], EMI[6], PLL[2:1][7], SLOTOCC#[6], THERMDP, THERMDN, $V_{CC1.5}$[7], $V_{CC2.5}$[7], V_{CCL2}[5], V_{CC5}[6], V_{CCCMOS}[7], V_{CCCORE}, $V_{COREDET}$[7], VID[3:0][7], VID[4:0][6], V_{REF}[7:0][7], V_{SS}, V_{TT}[14], RTTCTRL[12], BSEL[1:0][10], SLEWCTRL[13]

NOTES:

1. See Section 7.0 for information on the PWRGOOD signal.
2. See Section 7.0 for information on the SLP# signal.
3. See Section 7.0 for information on the THERMTRIP# signal.
4. These signals are specified for 2.5 V operation for S.E.P.P. and PPGA packages; they are specified at 1.5V operation for the FC-PGA package
5. V_{CCCORE} is the power supply for the processor core.
   VID[4:0] and VID[3:0] are described in Section 2.0.
   V_{TT} is used to terminate the system bus and generate V_{REF} on the processor substrate.
   V_{SS} is system ground.
   V_{CC5} is not connected to the Celeron processor. This supply is used for Voltage Transient Tools.
   SLOTOCC# is described in Section 7.0.
   BSEL is described in Section 2.7.2 and Section 7.0.
   EMI pins are described in Section 7.0.
   V_{CCL2} is a Pentium® II processor reserved signal provided to maintain compatibility with the Pentium® II processor and may be left as a no-connect for "Intel Celeron processor-only" designs.
6. Only applies to Intel Celeron processors in the S.E.P. Package.
7. Only applies to Intel Celeron processors in the PPGA and FC-PGA packages.
8. The BR0# pin is the only BREQ# signal that is bidirectional. See Section 7.0 for more information.
9. These signals are specified for 2.5 V operation.
10. BSEL1 is not used in Celeron processors.
11. RESET# must always be terminated to V_{TT} on the motherboard for PGA packages. On-die termination is not provided for this signal on FC-PGA.
12. For the FC-PGA, this signal is used to control the value of the processor on-die termination resistance. Refer to the specific platform design guide for the recommended pull-down resistor value.
13. Only applies to Intel Celeron processors in the FC-PGA Package.
14. S.E.P. Package and FC-PGA Package.

2.7.1 Asynchronous Vs. Synchronous for System Bus Signals

All AGTL+ signals are synchronous to BCLK. All of the CMOS, APIC, and TAP signals can be applied asynchronously to BCLK. All APIC signals are synchronous to PICCLK. All TAP signals are synchronous to TCK.

2.7.2 System Bus Frequency Select Signal (BSEL[1:0])

The BSEL pins have two functions. First, they can act as outputs and can be used by an external clock generator to select the proper system bus frequency. Second, they can act as an inputs and can be used by a system BIOS to detect and report the processor core frequency. See the *Intel® Celeron™ Processor with the Intel® 440ZX-66 AGPset Design Guide* (Order Number 245126) for an example implementation of BSEL.

BSEL0 is 3.3 V tolerant for the S.E.P. Package, while it is 2.5 V tolerant on the PPGA package. A logic-low on BSEL0 is defined as 66 MHz. On the FC-PGA a logic low on both BSEL0 and BSEL1 are defined as 66 MHz and are 3.3V tolerant.

2.8 Test Access Port (TAP) Connection

Due to the voltage levels supported by other components in the Test Access Port (TAP) logic, it is recommended that the Celeron processor be first in the TAP chain and followed by any other components within the system. A translation buffer should be used to connect to the rest of the chain unless one of the other components is capable of accepting a Vcc_{CMOS} (1.5V or 2.5 V) input. Similar considerations must be made for TCK, TMS, and TRST#. Two copies of each signal may be required with each driving a different voltage level.

A Debug Port may be placed at the start and end of the TAP chain with the TDI of the first component coming from the Debug Port and the TDO from the last component going to the Debug Port.

2.9 Maximum Ratings

Table 4 contains the Celeron processor stress ratings only. Functional operation at the absolute maximum and minimum is not implied nor guaranteed. The processor should not receive a clock while subjected to these conditions. Functional operating conditions are given in the AC and DC tables. Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the processor contains protective circuitry to resist damage from static electric discharge, one should always take precautions to avoid high static voltages or electric fields.

Table 4. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
$T_{STORAGE}$	Processor storage temperature	–40	85	°C	
VCC(All)	Any processor supply voltage with respect to VSS • PPGA and S.E.P.P. • FC-PGA	 –0.5 –0.5	 Operating voltage + 1.0 2.1	 V V	 1, 2
VinAGTL+	AGTL+ buffer DC input voltage with respect to VSS • PPGA and S.E.P.P. • FC-PGA	 –0.3 VTT - 2.18	 $V_{CC_{CORE}}$ + 0.7 2.18	 V V	 7, 8
VinCMOS	CMOS buffer DC input voltage with respect to VSS • PPGA and S.E.P.P. • FC-PGA	 -0.3 VTT - 2.18 -0.58	 3.3 2.18 3.18	 V V V	 3 7, 8, 9 10
IVID	Max VID pin current		5	mA	
ISLOTOCC#	Max SLOTOCC# pin current		5	mA	5
ICPUPRES#	Max CPUPRES# pin current		5	mA	6
Mech Max Edge Fingers[5]	Mechanical integrity of processor edge fingers		50	Insertions/ Extractions	4, 5

NOTES:
1. Operating voltage is the voltage to which the component is designed to operate. See Table 5.
2. This rating applies to the $V_{CC_{CORE}}$, V_{CC_5}, and any input (except as noted below) to the processor.
3. Parameter applies to CMOS, APIC, and TAP bus signal groups only.
4. The electrical and mechanical integrity of the processor edge fingers are specified to last for 50 insertion/ extraction cycles.
5. S.E.P. Package Only
6. PGA Packages Only
7. Input voltage can never exceed VSS + 2.8 volts.
8. Input voltage can never go below VTT - 2.18 volts.
9. Parameter applies to CMOS (except BCLK, PICCLK, and PWRGOOD), APIC, and TAP bus signal groups only for VinCMOS on the FC-PGA Package only.
10. Parameter applies to CMOS signals BCLK, PICCLK, and PWRGOOD for VinCMOS1.5 on FC-PGA Package only.

2.10 Processor DC Specifications

The processor DC specifications in this section are defined for the Celeron processor. See Section 7.0 for signal definitions and Section 5.0 for signal listings.

Most of the signals on the Intel Celeron processor system bus are in the AGTL+ signal group. These signals are specified to be terminated to 1.5 V. The DC specifications for these signals are listed in Table 6.

To allow connection with other devices, the Clock, CMOS, APIC, and TAP signals are designed to interface at non-AGTL+ levels. The DC specifications for these pins are listed in Table 7.

Table 5 through Table 8 list the DC specifications for Intel Celeron processors operating at 66 MHz Intel Celeron processor system bus frequencies. Specifications are valid only while meeting specifications for case temperature, clock frequency, and input voltages. Care should be taken to read all notes associated with each parameter.

Table 5. Voltage and Current Specifications (Sheet 1 of 5)

Symbol	Parameter	Processor Core Freq	Processor CPUID	Min	Typ	Max	Unit	Notes
V_{CCCORE}	V_{CC} for processor core	266 MHz	0650h	—	2.00	—	V	2, 3, 4
			0651h		2.00			2, 3, 4
		300 MHz	0650h		2.00			2, 3, 4
			0651h		2.00			2, 3, 4
		300A MHz	0660h		2.00			2, 3, 4
			0665h		2.00			2, 3, 4
		333 MHz	0660h		2.00			2, 3, 4
			0665h		2.00			2, 3, 4
		366 MHz	0660h		2.00			2, 3, 4
			0665h		2.00			2, 3, 4
		400 MHz	0660h		2.00			2, 3, 4
			0665h		2.00			2, 3, 4
		433 MHz	0660h		2.00			2, 3, 4
			0665h		2.00			2, 3, 4
		466 MHz	0665h		2.00			2, 3, 4
		500 MHz	0665h		2.00			2, 3, 4
		533 MHz	0665h		2.00			2, 3, 4
		533A MHz	0683h		1.50			2, 3, 4
			0686h		1.70			2, 3, 4
		566 MHz	0683h		1.50			2, 3, 4
			0686h		1.70			2, 3, 4
		600 MHz	0683h		1.50			2, 3, 4
			0686h		1.70			2, 3, 4
			068Ah		1.75			2, 3, 20
		633 MHz	0683h		1.65			2, 3, 20
			0686h		1.70			2, 3, 20
			068Ah		1.75			2, 3, 20
		667 MHz	0683h		1.65			2, 3, 20
			0686h		1.70			2, 3, 20
			068Ah		1.75			2, 3, 20
		700 MHz	0683h		1.65			2, 3, 20
			0686h		1.70			2, 3, 20
			068Ah		1.75			2, 3, 20
		733 MHz	0683h		1.65			2, 3, 20
			0686h		1.70			2, 3, 20
			068Ah		1.75			2, 3, 20
		766 MHz	0683h		1.65			2, 3, 20
			0686h		1.70			2, 3, 20
			068Ah		1.75			2, 3, 20

Table 5. Voltage and Current Specifications (Sheet 2 of 5)

Symbol	Parameter	Processor		Min	Typ	Max	Unit	Notes
		Core Freq	CPUID					
$V_{CC_{CORE}}$	V_{CC} for processor core	800 MHz	0683h	—	1.65	—	V	2, 3, 20
			0686h		1.70			2, 3, 20
			068Ah		1.75			2, 3, 20
		850 MHz	—		—			—
			0686h		1.70			2, 3, 20
			068Ah		1.75			2, 3, 20
		900 MHz	—		—			—
			—		—			—
			068Ah		1.75			2, 3, 20
		950 MHz	—		—			—
			—		—			—
			068Ah		1.75			2, 3, 20
		1 GHz	—		—			—
			—		—			—
			068Ah		1.75			2, 3, 20
		1.10 GHz	—		—			—
			—		—			—
			068Ah		1.75			2, 3, 20
V_{REF}[19]	AGTL+ input reference voltage	—	—	$^2/_3 V_{TT} - 2\%$		$^2/_3 V_{TT} + 2\%$	V	± 2%, 11
$V_{CC_{1.5}}$[16]	Static AGTL+ bus termination voltage	—	—	1.455	1.50	1.545	V	1.5 ± 3%
	Transient AGTL+ bus termination voltage	—	—	1.365	1.50	1.365	V	1.5 ± 3%
$V_{CC_{2.5}}$[18]	V_{CC} for $V_{CC_{CMOS}}$	—	—	2.375	2.5	2.625	V	2.5 ± 5%
V_{TT}	AGTL+ bus termination voltage	—	—	1.365	1.50	1.635	V	1.5 ± 9%[5]
Baseboard Tolerance, Static	Processor core voltage static tolerance level at SC242 pins	—	—	–0.070	—	0.100	V	6
Baseboard Tolerance, Transient	Processor core voltage transient tolerance level at SC242 pins	—	—	–0.120	—	0.120	V	6
$V_{CC_{CORE}}$ Tolerance, Static	Processor core voltage static tolerance level at:							
	• SC242 edge fingers	—	—	–0.085	—	0.100	V	7
	• PPGA processor pins	—	—	-0.089	—	0.100	V	8
	• FC-PGA processor pins	—	—	-0.080	—	0.040	V	17

Table 5. Voltage and Current Specifications (Sheet 3 of 5)

Symbol	Parameter	Processor		Min	Typ	Max	Unit	Notes
		Core Freq	CPUID					
$V_{CC_{CORE}}$ Tolerance, Transient	Processor core voltage transient tolerance level at:							
	• SC242 edge fingers	—	—	–0.140	—	0.140	V	7
	• PPGA processor pins	—	—	-0.144	—	0.144	V	8
	• FC-PGA processor pins	— —	— —	-0.130 -0.110	—	0.080 0.080	V	17 24
$I_{CC_{CORE}}$ I_{CC} for processor core		266 MHz	—	—		8.2	A	9, 10
		300 MHz	—			9.3		9, 10
		300A MHz	—			9.3		9, 10
		333 MHz	—			10.1		9, 10
		366 MHz	—			11.2		9, 10
		400 MHz	—			12.2		9, 10
		433 MHz	—			12.6		9, 10
		466 MHz	—			13.4		9, 10
		500 MHz	—			14.2		9, 10
		533 MHz	—			14.9		9, 10
		533A MHz	—			11.4		9, 10
		566 MHz	—			11.9		9, 10
		600 MHz	0686h			12.0		9, 10
			068Ah			12.6		9, 10
		633 MHz	0686h			12.7		9, 10
			068Ah			13.0		9, 10
		667 MHz	0686h			13.3		9, 10
			068Ah			13.9		9, 10
		700 MHz	0686h			14.0		9, 10
			068Ah			14.8		9, 10
		733 MHz	0686h			14.6		9, 10
			068Ah			15.4		9, 10
		766 MHz	0686h			15.5		9, 10
			068Ah			16.0		9, 10
		800 MHz	0686h			16.0		9, 10
			068Ah			16.6		9, 10
		850 MHz	0686h			16.2		9, 10
			068Ah			17.3		9, 10
		900 MHz	068Ah			18.4		9, 10
		950 MHz	068Ah			19.4		9, 10
		1 GHz	068Ah			20.2		9, 10
		1.10 GHz	068Ah			22.6		9, 10
I_{VTT}	Termination voltage supply current	—	—	—	—	2.7	A	11

Table 5. Voltage and Current Specifications (Sheet 4 of 5)

Symbol	Parameter	Processor		Min	Typ	Max	Unit	Notes
		Core Freq	CPUID					
I_{SGNT}	I_{CC} Stop-Grant for processor core	266 MHz	—	—	—	1.12	A	12
		300 MHz				1.15		
		300A MHz				1.15		
		333 MHz				1.18		
		366 MHz				1.21		
		400 MHz				1.25		
		433 MHz				1.30		
		466 MHz				1.35		
		500 MHz				1.43		
		533 MHz				1.52		
		533A MHz				2.5		
		566 MHz				2.5		
		600 MHz				6.9[21]		
		633 MHz				6.9[21]		
		667 MHz				6.9[21]		
		700 MHz				6.9[21]		
		733 MHz				6.9[21]		
		766 MHz				6.9[21]		
		800 MHz				6.9[21]		
		850 MHz				6.9[21]		
		900 MHz				6.9[21]		
		950 MHz				6.9[21]		
		1 GHz				6.9[21]		
		1.10 GHz				6.9[21]		

Table 5. Voltage and Current Specifications (Sheet 5 of 5)

Symbol	Parameter	Processor		Min	Typ	Max	Unit	Notes
		Core Freq	CPUID					
ISLP	ICC Sleep for processor core	266 MHz	—	—	—	0.90	A	
		300 MHz				0.94		
		300A MHz				0.94		
		333 MHz				0.96		
		366 MHz				0.97		
		400 MHz				0.99		
		433 MHz				1.01		
		466 MHz				1.03		
		500 MHz				1.09		
		533 MHz				1.16		
		533A MHz				2.5		
		566 MHz				2.5		
		600 MHz				6.9[22]		
		633 MHz				6.9[22]		
		667 MHz				6.9[22]		
		700 MHz				6.9[22]		
		733 MHz				6.9[22]		
		766 MHz				6.9[22]		
		800 MHz				6.9[22]		
		850 MHz				6.9[22]		
		900 MHz				6.9[22]		
		950 MHz				6.9[22]		
		1 GHz				6.9[22]		
		1.10 GHz				6.9[22]		
IDSLP	ICC Deep Sleep for processor core:							
	• S.E.P.P and PPGA	—	—	—	—	0.90	A	
	• FC-PGA	—	—	—	—	6.6[23]		
ICC_{CMOS}	ICC for VCC_{CMOS}							
	• S.E.P.P and PPGA	—	—	—	—	500	mA	
	• FC-PGA	—	—	—	—	250	mA	
$dICC_{CORE}/dt$	Power supply current slew rate							
	• S.E.P.P	—	—	—	—	20	A/µs	13, 14, 15
	• PPGA and FC-PGA	—	—	—	—	240	A/µs	13, 14
$dICC_{VTT}/dt$	Termination current slew rate	—	—	—	—	8	A/µs	See Table 8, Table 20, Table 22

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. $V_{CC_{CORE}}$ and $I_{CC_{CORE}}$ supply the processor core.
3. These voltages are targets only. A variable voltage source should exist on systems in the event that a different voltage is required.
4. Use the Typical Voltage specification with the Tolerance specifications to provide correct voltage regulation to the processor.
5. V_{TT} must be held to 1.5 V ± 9%. It is recommended that V_{TT} be held to 1.5 V ± 3% while the Celeron™ processor system bus is idle. This is measured at the processor edge fingers.
6. These are the tolerance requirements, across a 20 MHz bandwidth, **at the SC242 connector pin on the bottom side of the baseboard.** The requirements at the SC242 connector pins account for voltage drops (and impedance discontinuities) across the connector, processor edge fingers, and to the processor core. $V_{CC_{CORE}}$ must return to within the static voltage specification within 100 µs after a transient event.
7. These are the tolerance requirements, across a 20 MHz bandwidth, **at the processor edge fingers.** The requirements at the processor edge fingers account for voltage drops (and impedance discontinuities) at the processor edge fingers and to the processor core. $V_{CC_{CORE}}$ must return to within the static voltage specification within 100 µs after a transient event.
8. These are the tolerance requirements, across a 20 MHz bandwidth, **at the top of the PPGA package.** $V_{CC_{CORE}}$ must return to within the static voltage specification within 100 µs after a transient event.
9. Max $I_{CC_{CORE}}$ measurements are measured at $V_{CC_{CORE}}$ max voltage ($V_{CC_{CORE\_TYP}}$ + maximum static tolerance), under maximum signal loading conditions.
10. Voltage regulators may be designed with a minimum equivalent internal resistance to ensure that the output voltage, at maximum current output, is no greater than the nominal (i.e., typical) voltage level of $V_{CC_{CORE}}$ ($V_{CC_{CORE\_TYP}}$). In this case, the maximum current level for the regulator, $I_{CC_{CORE\_REG}}$, can be reduced from the specified maximum current $I_{CC_{CORE\_MAX}}$ and is calculated by the equation:
    $I_{CC_{CORE\_REG}} = I_{CC_{CORE\_MAX}} \times V_{CC_{CORE\_TYP}} / (V_{CC_{CORE\_TYP}} + V_{CC_{CORE}}$ Tolerance, Transient)
11. The current specified is the current required for a single Intel Celeron processor. A similar amount of current is drawn through the termination resistors on the opposite end of the AGTL+ bus, unless single-ended termination is used (see Section 2.1).
12. The current specified is also for AutoHALT state.
13. Maximum values are specified by design/characterization at nominal $V_{CC_{CORE}}$.
14. Based on simulation and averaged over the duration of any change in current. Use to compute the maximum inductance tolerable and reaction time of the voltage regulator. This parameter is not tested.
15. dI_{CC}/dt specifications are measured and specified at the SC242 connector pins.
16. FC-PGA only
17. These are the tolerance requirements across a 20 MHz bandwidth at the FC-PGA socket pins on the solder side of the motherboard. $V_{CC_{CORE}}$ must return to within the static voltage specification within 100 µs after a transient event.
18. PGA only
19. S.E.P Package and FC-PGA Packages only
20. These processors implement independent V_{TT} and $V_{CC_{CORE}}$ power planes.
21. For processors with CPUID of 0686h, the I_{SGNT} is 2.5A.
22. For processors with CPUID of 0686h, the I_{SLP} is 2.5A.
23. For processors with CPUID of 0686h, the I_{DSLP} is 2.2A.
24. This specification is applicable only for processor frequencies of 933 MHz and above.

Table 6. AGTL+ Signal Groups DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage				
	• S.E.P.P and PPGA	–0.3	0.82	V	
	• FC-PGA	–0.150	VREF - 0.200	V	9
V_{IH}	Input High Voltage				
	• S.E.P.P and PPGA	1.22	VTT	V	2, 3
	• FC-PGA	VREF + 0.200	VTT	V	2, 3
R_{ON}	Buffer On Resistance		16.67	Ω	8
I_L	Leakage Current for inputs, outputs, and I/O		±100	µA	6, 7

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Celeron processor frequencies and cache sizes.
2. V_{IH} and V_{OH} for the Intel Celeron processor may experience excursions of up to 200 mV above VTT for a single system bus clock. However, input signal drivers must comply with the signal quality specifications in Section 3.0.
3. Minimum and maximum VTT are given in Table 8.
4. Parameter correlated to measurement into a 25 Ω resistor terminated to 1.5 V.
5. I_{OH} for the Intel Celeron processor may experience excursions of up to 12 mA for a single system bus clock.
6. (0 ≤ VIN ≤ 2.0 V +5%) for S.E.P Package and PPGA Package; (0 ≤ VIN ≤ 1.5V +3%) for FC-PGA package.
7. (0 ≤ VOUT ≤ 2.0 V +5%) for S.E.P Package and PPGA Package; (0 ≤ VOUT ≤ 1.5V +3%) for FC-PGA package.
8. Refer to the I/O Buffer Models for IV characteristics.
9. Steady state input voltage must not be above V_{SS} + 1.65V or below V_{TT} - 1.65V.

Table 7. Non-AGTL+ Signal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage	–0.3	0.7	V	10
V_{IH}	Input High Voltage	1.7	2.625	V	2.5 V +5% maximum, Note 10
$V_{IL1.5}$	Input Low Voltage	–0.150	VREF - 0.200	V	8, 9
$V_{IL2.5}$	Input Low Voltage	-0.58	0.700	V	7, 9
$V_{IH1.5}$	Input High Voltage	VREF + 0.200	V_{TT}	V	5, 8, 9
$V_{IH2.5}$	Input High Voltage	2.0	3.18	V	7, 9
V_{OL}	Output Low Voltage		0.4	V	2
V_{OH}	Output High Voltage				
	• S.E.P.P and PPGA	N/A	2.625	V	All outputs are open-drain to 2.5 V +5%
	• FC-PGA		V_{TT}	V	6, 8, 9
I_{OL}	Output Low Current				
	• S.E.P.P and PPGA	14		mA	
	• FC-PGA	9		mA	9
I_L	Leakage Current for Inputs, Outputs, and I/O		±100	µA	3, 4, 5, 6

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Celeron processor frequencies.
2. Parameter measured at 14 mA (for use with TTL inputs) for S.E.P Package and PPGA Package. It is 9 mA for FC-PGA.
3. (0 ≤ VIN ≤ 2.5 V +5%) for PPGA Package and S.E.P Package only.
4. (0 ≤ VOUT ≤ 2.5 V +5%) for PPGA Package and S.E.P Package only.
5. (0≤ VIN ≤ 1.5V +3%) for FC-PGA Package only.
6. (0≤ VOUT ≤ 1.5V +3%) for FC-PGA Package only.
7. Applies to non-AGTL+ signals BCLK, PICCLK, and PWRGOOD for FC-PGA Package only.
8. Applies to non-AGTL+ signals **except** BCLK, PICCLK, and PWRGOOD for FC-PGA Package only.
9. These values are specified at the processor pins for FC-PGA Package only.
10. S.E.P. Package and PPGA Package only.

2.11 AGTL+ System Bus Specifications

It is recommended that the AGTL+ bus be routed in a daisy-chain fashion with termination resistors to VTT at each end of the signal trace. These termination resistors are placed electrically between the ends of the signal traces and the VTT voltage supply and generally are chosen to approximate the substrate impedance. The valid high and low levels are determined by the input buffers using a reference voltage called VREF. Single ended termination may be possible if trace lengths are tightly controlled, see the *Intel® 440EX AGPset Design Guide* (Order Number 290637) or the *Intel® Celeron™ Processor (PPGA) with the Intel® 440LX AGPset Design Guide* (Order Number 245088) for more information.

Table 8 below lists the nominal specification for the AGTL+ termination voltage (VTT). The AGTL+ reference voltage (VREF) is generated on the processor substrate (S.E.P. Package only) for the processor core, but should be set to $^{2}/_{3}$ VTT for other AGTL+ logic using a voltage divider on the motherboard. It is important that the motherboard impedance be specified and held to:

- ±20% tolerance (S.E.E.P. and PPGA)
- ±15% tolerance (FC-PGA)

It is also important that the intrinsic trace capacitance for the AGTL+ signal group traces is known and well-controlled. For more details on AGTL+, see the *Pentium® II Processor Developer's Manual* (Order Number 243502) and AP-585, *Pentium® II Processor AGTL+ Guidelines* (Order Number 243330).

Table 8. Processor AGTL+ Bus Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes
VTT	Bus Termination Voltage					
	• S.E.P.P and PPGA	1.365	1.50	1.635	V	1.5 V ± 9% 2
	• FC-PGA		1.50		V	4
RTT	Termination Resistor					
	• S.E.P.P and PPGA		56		Ω	± 5%
	• FC-PGA (on die RTT)	40		130	Ω	5
VREF	Bus Reference Voltage					
	• S.E.P.P and PPGA		$^{2}/_{3}$ VTT		V	± 2% 3
	• FC-PGA	0.950	2/3 VTT	1.05	V	6

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Celeron processor frequencies.
2. VTT must be held to 1.5 V ± 9%; $dICC_{VTT}/dt$ is specified in Table 5. It is recommended that VTT be held to 1.5 V ± 3% while the Intel Celeron processor system bus is idle. This is measured at the processor edge fingers.
3. VREF is generated on the processor substrate to be $^{2}/_{3}$ VTT nominally with the S.E.P. package. It must be created on the motherboard for processors in the PPGA package.
4. V_{TT} and $Vcc_{1.5}$ must be held to 1.5V ±9%. It is required that V_{TT} and $Vcc_{1.5}$ be held to 1.5V ±3% while the processor system bus is idle (static condition). This is measured at the PGA370 socket pins on the bottom side of the baseboard.
5. The value of the on-die R_{TT} is determined by the resistor value measured by the RTTCTRL signal pin. The on-die R_{TT} tolerance is ±15% based on the RTTCTRL resistor pull-down of ±1%. See Section 7.0 for more details on the RTTCTRL signal. Refer to the recommendation guidelines for the specific chipset/processor combination.
6. VREF is generated on the motherboard and should be 2/3 V_{TT} ±2% nominally. Insure that there is adequate VREF decoupling on the motherboard.

2.12 System Bus AC Specifications

The Celeron processor system bus timings specified in this section are defined at the Intel Celeron processor edge fingers and the processor core pins. Timings specified at the processor edge fingers only apply to the S.E.P. Package and timings given at the processor core pins apply to all S.E.P. Package and PGA packages. Unless otherwise specified, timings are tested at the processor core during manufacturing. Timings at the processor edge fingers are specified by design characterization. See Section 7.0 for the Intel Celeron processor signal definitions. **Note that at 66 MHz system bus operation, the Intel Celeron processor timings at the processor edge fingers are identical to the Pentium II processor timings at the edge fingers.** See the *Pentium® II Processor at 233, 266, 300, and 333 MHz* (Order Number 243335) for more detail.

Table 9 through Table 26 list the AC specifications associated with the Intel Celeron processor system bus. These specifications are broken into the following categories: Table 9 through Table 12 contain the system bus clock specifications, Table 13 and Table 14 contain the AGTL+ specifications, Table 17 and Table 18 are the CMOS signal group specifications, Table 20 contains timings for the Reset conditions, Table 22 and Table 23 cover APIC bus timing, and Table 25 and Table 26 cover TAP timing. For each pair of tables, the first table contains timing specifications for measurement or simulation at the processor edge fingers. The second table contains specifications for simulation at the processor core pads.

All Intel Celeron processor system bus AC specifications for the AGTL+ signal group are relative to the rising edge of the BCLK input. All AGTL+ timings are referenced to V_{REF} for both ‘0’ and ‘1’ logic levels unless otherwise specified.

The timings specified in this section should be used in conjunction with the I/O buffer models provided by Intel. These I/O buffer models, which include package information, are available in Quad format as the *Intel Celeron™ Processor I/O Buffer Models*, Quad XTK Format (Electronic Form). AGTL+ layout guidelines are also available in AP-585, *Pentium® II Processor AGTL+ Guidelines* (Order Number 243330).

Care should be taken to read all notes associated with a particular timing parameter.

Table 9. System Bus AC Specifications (Clock) at the Processor Edge Fingers (for S.E.P. Package)

T# Parameter	Min	Nom	Max	Unit	Figure	Notes
System Bus Frequency		66.67		MHz		
T1’: BCLK Period	15.0			ns	3	4, 5, 6
T1B’: SC242 to Core Logic BCLK Offset		0.78		ns	3	Absolute Value [7,8]
T2’: BCLK Period Stability			± 300	ps		See Table 10
T3’: BCLK High Time	4.44			ns	3	@>2.0 V [6]
T4’: BCLK Low Time	4.44			ns	3	@<0.5 V [6]
T5’: BCLK Rise Time	0.84		2.31	ns	3	(0.5 V–2.0 V) [6, 9]
T6’: BCLK Fall Time	0.84		2.31	ns	3	(2.0 V–0.5 V) [6, 9]

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all Celeron processor frequencies.
2. All AC timings for the AGTL+ signals are referenced to the BCLK rising edge at 0.70 V at the processor edge fingers. This reference is to account for trace length and capacitance on the processor substrate, allowing the processor core to receive the signal with a reference at 1.25 V. All AGTL+ signal timings (address bus, data bus, etc.) are referenced at 1.00 V at the processor edge fingers.
3. All AC timings for the CMOS signals are referenced to the BCLK rising edge at 0.70 V at the processor edge fingers. This reference is to account for trace length and capacitance on the processor substrate, allowing the processor core to receive the signal with a reference at 1.25 V. All CMOS signal timings (compatibility signals, etc.) are referenced at 1.25 V at the processor edge fingers.
4. The internal core clock frequency is derived from the Intel Celeron processor system bus clock. The system bus clock to core clock ratio is determined during initialization. Table 12 shows the supported ratios for each processor.
5. The BCLK period allows a +0.5 ns tolerance for clock driver variation.
6. This specification applies to Intel Celeron processors when operating at a system bus frequency of 66 MHz.
7. The BCLK offset time is the absolute difference needed between the BCLK signal arriving at the Intel Celeron processor edge finger at 0.5 V vs. arriving at the core logic at 1.25 V. The positive offset is needed to account for the delay between the SC242 connector and processor core. The positive offset ensures both the processor core and the core logic receive the BCLK edge concurrently.
8. See Section 3.1 for Intel Celeron processor system bus clock signal quality specifications.
9. Not 100% tested. Specified by design characterization as a clock driver requirement.

Table 10. System Bus AC Specifications (Clock) at the Processor Core Pins (for Both S.E.P. and PGA Packages)

T# Parameter	Min	Nom	Max	Unit	Figure	Notes
System Bus Frequency		66.67		MHz		
T1: BCLK Period	15.0			ns	3	4, 5, 6
T2: BCLK Period Stability			± 300	ps	3	6, 8, 9
T3: BCLK High Time	4.94			ns	3	@>2.0 V [6]
T4: BCLK Low Time	4.94			ns	3	@<0.5 V [6]
T5: BCLK Rise Time						
• S.E.P.P. and PPGA	0.34		1.36	ns	3	(0.5 V–2.0 V) [6, 10]
• FC-PGA	0.40		1.6	ns	3	10, 11
T6: BCLK Fall Time						
• S.E.P.P. and PPGA	0.34		1.36	ns	3	(2.0 V–0.5 V) [6, 10]
• FC-PGA	0.40		1.6	ns	3	10, 11

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Celeron processor frequencies.
2. All AC timings for the AGTL+ signals are referenced to the BCLK rising edge at 1.25 V at the processor core pin. All AGTL+ signal timings (address bus, data bus, etc.) are referenced at 1.00 V at the processor core pins.
3. All AC timings for the CMOS signals are referenced to the BCLK rising edge at 1.25 V at the processor core pin. All CMOS signal timings (compatibility signals, etc.) are referenced at 1.25 V at the processor core pins.
4. The internal core clock frequency is derived from the Intel Celeron processor system bus clock. The system bus clock to core clock ratio is determined during initialization. Table 12 shows the supported ratios for each processor.
5. The BCLK period allows a +0.5 ns tolerance for clock driver variation.
6. This specification applies to the Intel Celeron processor when operating at a system bus frequency of 66 MHz.
7. See Section 3.1 for Intel Celeron processor system bus clock signal quality specifications.
8. Due to the difficulty of accurately measuring clock jitter in a system, it is recommended that a clock driver be used that is designed to meet the period stability specification into a test load of 10 to 20 pF. This should be measured on the **rising edges of adjacent BCLKs crossing 1.25 V at the processor core pin**. The jitter present must be accounted for as a component of BCLK timing skew between devices.
9. The clock driver's closed loop jitter bandwidth must be set low to allow any PLL-based device to track the jitter created by the clock driver. The –20 dB attenuation point, as measured into a 10 to 20 pF load, should be less than 500 kHz. This specification may be ensured by design characterization and/or measured with a spectrum analyzer.
10. Not 100% tested. Specified by design characterization as a clock driver requirement.
11. BCLK Rise time is measure between 0.5V–2.0V. BCLK fall time is measured between 2.0V–0.5V.

Table 11. System Bus AC Specifications (SET Clock)[1, 2]

T# Parameter	Min	Nom	Max	Unit	Figure	Notes
System Bus Frequency		66.67 100.00		MHz		4
T1: BCLK Period	10.0 10.0			ns	3	4, 5, 10 4, 5, 11
T2: BCLK Period Stability			±250 ±250	ps		6, 7, 10 6, 7, 11
T3: BCLK High Time	2.5 2.5			ns	3	9, 10 9, 11
T4: BCLK Low Time	2.4 2.4			ns	3	9, 10 9, 11
T5: BCLK Rise Time	0.4		1.6	ns	3	3, 8
T6: BCLK Fall Time	0.4		1.6	ns	3	3, 8

NOTES:
1. Unless otherwise noted, all specifications in this table apply to Celeron processors at all frequencies.
2. All AC timings for the AGTL+ signals are referenced to the BCLK rising edge at 1.25V at the processor pin. All AGTL+ signal timings (address bus, data bus, etc.) are referenced at 1.00 V at the processor pins.
3. Not 100% tested. Specified by design characterization as a clock driver requirement.
4. The internal core clock frequency is derived from the processor system bus clock. The system bus clock to core clock ratio is determined during initialization. Individual processors will only operate at their specified system bus frequency, either 66 MHz or 100 MHz, not both. Table 12 shows the supported ratios for each processor.
5. The BCLK period allows a +0.5 ns tolerance for clock driver variation. See the appropriate clock synthesizer/driver specification for details.
6. Due to the difficulty of accurately measuring clock jitter in a system, it is recommended that a clock driver be used that is designed to meet the period stability specification into a test load of 10 to 20 pF. This should be measured on the **rising edges of adjacent BCLKs crossing 1.25 V at the processor pin**. The jitter present must be accounted for as a component of BCLK timing skew between devices.
7. The clock driver's closed loop jitter bandwidth must be set low to allow any PLL-based device to track the jitter created by the clock driver. The –20 dB attenuation point, as measured into a 10 to 20 pF load, should be less than 500 kHz. This specification may be ensured by design characterization and/or measured with a spectrum analyzer. See the appropriate clock synthesizer/driver specification for details
8. BCLK Rise time is measure between 0.5 V–2.0 V. BCLK fall time is measured between 2.0 V–0.5 V.
9. BCLK high time is measured as the period of time above 2.0 V. BCLK low time is measured as the period of time below 0.5 V.
10. This specification applies to Pentium III processors operating at a system bus frequency of 66 MHz.
11. This specification applies to Pentium III processors operating at a system bus frequency of 100 MHz

Table 12. Valid Intel® Celeron™ Processor System Bus, Core Frequency

Core Frequency (MHz)	BCLK Frequency (MHz)	Frequency Multiplier
266 MHz	66	4
300 MHz	66	4.5
333 MHz	66	5
366 MHz	66	5.5
400 MHz	66	6
433 MHz	66	6.5
466 MHz	66	7
500 MHz	66	7.5
533 MHz	66	8
566 MHz	66	8.5
600 MHz	66	9
633 MHz	66	9.5
667 MHz	66	10
700 MHz	66	10.5
733 MHz	66	11
766 MHz	66	11.5
800 MHz	100	8
850 MHz	100	8.5
900 MHz	100	9
950 MHz	100	9.5
1 GHz	100	10
1.10 GHz	100	11

NOTES:
1. Contact your local Intel representative for the latest information on processor frequencies and/or frequency multipliers.
2. While other bus ratios are defined, operation at frequencies other than those listed are not supported.

Table 13. System Bus AC Specifications (AGTL+ Signal Group) at the Processor Edge Fingers (for S.E.P. Package)

T# Parameter	Min	Max	Unit	Figure	Notes
T7’: AGTL+ Output Valid Delay	1.07	6.37	ns	4	4, 5
T8’: AGTL+ Input Setup Time	1.96		ns	5	4, 6, 7, 8
T9’: AGTL+ Input Hold Time	1.53		ns	5	4, 9
T10’: RESET# Pulse Width	1.00		ms	6	10

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Celeron processor frequencies.
2. Not 100% tested. Specified by design characterization.
3. All AC timings for the AGTL+ signals are referenced to the BCLK rising edge at 0.50 V at the processor edge fingers. All AGTL+ signal timings (compatibility signals, etc.) are referenced at 1.00 V at the processor edge fingers.
4. This specification applies to Intel Celeron processors operating with a 66 MHz Intel Celeron processor system bus only.
5. Valid delay timings for these signals are specified into 50 Ω to 1.5 V and with VREF at 1.0 V.
6. A minimum of 3 clocks must be guaranteed between two active-to-inactive transitions of TRDY#.
7. RESET# can be asserted (active) asynchronously, but must be deasserted synchronously.
8. Specification is for a minimum 0.40 V swing.
9. Specification is for a maximum 1.0 V swing.
10. After $V_{CC_{CORE}}$, and BCLK become stable.

Table 14. System Bus AC Specifications (AGTL+ Signal Group) at the Processor Core Pins (for S.E.P. Package)

T# Parameter	Min	Max	Unit	Figure	Notes
T7: AGTL+ Output Valid Delay	0.17	5.16	ns	4	5
T8: AGTL+ Input Setup Time	2.10		ns	5	5, 6, 7, 8
T9: AGTL+ Input Hold Time	0.77		ns	5	9
T10: RESET# Pulse Width	1.00		ms	6	7, 10

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Intel ®Celeron™ processor frequencies.
2. These specifications are tested during manufacturing.
3. All AC timings for the AGTL+ signals are referenced to the BCLK rising edge at 1.25 V at the processor core pin. All AGTL+ signal timings (compatibility signals, etc.) are referenced at 1.00 V at the processor core pins.
4. This specification applies to the Intel Celeron processor operating with a 66 MHz Intel Celeron processor system bus only.
5. Valid delay timings for these signals are specified into 25 Ω to 1.5 V and with VREF at 1.0 V.
6. A minimum of 3 clocks must be guaranteed between two active-to-inactive transitions of TRDY#.
7. RESET# can be asserted (active) asynchronously, but must be deasserted synchronously.
8. Specification is for a minimum 0.40 V swing.
9. Specification is for a maximum 1.0 V swing.
10. After $V_{CC_{CORE}}$ and BCLK become stable.

Table 15. Processor System Bus AC Specifications (AGTL+ Signal Group) at the Processor Core Pins (for PPGA Package)

T# Parameter	Min	Max	Unit	Figure	Notes
T7: AGTL+ Output Valid Delay	0.30	4.43	ns	4	5
T8: AGTL+ Input Setup Time	2.10		ns	5	5, 6, 7
T9: AGTL+ Input Hold Time	0.85		ns	5	
T10: RESET# Pulse Width	1.00		ms	6	7, 8

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. These specifications are tested during manufacturing.
3. All AC timings for the AGTL+ signals are REFerenced to the BCLK rising edge at 1.25 V at the processor pin. All GTL+ signal timings (compatibility signals, etc.) are referenced at 1.00 V at the processor pins.
4. This specification applies to the processor operating with a 66 MHz system bus only.
5. Valid delay timings for these signals are specified into 25 Ω to 1.5 V and with VREF at 1.0 V.
6. A minimum of 3 clocks must be guaranteed between two active-to-inactive transitions of TRDY#.
7. RESET# can be asserted (active) asynchronously, but must be deasserted synchronously.
8. After $V_{CC_{CORE}}$ and BCLK become stable.

Table 16. System Bus AC Specifications (AGTL+ Signal Group) at the Processor Core Pins (for FC-PGA Package)

T# Parameter	Min	Max	Unit	Figure	Notes
T7: AGTL+ Output Valid Delay	0.40	3.25	ns	4	4, 10, 11
T8: AGTL+ Input Setup Time	1.20		ns	5	5, 6, 7, 10, 11
T9: AGTL+ Input Hold Time	1.00		ns	5	8, 10, 11
T10: RESET# Pulse Width	1.00		ms	7	6, 9, 10, 11

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Celeron processors at all frequencies and cache sizes.
2. These specifications are tested during manufacturing.
3. All AC timings for the AGTL+ signals are referenced to the BCLK rising edge at 1.25V at the processor pin. All AGTL+ signal timings (compatibility signals, etc.) are referenced at 1.00V at the processor pins.
4. Valid delay timings for these signals are specified into 50 Ω to 1.5V and with VREF at 1.0 V.
5. A minimum of 3 clocks must be guaranteed between two active-to-inactive transitions of TRDY#.
6. RESET# can be asserted (active) asynchronously, but must be deasserted synchronously.
7. Specification is for a minimum 0.40 V swing from VREF - 200 mV to VREF + 200 mV. This assumes an edge rate of 0.3V/ns.
8. Specification is for a maximum 1.0 V swing from VTT - 1V to VTT. This assumes an edge rate of 3 V/ns.
9. This should be measured after $V_{CC_{CORE}}$, $V_{CC_{CMOS}}$, and BCLK become stable.
10. This specification applies to the FC-PGA running at 66 MHz system bus frequency.
11. This specification applies to the FC-PGA running at 100 MHz system bus frequency.

Table 17. System Bus AC Specifications (CMOS Signal Group) at the Processor Edge Fingers (for S.E.P. Package)

T# Parameter	Min	Max	Unit	Figure	Notes
T14’: CMOS Input Pulse Width, except PWRGOOD	2		BCLKs	8	Active and Inactive states
T14B: LINT[1:0] Input Pulse Width	6		BCLKs	8	5
T15’: PWRGOOD Inactive Pulse Width	10		BCLKs	8	6, 7

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Celeron processor frequencies.
2. Not 100% tested. Specified by design characterization.
3. All AC timings for the CMOS signals are referenced to the BCLK rising edge at 0.50 V at the processor edge fingers. All CMOS signal timings (address bus, data bus, etc.) are referenced at 1.25 V.
4. These signals may be driven asynchronously.
5. This specification only applies when the APIC is enabled and the LINT1 or LINT0 pin is configured as an edge-triggered interrupt with fixed delivery; otherwise, specification T14 applies.

   PWRGOOD must remain below $V_{IL,max}$ (Table 6) until all the voltage planes meet the voltage tolerance specifications in Table 5 and BCLK has met the BCLK AC specifications in Table 10 for at least 10 clock cycles. PWRGOOD must rise glitch-free and monotonically to 2.5 V.
6. When driven inactive or after VCC_{CORE}, and BCLK become stable.
7. If the BCLK signal meets its AC specification within 150 ns of turning on, then the PWRGOOD inactive pulse width specification (T15) is waived and BCLK may start after PWRGOOD is asserted. PWRGOOD must still remain below $V_{IL,max}$ until all the voltage planes meet the voltage tolerance specifications.

Table 18. System Bus AC Specifications (CMOS Signal Group) at the Processor Core Pins (for Both S.E.P., PGA, and FC-PGA Packages)

T# Parameter	Min	Max	Unit	Figure	Notes
T14: CMOS Input Pulse Width, except PWRGOOD	2		BCLKs	8	Active and Inactive states
T14B: LINT[1:0] Input Pulse Width (S.E.P.P. Only)	6		BCLKs	8	5
T15: PWRGOOD Inactive Pulse Width	10		BCLKs	8	6, 7

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Celeron processor frequencies.
2. These specifications are tested during manufacturing.
3. All AC timings for the CMOS signals are referenced to the BCLK rising edge at 1.25 V at the processor core pins. All CMOS signal timings (address bus, data bus, etc.) are referenced at 1.25 V.
4. These signals may be driven asynchronously.
5. This specification only applies when the APIC is enabled and the LINT1 or LINT0 pin is configured as an edge-triggered interrupt with fixed delivery; otherwise, specification T14 applies.
6. When driven inactive or after VCC_{CORE}, and BCLK become stable.
7. If the BCLK signal meets its AC specification within 150 ns of turning on, then the PWRGOOD inactive pulse width specification (T15) is waived and BCLK may start after PWRGOOD is asserted. PWRGOOD must still remain below $V_{IL,max}$ until all the voltage planes meet the voltage tolerance specifications.

   PWRGOOD must remain below $V_{IL,max}$ (Table 6) until all the voltage planes meet the voltage tolerance specifications in Table 5 and BCLK has met the BCLK AC specifications in Table 10 for at least 10 clock cycles. PWRGOOD must rise glitch-free and monotonically to 2.5 V.

Table 19. System Bus AC Specifications (CMOS Signal Group) [1, 2, 3, 4]

T# Parameter	Min	Max	Unit	Figure	Notes
T14: CMOS Input Pulse Width, except PWRGOOD	2		BCLKs	4	Active and Inactive states
T15: PWRGOOD Inactive Pulse Width	10		BCLKs	4, 8	5

NOTES:
1. Unless otherwise noted, all specifications in this table apply to Celeron processors at all frequencies
2. These specifications are tested during manufacturing.
3. These signals may be driven asynchronously.
4. All CMOS outputs shall be asserted for at least 2 BCLKs.
5. When driven inactive or after $V_{CC_{CORE}}$, V_{TT}, $V_{CC_{CMOS}}$, and BCLK become stable.

Table 20. System Bus AC Specifications (Reset Conditions) (for Both S.E.P. and PPGA Packages)

T# Parameter	Min	Max	Unit	Figure	Notes
T16: Reset Configuration Signals (A[14:5]#, BR0#, FLUSH#, INIT#) Setup Time	4		BCLKs	6	Before deassertion of RESET#
T17: Reset Configuration Signals (A[14:5]#, BR0#, FLUSH#, INIT#) Hold Time	2	20	BCLKs	6	After clock that deasserts RESET#

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.

Table 21. System Bus AC Specifications (Reset Conditions) (for the FC-PGA Package)

T# Parameter	Min	Max	Unit	Figure	Notes
T16: Reset Configuration Signals (A[14:5]#, BR0#, INIT#) Setup Time	4		BCLKs	7	Before deassertion of RESET#
T17: Reset Configuration Signals (A[14:5]#, BR0#, INIT#) Hold Time	2	20	BCLKs	7	After clock that deasserts RESET#
T18: Reset Configuration Signals (A20M#, IGNNE#, LINT[1:0]) Setup Time	1		ms	7	Before deassertion of RESET#, 3
T19: Reset Configuration Signals (A20M#, IGNNE#, LINT[1:0]) Delay Time		5	BCLKs	7	After assertion of RESET#, 2, 3
T20: Reset Configuration Signals (A20M#, IGNNE#, LINT[1:0]) Hold Time	2	20	BCLKs	7	After clock that deasserts RESET#, 3

NOTES:
1. Unless otherwise noted, all specifications in this table apply to Celeron FC-PGA processors at all frequencies and cache sizes.
2. For a reset, the clock ratio defined by these signals must be a safe value (their final or a lower-multiplier) within this delay unless PWRGOOD is being driven inactive.
3. These parameters apply to processor engineering samples only. For production units, the processor core frequency will be determined through the processor internal logic.

Table 22. System Bus AC Specifications (APIC Clock and APIC I/O) at the Processor Edge Fingers (for S.E.P. Package)

T# Parameter	Min	Max	Unit	Figure	Notes
T21’: PICCLK Frequency	2.0	33.3	MHz		
T22’: PICCLK Period	30.0	500.0	ns	3	
T23’: PICCLK High Time	12.0		ns	3	
T24’: PICCLK Low Time	12.0		ns	3	
T25’: PICCLK Rise Time	0.25	3.0	ns	3	
T26’: PICCLK Fall Time	0.25	3.0	ns	3	
T27’: PICD[1:0] Setup Time	8.5		ns	5	5
T28’: PICD[1:0] Hold Time	3.0		ns	5	5
T29’: PICD[1:0] Valid Delay	3.0	12.0	ns	4	5, 6, 7

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Celeron processor frequencies.
2. Not 100% tested. Specified by design characterization.
3. All AC timings for the APIC I/O signals are referenced to the PICCLK rising edge at 0.7 V at the processor edge fingers. All APIC I/O signal timings are referenced at 1.25 V at the processor edge fingers.
4. This specification applies to Intel Celeron processors operating with a 66 MHz Intel Celeron processor system bus only.
5. Referenced to PICCLK rising edge.
6. For open drain signals, valid delay is synonymous with float delay.
7. Valid delay timings for these signals are specified to 2.5 V +5%.

Table 23. System Bus AC Specifications (APIC Clock and APIC I/O) at the Processor Core Pins (For S.E.P. and PGA Packages)

T# Parameter	Min	Max	Unit	Figure	Notes
T21: PICCLK Frequency	2.0	33.3	MHz		
T22: PICCLK Period	30.0	500.0	ns	3	
T23: PICCLK High Time • S.E.P.P and PPGA • FC-PGA	 11.0 10.5		 ns ns	 3 3	 @>2.0V @>1.7V
T24: PICCLK Low Time • S.E.P.P and PPGA • FC-PGA	 11.0 10.5		 ns ns	 3 3	 @<0.5V @<0.7V
T25: PICCLK Rise Time	0.25	3.0	ns	3	(0.5V-2.0V)
T26: PICCLK Fall Time	0.25	3.0	ns	3	(2.0V-0.5V)
T27: PICD[1:0] Setup Time • S.E.P.P and PPGA • FC-PGA	 8.0 5.0		 ns ns	 5 5	 5 5
T28: PICD[1:0] Hold Time	2.5		ns	5	5
T29: PICD[1:0] Valid Delay (S.E.P.P and PPGA only)	1.5	10.0	ns	4	5, 6, 7
T29a: PICD[1:0] Valid Delay (Rising Edge) (FC-PGA only)	1.5	8.7	ns	4	5, 6, 8
T29b: PICD[1:0] Valid Delay (Falling Edge) (FC-PGA only)	1.5	12.0	ns	4	5, 6, 8

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Celeron processor frequencies.
2. These specifications are tested during manufacturing.
3. All AC timings for the APIC I/O signals are referenced to the PICCLK rising edge at 1.25 V at the processor core pins. All APIC I/O signal timings are referenced at 1.25 V at the processor core pins.
4. This specification applies to Intel Celeron processors operating with a 66 MHz Intel Celeron processor system bus only.
5. Referenced to PICCLK rising edge.
6. For open drain signals, valid delay is synonymous with float delay.
7. Valid delay timings for these signals are specified to 2.5 V +5%.
8. Valid delay timings for these signals are specified to 1.5 V +5%.

Table 24. System Bus AC Specifications (APIC Clock and APIC I/O)[1, 2, 3]

T# Parameter	Min	Max	Unit	Figure	Notes
T21: PICCLK Frequency	2.0	33.3	MHz		
T22: PICCLK Period	30.0	500.0	ns	3	
T23: PICCLK High Time	10.5		ns	3	@ > 1.7V
T24: PICCLK Low Time	10.5		ns	3	@ < 0.7V
T25: PICCLK Rise Time	0.25	3.0	ns	3	(0.7V - 1.7V)
T26: PICCLK Fall Time	0.25	3.0	ns	3	(1.7V - 0.7V)
T27: PICD[1:0] Setup Time	5.0		ns	5	4
T28: PICD[1:0] Hold Time	2.5		ns	5	4
T29a: PICD[1:0] Valid Delay (Rising Edge)	1.5	8.7	ns	3, 4	4, 5, 6
T29b: PICD[1:0] Valid Delay (Falling Edge)	1.5	12.0	ns	3, 4	4, 5, 6

NOTES:
1. Unless otherwise noted, all specifications in this table apply to Celeron processors at all frequencies.
2. These specifications are tested during manufacturing.
3. All AC timings for the APIC I/O signals are referenced to the PICCLK rising edge at 1.25 V at the processor pins. All APIC I/O signal timings are referenced at 0.75 V at the processor pins.
4. Referenced to PICCLK rising edge.
5. For open drain signals, valid delay is synonymous with float delay.
6. Valid delay timings for these signals are specified into 150 Ω load pulled up to 1.5 V.

Table 25. System Bus AC Specifications (TAP Connection) at the Processor Edge Fingers (For S.E.P. Package)

T# Parameter	Min	Max	Unit	Figure	Notes
T30’: TCK Frequency		16.667	MHz		
T31’: TCK Period	60.0		ns	3	
T32’: TCK High Time	25.0		ns	3	@1.7 V
T33’: TCK Low Time	25.0		ns	3	@0.7 V
T34’: TCK Rise Time		5.0	ns	3	(0.7 V–1.7 V) [4]
T35’: TCK Fall Time		5.0	ns	3	(1.7 V–0.7 V) [4]
T36’: TRST# Pulse Width	40.0		ns	6	Asynchronous
T37’: TDI, TMS Setup Time	5.5		ns	9	5
T38’: TDI, TMS Hold Time	14.5		ns	9	5
T39’: TDO Valid Delay	2.0	13.5	ns	9	6, 7
T40’: TDO Float Delay		28.5	ns	9	6, 7
T41’: All Non-Test Outputs Valid Delay	2.0	27.5	ns	9	6, 8, 9
T42’: All Non-Test Inputs Setup Time		27.5	ns	9	6, 8, 9
T43’: All Non-Test Inputs Setup Time	5.5		ns	9	5, 8, 9
T44’: All Non-Test Inputs Hold Time	14.5		ns	9	5, 8, 9

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.
2. All AC timings for the TAP signals are referenced to the TCK rising edge at 0.70 V at the processor edge fingers. All TAP signal timings (TMS, TDI, etc.) are referenced at 1.25 V at the processor edge fingers.
3. Not 100% tested. Specified by design characterization.
4. 1 ns can be added to the maximum TCK rise and fall times for every 1 MHz below 16.667 MHz.
5. Referenced to TCK rising edge.
6. Referenced to TCK falling edge.
7. Valid delay timing for this signal is specified to 2.5 V +5%.
8. Non-Test Outputs and Inputs are the normal output or input signals (besides TCK, TRST#, TDI, TDO, and TMS). These timings correspond to the response of these signals due to TAP operations.
9. During Debug Port operation, use the normal specified timings rather than the TAP signal timings.

Table 26. System Bus AC Specifications (TAP Connection) at the Processor Core Pins (for Both S.E.P. and PPGA Packages)

T# Parameter	Min	Max	Unit	Figure	Notes
T30: TCK Frequency		16.667	MHz		
T31: TCK Period	60.0		ns	3	
T32: TCK High Time	25.0		ns	3	@1.7 V; 10
T33: TCK Low Time	25.0		ns	3	@0.7 V; 10
T34: TCK Rise Time		5.0	ns	3	(0.7 V–1.7 V); 4, 10
T35: TCK Fall Time		5.0	ns	3	(1.7 V–0.7 V); 4, 10
T36: TRST# Pulse Width	40.0		ns	6	Asynchronous; 10
T37: TDI, TMS Setup Time	5.0		ns	9	5
T38: TDI, TMS Hold Time	14.0		ns	9	5
T39: TDO Valid Delay	1.0	10.0	ns	9	6, 7
T40: TDO Float Delay		25.0	ns	9	6, 7, 10
T41: All Non-Test Outputs Valid Delay	2.0	25.0	ns	9	6, 8, 9
T42: All Non-Test Inputs Setup Time		25.0	ns	9	6, 8, 9, 10
T43: All Non-Test Inputs Setup Time	5.0		ns	9	5, 8, 9
T44: All Non-Test Inputs Hold Time	13.0		ns	9	5, 8, 9

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Celeron processor frequencies.
2. For the S.E.P. and PPGA packages: All AC timings for the TAP signals are referenced to the TCK rising edge at 1.25 V at the processor core pins. All TAP signal timings (TMS, TDI, etc.) are referenced at 1.25 V at the processor core pins.
   For the FC-PGA package: All AC timings for the TAP signals are referenced to the TCK rising edge at 0.75 V at the processor pins. All TAP signal timings (TMS, TDI, etc.) are referenced at 0.75 V at the processor pins.
3. These specifications are tested during manufacturing, unless otherwise noted.
4. 1 ns can be added to the maximum TCK rise and fall times for every 1 MHz below 16.667 MHz.
5. Referenced to TCK rising edge.
6. Referenced to TCK falling edge.
7. For the S.E.P. and PPGA packages: Valid delay timing for this signal is specified to 2.5 V +5%.
   For the FC-PGA package: Valid delay timing for this signal is specified to 1.5 V +3%.
8. Non-Test Outputs and Inputs are the normal output or input signals (besides TCK, TRST#, TDI, TDO, and TMS). These timings correspond to the response of these signals due to TAP operations.
9. During Debug Port operation, use the normal specified timings rather than the TAP signal timings.
10. Not 100% tested. Specified by design characterization.

Table 27. System Bus AC Specifications (TAP Connection)[1, 2, 3]

T# Parameter	Min	Max	Unit	Figure	Notes
T30: TCK Frequency		16.667	MHz		
T31: TCK Period	60.0		ns	3	
T32: TCK High Time	25.0		ns	3	V_{REF} + 0.200 V, 10
T33: TCK Low Time	25.0		ns	3	V_{REF} - 0.200 V, 10
T34: TCK Rise Time		5.0	ns	3	(V_{REF} – 0.200 V) – (V_{REF} + 0.200 V), 4, 10
T35: TCK Fall Time		5.0	ns	3	(V_{REF} + 0.200 V) – (V_{REF} – 0.200 V), 4, 10
T36: TRST# Pulse Width	40.0		ns	10	Asynchronous, 10
T37: TDI, TMS Setup Time	5.0		ns	9	5
T38: TDI, TMS Hold Time	14.0		ns	9	5
T39: TDO Valid Delay	1.0	10.0	ns	9	6, 7
T40: TDO Float Delay		25.0	ns	9	6, 7, 10
T41: All Non-Test Outputs Valid Delay	2.0	25.0	ns	9	6, 8, 9
T42: All Non-Test Inputs Setup Time		25.0	ns	9	6, 8, 9, 10
T43: All Non-Test Inputs Setup Time	5.0		ns	9	5, 8, 9
T44: All Non-Test Inputs Hold Time	13.0		ns	9	5, 8, 9

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Celeron processors frequencies.
2. All AC timings for the TAP signals are referenced to the TCK rising edge at 0.75 V at the processor pins. All TAP signal timings (TMS, TDI, etc.) are referenced at 0.75 V at the processor pins.
3. These specifications are tested during manufacturing, unless otherwise noted.
4. 1 ns can be added to the maximum TCK rise and fall times for every 1 MHz below 16.667 MHz.
5. Referenced to TCK rising edge.
6. Referenced to TCK falling edge.
7. Valid delay timing for this signal is specified to 1.5 V (1.25 V for AGTL platforms).
8. Non-Test Outputs and Inputs are the normal output or input signals (besides TCK, TRST#, TDI, TDO, and TMS). These timings correspond to the response of these signals due to TAP operations.
9. During Debug Port operation, use the normal specified timings rather than the TAP signal timings.
10. Not 100% tested. Specified by design characterization.

Note: For Figure 3 through Figure 10, the following apply:

1. Figure 3 through Figure 10 are to be used in conjunction with Table 9 through Table 26.
2. All AC timings for the AGTL+ signals at the processor edge fingers are referenced to the BCLK rising edge at 0.50 V. This reference is to account for trace length and capacitance on the processor substrate, allowing the processor core to receive the signal with a reference at 1.25 V. All AGTL+ signal timings (address bus, data bus, etc.) are referenced at 1.00 V at the processor edge fingers.
3. All AC timings for the AGTL+ signals at the processor core pins are referenced to the BCLK rising edge at 1.25 V. All AGTL+ signal timings (address bus, data bus, etc.) are referenced at 1.00 V at the processor core pins.
4. All AC timings for the CMOS signals at the processor edge fingers are referenced to the BCLK rising edge at 0.50 V. This reference is to account for trace length and capacitance on the processor substrate, allowing the processor core to receive the signal with a reference at 1.25 V. All CMOS signal timings (compatibility signals, etc.) are referenced at 1.25 V at the processor edge fingers.
5. All AC timings for the APIC I/O signals at the processor edge fingers are referenced to the PICCLK rising edge at: 0.7 V for S.E.P. and PPGA packages and 0.75 V for the FC-PGA package. All APIC I/O signal timings are referenced at 1.25 V for S.E.P. and PPGA packages and 0.75 V for the FC-PGA package at the processor edge fingers.
6. All AC timings for the TAP signals at the processor edge fingers are referenced to the TCK rising edge at 0.70 V for S.E.P. and PPGA packages and 0.75 V for the FC-PGA package. All TAP signal timings (TMS, TDI, etc.) are referenced at 1.25 V for S.E.P. and PPGA packages and 0.75 V for the FC-PGA package at the processor edge fingers.

Figure 2. BCLK to Core Logic Offset

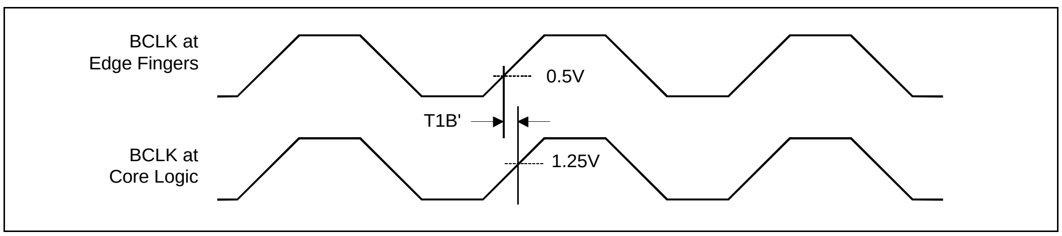
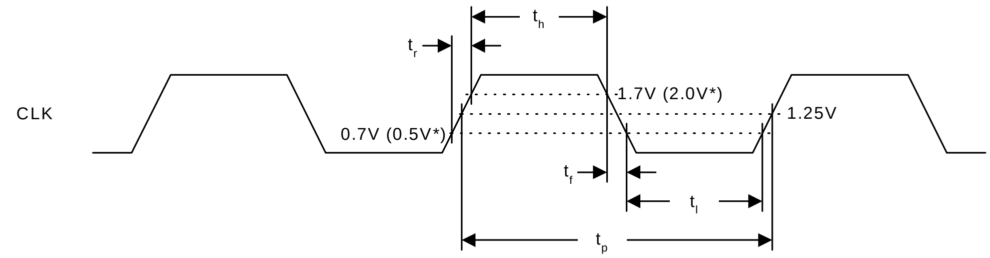


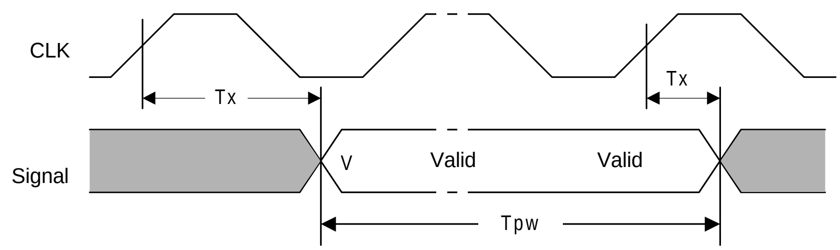
Figure 3. BCLK*, PICCLK, and TCK Generic Clock Waveform



T_r = T5, T25, T34 (Rise Time)
T_f = T6, T26, T35 (Fall Time)
T_h = T3, T23, T32 (High Time)
T_l = T4, T24, T33 (Low Time)
T_p = T1, T22, T31 (BLCK, TCK, PICCLK Period)

Note: BCLK is referenced to 0.5 V and 2.0 V. PICCLK is referenced to 0.7 V and 1.7 V.
For S.E.P. and PPGA packages, TCK is referenced to 0.7 V and 1.7 V.
For the FC-PGA package, TCK is referenced to V_{REF} ±200mV.

Figure 4. System Bus Valid Delay Timings

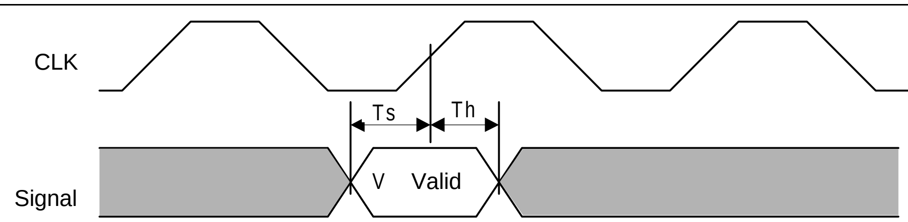


Tx = T7, T11, T29a, T29b (Valid Delay)

Tpw = T14, T14B, T15 (Pulse Width)

V = 1.0V for AGTL+ signal group;
For S.E.P and PPGA packages, 1.25V for CMOS, APIC and JTAG signal groups
For FC-PGA package, 0.75V for CMOS, APIC and TAP signal groups

Figure 5. System Bus Setup and Hold Timings



Ts = T8, T12, T27 (Setup Time)
Th = T9, T13, T28 (Hold Time)
V = 1.0V for AGTL+ signal group;
For S.E.P. and PPGA packages, 1.25V for APIC and JTAG signal groups
For the FC-PGA package, 0.75V for APIC and TAP signal groups

Figure 6. System Bus Reset and Configuration Timings (For the S.E.P. and PPGA Packages)

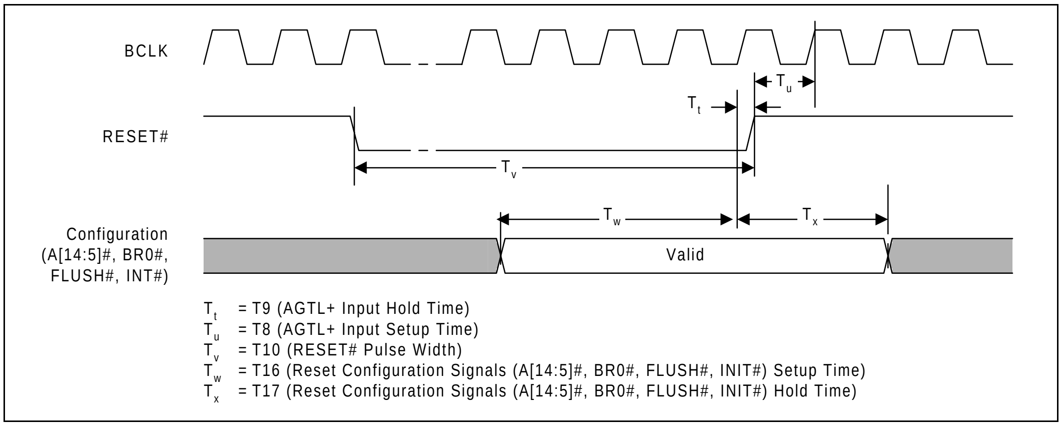


Figure 7. System Bus Reset and Configuration Timings (For the FC-PGA Package)

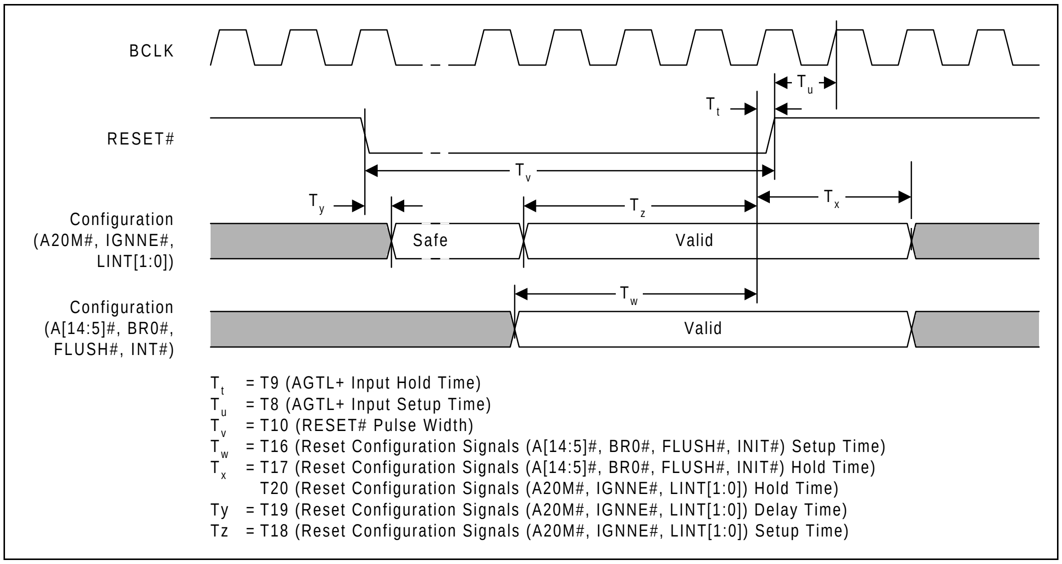
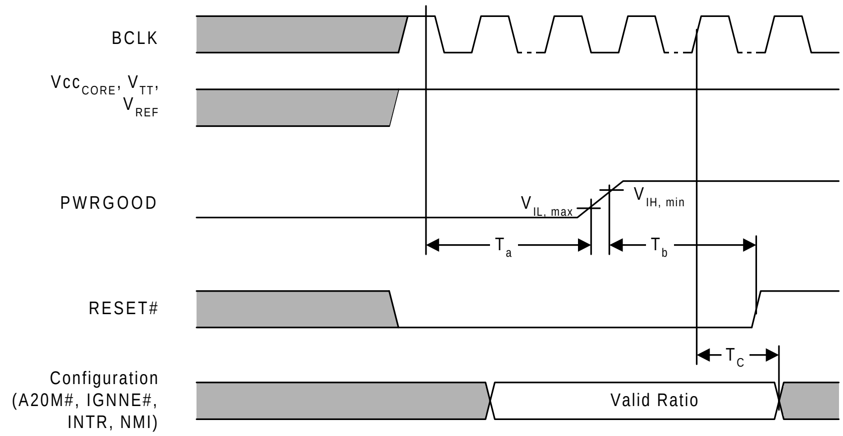
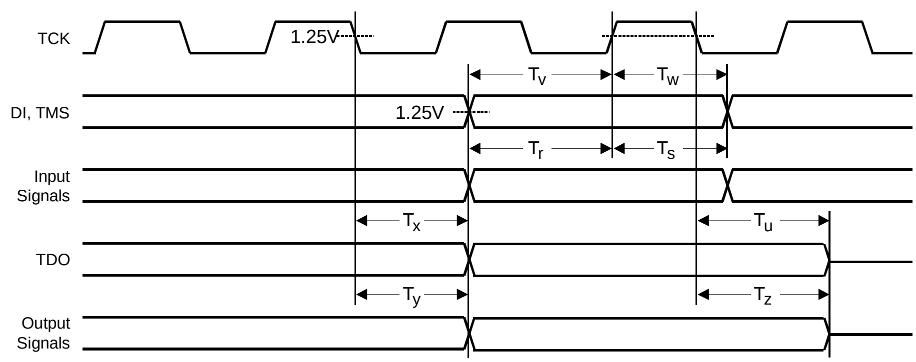


Figure 8. Power-On Reset and Configuration Timings



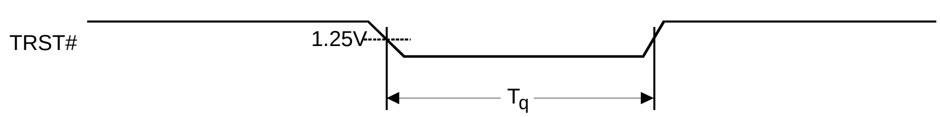
T_a = T15 (PWRGOOD Inactive Pulse)
T_b = T10 (RESET# Pulse Width)
T_c = T20 (Reset Configuration Signals (A20M#, IGNNE#, LINT[1:0]) Hold Time) (FC-PGA)

Figure 9. Test Timings (TAP Connection)



T_r = T43 (All Non-Test Inputs Setup Time)
T_s = T44 (All Non-Test Inputs Hold Time)
T_u = T40 (TDO Float Delay)
T_v = T37 (TDI, TMS Setup Time)
T_w = T38 (TDI, TMS Hold Time)
T_x = T39 (TDO Valid Delay)
T_y = T41 (All Non-Test Outputs Valid Delay)
T_z = T42 (All Non-Test Outputs Float Delay)

Figure 10. Test Reset Timings



T_q = T37 (TRST# Pulse Width)

3.0 System Bus Signal Simulations

Signals driven on the Celeron processor system bus should meet signal quality specifications to ensure that the components read data properly and to ensure that incoming signals do not affect the long term reliability of the component. Specifications are provided for simulation at the processor core; guidelines are provided for correlation to the processor edge fingers. These edge finger guidelines are intended for use during testing and measurement of system signal integrity. Violations of these guidelines are permitted, but if they occur, simulation of signal quality at the processor core should be performed to ensure that no violations of signal quality specifications occur. Meeting the specifications at the processor core in Table 28, Table 31, and Table 34 ensures that signal quality effects will not adversely affect processor operation, but does not necessarily guarantee that the guidelines in Table 30, Table 33, and Table 35 will be met.

3.1 System Bus Clock (BCLK) Signal Quality Specifications and Measurement Guidelines

Table 28 describes the BCLK signal quality specifications at the processor core for both S.E.P. and PPGA Packages. Table 29 shows the BCLK and PICCLK signal quality specifications at the processor core for the FC-PGA package. Table 30 describes guidelines for signal quality measurement at the processor edge fingers. Figure 11 describes the signal quality waveform for the system bus clock at the processor core pins; Figure 12 describes the signal quality waveform for the system bus clock at the processor edge fingers.

Table 28. BCLK Signal Quality Specifications for Simulation at the Processor Core (for Both S.E.P. and PPGA Packages)

T# Parameter	Min	Nom	Max	Unit	Figure	Notes
V1: BCLK V_{IL}			0.5	V	11	
V2: BCLK V_{IH}	2.0			V	11	2
V3: V_{IN} Absolute Voltage Range	–0.7		3.5	V	11	2
V4: Rising Edge Ringback	1.7			V	11	3
V5: Falling Edge Ringback			0.7	V	11	3

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Celeron processor frequencies.
2. This is the Intel Celeron processor system bus clock overshoot and undershoot specification for 66 MHz system bus operation.
3. The rising and falling edge ringback voltage specified is the minimum (rising) or maximum (falling) absolute voltage the BCLK signal can dip back to after passing the V_{IH} (rising) or V_{IL} (falling) voltage limits. This specification is an absolute value.

Table 29. BCLK/PICCLK Signal Quality Specifications for Simulation at the Processor Pins (for the FC-PGA Package)

T# Parameter	Min	Nom	Max	Unit	Figure	Notes
V1: BCLK V_{IL}			0.50	V	11	
V1: PICCLK V_{IL}			0.70	V	11	
V2: BCLK V_{IH}	2.00			V	11	
V2: PICCLK V_{IH}	2.00			V	11	
V3: V_{IN} Absolute Voltage Range	–0.58		3.18	V	11	
V4: BCLK Rising Edge Ringback	2.00			V	11	2
V4: PICCLK Rising Edge Ringback	2.00			V	11	2
V5: BCLK Falling Edge Ringback			0.50	V	11	2
V5: PICCLK Falling Edge Ringback			0.70	V	11	2

NOTES:
1. Unless otherwise noted, all specifications in this table apply to FC-PGA processors frequencies and cache sizes.
2. The rising and falling edge ringback voltage specified is the minimum (rising) or maximum (falling) absolute voltage the BCLK/PICCLK signal can dip back to after passing the V_{IH} (rising) or V_{IL} (falling) voltage limits. This specification is an absolute value.

Figure 11. BCLK, TCK, PICCLK Generic Clock Waveform at the Processor Core Pins

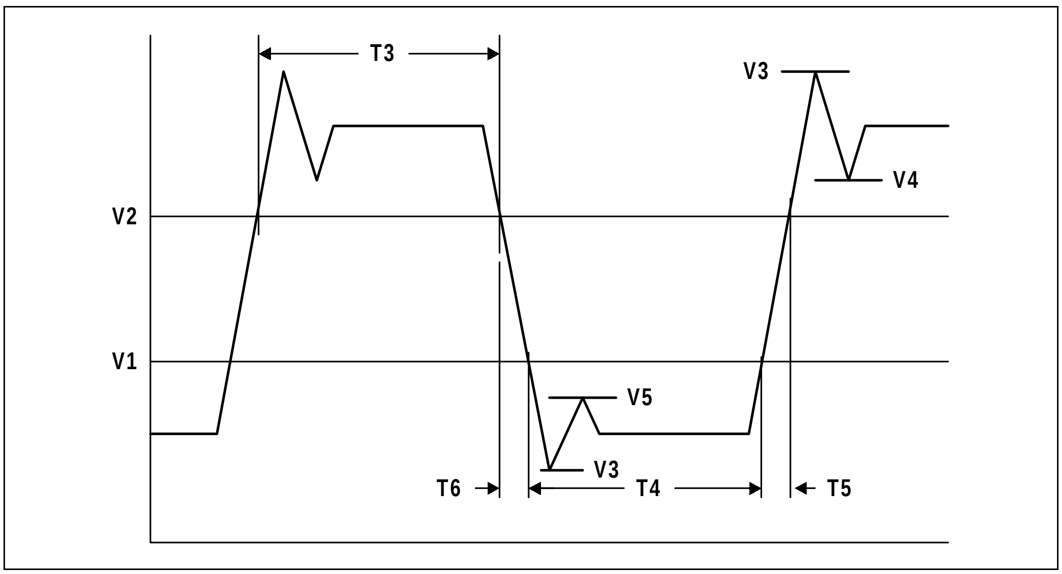
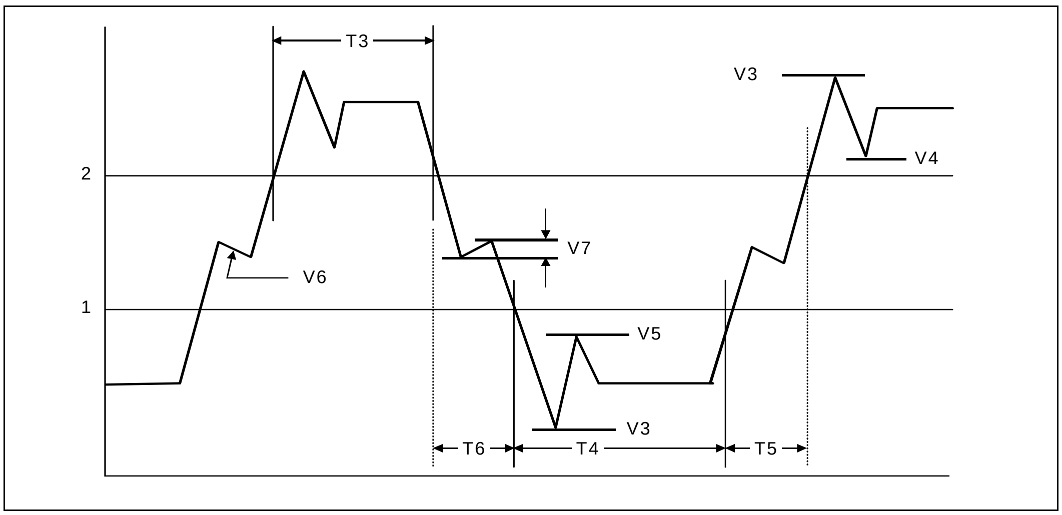


Table 30. BCLK Signal Quality Guidelines for Edge Finger Measurement (for the S.E.P. Package)

T# Parameter	Min	Nom	Max	Unit	Figure	Notes
V1’: BCLK V_{IL}			0.5	V	12	
V2’: BCLK V_{IH}	2.0			V	12	
V3’: VIN Absolute Voltage Range	–0.5		3.3	V	12	2
V4’: Rising Edge Ringback	2.0			V	12	3
V5’: Falling Edge Ringback			0.5	V	12	3
V6’: Tline Ledge Voltage	1.0		1.7	V	12	At Ledge Midpoint [4]
V7’: Tline Ledge Oscillation			0.2	V	12	Peak-to-Peak [5]

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Celeron processor frequencies.
2. This is the Intel Celeron processor system bus clock overshoot and undershoot measurement guideline.
3. The rising and falling edge ringback voltage guideline is the minimum (rising) or maximum (falling) absolute voltage the BCLK signal may dip back to after passing the V_{IH} (rising) or V_{IL} (falling) voltage limits. This guideline is an absolute value.
4. The BCLK at the processor edge fingers may have a dip or ledge midway on the rising or falling edge. The midpoint voltage level of this ledge should be within the range of the guideline.
5. The ledge (V7) is allowed to have peak-to-peak oscillation as given in the guideline.

Figure 12. BCLK, TCK, PICCLK Generic Clock Waveform at the Processor Edge Fingers



3.2 AGTL+ Signal Quality Specifications and Measurement Guidelines

Many scenarios have been simulated to generate a set of AGTL+ layout guidelines which are available in AP-585, *Pentium® II Processor AGTL+ Guidelines* (Order Number 243330). Refer to the *Pentium® II Processor Developer's Manual* (Order Number 243502) for the AGTL+ buffer specification.

Table 31 provides the AGTL+ signal quality specifications (for both the S.E.P. and PPGA Packages) for use in simulating signal quality at the processor core. Table 32 provides the AGTL+ signal quality specifications (for the FC-PGA Packages) for use in simulating signal quality at the processor core. Table 33 provides AGTL+ signal quality guidelines for measuring and testing signal quality at the processor edge fingers. Figure 13 describes the signal quality waveform for AGTL+ signals at the processor core and edge fingers. For more information on the AGTL+ interface, see the *Pentium® II Processor Developer's Manual* (Order Number 243502).

Table 31. AGTL+ Signal Groups Ringback Tolerance Specifications at the Processor Core (For Both the S.E.P. and PPGA Packages)

T# Parameter	Min	Unit	Figure	Notes
α: Overshoot	100	mV	13	4
τ: Minimum Time at High	1.00	ns	13	4
ρ: Amplitude of Ringback	–100	mV	13	4, 5
ϕ: Final Settling Voltage	100	mV	13	4
δ: Duration of Squarewave Ringback	N/A	ns	13	

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Celeron processor frequencies.
2. Specifications are for the edge rate of 0.3 – 0.8 V/ns. See Figure 13 for the generic waveform.
3. All values specified by design characterization.
4. This specification applies to Intel Celeron processors operating with a 66 MHz Intel Celeron processor system bus only.
5. Ringback below V_{REF} + 20 mV is not supported.

Table 32. AGTL+ Signal Groups Ringback Tolerance Specifications at the Processor Pins (For FC-PGA Packages)

T# Parameter	Min	Unit	Figure	Notes
α: Overshoot	100	mV	13	4, 8, 9, 10
τ: Minimum Time at High	0.50	ns	13	9
ρ: Amplitude of Ringback	–200	mV	13	5, 6, 7, 8
ϕ: Final Settling Voltage	200	mV	13	8
δ: Duration of Squarewave Ringback	N/A	ns	13	

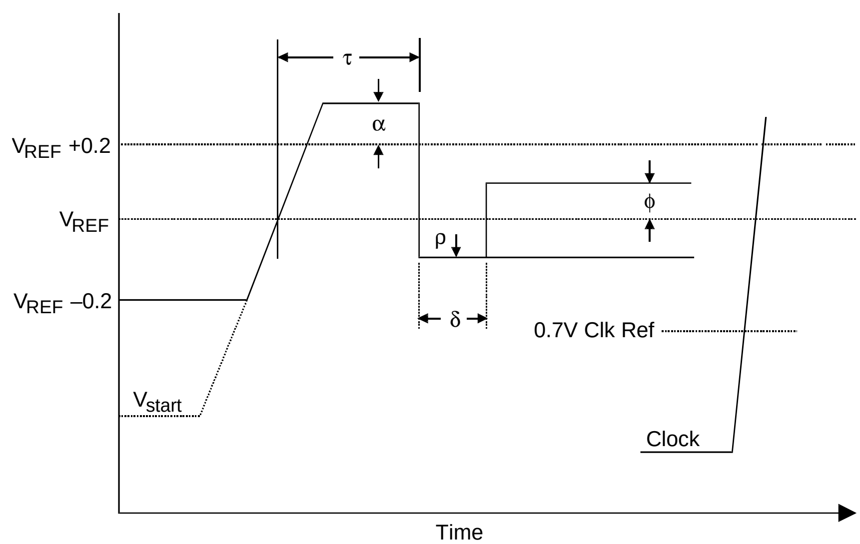
NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Celeron processor frequencies.
2. Specifications are for the edge rate of 0.3 – 0.8V/ns. See Figure 13 for the generic waveform.
3. All values specified by design characterization.
4. See Table 36 for maximum allowable overshoot.
5. Ringback between V_{REF} + 100 mV and V_{REF} + 200 mV or V_{REF} – 200 mV and V_{REF} – 100 mVs requires the flight time measurements to be adjusted as described in the Intel AGTL+ Specifications (*Intel®Pentium®II Developers Manual*). Ringback below V_{REF} + 100 mV or above V_{REF} – 100 mV is not supported.
6. Intel recommends simulations not exceed a ringback value of V_{REF} ±200 mV to allow margin for other sources of system noise.
7. A negative value for ρ indicates that the amplitude of ringback is above V_{REF}. (i.e., ϕ = –100 mV specifies the signal cannot ringback below V_{REF} + 100 mV).
8. ϕ and ρ: are measured relative to V_{REF}. α: is measured relative to V_{REF} + 200 mV.
9. All Ringback entering the Overdrive Region must have flight time correction.
10. Overshoot specifications for Ringback do not correspond to Overshoot specifications in Section 3.4.

Table 33. AGTL+ Signal Groups Ringback Tolerance Guidelines for Edge Finger Measurement on the S.E.P. Package

T# Parameter	Min	Unit	Figure	Notes
α': Overshoot	100	mV	13	
τ': Minimum Time at High	1.5	ns	13	4
ρ': Amplitude of Ringback	–250	mV	13	4, 5
φ': Final Settling Voltage	250	mV	13	4
δ': Duration of Squarewave Ringback	N/A	ns	13	

NOTES:
1. Unless otherwise noted, all guidelines in this table apply to all Celeron processor frequencies.
2. Guidelines are for the edge rate of 0.3 – 0.8 V/ns. See Figure 13 for the generic waveform.
3. All values specified by design characterization.
4. This guideline applies to Intel Celeron processors operating with a 66 MHz system bus only.
5. Ringback below VREF + 250 mV is not supported.

Figure 13. Low to High AGTL+ Receiver Ringback Tolerance

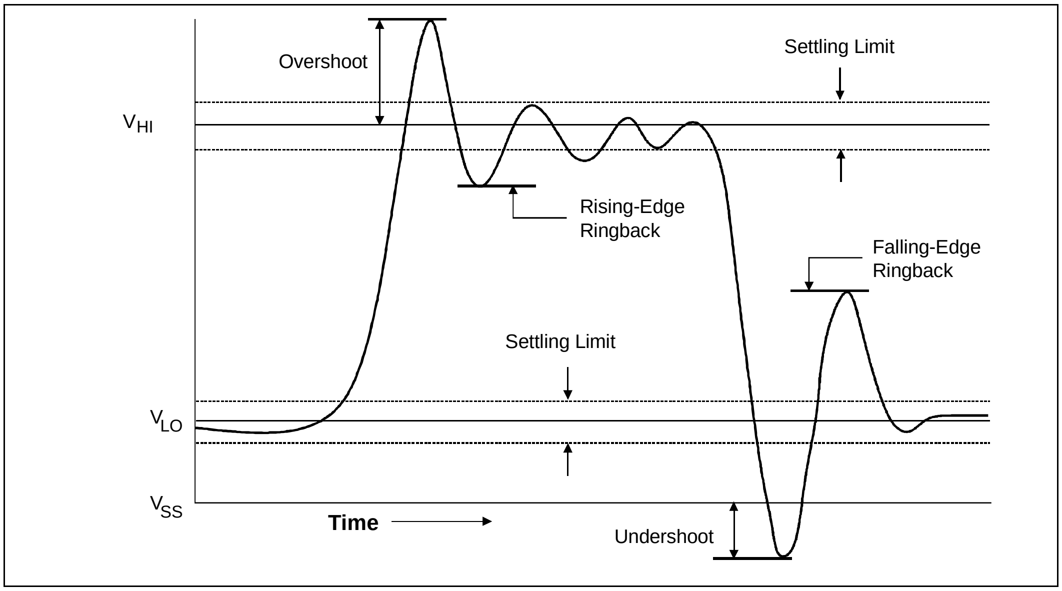


Note: High to Low case is analogous.

3.3 Non-AGTL+ Signal Quality Specifications and Measurement Guidelines

There are three signal quality parameters defined for non-AGTL+ signals: overshoot/undershoot, ringback, and settling limit. All three signal quality parameters are shown in Figure 14 for the non-AGTL+ signal group.

Figure 14. Non-AGTL+ Overshoot/Undershoot, Settling Limit, and Ringback



NOTES:

1. For the FC-PGA package, V_{HI} = 1.5V for all non-AGTL+ signals except for BCLK, PICCLK, and PWRGOOD. V_{HI} = 2.5 V for BCLK, PICCLK, and PWRGOOD. BCLK and PICCLK signal quality is detailed in Section 3.1.

3.3.1 Overshoot/Undershoot Guidelines

Overshoot (or undershoot) is the absolute value of the maximum voltage above the nominal high voltage or below VSS. The overshoot/undershoot guideline limits transitions beyond VCC or VSS due to the fast signal edge rates. (See Figure 14 for non-AGTL+ signals.) The processor can be damaged by repeated overshoot events on the voltage tolerant buffers if the charge is large enough (i.e., if the overshoot is great enough). The PPGA and S.E.P. packages have 2.5 V tolerant buffers and the FC-PGA package has 1.5 V or 2.5 V tolerant buffers.

However, excessive ringback is the dominant detrimental system timing effect resulting from overshoot/undershoot (i.e., violating the overshoot/undershoot guideline will make satisfying the ringback specification difficult). **The overshoot/undershoot guideline is 0.7 V for the PPGA and S.E.P. packages and 0.3 V for the FC-PGA package** and assumes the absence of diodes on the input. These guidelines should be verified in simulations **without the on-chip ESD protection diodes present** because the diodes will begin clamping the signals (2.5 V tolerant signals for the S.E.P. and PPGA packages, and 2.5 V or 1.5 V tolerant signals for the FC-PGA package) beginning at approximately 0.7 V above the appropriate supply and 0.7 V below VSS. If signals are not reaching the clamping voltage, this will not be an issue. A system should not rely on the diodes for overshoot/undershoot protection as this will negatively affect the life of the components and make meeting the ringback specification very difficult.

3.3.2 Ringback Specification

Ringback refers to the amount of reflection seen after a signal has switched. The ringback specification is **the voltage that the signal rings back to after achieving its maximum absolute value**. (See Figure 14 for an illustration of ringback.) Excessive ringback can cause false signal detection or extend the propagation delay. The ringback specification applies to the input pin of each receiving agent. Violations of the signal ringback specification are not allowed under any circumstances for non-AGTL+ signals.

Ringback can be simulated with or without the input protection diodes that can be added to the input buffer model. However, signals that reach the clamping voltage should be evaluated further. See Table 34 for the signal ringback specifications for non-AGTL+ signals for simulations at the processor core, and Table 35 for guidelines on measuring ringback at the edge fingers. Table 36 lists the ringback specifications for the FC-PGA package.

Table 34. Signal Ringback Specifications for Non-AGTL+ Signal Simulation at the Processor Core (S.E.P. and PPGA Packages)

Input Signal Group	Transition	Maximum Ringback (with Input Diodes Present)	Unit	Figure	Notes
Non-AGTL+ Signals	$0 \rightarrow 1$	1.7	V	14	
Non-AGTL+ Signals	$1 \rightarrow 0$	0.7	V	14	

NOTE:
1. Unless otherwise noted, all specifications in this table apply to all Celeron processor frequencies.

Table 35. Signal Ringback Guidelines for Non-AGTL+ Signal Edge Finger Measurement (S.E.P. Package)

Input Signal Group	Transition	Maximum Ringback (with Input Diodes Present)	Unit	Figure	Notes
Non-AGTL+ Signals	$0 \rightarrow 1$	2.0	V	14	
Non-AGTL+ Signals	$1 \rightarrow 0$	0.7	V	14	

NOTE:
1. Unless otherwise noted, all specifications in this table apply to all Celeron processor frequencies.

Table 36. Signal Ringback Specifications for Non-AGTL+ Signal Simulation at the Processor Pins (FC-PGA Package)

Input Signal Group	Transition	Maximum Ringback (with Input Diodes Present)	Unit	Figure
Non-AGTL+ Signals	$0 \rightarrow 1$	$V_{REF} + 0.200$	V	16
PWRGOOD	$0 \rightarrow 1$	2.0	V	16
Non-AGTL+ Signals	$1 \rightarrow 0$	$V_{REF} - 0.200$	V	16

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all FC-PGA processor frequencies and cache sizes.

3.3.3 Settling Limit Guideline

Settling limit defines the maximum amount of ringing at the receiving pin that a signal must reach before its next transition. The amount allowed is 10 percent of the total signal swing ($V_{HI} - V_{LO}$) above and below its final value. A signal should be within the settling limits of its final value, when either in its high state or low state, before it transitions again.

Signals that are not within their settling limit before transitioning are at risk of unwanted oscillations which could jeopardize signal integrity. Simulations to verify settling limit may be done either with or without the input protection diodes present. Violation of the settling limit guideline is acceptable if simulations of 5 to 10 successive transitions do not show the amplitude of the ringing increasing in the subsequent transitions.

3.4 AGTL+ Signal Quality Specifications and Measurement Guidelines (FC-PGA Package)

3.4.1 Overshoot/Undershoot Guidelines (FC-PGA Package)

Overshoot (or undershoot) is the absolute value of the maximum voltage above the nominal high voltage or below V_{SS}. The overshoot guideline limits transitions beyond V_{CC} or V_{SS} due to the fast signal edge rates. The processor can be damaged by repeated overshoot events on 1.5 V or 2.5 V tolerant buffers if the charge is large enough (i.e., if the overshoot is great enough). Determining the impact of an overshoot/undershoot condition requires knowledge of the magnitude, the pulse direction and the activity factor (AF). Permanent damage to the processor is the likely result of excessive overshoot/undershoot. Violating the overshoot/undershoot guideline will also make satisfying the ringback specification difficult.

When performing simulations to determine impact of overshoot and overshoot, ESD diodes must be properly characterized. ESD protection diodes do not act as voltage clamps and will not provide overshoot or undershoot protection. ESD diodes modeled within Intel I/O Buffer models do not clamp undershoot or overshoot and will yield correct simulation results. If other I/O buffer models are being used to characterize the FC-PGA processor performance, care must be taken to ensure that ESD models do not clamp extreme voltage levels. Intel I/O Buffer models also contain I/O capacitance characterization. Therefore, removing the ESD diodes from an I/O Buffer model will impact results and may yield excessive overshoot/undershoot.

3.4.2 Overshoot/Undershoot Magnitude (FC-PGA Package)

Magnitude describes the maximum potential difference between a signal and its voltage reference level, V_{SS} (overshoot) and V_{TT} (undershoot). While overshoot can be measured relative to V_{SS} using one probe (probe to signal and GND lead to V_{SS}), undershoot must be measured relative to V_{TT}. This can be accomplished by simultaneously measuring the V_{TT} plane while measuring the signal undershoot. Today's oscilloscopes can easily calculate the true undershoot waveform using a Math function where the Signal waveform is subtracted from the V_{TT} waveform. The true undershoot waveform can also be obtained with the following oscilloscope data file analysis:

$$\text{Converted Undershoot Waveform} = V_{TT} - \text{Signal\_measured}$$

Note: The converted undershoot waveform appears as a positive (overshoot) signal.

Note: Overshoot (rising edge) and undershoot (falling edge) conditions are separate and their impact must be determined independently.

After the true waveform conversion, the undershoot/overshoot specifications shown in Table 38 and Table 39 can be applied to the converted undershoot waveform using the same magnitude and pulse duration specifications used with an overshoot waveform.

Overshoot/undershoot magnitude levels must observe the Absolute Maximum Specifications listed in Table 38 and Table 39. These specifications must not be violated at any time regardless of bus activity or system state. Within these specifications are threshold levels that define different allowed pulse durations. Provided that the magnitude of the overshoot/undershoot is within the Absolute Maximum Specifications (2.18V), the pulse magnitude, duration and activity factor must all be used to determine if the overshoot/undershoot pulse is within specifications.

3.4.3 Overshoot/Undershoot Pulse Duration (FC-PGA Package)

Pulse duration describes the total time an overshoot/undershoot event exceeds the overshoot/undershoot reference voltage (V_{os_ref} = 1.635V). The total time could encompass several oscillations above the reference voltage. Multiple overshoot/undershoot pulses within a single overshoot/undershoot event may need to be measured to determine the total pulse duration.

Note: Oscillations below the reference voltage can not be subtracted from the total overshoot/undershoot pulse duration.

Note: Multiple Overshoot/Undershoot events occurring within the same clock cycle must be considered together as one event. Using the worst case Overshoot/Undershoot Magnitude, sum together the individual Pulse Durations to determine the total Overshoot/Undershoot Pulse Duration for that total event.

3.4.4 Activity Factor (FC-PGA Package)

Activity Factor (AF) describes the frequency of overshoot (or undershoot) occurrence relative to a clock. Since the highest frequency of assertion of an AGTL+ or a CMOS signal is every other clock, an AF = 1 indicates that the specific overshoot (or undershoot) waveform occurs EVERY OTHER clock cycle. Thus, an AF = 0.01 indicates that the specific overshoot (or undershoot) waveform occurs one time in every 200 clock cycles.

The specifications provided in Table 38 and Table 39 show the Maximum Pulse Duration allowed for a given Overshoot/Undershoot Magnitude at a specific Activity Factor. Each table entry is independent of all others, meaning that the Pulse Duration reflects the existence of overshoot/undershoot events of that magnitude ONLY. A platform with an overshoot/undershoot that just meets the pulse duration for a specific magnitude where the AF < 1, means that there can be NO other overshoot/undershoot events, even of lesser magnitude (note that if AF = 1, then the event occurs at all times and no other events can occur).

Note: Activity factor for AGTL+ signals is referenced to BCLK frequency.

Note: Activity factor for CMOS signals is referenced to PICCLK frequency.

3.4.5 Reading Overshoot/Undershoot Specification Tables (FC-PGA Package)

The overshoot/undershoot specification for the FC-PGA package processor is not a simple single value. Instead, many factors are needed to determine the over/undershoot specification. In addition to the magnitude of the overshoot, the following parameters must also be known: the junction temperature the processor will be operating, the width of the overshoot (as measured above 1.635 V) and the Activity Factor (AF). To determine the allowed overshoot for a particular overshoot event, the following must be done:

1. Determine the signal group that particular signal falls into. If the signal is an AGTL+ signal operating with a 66 MHz system bus, use Table 38 (66 MHz AGTL+ signal group). If the signal is a CMOS signal, use Table 39 (33 MHz CMOS signal group).
2. Determine the maximum junction temperature (Tj) for the range of processors that the system will support (80°C or 90°C).
3. Determine the Magnitude of the overshoot (relative to Vss)
4. Determine the Activity Factor (how often does this overshoot occur?)
5. From the appropriate Specification table, read off the Maximum Pulse Duration (in ns) allowed.
6. Compare the specified Maximum Pulse Duration to the signal being measured. If the Pulse Duration measured is less than the Pulse Duration shown in the table, then the signal meets the specifications.

The above procedure is similar for undershoots after the undershoot waveform has been converted to look like an overshoot. Undershoot events must be analyzed separately from Overshoot events as they are mutually exclusive.

Table 37 shows an example of how the maximum pulse duration is determined for a given waveform.

Table 37. Example Platform Information

Required Information	Maximum Platform Support	Notes
FSB Signal Group	66 MHz AGTL+	
Max Tj	90 °C	
Overshoot Magnitude	2.13V	Measured Value
Activity Factor (AF)	0.1	Measured overshoot occurs on average every 20 clocks

NOTES:
1. Corresponding Maximum Pulse Duration Specification – 3.2 ns
2. Pulse Duration (measured) – 2.0 ns

Given the above parameters, and using Table 38 (90°C/AF=0.1 column) the maximum allowed pulse duration is 3.2 ns. Since the measured pulse duration is 2.0ns, this particular overshoot event passes the overshoot specifications, although this doesn't guarantee that the combined overshoot/ undershoot events meet the specifications.

3.4.6 Determining if a System meets the Overshoot/Undershoot Specifications (FC-PGA Package)

The overshoot/undershoot specifications listed in the following tables specify the allowable overshoot/undershoot for a single overshoot/undershoot event. However most systems will have multiple overshoot and/or undershoot events that each have their own set of parameters (duration, AF and magnitude). While each overshoot on its own may meet the overshoot specification, when the total impact of all overshoot events is accounted for, the system may fail. A guideline to ensure a system passes the overshoot and undershoot specifications is shown below. It is important to meet these guidelines; otherwise, contact your Intel field representative.

1. Insure no signal (CMOS or AGTL+) ever exceed the 1.635V; OR
2. If only one overshoot/undershoot event magnitude occurs, ensure it meets the over/undershoot specifications in the following tables; OR
3. If multiple overshoots and/or multiple undershoots occur, measure the worst case pulse duration for each magnitude and compare the results against the AF = 1 specifications. If all of these worst case overshoot or undershoot events meet the specifications (measured time < specifications) in the table (where AF=1), then the system passes.

The following notes apply to Table 38 and Table 39.

NOTES:
1. Overshoot/Undershoot Magnitude = 2.18V is an Absolute value and should never be exceeded
2. Overshoot is measured relative to V_{SS}
3. Undershoot is measured relative to V_{TT}
4. Overshoot/Undershoot Pulse Duration is measured relative to 1.635V.
5. Ringbacks below V_{TT} can not be subtracted from Overshoots/Undershoots.
6. Lesser Undershoot does not allocate longer or larger Overshoot.
7. Consult the appropriate layout guidelines provided in the specific platform design guide.
8. All values specified by design characterization.

Table 38. 66 MHz AGTL+ Signal Group Overshoot/Undershoot Tolerance at Processor Pins (FC-PGA Package)

Overshoot/ Undershoot Magnitude	Maximum Pulse Duration at Tj = 80 °C (ns)			Maximum Pulse Duration at Tj = 90 °C (ns)		
	AF = 0.01	AF = 0.1	AF = 1	AF = 0.01	AF = 0.1	AF = 1
2.18 V	30	3.8	0.38	18	1.8	0.18
2.13 V	30	7.4	0.74	30	3.2	0.32
2.08 V	30	13.6	1.36	30	6.4	0.64
2.03 V	30	25	2.5	30	12	1.1
1.98 V	30	30	4.56	30	22	2
1.93 V	30	30	8.2	30	30	3.8
1.88 V	30	30	15	30	30	6.8

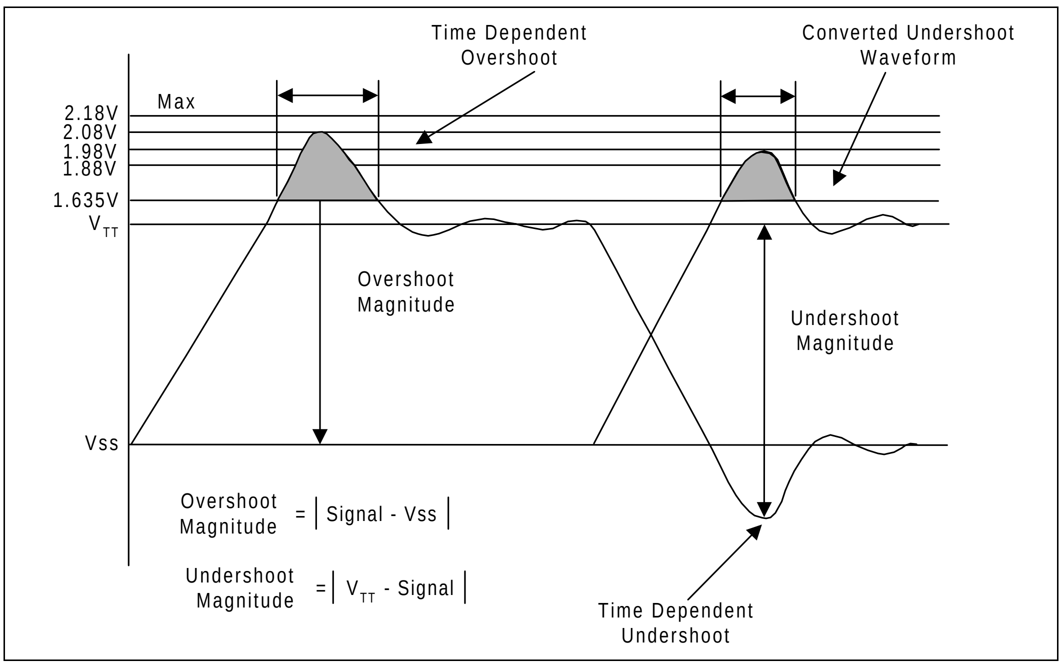
NOTES:
1. BCLK period is 30.0 ns.
2. Measurements taken at the processor socket pins on the solder-side of the motherboard.

Table 39. 33 MHz CMOS Signal Group Overshoot/Undershoot Tolerance at Processor Pins (FC-PGA Package)

Overshoot/ Undershoot Magnitude	Maximum Pulse Duration at Tj = 80 °C (ns)			Maximum Pulse Duration at Tj = 90 °C (ns)		
	AF = 0.01	AF = 0.1	AF = 1	AF = 0.01	AF = 0.1	AF = 1
2.18 V	60	7.6	0.76	36	3.6	0.36
2.13 V	60	14.8	1.48	60	6.4	0.64
2.08 V	60	27.2	2.7	60	12.8	1.2
2.03 V	60	50	5	60	24	2.2
1.98 V	60	60	9.1	60	44	4
1.93 V	60	60	16.4	60	60	7.6
1.88 V	60	60	30	60	60	13.6

NOTES:
1. PICCLK period is 30 ns.
2. Measurements taken at the processor socket pins on the solder-side of the motherboard.

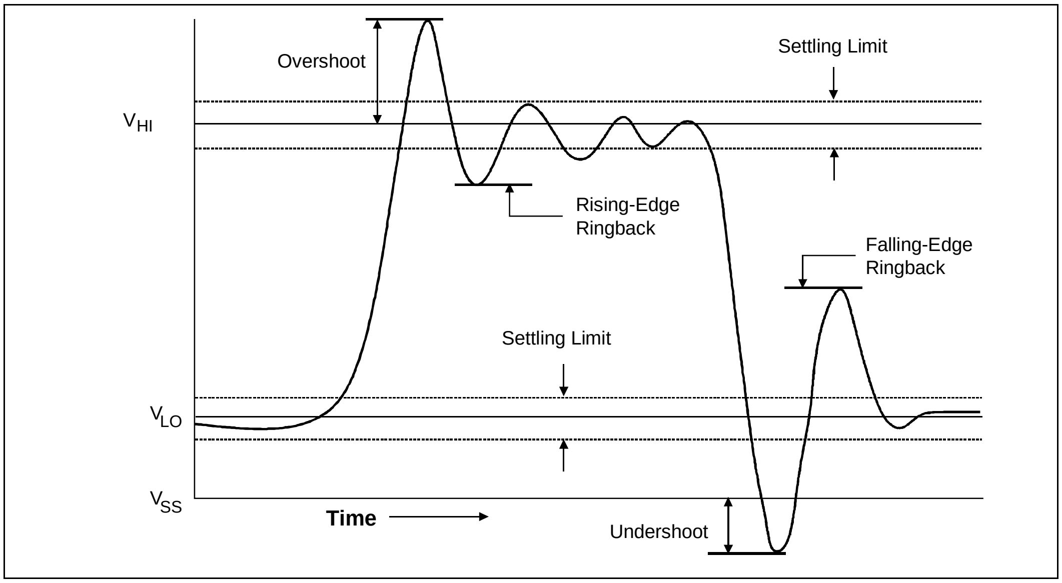
Figure 15. Maximum Acceptable AGTL+ Overshoot/Undershoot Waveform (FC-PGA Package)



3.5 Non-AGTL+ Signal Quality Specifications and Measurement Guidelines

There are three signal quality parameters defined for non-AGTL+ signals: overshoot/undershoot, ringback, and settling limit. All three signal quality parameters are shown in Figure 16 for the non-AGTL+ signal group.

Figure 16. Non-AGTL+ Overshoot/Undershoot, Settling Limit, and Ringback [1]



NOTES:

1. V_{HI} = 1.5V for all non-AGTL+ signals except for BCLK, PICCLK, and PWRGOOD. V_{HI} = 2.5 V for BCLK, PICCLK, and PWRGOOD. BCLK and PICCLK signal quality is detailed in Section 3.1.

4.0 Thermal Specifications and Design Considerations

This section provides needed data for designing a thermal solution. However, for the correct thermal measuring processes, refer to AP-905, *Intel® Pentium® III Processor Thermal Design Guidelines* (Order Number 245087). For the FC-PGA using flip chip pin grid array packaging technology, Intel specifies the **junction** temperature ($T_{junction}$). For the S.E.P. package and PPGA package, Intel specifies the **case** temperature (T_{case}).

4.1 Thermal Specifications

Table 40 provides both the Processor Power and Heatsink Design Target for Celeron processors. Processor Power is defined as the total power dissipated by the processor core and its package. Therefore, the S.E.P. Package's Processor Power would also include power dissipated by the AGTL+ termination resistors. The overall system chassis thermal design must comprehend the entire Processor Power. The Heatsink Design Target consists of only the processor core, which dissipates the majority of the thermal power.

Systems should design for the highest possible thermal power, even if a processor with a lower thermal dissipation is planned. The processor's heatslug is the attach location for all thermal solutions. The maximum and minimum case temperatures are also specified in Table 40. A thermal solution should be designed to ensure the temperature of the case never exceeds these specifications. Refer to the Intel developer Web site at http://developer.intel.com for more information.

Table 40. Processor Power for the PPGA and FC-PGA Packages

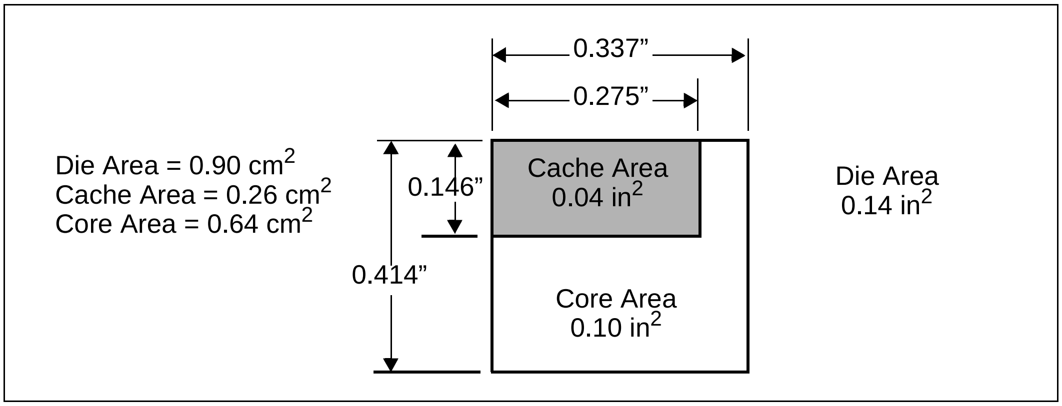
Processor Core Frequency	L2 Cache Size (KB)	Processor Thermal Design Power[2,3] (W) up to CPUID 0686h	Processor Thermal Design Power[2,3] (W) for CPUID 068Ah	Power Density[5] (W/cm^2) For CPUID 0686h	Power Density[5] (W/cm^2) For CPUID 068Ah	Min T_{CASE} (°C)	Max T_{CASE} (°C)	Max[10] $T_{JUNCTION}$ (°C)	$T_{JUNCTION}$ Offset[6] (°C)
333 MHz	128	19.7	NA	NA	NA	5	85	NA	NA
366 MHz	128	21.7	NA	NA	NA	5	85	NA	NA
400 MHz	128	23.7	NA	NA	NA	5	85	NA	NA
433 MHz	128	24.1	NA	NA	NA	5	85	NA	NA
466 MHz	128	25.6	NA	NA	NA	5	70	NA	NA
500 MHz	128	27.0	NA	NA	NA	5	70	NA	NA
533 MHz	128	28.3	NA	NA	NA	5	70	NA	NA
533A[3] MHz	128	14.0[4,7]	NA	17.5[4]	NA	NA	NA	90	2.6
566[3] MHz	128	14.9[4,8]	NA	18.5[4]	NA	NA	NA	90	2.6
600[3] MHz	128	15.8[4,9]	19.6[4]	19.7[4]	30.5[4]	NA	NA	90	2.6
633 MHz	128	16.5[4]	20.2[4]	25.8[4]	31.5[4]	NA	NA	82	2.6
667 MHz	128	17.5[4]	21.1[4]	27.3[4]	32.9[4]	NA	NA	82	2.6
700 MHz	128	18.3[4]	21.9[4]	28.6[4]	34.1[4]	NA	NA	80	2.7
733 MHz	128	19.1[4]	22.8[4]	29.8[4]	35.5[4]	NA	NA	80	2.8
766 MHz	128	20.0[4]	23.6[4]	31.3[4]	36.8[4]	NA	NA	80	3.0
800 MHz	128	20.8[4]	24.5[4]	32.6[4]	38.2[4]	NA	NA	80	3.0
850 MHz	128	22.5[4]	25.7[4]	35.2[4]	40.0[4]	NA	NA	80	3.3
900 MHz	128	NA	26.7[4]	NA	41.6[4]	NA	NA	77	3.6
950 MHz	128	NA	28.0	NA	43.6[4]	NA	NA	79	3.8
1 GHz	128	NA	29.0	NA	45.2[4]	NA	NA	75	3.8
1.10 GHz	128	NA	33.0	NA	51.4[4]	NA	NA	77	4.4

NOTES:

1. These values are specified at nominal $V_{CC_{CORE}}$ for the processor core.
2. Thermal Design Power (TDP) represents the maximum amount of power the thermal solution is required to dissipate. The thermal solution should be designed to dissipate the TDP power without exceeding the maximum $T_{JUNCTION}$ specification.
3. FC-PGA package only.
4. The Thermal Design Power (TDP) Celeron™ processors in production has been redefined. The updated TDP values are based on device characterization and do not reflect any silicon design changes to lower processor power consumption. The TDP values represent the thermal design point required to cool Celeron™ processors in the platform environment while executing thermal validation type software.
5. Power density is the maximum power the processor die can dissipate (i.e., processor power) divided by the die area over which the power is generated. Power for these processors is generated from the core area shown in Figure 17.
6. $T_{junctionoffset}$ is the worst-case difference between the thermal reading from the on-die thermal diode and the hottest location on the processor's core. $T_{junctionoffset}$ values do not include any thermal diode kit measurement error. Diode kit measurement error must be added to the $T_{junctionoffset}$ value from the table. Intel has characterized the use of the Analog Devices AD1021 diode measurement kit and found its measurement error to be ±1 ^{o}C.
7. For processors with a CPUID of 0683h, the TDP number is 11.2 W.
8. For processors with a CPUID of 0683h, the TDP number is 11.9 W.
9. For processors with a CPUID of 0683h, the TDP number is 12.6 W.
10. The Tj min for processors with a CPUID of 068x is 0 ^{o}C with a 3 ^{o}C– 5 ^{o}C margin error.

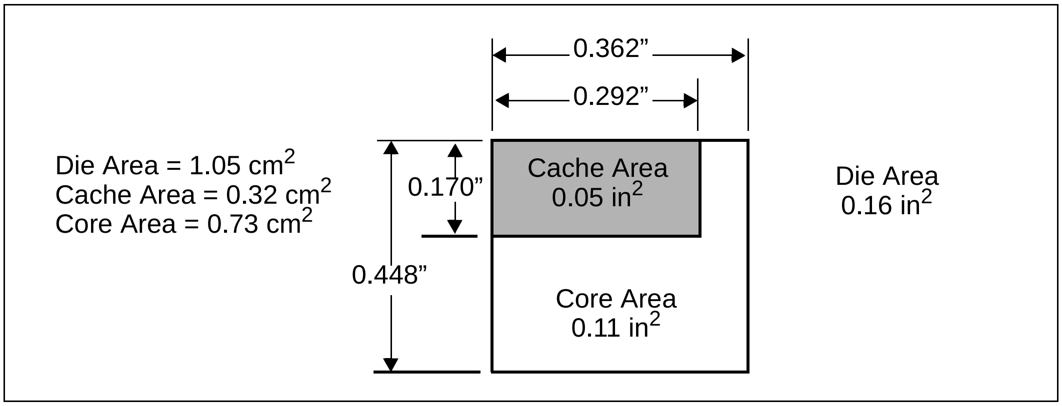
Figure 17 is a block diagram of the Intel Celeron FC-PGA processor die layout. The layout differentiates the processor core from the cache die area. In effect, the thermal design power identified in Table 40 is dissipated entirely from the processor core area. Thermal solution designs should compensate for this smaller heat flux area and not assume that the power is uniformly distributed across the entire die area.

Figure 17. Processor Functional Die Layout (CPUID 0686h)(1)



1. For CPUID 0x68A, the die area is 0.94 cm^2, the cache area is 0.30 cm^2, and the core area is 0.64 cm^2.

Figure 18. Processor Functional Die Layout (up to CPUID 0683h)



4.1.1 Thermal Diode

The Celeron processor incorporates an on-die diode that can be used to monitor the die temperature. A thermal sensor located on the motherboard or a standalone measurement kit may monitor the die temperature of the Intel Celeron processor for thermal management purposes. Table 41 to Table 43 provide the diode parameter and interface specifications.

Note: The reading of the thermal sensor connected to the thermal diode will not necessarily reflect the temperature of the hottest location on the die. This is due to inaccuracies in the thermal sensor, on-die temperature gradients between the location of the thermal diode and the hottest location on the die at a given point in time, and time based variations in the die temperature measurement. Time based variations can occur when the sampling rate of the thermal diode (by the thermal sensor) is slower than the rate at which the $T_{junction}$ temperature can change.

Table 41. Thermal Diode Parameters (S.E.P. and PPGA Packages)

Symbol	Min	Typ	Max	Unit	Notes
$I_{forward\ bias}$	5		500	uA	1
n_ideality	1.0000	1.0065	1.0173		2,3

NOTES:
1. Intel does not support or recommend operation of the thermal diode under reverse bias.
2. At room temperature with a forward bias of 630 mV.
3. n_ideality is the diode ideality factor parameter, as represented by the diode equation: I-Io(e (Vd*q)/(nkT) – 1).
4. Not 100% tested. Specified by design characterization.

Table 42. Thermal Diode Parameters (FC-PGA Package)

Symbol	Min	Typ	Max	Unit	Notes
$I_{forward\ bias}$	5		300	uA	1
n_ideality	1.0057	1.0080	1.0125		2, 3

NOTES:
1. Intel does not support or recommend operation of the thermal diode under reverse bias.
2. Characterized at 100° C with a forward bias current of 5–300 µA.
3. The ideality factor, n, represents the deviation from ideal diode behavior as exemplified by the diode equation:
   I_{fw}=Is(e^ ((Vd*q)/(nkT)) – 1), where Is = saturation current, q = electronic charge, Vd = voltage across the diode, k = Boltzmann Constant, and T = absolute temperature (Kelvin).
4. Not 100% tested. Specified by design characterization.

Table 43. Thermal Diode Interface

Pin Name	SC242 Connector Signal #	370-Pin Socket Pin #	Pin Description
THERMDP	B14	AL31	diode anode (p junction)
THERMDN	B15	AL29	diode cathode (n junction)

5.0 Mechanical Specifications

There are three package technologies which Celeron processors use. They are the S.E.P. Package, the PPGA package, and the FC-PGA package. The S.E.P. Package and FC-PGA package contain the processor core and passive components, while the PPGA package does not have passive components.

The processor edge connector defined in this document is referred to as the “SC242 connector.” See the *SC242 Design Guidelines* (Order Number 243397) for further details on the edge connector.

The processor socket connector is defined in this document is referred to as the “370-pin socket.” See the *370-Pin Socket (PGA370) Design Guidelines* (Order Number 244410) for further details on the socket.

5.1 S.E.P. Package

This section defines the mechanical specifications and signal definitions for the Celeron processor in the S.E.P. Package.

5.1.1 Materials Information

The Celeron processor requires a retention mechanism. This retention mechanism may require motherboard holes to be 0.159" diameter if low cost plastic fasteners are used to secure the retention mechanisms. The larger diameter holes are necessary to provide a robust structural design that can shock and vibe testing. If captive nuts are used in place of the plastic fasteners, then either the 0.159" or the 0.140" diameter holes will suffice as long as the attach mount is used.

Figure 19 with substrate dimensions is provided to aid in the design of a heatsink and clip. In Figure 20 all area on the secondary side of the substrate is zoned “keepout”, except for 25 mils around the tooling holes and the top and side edges of the substrate.

Figure 19. Processor Substrate Dimensions (S.E.P. Package)

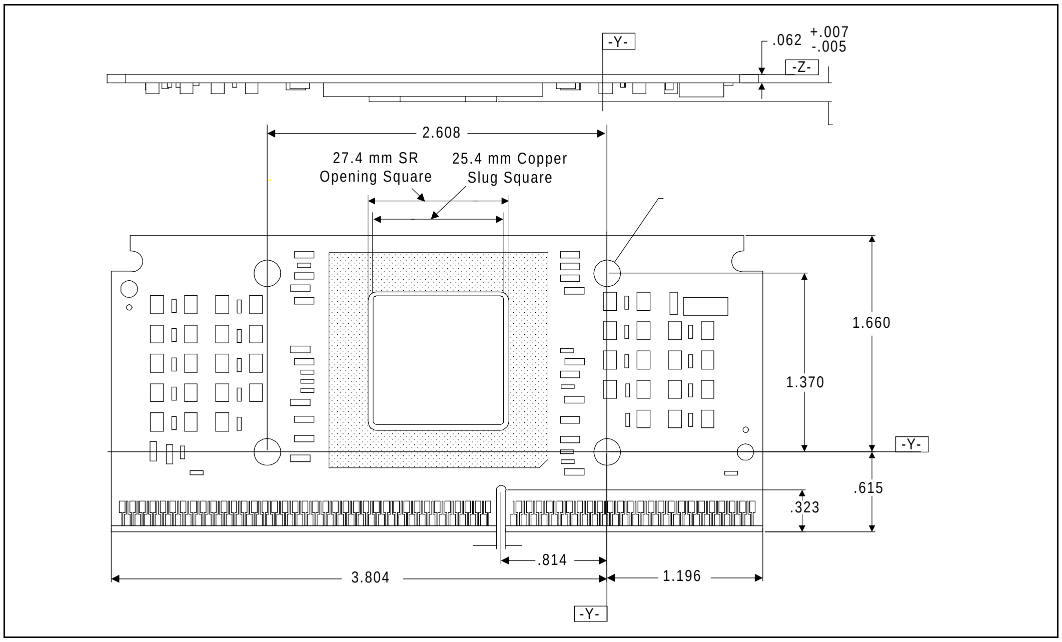
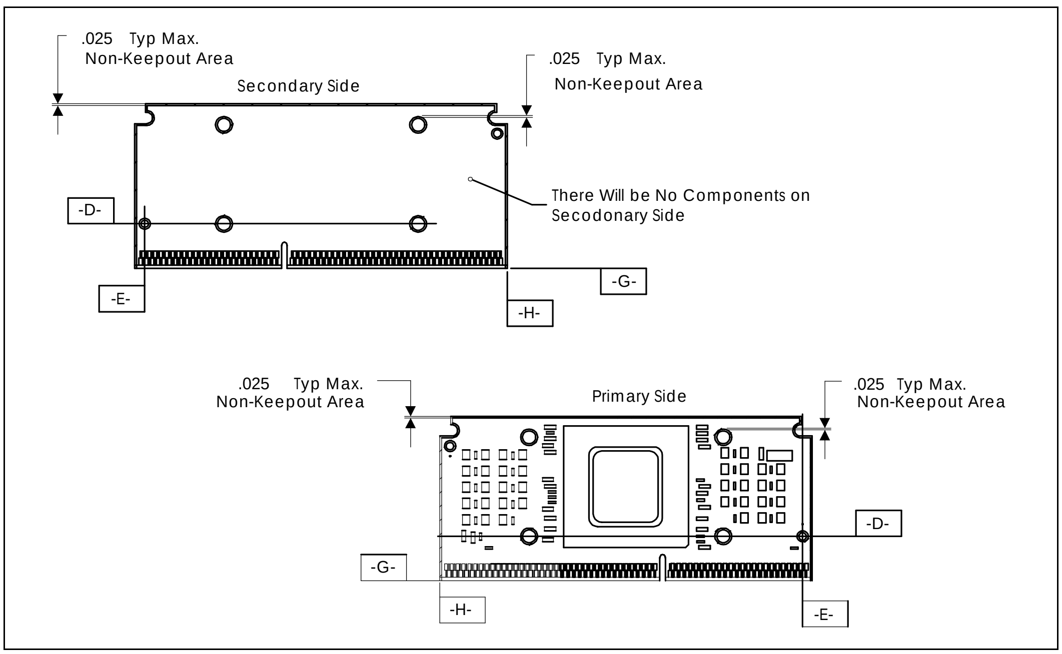


Figure 20. Processor Substrate Primary/Secondary Side Dimensions (S.E.P. Package)



5.1.2 Signal Listing (S.E.P. Package)

Table 44 and Table 45 provide the processor edge finger and SC242 connector signal definitions for Celeron processor. The signal locations on the SC242 edge connector are to be used for signal routing, simulation, and component placement on the motherboard.

Table 44. S.E.P. Package Signal Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type
A1	VTT	Power/Other
A2	Vss	Power/Other
A3	VTT	Power/Other
A4	IERR#	CMOS Output
A5	A20M#	CMOS Input
A6	Vss	Power/Other
A7	FERR#	CMOS Output
A8	IGNNE#	CMOS Input
A9	TDI	TAP Input
A10	Vss	Power/Other
A11	TDO	TAP Output
A12	PWRGOOD	CMOS Input
A13	TESTHI	CMOS Test Input
A14	Vss	Power/Other
A15	THERMTRIP#	CMOS Output
A16	Reserved	Reserved for Future Use
A17	LINT0/INTR	CMOS Input
A18	Vss	Power/Other
A19	PICD0	APIC I/O
A20	PREQ#	CMOS Input
A21	BP3#	AGTL+ I/O
A22	Vss	Power/Other
A23	BPM0#	AGTL+ I/O
A24	Reserved	Reserved for Pentium II processor
A25	Reserved	Reserved for Pentium II processor
A26	Vss	Power/Other
A27	Reserved	Reserved for Pentium II processor
A28	Reserved	Reserved for Pentium II processor
A29	Reserved	Reserved for Pentium II processor
A30	Vss	Power/Other
A31	Reserved	Reserved for Pentium II processor
A32	D61#	AGTL+ I/O
A33	D55#	AGTL+ I/O
A34	Vss	Power/Other
A35	D60#	AGTL+ I/O
A36	D53#	AGTL+ I/O

Table 44. S.E.P. Package Signal Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type
A37	D57#	AGTL+ I/O
A38	Vss	Power/Other
A39	D46#	AGTL+ I/O
A40	D49#	AGTL+ I/O
A41	D51#	AGTL+ I/O
A42	Vss	Power/Other
A43	D42#	AGTL+ I/O
A44	D45#	AGTL+ I/O
A45	D39#	AGTL+ I/O
A46	Vss	Power/Other
A47	Reserved	Reserved for Future Use
A48	D43#	AGTL+ I/O
A49	D37#	AGTL+ I/O
A50	Vss	Power/Other
A51	D33#	AGTL+ I/O
A52	D35#	AGTL+ I/O
A53	D31#	AGTL+ I/O
A54	Vss	Power/Other
A55	D30#	AGTL+ I/O
A56	D27#	AGTL+ I/O
A57	D24#	AGTL+ I/O
A58	Vss	Power/Other
A59	D23#	AGTL+ I/O
A60	D21#	AGTL+ I/O
A61	D16#	AGTL+ I/O
A62	Vss	Power/Other
A63	D13#	AGTL+ I/O
A64	D11#	AGTL+ I/O
A65	D10#	AGTL+ I/O
A66	Vss	Power/Other
A67	D14#	AGTL+ I/O
A68	D9#	AGTL+ I/O
A69	D8#	AGTL+ I/O
A70	Vss	Power/Other
A71	D5#	AGTL+ I/O
A72	D3#	AGTL+ I/O
A73	D1#	AGTL+ I/O
A74	Vss	Power/Other
A75	BCLK	System Bus Clock Input
A76	Reserved	Reserved for Pentium II processor

Table 44. S.E.P. Package Signal Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type
A77	Reserved	Reserved for Pentium II processor
A78	Vss	Power/Other
A79	Reserved	Reserved for Pentium II processor
A80	Reserved	Reserved for Pentium II processor
A81	A30#	AGTL+ I/O
A82	Vss	Power/Other
A83	A31#	AGTL+ I/O
A84	A27#	AGTL+ I/O
A85	A22#	AGTL+ I/O
A86	Vss	Power/Other
A87	A23#	AGTL+ I/O
A88	Reserved	Reserved for Future Use
A89	A19#	AGTL+ I/O
A90	Vss	Power/Other
A91	A18#	AGTL+ I/O
A92	A16#	AGTL+ I/O
A93	A13#	AGTL+ I/O
A94	Vss	Power/Other
A95	A14#	AGTL+ I/O
A96	A10#	AGTL+ I/O
A97	A5#	AGTL+ I/O
A98	Vss	Power/Other
A99	A9#	AGTL+ I/O
A100	A4#	AGTL+ I/O
A101	BNR#	AGTL+ I/O
A102	Vss	Power/Other
A103	BPRI#	AGTL+ Input
A104	TRDY#	AGTL+ Input
A105	DEFER#	AGTL+ Input
A106	Vss	Power/Other
A107	REQ2#	AGTL+ I/O
A108	REQ3#	AGTL+ I/O
A109	HITM#	AGTL+ I/O
A110	Vss	Power/Other
A111	DBSY#	AGTL+ I/O
A112	RS1#	AGTL+ Input
A113	Reserved	Reserved for Future Use
A114	Vss	Power/Other

Table 44. S.E.P. Package Signal Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type
A115	ADS#	AGTL+ I/O
A116	Reserved	Reserved for Future Use
A117	Reserved	Reserved for Pentium II processor
A118	Vss	Power/Other
A119	VID2	Power/Other
A120	VID1	Power/Other
A121	VID4	Power/Other
B1	EMI	Power/Other
B2	FLUSH#	CMOS Input
B3	SMI#	CMOS Input
B4	INIT#	CMOS Input
B5	VTT	Power/Other
B6	STPCLK#	CMOS Input
B7	TCK	TAP Input
B8	SLP#	CMOS Input
B9	VTT	Power/Other
B10	TMS	TAP Input
B13	$V_{CC_{CORE}}$	Power/Other
B14	THERMDP	Power/Other
B15	THERMDN	Power/Other
B16	LINT1/NMI	CMOS Input
B17	$V_{CC_{CORE}}$	Power/Other
B18	PICCLK	APIC Clock Input
B19	BP2#	AGTL+ I/O
B20	Reserved	Reserved for Future Use
B21	BSEL	Power/Other
B22	PICD1	APIC I/O
B23	PRDY#	AGTL+ Output
B24	BPM1#	AGTL+ I/O
B25	$V_{CC_{CORE}}$	Power/Other
B26	Reserved	Reserved for Pentium II processor
B27	Reserved	Reserved for Pentium II processor
B28	Reserved	Reserved for Pentium II processor
B29	$V_{CC_{CORE}}$	Power/Other
B30	D62#	AGTL+ I/O
B31	D58#	AGTL+ I/O
B32	D63#	AGTL+ I/O
B33	$V_{CC_{CORE}}$	Power/Other

Table 44. S.E.P. Package Signal Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type
B34	D56#	AGTL+ I/O
B35	D50#	AGTL+ I/O
B36	D54#	AGTL+ I/O
B37	$V_{CC_{CORE}}$	Power/Other
B38	D59#	AGTL+ I/O
B39	D48#	AGTL+ I/O
B40	D52#	AGTL+ I/O
B41	EMI	Power/Other
B42	D41#	AGTL+ I/O
B43	D47#	AGTL+ I/O
B44	D44#	AGTL+ I/O
B45	$V_{CC_{CORE}}$	Power/Other
B46	D36#	AGTL+ I/O
B47	D40#	AGTL+ I/O
B48	D34#	AGTL+ I/O
B49	$V_{CC_{CORE}}$	Power/Other
B50	D38#	AGTL+ I/O
B51	D32#	AGTL+ I/O
B52	D28#	AGTL+ I/O
B53	$V_{CC_{CORE}}$	Power/Other
B54	D29#	AGTL+ I/O
B55	D26#	AGTL+ I/O
B56	D25#	AGTL+ I/O
B57	$V_{CC_{CORE}}$	Power/Other
B58	D22#	AGTL+ I/O
B59	D19#	AGTL+ I/O
B60	D18#	AGTL+ I/O
B61	EMI	Power/Other
B62	D20#	AGTL+ I/O
B63	D17#	AGTL+ I/O
B64	D15#	AGTL+ I/O
B65	$V_{CC_{CORE}}$	Power/Other
B66	D12#	AGTL+ I/O
B67	D7#	AGTL+ I/O
B68	D6#	AGTL+ I/O
B69	$V_{CC_{CORE}}$	Power/Other
B70	D4#	AGTL+ I/O
B71	D2#	AGTL+ I/O
B72	D0#	AGTL+ I/O
B73	$V_{CC_{CORE}}$	Power/Other

Table 44. S.E.P. Package Signal Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type
B74	RESET#	AGTL+ Input
B75	Reserved	Reserved for Future Use
B76	Reserved	Reserved for Future Use
B77	$V_{CC_{CORE}}$	Power/Other
B78	Reserved	Reserved for Pentium II processor
B79	Reserved	Reserved for Pentium II processor
B80	A29#	AGTL+ I/O
B81	EMI	Power/Other
B82	A26#	AGTL+ I/O
B83	A24#	AGTL+ I/O
B84	A28#	AGTL+ I/O
B85	$V_{CC_{CORE}}$	Power/Other
B86	A20#	AGTL+ I/O
B87	A21#	AGTL+ I/O
B88	A25#	AGTL+ I/O
B89	$V_{CC_{CORE}}$	Power/Other
B90	A15#	AGTL+ I/O
B91	A17#	AGTL+ I/O
B92	A11#	AGTL+ I/O
B93	$V_{CC_{CORE}}$	Power/Other
B94	A12#	AGTL+ I/O
B95	A8#	AGTL+ I/O
B96	A7#	AGTL+ I/O
B97	$V_{CC_{CORE}}$	Power/Other
B98	A3#	AGTL+ I/O
B99	A6#	AGTL+ I/O
B100	EMI	Power/Other
B101	SLOTOCC#	Power/Other
B102	REQ0#	AGTL+ I/O
B103	REQ1#	AGTL+ I/O
B104	REQ4#	AGTL+ I/O
B105	$V_{CC_{CORE}}$	Power/Other
B106	LOCK#	AGTL+ I/O
B107	DRDY#	AGTL+ I/O
B108	RS0#	AGTL+ Input
B109	V_{CC_5}	Power/Other
B11	TRST#	TAP Input
B110	HIT#	AGTL+ I/O
B111	RS2#	AGTL+ Input

Table 44. S.E.P. Package Signal Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type
B112	Reserved	Reserved for Future Use
B113	V_{CCL2}	Power/Other. Reserved for Pentium II processor
B114	Reserved	Reserved for Pentium II processor
B115	Reserved	Reserved for Pentium II processor
B116	Reserved	Reserved for Pentium II processor

Table 44. S.E.P. Package Signal Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type
B117	V_{CCL2}	Power/Other. Reserved for Pentium II processor
B118	Reserved	Reserved for Pentium II processor
B119	VID3	Power/Other
B12	Reserved	Reserved for Future Use
B120	VID0	Power/Other
B121	V_{CCL2}	Power/Other. Reserved for Pentium II processor

Table 45. S.E.P. Package Signal Listing by Signal Name

Pin Name	Pin No.	Signal Buffer Type
A3#	B98	AGTL+ I/O
A4#	A100	AGTL+ I/O
A5#	A97	AGTL+ I/O
A6#	B99	AGTL+ I/O
A7#	B96	AGTL+ I/O
A8#	B95	AGTL+ I/O
A9#	A99	AGTL+ I/O
A10#	A96	AGTL+ I/O
A11#	B92	AGTL+ I/O
A12#	B94	AGTL+ I/O
A13#	A93	AGTL+ I/O
A14#	A95	AGTL+ I/O
A15#	B90	AGTL+ I/O
A16#	A92	AGTL+ I/O
A17#	B91	AGTL+ I/O
A18#	A91	AGTL+ I/O
A19#	A89	AGTL+ I/O
A20#	B86	AGTL+ I/O
A20M#	A5	CMOS Input
A21#	B87	AGTL+ I/O
A22#	A85	AGTL+ I/O
A23#	A87	AGTL+ I/O
A24#	B83	AGTL+ I/O
A25#	B88	AGTL+ I/O
A26#	B82	AGTL+ I/O
A27#	A84	AGTL+ I/O
A28#	B84	AGTL+ I/O
A29#	B80	AGTL+ I/O
A30#	A81	AGTL+ I/O
A31#	A83	AGTL+ I/O
ADS#	A115	AGTL+ I/O
BCLK	A75	System Bus Clock Input
BNR#	A101	AGTL+ I/O
BP2#	B19	AGTL+ I/O
BP3#	A21	AGTL+ I/O
BPM0#	A23	AGTL+ I/O
BPM1#	B24	AGTL+ I/O

Table 45. S.E.P. Package Signal Listing by Signal Name

Pin Name	Pin No.	Signal Buffer Type
BPRI#	A103	AGTL+ Input
BSEL	B21	Power/Other
D00#	B72	AGTL+ I/O
D1#	A73	AGTL+ I/O
D2#	B71	AGTL+ I/O
D3#	A72	AGTL+ I/O
D5#	A71	AGTL+ I/O
D6#	B68	AGTL+ I/O
D7#	B67	AGTL+ I/O
D8#	A69	AGTL+ I/O
D9#	A68	AGTL+ I/O
D10#	A65	AGTL+ I/O
D11#	A64	AGTL+ I/O
D12#	B66	AGTL+ I/O
D13#	A63	AGTL+ I/O
D14#	A67	AGTL+ I/O
D15#	B64	AGTL+ I/O
D16#	A61	AGTL+ I/O
D17#	B63	AGTL+ I/O
D18#	B60	AGTL+ I/O
D19#	B59	AGTL+ I/O
D20#	B62	AGTL+ I/O
D21#	A60	AGTL+ I/O
D22#	B58	AGTL+ I/O
D23#	A59	AGTL+ I/O
D24#	A57	AGTL+ I/O
D25#	B56	AGTL+ I/O
D26#	B55	AGTL+ I/O
D27#	A56	AGTL+ I/O
D28#	B52	AGTL+ I/O
D29#	B54	AGTL+ I/O
D30#	A55	AGTL+ I/O
D31#	A53	AGTL+ I/O
D32#	B51	AGTL+ I/O
D33#	A51	AGTL+ I/O
D34#	B48	AGTL+ I/O
D35#	A52	AGTL+ I/O

Table 45. S.E.P. Package Signal Listing by Signal Name

Pin Name	Pin No.	Signal Buffer Type
D36#	B46	AGTL+ I/O
D37#	A49	AGTL+ I/O
D38#	B50	AGTL+ I/O
D39#	A45	AGTL+ I/O
D4#	B70	AGTL+ I/O
D40#	B47	AGTL+ I/O
D41#	B42	AGTL+ I/O
D42#	A43	AGTL+ I/O
D43#	A48	AGTL+ I/O
D44#	B44	AGTL+ I/O
D45#	A44	AGTL+ I/O
D46#	A39	AGTL+ I/O
D47#	B43	AGTL+ I/O
D48#	B39	AGTL+ I/O
D49#	A40	AGTL+ I/O
D50#	B35	AGTL+ I/O
D51#	A41	AGTL+ I/O
D52#	B40	AGTL+ I/O
D53#	A36	AGTL+ I/O
D54#	B36	AGTL+ I/O
D55#	A33	AGTL+ I/O
D56#	B34	AGTL+ I/O
D57#	A37	AGTL+ I/O
D58#	B31	AGTL+ I/O
D59#	B38	AGTL+ I/O
D60#	A35	AGTL+ I/O
D61#	A32	AGTL+ I/O
D62#	B30	AGTL+ I/O
D63#	B32	AGTL+ I/O
DBSY#	A111	AGTL+ I/O
DEFER#	A105	AGTL+ Input
DRDY#	B107	AGTL+ I/O
EMI	B1	Power/Other
EMI	B41	Power/Other
EMI	B61	Power/Other
EMI	B81	Power/Other
EMI	B100	Power/Other

Table 45. S.E.P. Package Signal Listing by Signal Name

Pin Name	Pin No.	Signal Buffer Type
FERR#	A7	CMOS Output
FLUSH#	B2	CMOS Input
HIT#	B110	AGTL+ I/O
HITM#	A109	AGTL+ I/O
IERR#	A4	CMOS Output
IGNNE#	A8	CMOS Input
INIT#	B4	CMOS Input
LINT0/INTR	A17	CMOS Input
LINT1/NMI	B16	CMOS Input
LOCK#	B106	AGTL+ I/O
PICCLK	B18	APIC Clock Input
PICD0	A19	APIC I/O
PICD1	B22	APIC I/O
PRDY#	B23	AGTL+ Output
PREQ#	A20	CMOS Input
PWRGOOD	A12	CMOS Input
REQ0#	B102	AGTL+ I/O
REQ1#	B103	AGTL+ I/O
REQ2#	A107	AGTL+ I/O
REQ3#	A108	AGTL+ I/O
REQ4#	B104	AGTL+ I/O
Reserved	A16	Reserved for Future Use
Reserved	A47	Reserved for Future Use
Reserved	A77	Reserved for Pentium II processor
Reserved	A88	Reserved for Future Use
Reserved	A116	Reserved for Future Use
Reserved	B12	Reserved for Future Use
Reserved	A113	Reserved for Future Use
Reserved	B20	Reserved for Future Use
Reserved	B76	Reserved for Future Use
Reserved	B112	Reserved for Future Use
Reserved	B79	Reserved for Pentium II processor
Reserved	B114	Reserved for Pentium II processor
Reserved	B115	Reserved for Pentium II processor

Table 45. S.E.P. Package Signal Listing by Signal Name

Pin Name	Pin No.	Signal Buffer Type
Reserved	A117	Reserved for Pentium II processor
Reserved	B116	Reserved for Pentium II processor
Reserved	A24	Reserved for Pentium II processor
Reserved	A76	Reserved for Pentium II processor
Reserved	B75	Reserved for Future Use
Reserved	A79	Reserved for Pentium II processor
Reserved	A80	Reserved for Pentium II processor
Reserved	B78	Reserved for Pentium II processor
Reserved	B118	Reserved for Pentium II processor
Reserved	A25	Reserved for Pentium II processor
Reserved	A27	Reserved for Pentium II processor
Reserved	B26	Reserved for Pentium II processor
Reserved	A28	Reserved for Pentium II processor
Reserved	B27	Reserved for Pentium II processor
Reserved	A29	Reserved for Pentium II processor
Reserved	A31	Reserved for Pentium II processor
Reserved	B28	Reserved for Pentium II processor
RESET#	B74	AGTL+ Input
RS0#	B108	AGTL+ Input
RS1#	A112	AGTL+ Input
RS2#	B111	AGTL+ Input
SLOTOCC#	B101	Power/Other
SLP#	B8	CMOS Input
SMI#	B3	CMOS Input
STPCLK#	B6	CMOS Input
TCK	B7	TAP Input
TDI	A9	TAP Input
TDO	A11	TAP Output
TESTHI	A13	CMOS Test Input
THERMDN	B15	Power/Other
THERMDP	B14	Power/Other
THERMTRIP#	A15	CMOS Output
TMS	B10	TAP Input
TRDY#	A104	AGTL+ Input
TRST#	B11	TAP Input
V_{CC_5}	B109	Power/Other
$V_{CC_{CORE}}$	B13	Power/Other
$V_{CC_{CORE}}$	B17	Power/Other
$V_{CC_{CORE}}$	B25	Power/Other
$V_{CC_{CORE}}$	B29	Power/Other
$V_{CC_{CORE}}$	B33	Power/Other
$V_{CC_{CORE}}$	B37	Power/Other
$V_{CC_{CORE}}$	B45	Power/Other
$V_{CC_{CORE}}$	B49	Power/Other
$V_{CC_{CORE}}$	B53	Power/Other
$V_{CC_{CORE}}$	B57	Power/Other
$V_{CC_{CORE}}$	B65	Power/Other
$V_{CC_{CORE}}$	B69	Power/Other
$V_{CC_{CORE}}$	B73	Power/Other
$V_{CC_{CORE}}$	B77	Power/Other
$V_{CC_{CORE}}$	B85	Power/Other
$V_{CC_{CORE}}$	B89	Power/Other
$V_{CC_{CORE}}$	B93	Power/Other
$V_{CC_{CORE}}$	B97	Power/Other
$V_{CC_{CORE}}$	B105	Power/Other
$V_{CC_{L2}}$	B113	Power/Other. Reserved for Pentium II processor
$V_{CC_{L2}}$	B117	Power/Other. Reserved for Pentium II processor
$V_{CC_{L2}}$	B121	Power/Other. Reserved for Pentium II processor
VID0	B120	Power/Other
VID1	A120	Power/Other
VID2	A119	Power/Other
VID3	B119	Power/Other
VID4	A121	Power/Other
V_{SS}	A114	Power/Other

Table 45. S.E.P. Package Signal Listing by Signal Name

Pin Name	Pin No.	Signal Buffer Type
V_{SS}	A118	Power/Other
V_{SS}	A46	Power/Other
V_{SS}	A38	Power/Other
V_{SS}	A42	Power/Other
V_{SS}	A50	Power/Other
V_{SS}	A54	Power/Other
V_{SS}	A58	Power/Other
V_{SS}	A62	Power/Other
V_{SS}	A66	Power/Other
V_{SS}	A70	Power/Other
V_{SS}	A74	Power/Other
V_{SS}	A78	Power/Other
V_{SS}	A82	Power/Other
V_{SS}	A86	Power/Other
V_{SS}	A2	Power/Other
V_{SS}	A6	Power/Other

Table 45. S.E.P. Package Signal Listing by Signal Name

Pin Name	Pin No.	Signal Buffer Type
V_{SS}	A10	Power/Other
V_{SS}	A14	Power/Other
V_{SS}	A18	Power/Other
V_{SS}	A22	Power/Other
V_{SS}	A26	Power/Other
V_{SS}	A30	Power/Other
V_{SS}	A34	Power/Other
V_{SS}	A98	Power/Other
V_{SS}	A102	Power/Other
V_{SS}	A106	Power/Other
V_{SS}	A110	Power/Other
V_{TT}	A1	Power/Other
V_{TT}	A3	Power/Other
V_{TT}	B5	Power/Other
V_{TT}	B9	Power/Other

5.2 PPGA Package

This section defines the mechanical specifications and signal definitions for the Celeron processor in the PPGA packages.

5.2.1 PPGA Package Materials Information

Figure 21 and Table 46 are provided to aid in the design of a heatsink and clip.

Figure 21. Package Dimensions (PPGA Package)

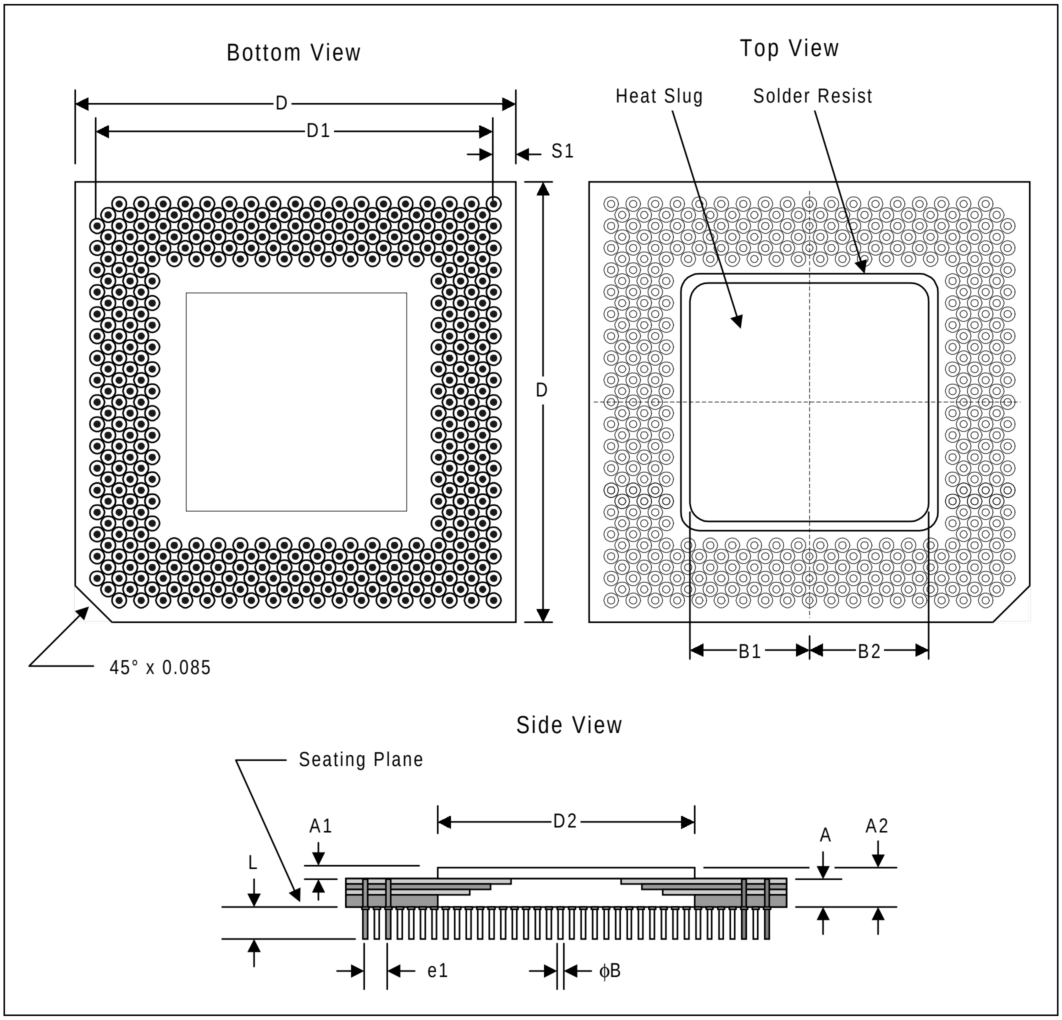


Table 46. Package Dimensions (PPGA Package)

Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	1.83	2.23		0.072	0.088	
A1	1.00			0.039		
A2	2.72	3.33		0.107	0.131	
B	0.40	0.51		0.016	0.020	
D	49.43	49.63		1.946	1.954	
D1	45.59	45.85		1.795	1.805	
D2	25.15	25.65		0.099	1.010	
e1	2.29	2.79		0.090	0.110	
L	3.05	3.30		0.120	0.130	
N	370		Lead Count	370		Lead Count
S1	1.52	2.54		0.060	0.100	

Table 47. Information Summary (PPGA Package)

Package Type	Total Pins	Pin Array	Package Size
Plastic Staggered Pin Grid Array (PPGA)	370	37 x 37	1.95" x 1.95" 4.95 cm x 4.95 cm

5.2.2 PPGA Package Signal Listing

Figure 22. PPGA Package (Pin Side View)

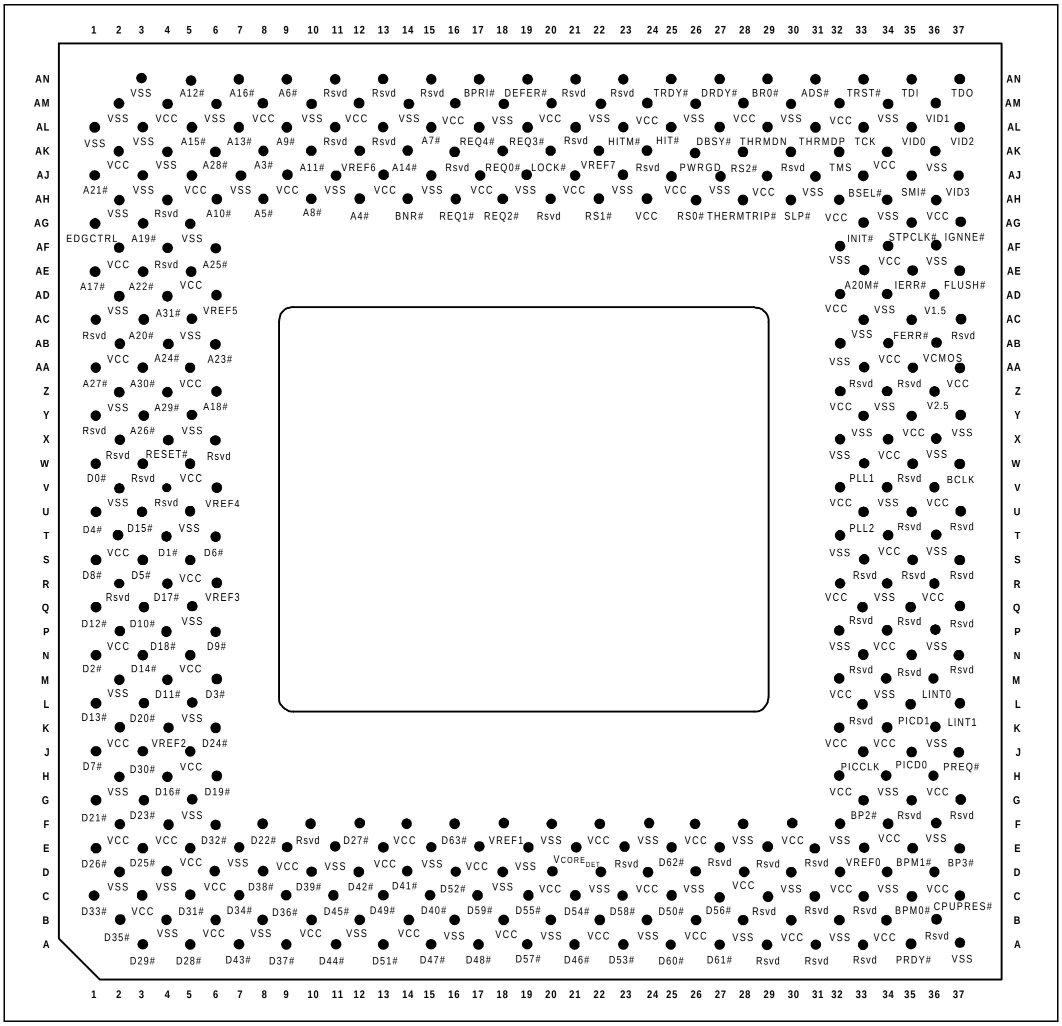


Table 48. PPGA Package Signal Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type
A3	D29#	AGTL+ I/O
A5	D28#	AGTL+ I/O
A7	D43#	AGTL+ I/O
A9	D37#	AGTL+ I/O
A11	D44#	AGTL+ I/O
A13	D51#	AGTL+ I/O
A15	D47#	AGTL+ I/O
A17	D48#	AGTL+ I/O
A19	D57#	AGTL+ I/O
A21	D46#	AGTL+ I/O
A23	D53#	AGTL+ I/O
A25	D60#	AGTL+ I/O
A27	D61#	AGTL+ I/O
A29	Reserved	Reserved for Future Use
A31	Reserved	Reserved for Future Use
A33	Reserved	Reserved for Future Use
A35	PRDY#	AGTL+ Output
A37	V_{SS}	Power/Other
AA1	A27#	AGTL+ I/O
AA3	A30#	AGTL+ I/O
AA5	$V_{CC_{CORE}}$	Power/Other
AA33	Reserved	Reserved for Future Use
AA35	Reserved	Reserved for Future Use
AA37	$V_{CC_{CORE}}$	Power/Other
AB2	$V_{CC_{CORE}}$	Power/Other
AB4	A24#	AGTL+ I/O
AB6	A23#	AGTL+ I/O
AB32	V_{SS}	Power/Other
AB34	$V_{CC_{CORE}}$	Power/Other
AB36	$V_{CC_{CMOS}}$	Power/Other
AC1	Reserved	Reserved for Future Use
AC3	A20#	AGTL+ I/O
AC5	V_{SS}	Power/Other
AC33	V_{SS}	Power/Other
AC35	FERR#	CMOS Output
AC37	Reserved	Reserved for Future Use
AD2	V_{SS}	Power/Other

Table 48. PPGA Package Signal Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type
AD4	A31#	AGTL+ I/O
AD6	V_{REF_5}	Power/Other
AD32	$V_{CC_{CORE}}$	Power/Other
AD34	V_{SS}	Power/Other
AD36	$V_{CC_{1.5}}$	Power/Other
AE1	A17#	AGTL+ I/O
AE3	A22#	AGTL+ I/O
AE5	$V_{CC_{CORE}}$	Power/Other
AE33	A20M#	CMOS Input
AE35	IERR#	CMOS Output
AE37	FLUSH#	CMOS Input
AF2	$V_{CC_{CORE}}$	Power/Other
AF4	Reserved	Reserved for Future Use
AF6	A25#	AGTL+ I/O
AF32	V_{SS}	Power/Other
AF34	$V_{CC_{CORE}}$	Power/Other
AF36	V_{SS}	Power/Other
AG1	EDGCTRL	Power/Other
AG3	A19#	AGTL+ I/O
AG5	V_{SS}	Power/Other
AG33	INIT#	CMOS Input
AG35	STPCLK#	CMOS Input
AG37	IGNNE#	CMOS Input
AH2	V_{SS}	Power/Other
AH4	Reserved	Reserved for Future Use
AH6	A10#	AGTL+ I/O
AH8	A5#	AGTL+ I/O
AH10	A8#	AGTL+ I/O
AH12	A4#	AGTL+ I/O
AH14	BNR#	AGTL+ I/O
AH16	REQ1#	AGTL+ I/O
AH18	REQ2#	AGTL+ I/O
AH20	Reserved	Reserved for Future Use
AH22	RS1#	AGTL+ Input
AH24	$V_{CC_{CORE}}$	Power/Other
AH26	RS0#	AGTL+ Input
AH28	THERMTRIP#	CMOS Output
AH30	SLP#	CMOS Input

Table 48. PPGA Package Signal Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type
AH32	$V_{CC_{CORE}}$	Power/Other
AH34	V_{SS}	Power/Other
AH36	$V_{CC_{CORE}}$	Power/Other
AJ01	A21#	AGTL+ I/O
AJ03	V_{SS}	Power/Other
AJ05	$V_{CC_{CORE}}$	Power/Other
AJ07	V_{SS}	Power/Other
AJ09	$V_{CC_{CORE}}$	Power/Other
AJ11	V_{SS}	Power/Other
AJ13	$V_{CC_{CORE}}$	Power/Other
AJ15	V_{SS}	Power/Other
AJ17	$V_{CC_{CORE}}$	Power/Other
AJ19	V_{SS}	Power/Other
AJ21	$V_{CC_{CORE}}$	Power/Other
AJ23	V_{SS}	Power/Other
AJ25	$V_{CC_{CORE}}$	Power/Other
AJ27	V_{SS}	Power/Other
AJ29	$V_{CC_{CORE}}$	Power/Other
AJ31	V_{SS}	Power/Other
AJ33	BSEL	Power/Other
AJ35	SMI#	CMOS Input
AJ37	VID3	Power/Other
AK02	$V_{CC_{CORE}}$	Power/Other
AK04	V_{SS}	Power/Other
AK06	A28#	AGTL+ I/O
AK08	A3#	AGTL+ I/O
AK10	A11#	AGTL+ I/O
AK12	V_{REF6}	Power/Other
AK14	A14#	AGTL+ I/O
AK16	Reserved	Reserved for Future Use
AK18	REQ0#	AGTL+ I/O
AK20	LOCK#	AGTL+ I/O
AK22	V_{REF7}	Power/Other
AK24	Reserved	Reserved for Future Use
AK26	PWRGOOD	CMOS Input
AK28	RS2#	AGTL+ Input
AK30	Reserved	Reserved for Future Use
AK32	TMS	TAP Input

Table 48. PPGA Package Signal Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type
AK34	$V_{CC_{CORE}}$	Power/Other
AK36	V_{SS}	Power/Other
AL01	V_{SS}	Power/Other
AL03	V_{SS}	Power/Other
AL05	A15#	AGTL+ I/O
AL07	A13#	AGTL+ I/O
AL09	A9#	AGTL+ I/O
AL11	Reserved	Reserved for Future Use
AL13	Reserved	Reserved for Future Use
AL15	A7#	AGTL+ I/O
AL17	REQ4#	AGTL+ I/O
AL19	REQ3#	AGTL+ I/O
AL21	Reserved	Reserved for Future Use
AL23	HITM#	AGTL+ I/O
AL25	HIT#	AGTL+ I/O
AL27	DBSY#	AGTL+ I/O
AL29	THERMDN	Power/Other
AL31	THERMDP	Power/Other
AL33	TCK	TAP Input
AL35	VID0	Voltage Identification
AL37	VID2	Voltage Identification
AM04	$V_{CC_{CORE}}$	Power/Other
AM06	V_{SS}	Power/Other
AM08	$V_{CC_{CORE}}$	Power/Other
AM10	V_{SS}	Power/Other
AM12	$V_{CC_{CORE}}$	Power/Other
AM14	V_{SS}	Power/Other
AM16	$V_{CC_{CORE}}$	Power/Other
AM18	V_{SS}	Power/Other
AM2	V_{SS}	Power/Other
AM20	$V_{CC_{CORE}}$	Power/Other
AM22	V_{SS}	Power/Other
AM24	$V_{CC_{CORE}}$	Power/Other
AM26	V_{SS}	Power/Other
AM28	$V_{CC_{CORE}}$	Power/Other
AM30	V_{SS}	Power/Other
AM32	$V_{CC_{CORE}}$	Power/Other
AM34	V_{SS}	Power/Other

Table 48. PPGA Package Signal Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type
AM36	VID1	Voltage Identification
AN3	Vss	Power/Other
AN5	A12#	AGTL+ I/O
AN7	A16#	AGTL+ I/O
AN9	A6#	AGTL+ I/O
AN11	Reserved	Reserved for Future Use
AN13	Reserved	Reserved for Future Use
AN15	Reserved	Reserved for Future Use
AN17	BPRI#	AGTL+ Input
AN19	DEFER#	AGTL+ Input
AN21	Reserved	Reserved for Future Use
AN23	Reserved	Reserved for Future Use
AN25	TRDY#	AGTL+ Input
AN27	DRDY#	AGTL+ I/O
AN29	BR0#	AGTL+ I/O
AN31	ADS#	AGTL+ I/O
AN33	TRST#	TAP Input
AN35	TDI	TAP Input
AN37	TDO	TAP Output
B2	D35#	AGTL+ I/O
B4	Vss	Power/Other
B6	$V_{CC_{CORE}}$	Power/Other
B8	Vss	Power/Other
B10	$V_{CC_{CORE}}$	Power/Other
B12	Vss	Power/Other
B14	$V_{CC_{CORE}}$	Power/Other
B16	Vss	Power/Other
B18	$V_{CC_{CORE}}$	Power/Other
B20	Vss	Power/Other
B22	$V_{CC_{CORE}}$	Power/Other
B24	Vss	Power/Other
B26	$V_{CC_{CORE}}$	Power/Other
B28	Vss	Power/Other
B30	$V_{CC_{CORE}}$	Power/Other
B32	Vss	Power/Other
B34	$V_{CC_{CORE}}$	Power/Other
B36	Reserved	Reserved for Future Use
C1	D33#	AGTL+ I/O

Table 48. PPGA Package Signal Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type
C3	$V_{CC_{CORE}}$	Power/Other
C5	D31#	AGTL+ I/O
C7	D34#	AGTL+ I/O
C9	D36#	AGTL+ I/O
C11	D45#	AGTL+ I/O
C13	D49#	AGTL+ I/O
C15	D40#	AGTL+ I/O
C17	D59#	AGTL+ I/O
C19	D55#	AGTL+ I/O
C21	D54#	AGTL+ I/O
C23	D58#	AGTL+ I/O
C25	D50#	AGTL+ I/O
C27	D56#	AGTL+ I/O
C29	Reserved	Reserved for Future Use
C31	Reserved	Reserved for Future Use
C33	Reserved	Reserved for Future Use
C35	BPM0#	AGTL+ I/O
C37	CPUPRES#	Power/Other
D2	Vss	Power/Other
D4	Vss	Power/Other
D6	$V_{CC_{CORE}}$	Power/Other
D8	D38#	AGTL+ I/O
D10	D39#	AGTL+ I/O
D12	D42#	AGTL+ I/O
D14	D41#	AGTL+ I/O
D16	D52#	AGTL+ I/O
D18	Vss	Power/Other
D20	$V_{CC_{CORE}}$	Power/Other
D22	Vss	Power/Other
D24	$V_{CC_{CORE}}$	Power/Other
D26	Vss	Power/Other
D28	$V_{CC_{CORE}}$	Power/Other
D30	Vss	Power/Other
D32	$V_{CC_{CORE}}$	Power/Other
D34	Vss	Power/Other
D36	$V_{CC_{CORE}}$	Power/Other
E1	D26#	AGTL+ I/O
E3	D25#	AGTL+ I/O

Table 48. PPGA Package Signal Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type
E5	$V_{CC_{CORE}}$	Power/Other
E7	V_{SS}	Power/Other
E9	$V_{CC_{CORE}}$	Power/Other
E11	V_{SS}	Power/Other
E13	$V_{CC_{CORE}}$	Power/Other
E15	V_{SS}	Power/Other
E17	$V_{CC_{CORE}}$	Power/Other
E19	V_{SS}	Power/Other
E21	$V_{CORE_{DET}}$	Power/Other
E23	Reserved	Reserved for Future Use
E25	D62#	Power/Other
E27	Reserved	Reserved for Future Use
E29	Reserved	Reserved for Future Use
E31	Reserved	Reserved for Future Use
E33	$V_{REF}0$	Power/Other
E35	BPM1#	AGTL+ I/O
E37	BP3#	AGTL+ I/O
F2	$V_{CC_{CORE}}$	Power/Other
F4	$V_{CC_{CORE}}$	Power/Other
F6	D32#	AGTL+ I/O
F8	D22#	AGTL+ I/O
F10	Reserved	Reserved for Future Use
F12	D27#	AGTL+ I/O
F14	$V_{CC_{CORE}}$	Power/Other
F16	D63#	AGTL+ I/O
F18	$V_{REF}1$	Power/Other
F20	V_{SS}	Power/Other
F22	$V_{CC_{CORE}}$	Power/Other
F24	V_{SS}	Power/Other
F26	$V_{CC_{CORE}}$	Power/Other
F28	V_{SS}	Power/Other
F30	$V_{CC_{CORE}}$	Power/Other
F32	V_{SS}	Power/Other
F34	$V_{CC_{CORE}}$	Power/Other
F36	V_{SS}	Power/Other
G1	D21#	AGTL+ I/O
G3	D23#	AGTL+ I/O
G5	V_{SS}	Power/Other

Table 48. PPGA Package Signal Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type
G33	BP2#	AGTL+ I/O
G35	Reserved	Reserved for Future Use
G37	Reserved	Reserved for Future Use
H2	V_{SS}	Power/Other
H4	D16#	AGTL+ I/O
H6	D19#	AGTL+ I/O
H32	$V_{CC_{CORE}}$	Power/Other
H34	V_{SS}	Power/Other
H36	$V_{CC_{CORE}}$	Power/Other
J1	D7#	AGTL+ I/O
J3	D30#	AGTL+ I/O
J5	$V_{CC_{CORE}}$	Power/Other
J33	PICCLK	APIC Clock Input
J35	PICD0	APIC I/O
J37	PREQ#	CMOS Input
K2	$V_{CC_{CORE}}$	Power/Other
K4	$V_{REF}2$	Power/Other
K6	D24#	AGTL+ I/O
K32	$V_{CC_{CORE}}$	Power/Other
K34	$V_{CC_{CORE}}$	Power/Other
K36	V_{SS}	Power/Other
L1	D13#	AGTL+ I/O
L3	D20#	AGTL+ I/O
L5	V_{SS}	Power/Other
L33	Reserved	Reserved for Future Use
L35	PICD1	APIC I/O
L37	LINT1/NMI	CMOS Input
M2	V_{SS}	Power/Other
M4	D11#	AGTL+ I/O
M6	D3#	AGTL+ I/O
M32	$V_{CC_{CORE}}$	Power/Other
M34	V_{SS}	Power/Other
M36	LINT0/INTR	CMOS Input
N1	D2#	AGTL+ I/O
N3	D14#	AGTL+ I/O
N5	$V_{CC_{CORE}}$	Power/Other
N33	Reserved	Reserved for Future Use
N35	Reserved	Reserved for Future Use

Table 48. PPGA Package Signal Listing by Pin Number

Table 48. PPGA Package Signal Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type
N37	Reserved	Reserved for Future Use
P2	VCC$_{CORE}$	Power/Other
P4	D18#	AGTL+ I/O
P6	D9#	AGTL+ I/O
P32	VSS	Power/Other
P34	VCC$_{CORE}$	Power/Other
P36	VSS	Power/Other
Q1	D12#	AGTL+ I/O
Q3	D10#	AGTL+ I/O
Q5	VSS	Power/Other
Q33	Reserved	Reserved for Future Use
Q35	Reserved	Reserved for Future Use
Q37	Reserved	Reserved for Future Use
R2	Reserved	Reserved for Future Use
R4	D17#	AGTL+ I/O
R6	VREF3	Power/Other
R32	VCC$_{CORE}$	Power/Other
R34	VSS	Power/Other
R36	VCC$_{CORE}$	Power/Other
S1	D8#	AGTL+ I/O
S3	D5#	AGTL+ I/O
S5	VCC$_{CORE}$	Power/Other
S33	Reserved	Reserved for Future Use
S35	Reserved	Reserved for Future Use
S37	Reserved	Reserved for Future Use
T2	VCC$_{CORE}$	Power/Other
T4	D1#	AGTL+ I/O
T6	D6#	AGTL+ I/O
T32	VSS	Power/Other
T34	VCC$_{CORE}$	Power/Other
T36	VSS	Power/Other
U1	D4#	AGTL+ I/O
U3	D15#	AGTL+ I/O
U5	VSS	Power/Other
U33	PLL2	Power/Other
U35	Reserved	Reserved for Future Use
U37	Reserved	Reserved for Future Use
V2	VSS	Power/Other
V4	Reserved	Reserved for Future Use
V6	VREF4	Power/Other
V32	VCC$_{CORE}$	Power/Other
V34	VSS	Power/Other
V36	VCC$_{CORE}$	Power/Other
W1	D0#	AGTL+ I/O
W3	Reserved	Reserved for Future Use
W5	VCC$_{CORE}$	Power/Other
W33	PLL1	Power/Other
W35	Reserved	Reserved for Future Use
W37	BCLK	System Bus Clock Input
X2	Reserved	Reserved for Future Use
X4	RESET#	AGTL+ Input
X6	Reserved	Reserved for Future Use
X32	VSS	Power/Other
X34	VCC$_{CORE}$	Power/Other
X36	VSS	Power/Other
Y1	Reserved	Reserved for Future Use
Y3	A26#	AGTL+ I/O
Y5	VSS	Power/Other
Y33	VSS	Power/Other
Y35	VCC$_{CORE}$	Power/Other
Y37	VSS	Power/Other
Z2	VSS	Power/Other
Z4	A29#	AGTL+ I/O
Z6	A18#	AGTL+ I/O
Z32	VCC$_{CORE}$	Power/Other
Z34	VSS	Power/Other
Z36	VCC$_{2.5}$	Power/Other

Table 49. PPGA Package Signal Listing in Order by Signal Name

Pin Name	Pin No.	Signal Buffer Type
A3#	AK8	AGTL+ I/O
A4#	AH12	AGTL+ I/O
A5#	AH8	AGTL+ I/O
A6#	AN9	AGTL+ I/O
A7#	AL15	AGTL+ I/O
A8#	AH10	AGTL+ I/O
A9#	AL9	AGTL+ I/O
A10#	AH6	AGTL+ I/O
A11#	AK10	AGTL+ I/O
A12#	AN5	AGTL+ I/O
A13#	AL7	AGTL+ I/O
A14#	AK14	AGTL+ I/O
A15#	AL5	AGTL+ I/O
A16#	AN7	AGTL+ I/O
A17#	AE1	AGTL+ I/O
A18#	Z6	AGTL+ I/O
A19#	AG3	AGTL+ I/O
A20#	AC3	AGTL+ I/O
A21#	AJ1	AGTL+ I/O
A22#	AE3	AGTL+ I/O
A23#	AB6	AGTL+ I/O
A24#	AB4	AGTL+ I/O
A25#	AF6	AGTL+ I/O
A26#	Y3	AGTL+ I/O
A27#	AA1	AGTL+ I/O
A28#	AK6	AGTL+ I/O
A29#	Z4	AGTL+ I/O
A30#	AA3	AGTL+ I/O
A31#	AD4	AGTL+ I/O
A20M#	AE33	CMOS Input
ADS#	AN31	AGTL+ I/O
BCLK	W37	System Bus Clock Input
BNR#	AH14	AGTL+ I/O
BP2#	G33	AGTL+ I/O
BP3#	E37	AGTL+ I/O
BPM0#	C35	AGTL+ I/O
BPM1#	E35	AGTL+ I/O
BPRI#	AN17	AGTL+ Input
BR0#	AN29	AGTL+ I/O
BSEL	AJ33	Power/Other

Table 49. PPGA Package Signal Listing in Order by Signal Name

Pin Name	Pin No.	Signal Buffer Type
CPUPRES#	C37	Power/Other
D0#	W1	AGTL+ I/O
D1#	T4	AGTL+ I/O
D2#	N1	AGTL+ I/O
D3#	M6	AGTL+ I/O
D4#	U1	AGTL+ I/O
D5#	S3	AGTL+ I/O
D6#	T6	AGTL+ I/O
D7#	J1	AGTL+ I/O
D8#	S1	AGTL+ I/O
D9#	P6	AGTL+ I/O
D10#	Q3	AGTL+ I/O
D11#	M4	AGTL+ I/O
D12#	Q1	AGTL+ I/O
D13#	L1	AGTL+ I/O
D14#	N3	AGTL+ I/O
D15#	U3	AGTL+ I/O
D16#	H4	AGTL+ I/O
D17#	R4	AGTL+ I/O
D18#	P4	AGTL+ I/O
D19#	H6	AGTL+ I/O
D20#	L3	AGTL+ I/O
D21#	G1	AGTL+ I/O
D22#	F8	AGTL+ I/O
D23#	G3	AGTL+ I/O
D24#	K6	AGTL+ I/O
D25#	E3	AGTL+ I/O
D26#	E1	AGTL+ I/O
D27#	F12	AGTL+ I/O
D28#	A5	AGTL+ I/O
D29#	A3	AGTL+ I/O
D30#	J3	AGTL+ I/O
D31#	C5	AGTL+ I/O
D32#	F6	AGTL+ I/O
D33#	C1	AGTL+ I/O
D34#	C7	AGTL+ I/O
D35#	B2	AGTL+ I/O
D36#	C9	AGTL+ I/O
D37#	A9	AGTL+ I/O
D38#	D8	AGTL+ I/O

Table 49. PPGA Package Signal Listing in Order by Signal Name

Pin Name	Pin No.	Signal Buffer Type
D39#	D10	AGTL+ I/O
D40#	C15	AGTL+ I/O
D41#	D14	AGTL+ I/O
D42#	D12	AGTL+ I/O
D43#	A7	AGTL+ I/O
D44#	A11	AGTL+ I/O
D45#	C11	AGTL+ I/O
D46#	A21	AGTL+ I/O
D47#	A15	AGTL+ I/O
D48#	A17	AGTL+ I/O
D49#	C13	AGTL+ I/O
D50#	C25	AGTL+ I/O
D51#	A13	AGTL+ I/O
D52#	D16	AGTL+ I/O
D53#	A23	AGTL+ I/O
D54#	C21	AGTL+ I/O
D55#	C19	AGTL+ I/O
D56#	C27	AGTL+ I/O
D57#	A19	AGTL+ I/O
D58#	C23	AGTL+ I/O
D59#	C17	AGTL+ I/O
D60#	A25	AGTL+ I/O
D61#	A27	AGTL+ I/O
D62#	E25	AGTL+ I/O
D63#	F16	AGTL+ I/O
DBSY#	AL27	AGTL+ I/O
DEFER#	AN19	AGTL+ Input
DRDY#	AN27	AGTL+ I/O
EDGCTRL	AG1	Power/Other
FERR#	AC35	CMOS Output
FLUSH#	AE37	CMOS Input
HIT#	AL25	AGTL+ I/O
HITM#	AL23	AGTL+ I/O
IERR#	AE35	CMOS Output
IGNNE#	AG37	CMOS Input
INIT#	AG33	CMOS Input
LINT0/INTR	M36	CMOS Input
LINT1/NMI	L37	CMOS Input
LOCK#	AK20	AGTL+ I/O
PICCLK	J33	APIC Clock Input

Table 49. PPGA Package Signal Listing in Order by Signal Name

Pin Name	Pin No.	Signal Buffer Type
PICD0	J35	APIC I/O
PICD1	L35	APIC I/O
PLL1	W33	Power/Other
PLL2	U33	Power/Other
PRDY#	A35	AGTL+ Output
PREQ#	J37	CMOS Input
PWRGOOD	AK26	CMOS Input
REQ0#	AK18	AGTL+ I/O
REQ1#	AH16	AGTL+ I/O
REQ2#	AH18	AGTL+ I/O
REQ3#	AL19	AGTL+ I/O
REQ4#	AL17	AGTL+ I/O
Reserved	AC1	Reserved for Future Use
Reserved	AC37	Reserved for Future Use
Reserved	AF4	Reserved for Future Use
Reserved	AK16	Reserved for Future Use
Reserved	AK24	Reserved for Future Use
Reserved	AK30	Reserved for Future Use
Reserved	AL11	Reserved for Future Use
Reserved	AL13	Reserved for Future Use
Reserved	AL21	Reserved for Future Use
Reserved	AN11	Reserved for Future Use
Reserved	AN13	Reserved for Future Use
Reserved	AN15	Reserved for Future Use
Reserved	AN21	Reserved for Future Use
Reserved	AN23	Reserved for Future Use
Reserved	B36	Reserved for Future Use
Reserved	C29	Reserved for Future Use
Reserved	C31	Reserved for Future Use
Reserved	C33	Reserved for Future Use
Reserved	E23	Reserved for Future Use
Reserved	E29	Reserved for Future Use
Reserved	E31	Reserved for Future Use
Reserved	F10	Reserved for Future Use
Reserved	G35	Reserved for Future Use
Reserved	G37	Reserved for Future Use
Reserved	L33	Reserved for Future Use
Reserved	N33	Reserved for Future Use
Reserved	N35	Reserved for Future Use
Reserved	N37	Reserved for Future Use

Table 49. PPGA Package Signal Listing in Order by Signal Name

Pin Name	Pin No.	Signal Buffer Type
Reserved	Q33	Reserved for Future Use
Reserved	Q35	Reserved for Future Use
Reserved	Q37	Reserved for Future Use
Reserved	S33	Reserved for Future Use
Reserved	S37	Reserved for Future Use
Reserved	U35	Reserved for Future Use
Reserved	U37	Reserved for Future Use
Reserved	V4	Reserved for Future Use
Reserved	W3	Reserved for Future Use
Reserved	W35	Reserved for Future Use
Reserved	AH20	Reserved for Future Use
Reserved	AH4	Reserved for Future Use
Reserved	A29	Reserved for Future Use
Reserved	A31	Reserved for Future Use
Reserved	A33	Reserved for Future Use
Reserved	AA33	Reserved for Future Use
Reserved	AA35	Reserved for Future Use
Reserved	X6	Reserved for Future Use
Reserved	Y1	Reserved for Future Use
Reserved	E27	Reserved for Future Use
Reserved	R2	Reserved for Future Use
Reserved	S35	Reserved for Future Use
Reserved	X2	Reserved for Future Use
RESET#	X4	AGTL+ Input
RS0#	AH26	AGTL+ Input
RS1#	AH22	AGTL+ Input
RS2#	AK28	AGTL+ Input
SLP#	AH30	CMOS Input
SMI#	AJ35	CMOS Input
STPCLK#	AG35	CMOS Input
TCK	AL33	TAP Input
TDI	AN35	TAP Input
TDO	AN37	TAP Output
THERMDN	AL29	Power/Other
THERMDP	AL31	Power/Other
THERMTRIP#	AH28	CMOS Output
TMS	AK32	TAP Input
TRDY#	AN25	AGTL+ Input
TRST#	AN33	TAP Input
$V_{CC1.5}$	AD36	Power/Other

Table 49. PPGA Package Signal Listing in Order by Signal Name

Pin Name	Pin No.	Signal Buffer Type
$V_{CC2.5}$	Z36	Power/Other
V_{CCCMOS}	AB36	Power/Other
V_{CCCORE}	AJ25	Power/Other
V_{CCCORE}	AJ29	Power/Other
V_{CCCORE}	AJ5	Power/Other
V_{CCCORE}	AJ9	Power/Other
V_{CCCORE}	AK2	Power/Other
V_{CCCORE}	AK34	Power/Other
V_{CCCORE}	AM12	Power/Other
V_{CCCORE}	AM16	Power/Other
V_{CCCORE}	AM20	Power/Other
V_{CCCORE}	AM24	Power/Other
V_{CCCORE}	AM28	Power/Other
V_{CCCORE}	AM32	Power/Other
V_{CCCORE}	AM4	Power/Other
V_{CCCORE}	AM8	Power/Other
V_{CCCORE}	B10	Power/Other
V_{CCCORE}	B14	Power/Other
V_{CCCORE}	B18	Power/Other
V_{CCCORE}	B22	Power/Other
V_{CCCORE}	B26	Power/Other
V_{CCCORE}	B30	Power/Other
V_{CCCORE}	B34	Power/Other
V_{CCCORE}	B6	Power/Other
V_{CCCORE}	C3	Power/Other
V_{CCCORE}	D20	Power/Other
V_{CCCORE}	D24	Power/Other
V_{CCCORE}	D28	Power/Other
V_{CCCORE}	D32	Power/Other
V_{CCCORE}	D36	Power/Other
V_{CCCORE}	D6	Power/Other
V_{CCCORE}	E13	Power/Other
V_{CCCORE}	E17	Power/Other
V_{CCCORE}	E5	Power/Other
V_{CCCORE}	E9	Power/Other
V_{CCCORE}	F14	Power/Other
V_{CCCORE}	F2	Power/Other
V_{CCCORE}	F22	Power/Other
V_{CCCORE}	F26	Power/Other
V_{CCCORE}	AA37	Power/Other

Table 49. PPGA Package Signal Listing in Order by Signal Name

Pin Name	Pin No.	Signal Buffer Type
VCC_{CORE}	AA5	Power/Other
VCC_{CORE}	AB2	Power/Other
VCC_{CORE}	AB34	Power/Other
VCC_{CORE}	AD32	Power/Other
VCC_{CORE}	AE5	Power/Other
VCC_{CORE}	AF2	Power/Other
VCC_{CORE}	AF34	Power/Other
VCC_{CORE}	AH24	Power/Other
VCC_{CORE}	AH32	Power/Other
VCC_{CORE}	AH36	Power/Other
VCC_{CORE}	AJ13	Power/Other
VCC_{CORE}	AJ17	Power/Other
VCC_{CORE}	AJ21	Power/Other
VCC_{CORE}	F30	Power/Other
VCC_{CORE}	F34	Power/Other
VCC_{CORE}	F4	Power/Other
VCC_{CORE}	H32	Power/Other
VCC_{CORE}	H36	Power/Other
VCC_{CORE}	J5	Power/Other
VCC_{CORE}	K2	Power/Other
VCC_{CORE}	K32	Power/Other
VCC_{CORE}	K34	Power/Other
VCC_{CORE}	M32	Power/Other
VCC_{CORE}	N5	Power/Other
VCC_{CORE}	P2	Power/Other
VCC_{CORE}	P34	Power/Other
VCC_{CORE}	R32	Power/Other
VCC_{CORE}	R36	Power/Other
VCC_{CORE}	S5	Power/Other
VCC_{CORE}	T2	Power/Other
VCC_{CORE}	T34	Power/Other
VCC_{CORE}	V32	Power/Other
VCC_{CORE}	V36	Power/Other
VCC_{CORE}	W5	Power/Other
VCC_{CORE}	X34	Power/Other
VCC_{CORE}	Y35	Power/Other
VCC_{CORE}	Z32	Power/Other
$VCORE_{DET}$	E21	Power/Other
VID0	AL35	Power/Other
VID1	AM36	Power/Other

Table 49. PPGA Package Signal Listing in Order by Signal Name

Pin Name	Pin No.	Signal Buffer Type
VID2	AL37	Power/Other
VID3	AJ37	Power/Other
VREF0	E33	Power/Other
VREF1	F18	Power/Other
VREF2	K4	Power/Other
VREF3	R6	Power/Other
VREF4	V6	Power/Other
VREF5	AD6	Power/Other
VREF6	AK12	Power/Other
VREF7	AK22	Power/Other
VSS	B16	Power/Other
VSS	B20	Power/Other
VSS	B24	Power/Other
VSS	B28	Power/Other
VSS	B32	Power/Other
VSS	B4	Power/Other
VSS	B8	Power/Other
VSS	D18	Power/Other
VSS	D2	Power/Other
VSS	D22	Power/Other
VSS	D26	Power/Other
VSS	D30	Power/Other
VSS	D34	Power/Other
VSS	D4	Power/Other
VSS	E11	Power/Other
VSS	E15	Power/Other
VSS	E19	Power/Other
VSS	E7	Power/Other
VSS	F20	Power/Other
VSS	F24	Power/Other
VSS	F28	Power/Other
VSS	F32	Power/Other
VSS	F36	Power/Other
VSS	G5	Power/Other
VSS	H2	Power/Other
VSS	H34	Power/Other
VSS	K36	Power/Other
VSS	L5	Power/Other
VSS	M2	Power/Other
VSS	M34	Power/Other

Table 49. PPGA Package Signal Listing in Order by Signal Name

Pin Name	Pin No.	Signal Buffer Type
Vss	P32	Power/Other
Vss	P36	Power/Other
Vss	Q5	Power/Other
Vss	R34	Power/Other
Vss	T32	Power/Other
Vss	T36	Power/Other
Vss	U5	Power/Other
Vss	V2	Power/Other
Vss	A37	Power/Other
Vss	AB32	Power/Other
Vss	AC33	Power/Other
Vss	AC5	Power/Other
Vss	AD2	Power/Other
Vss	AD34	Power/Other
Vss	AF32	Power/Other
Vss	AF36	Power/Other
Vss	AG5	Power/Other
Vss	AH2	Power/Other
Vss	AH34	Power/Other
Vss	AJ11	Power/Other
Vss	AJ15	Power/Other
Vss	AJ19	Power/Other
Vss	AJ23	Power/Other
Vss	AJ27	Power/Other
Vss	AJ3	Power/Other

Table 49. PPGA Package Signal Listing in Order by Signal Name

Pin Name	Pin No.	Signal Buffer Type
Vss	AJ7	Power/Other
Vss	AK36	Power/Other
Vss	AK4	Power/Other
Vss	AL1	Power/Other
Vss	AL3	Power/Other
Vss	AM10	Power/Other
Vss	AM14	Power/Other
Vss	AM18	Power/Other
Vss	AM2	Power/Other
Vss	AM22	Power/Other
Vss	AM26	Power/Other
Vss	AM30	Power/Other
Vss	AM34	Power/Other
Vss	AM6	Power/Other
Vss	AN3	Power/Other
Vss	B12	Power/Other
Vss	V34	Power/Other
Vss	X32	Power/Other
Vss	X36	Power/Other
Vss	Y37	Power/Other
Vss	Y5	Power/Other
Vss	Z2	Power/Other
Vss	Z34	Power/Other
Vss	AJ31	Power/Other
Vss	Y33	Power/Other

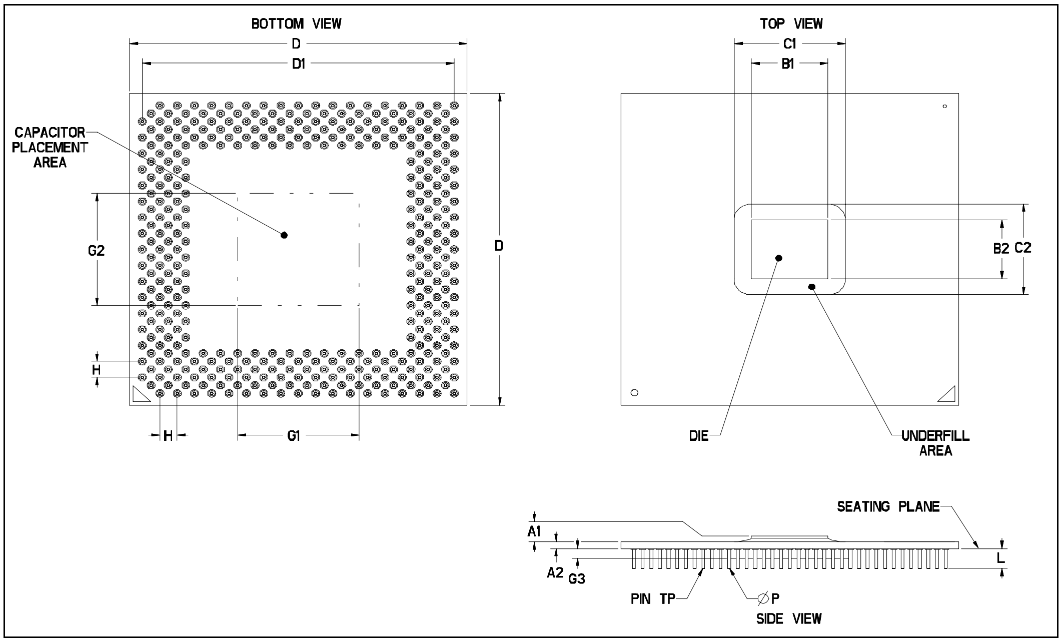
5.3 FC-PGA Package

This section defines the mechanical specifications and signal definitions for the Celeron processor in the FC-PGA package.

5.3.1 Materials Information

Figure 23 with package dimensions is provided to aid in the design of heatsink and clip solutions as well as demonstrate where pin-side capacitors will be located on the processor. Table 50 includes the measurements for these dimensions in both inches and millimeters.

Figure 23. Package Dimensions (FC-PGA Package)



NOTES:
1. Unless otherwise specified, the following drawings are dimensioned in inches.
2. All dimensions provided with tolerances are guaranteed to be met for all normal production product.
3. Figures and drawings labeled as “Reference Dimensions” are provided for informational purposes only. Reference dimensions are extracted from the mechanical design database and are nominal dimensions with no tolerance information applied. Reference dimensions are NOT checked as part of the processor manufacturing. Unless noted as such, dimensions in parentheses without tolerances are reference dimensions.
4. Drawing not to scale.

Table 50. Package Dimensions

Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A1	0.787	0.889		0.031	0.035	
A2	1.000	1.200		0.039	0.047	
B1	11.183	11.285		0.440	0.445	
B2	9.225	9.327		0.363	0.368	
C1	23.495 max			0.925 max		
C2	21.590 max			0.850 max		
D	49.428	49.632		1.946	1.954	
D1	45.466	45.947		1.790	1.810	
G1	0.000	17.780	1	0.000	0.700	
G2	0.000	17.780	1	0.000	0.700	
G3	0.000	0.889	1	0.000	0.035	
H	2.540		Nominal	0.100		Nominal
L	3.048	3.302		0.120	0.130	
φP	0.431	0.483		0.017	0.019	
Pin TP	0.508 Diametric True Position (Pin-to-Pin)			0.020 Diametric True Position (Pin-to-Pin)		

NOTES:
1. Capacitors and resistors may be placed on the pin-side of the FC-PGA package in the area defined by G1, G2, and G3. This area is a keepout zone for motherboard designers.

The bare processor die has mechanical load limits that should not be exceeded during heatsink assembly, mechanical stress testing, or standard drop and shipping conditions. The heatsink attach solution must not induce permanent stress into the processor substrate with the exception of a uniform load to maintain the heatsink to the processor thermal interface. The package dynamic and static loading parameters are listed in Table 51.

For Table 51, the following apply:

1. It is not recommended to use any portion of the processor substrate as a mechanical reference or load bearing surface for thermal solutions.
2. Parameters assume uniformly applied loads

Table 51. Processor Die Loading Parameters (FC-PGA Package)

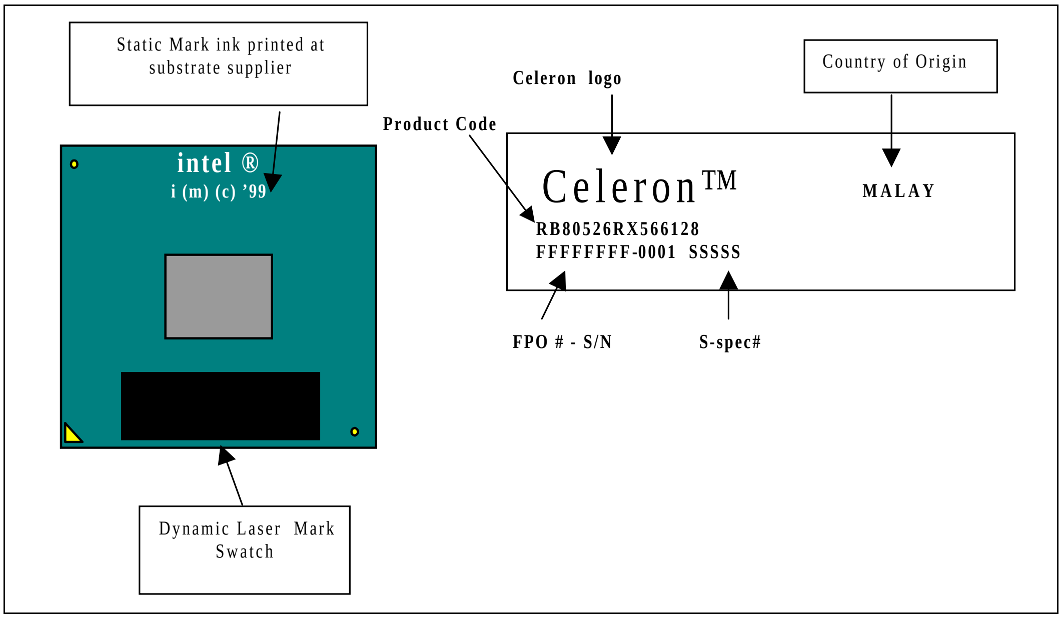
Parameter	Dynamic (max)[1]	Static (max)[2]	Unit
Silicon Die Surface	200	50	lbf
Silicon Die Edge	100	12	lbf

NOTES:
1. This specification applies to a uniform and a non-uniform load.
2. This is the maximum static force that can be applied by the heatsink and clip to maintain the heatsink and processor interface.

5.3.2 Processor Markings

Figure 24 exemplifies the processor top-side markings and it is provided to aid in the identification of an Pentium III processor for the PGA370 socket. Table 50 lists the measurements for the package dimensions.

Figure 24. Top Side Processor Markings (PPGA and FC-PGA Packages)



5.4 FC-PGA Signal List

Figure 25. Package Dimensions (FC-PGA Package)

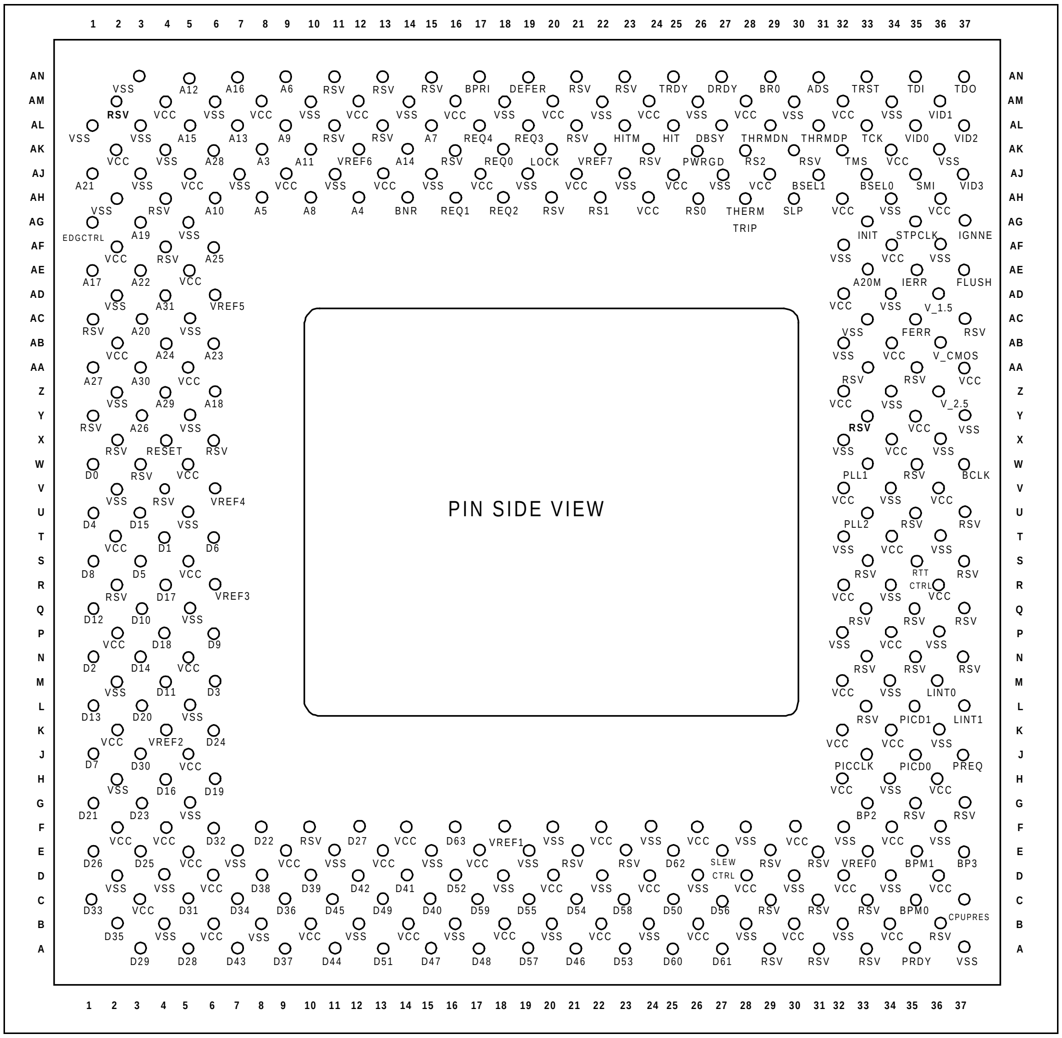


Table 52 and Table 53 provide the processor pin definitions. The signal locations on the PGA370 socket are to be used for signal routing, simulation, and component placement on the baseboard. Figure 25 provides a pin-side view of the Celeron FC-PGA processor pin-out.

Table 52. FC-PGA Signal Listing in Order by Signal Name

Pin Name	Pin	Signal Group
A3#	AK8	AGTL+ I/O
A4#	AH12	AGTL+ I/O
A5#	AH8	AGTL+ I/O
A6#	AN9	AGTL+ I/O
A7#	AL15	AGTL+ I/O
A8#	AH10	AGTL+ I/O
A9#	AL9	AGTL+ I/O
A10#	AH6	AGTL+ I/O
A11#	AK10	AGTL+ I/O
A12#	AN5	AGTL+ I/O
A13#	AL7	AGTL+ I/O
A14#	AK14	AGTL+ I/O
A15#	AL5	AGTL+ I/O
A16#	AN7	AGTL+ I/O
A17#	AE1	AGTL+ I/O
A18#	Z6	AGTL+ I/O
A19#	AG3	AGTL+ I/O
A20#	AC3	AGTL+ I/O
A21#	AJ1	AGTL+ I/O
A22#	AE3	AGTL+ I/O
A23#	AB6	AGTL+ I/O
A24#	AB4	AGTL+ I/O
A25#	AF6	AGTL+ I/O
A26#	Y3	AGTL+ I/O
A27#	AA1	AGTL+ I/O
A28#	AK6	AGTL+ I/O
A29#	Z4	AGTL+ I/O
A30#	AA3	AGTL+ I/O
A31#	AD4	AGTL+ I/O
A20M#	AE33	CMOS Input
ADS#	AN31	AGTL+ I/O
BCLK	W37	System Bus Clock
BNR#	AH14	AGTL+ I/O
BP2#	G33	AGTL+ I/O
BP3#	E37	AGTL+ I/O
BPM0#	C35	AGTL+ I/O
BPM1#	E35	AGTL+ I/O
BPRI#	AN17	AGTL+ Input
BR0#	AN29	AGTL+ I/O

Table 52. FC-PGA Signal Listing in Order by Signal Name

Pin Name	Pin	Signal Group
BSEL0	AJ33	CMOS I/O
BSEL1[5]	AJ31	Power/Other
CPUPRES#	C37	Power/Other
D0#	W1	AGTL+ I/O
D1#	T4	AGTL+ I/O
D2#	N1	AGTL+ I/O
D3#	M6	AGTL+ I/O
D4#	U1	AGTL+ I/O
D5#	S3	AGTL+ I/O
D6#	T6	AGTL+ I/O
D7#	J1	AGTL+ I/O
D8#	S1	AGTL+ I/O
D9#	P6	AGTL+ I/O
D10#	Q3	AGTL+ I/O
D11#	M4	AGTL+ I/O
D12#	Q1	AGTL+ I/O
D13#	L1	AGTL+ I/O
D14#	N3	AGTL+ I/O
D15#	U3	AGTL+ I/O
D16#	H4	AGTL+ I/O
D17#	R4	AGTL+ I/O
D18#	P4	AGTL+ I/O
D19#	H6	AGTL+ I/O
D20#	L3	AGTL+ I/O
D21#	G1	AGTL+ I/O
D22#	F8	AGTL+ I/O
D23#	G3	AGTL+ I/O
D24#	K6	AGTL+ I/O
D25#	E3	AGTL+ I/O
D26#	E1	AGTL+ I/O
D27#	F12	AGTL+ I/O
D28#	A5	AGTL+ I/O
D29#	A3	AGTL+ I/O
D30#	J3	AGTL+ I/O
D31#	C5	AGTL+ I/O
D32#	F6	AGTL+ I/O
D33#	C1	AGTL+ I/O
D34#	C7	AGTL+ I/O
D35#	B2	AGTL+ I/O

Table 52. FC-PGA Signal Listing in Order by Signal Name

Pin Name	Pin	Signal Group
D36#	C9	AGTL+ I/O
D37#	A9	AGTL+ I/O
D38#	D8	AGTL+ I/O
D39#	D10	AGTL+ I/O
D40#	C15	AGTL+ I/O
D41#	D14	AGTL+ I/O
D42#	D12	AGTL+ I/O
D43#	A7	AGTL+ I/O
D44#	A11	AGTL+ I/O
D45#	C11	AGTL+ I/O
D46#	A21	AGTL+ I/O
D47#	A15	AGTL+ I/O
D48#	A17	AGTL+ I/O
D49#	C13	AGTL+ I/O
D50#	C25	AGTL+ I/O
D51#	A13	AGTL+ I/O
D52#	D16	AGTL+ I/O
D53#	A23	AGTL+ I/O
D54#	C21	AGTL+ I/O
D55#	C19	AGTL+ I/O
D56#	C27	AGTL+ I/O
D57#	A19	AGTL+ I/O
D58#	C23	AGTL+ I/O
D59#	C17	AGTL+ I/O
D60#	A25	AGTL+ I/O
D61#	A27	AGTL+ I/O
D62#	E25	AGTL+ I/O
D63#	F16	AGTL+ I/O
DBSY#	AL27	AGTL+ I/O
DEFER#	AN19	AGTL+ Input
DRDY#	AN27	AGTL+ I/O
EDGCTRL [2]	AG1	Power/Other
FERR#	AC35	CMOS Output
FLUSH#	AE37	CMOS Input
GND	A37	Power/Other
GND	AB32	Power/Other
GND	AC5	Power/Other
GND	AC33	Power/Other
GND	AD2	Power/Other

Table 52. FC-PGA Signal Listing in Order by Signal Name

Pin Name	Pin	Signal Group
GND	AD34	Power/Other
GND	AF32	Power/Other
GND	AF36	Power/Other
GND	AG5	Power/Other
GND	AH2	Power/Other
GND	AH34	Power/Other
GND	AJ3	Power/Other
GND	AJ7	Power/Other
GND	AJ11	Power/Other
GND	AJ15	Power/Other
GND	AJ19	Power/Other
GND	AJ23	Power/Other
GND	AJ27	Power/Other
GND	AK4	Power/Other
GND	AK36	Power/Other
GND	AL1	Power/Other
GND	AL3	Power/Other
GND	AM6	Power/Other
GND	AM10	Power/Other
GND	AM14	Power/Other
GND	AM18	Power/Other
GND	AM22	Power/Other
GND	AM26	Power/Other
GND	AM30	Power/Other
GND	AM34	Power/Other
GND	AN3	Power/Other
GND	B4	Power/Other
GND	B8	Power/Other
GND	B12	Power/Other
GND	B16	Power/Other
GND	B20	Power/Other
GND	B24	Power/Other
GND	B28	Power/Other
GND	B32	Power/Other
GND	D2	Power/Other
GND	D4	Power/Other
GND	D18	Power/Other
GND	D22	Power/Other
GND	D26	Power/Other

Table 52. FC-PGA Signal Listing in Order by Signal Name

Pin Name	Pin	Signal Group
GND	D30	Power/Other
GND	D34	Power/Other
GND	E7	Power/Other
GND	E11	Power/Other
GND	E15	Power/Other
GND	E19	Power/Other
GND	F20	Power/Other
GND	F24	Power/Other
GND	F28	Power/Other
GND	F32	Power/Other
GND	F36	Power/Other
GND	G5	Power/Other
GND	H2	Power/Other
GND	H34	Power/Other
GND	K36	Power/Other
GND	L5	Power/Other
GND	M2	Power/Other
GND	M34	Power/Other
GND	P32	Power/Other
GND	P36	Power/Other
GND	Q5	Power/Other
GND	R34	Power/Other
GND	T32	Power/Other
GND	T36	Power/Other
GND	U5	Power/Other
GND	V2	Power/Other
GND	V34	Power/Other
GND	X32	Power/Other
Reserved	X34[8]	Reserved for future use
GND	X36	Power/Other
GND	Y5	Power/Other
GND	Y37	Power/Other
GND	Z2	Power/Other
GND	Z34	Power/Other
HIT#	AL25	AGTL+ I/O
HITM#	AL23	AGTL+ I/O
IERR#	AE35	CMOS Output
IGNNE#	AG37	CMOS Input
INIT#	AG33	CMOS Input

Table 52. FC-PGA Signal Listing in Order by Signal Name

Pin Name	Pin	Signal Group
LINT0/INTR	M36	CMOS Input
LINT1/NMI	L37	CMOS Input
LOCK#	AK20	AGTL+ I/O
PICCLK	J33	APIC Clock Input
PICD0	J35	APIC I/O
PICD1	L35	APIC I/O
PLL1	W33	Power/Other
PLL2	U33	Power/Other
PRDY#	A35	AGTL+ Output
PREQ#	J37	CMOS Input
PWRGOOD	AK26	CMOS Input
REQ0#	AK18	AGTL+ I/O
REQ1#	AH16	AGTL+ I/O
REQ2#	AH18	AGTL+ I/O
REQ3#	AL19	AGTL+ I/O
REQ4#	AL17	AGTL+ I/O
Reserved	A29	Reserved for future use
Reserved	A31	Reserved for future use
Reserved	A33	Reserved for future use
Reserved	AC1	Reserved for future use
Reserved	AC37	Reserved for future use
Reserved	AF4	Reserved for future use
Reserved	AH20	Reserved for future use
Reserved	AK16	Reserved for future use
Reserved	AK24	Reserved for future use
Reserved	AK30	Reserved for future use
Reserved	AL11	Reserved for future use
Reserved	AL13	Reserved for future use
Reserved	AL21	Reserved for future use
Reserved	AN11	Reserved for future use
Reserved	AN13	Reserved for future use
Reserved	AN15	Reserved for future use
Reserved	AN21	Reserved for future use
Reserved	AN23	Reserved for future use
Reserved	B36	Reserved for future use
Reserved	C29	Reserved for future use
Reserved	C31	Reserved for future use
Reserved	C33	Reserved for future use
Reserved	E23	Reserved for future use

Table 52. FC-PGA Signal Listing in Order by Signal Name

Pin Name	Pin	Signal Group
Reserved	E29	Reserved for future use
Reserved	E31	Reserved for future use
Reserved	F10	Reserved for future use
Reserved	G35	Reserved for future use
Reserved	G37	Reserved for future use
Reserved	L33	Reserved for future use
Reserved	N33	Reserved for future use
Reserved	N35	Reserved for future use
Reserved	N37	Reserved for future use
Reserved	Q33	Reserved for future use
Reserved	Q35	Reserved for future use
Reserved	Q37	Reserved for future use
Reserved	R2	Reserved for future use
Reserved	S33	Reserved for future use
Reserved	S37	Reserved for future use
Reserved	U35	Reserved for future use
Reserved	U37	Reserved for future use
Reserved	V4	Reserved for future use
Reserved	W3	Reserved for future use
Reserved	W35	Reserved for future use
Reserved	X6	Reserved for future use
Reserved	X20	Reserved for future use
Reserved	Y1	Reserved for future use
Reserved	AA33	Reserved for future use
Reserved	AA35	Reserved for future use
Reserved[3]	AM2	Reserved for future use
Reserved[4]	Y33	Reserved for future use
RESET#[6]	AH4	Power/Other
RESET#[7]	X4	Power/Other
RS0#	AH26	AGTL+ Input
RS1#	AH22	AGTL+ Input
RS2#	AK28	AGTL+ Input
RTTCTRL	S35	Power/Other
SLEWCTRL	E27	Power/Other
SLP#	AH30	CMOS Input
SMI#	AJ35	CMOS Input
STPCLK#	AG35	CMOS Input
TCK	AL33	TAP Input
TDI	AN35	TAP Input

Table 52. FC-PGA Signal Listing in Order by Signal Name

Pin Name	Pin	Signal Group
TDO	AN37	TAP Output
THERMDN	AL29	Power/Other
THERMDP	AL31	Power/Other
THERMTRIP#	AH28	CMOS Output
TMS	AK32	TAP Input
TRDY#	AN25	AGTL+ Input
TRST#	AN33	TAP Input
$V_{CC_{1.5}}$ [1]	AD36	Power/Other
$V_{CC_{2.5}}$	Z36	Power/Other
$V_{CC_{CMOS}}$	AB36	Power/Other
$V_{CC_{CORE}}$	AA5	Power/Other
$V_{CC_{CORE}}$	AA37	Power/Other
$V_{CC_{CORE}}$	AB2	Power/Other
$V_{CC_{CORE}}$	AB34	Power/Other
$V_{CC_{CORE}}$	AD32	Power/Other
$V_{CC_{CORE}}$	AE5	Power/Other
$V_{CC_{CORE}}$	AF2	Power/Other
$V_{CC_{CORE}}$	AF34	Power/Other
$V_{CC_{CORE}}$	AH24	Power/Other
$V_{CC_{CORE}}$	AH32	Power/Other
$V_{CC_{CORE}}$	AH36	Power/Other
$V_{CC_{CORE}}$	AJ5	Power/Other
$V_{CC_{CORE}}$	AJ9	Power/Other
$V_{CC_{CORE}}$	AJ13	Power/Other
$V_{CC_{CORE}}$	AJ17	Power/Other
$V_{CC_{CORE}}$	AJ21	Power/Other
$V_{CC_{CORE}}$	AJ25	Power/Other
$V_{CC_{CORE}}$	AJ29	Power/Other
$V_{CC_{CORE}}$	AK2	Power/Other
$V_{CC_{CORE}}$	AK34	Power/Other
$V_{CC_{CORE}}$	AM4	Power/Other
$V_{CC_{CORE}}$	AM8	Power/Other
$V_{CC_{CORE}}$	AM12	Power/Other
$V_{CC_{CORE}}$	AM16	Power/Other
$V_{CC_{CORE}}$	AM20	Power/Other
$V_{CC_{CORE}}$	AM24	Power/Other
$V_{CC_{CORE}}$	AM28	Power/Other
$V_{CC_{CORE}}$	AM32	Power/Other
$V_{CC_{CORE}}$	B6	Power/Other

Table 52. FC-PGA Signal Listing in Order by Signal Name

Pin Name	Pin	Signal Group
VCC$_{CORE}$	B10	Power/Other
VCC$_{CORE}$	B14	Power/Other
VCC$_{CORE}$	B18	Power/Other
VCC$_{CORE}$	B22	Power/Other
VCC$_{CORE}$	B26	Power/Other
VCC$_{CORE}$	B30	Power/Other
VCC$_{CORE}$	B34	Power/Other
VCC$_{CORE}$	C3	Power/Other
VCC$_{CORE}$	D6	Power/Other
VCC$_{CORE}$	D20	Power/Other
VCC$_{CORE}$	D24	Power/Other
VCC$_{CORE}$	D28	Power/Other
VCC$_{CORE}$	D32	Power/Other
VCC$_{CORE}$	D36	Power/Other
VCC$_{CORE}$	E5	Power/Other
VCC$_{CORE}$	E9	Power/Other
VCC$_{CORE}$	E13	Power/Other
VCC$_{CORE}$	E17	Power/Other
VCC$_{CORE}$	F2	Power/Other
VCC$_{CORE}$	F4	Power/Other
VCC$_{CORE}$	F14	Power/Other
VCC$_{CORE}$	F22	Power/Other
VCC$_{CORE}$	F26	Power/Other
VCC$_{CORE}$	F30	Power/Other
VCC$_{CORE}$	F34	Power/Other
VCC$_{CORE}$	H32	Power/Other
VCC$_{CORE}$	H36	Power/Other
VCC$_{CORE}$	J5	Power/Other
VCC$_{CORE}$	K2	Power/Other
VCC$_{CORE}$	K32	Power/Other
VCC$_{CORE}$	K34	Power/Other
VCC$_{CORE}$	M32	Power/Other
VCC$_{CORE}$	N5	Power/Other
VCC$_{CORE}$	P2	Power/Other
VCC$_{CORE}$	P34	Power/Other
VCC$_{CORE}$	R32	Power/Other
VCC$_{CORE}$	R36	Power/Other
VCC$_{CORE}$	S5	Power/Other
VCC$_{CORE}$	T2	Power/Other

Table 52. FC-PGA Signal Listing in Order by Signal Name

Pin Name	Pin	Signal Group
VCC$_{CORE}$	T34	Power/Other
VCC$_{CORE}$	V32	Power/Other
VCC$_{CORE}$	V36	Power/Other
VCC$_{CORE}$	W5	Power/Other
VCC$_{CORE}$	Y35	Power/Other
VCC$_{CORE}$	Z32	Power/Other
VCORE_DET	E21	Power/Other
VID0	AL35	Power/Other
VID1	AM36	Power/Other
VID2	AL37	Power/Other
VID3	AJ37	Power/Other
VREF0	E33	Power/Other
VREF1	F18	Power/Other
VREF2	K4	Power/Other
VREF3	R6	Power/Other
VREF4	V6	Power/Other
VREF5	AD6	Power/Other
VREF6	AK12	Power/Other
VREF7	AK22	Power/Other

NOTES:
1. VCC$_{1.5}$ must be supplied by the same voltage source supplying VTT on the motherboard.
2. Previously this pin functioned as the EDGCTRL signal.
3. Previously, PGA370 designs defined this pin as a GND. For flexible PGA370 designs, it must be left unconnected (N/C).
4. Previously, PGA370 designs defined this pin as a GND.
5. Celeron processor in the FC-PGA package does not make use of this pin.
6. This pin is only reset for processors with a CPUID of 0686h. For previous Celeron processors prior to 0686h (not including 0686h) this pin is reserved.
7. This pin is reserved for Celeron processors with a CPUID of 0686h.
8. For Celeron processors with a CPUID = 0683h, this pin is a CLKREF signal.

Table 53. FC-PGA Signal Listing in Order by Pin Number

Pin No.	Pin Name	Signal Group
A3	D29#	AGTL+ I/O
A5	D28#	AGTL+ I/O
A7	D43#	AGTL+ I/O
A9	D37#	AGTL+ I/O
A11	D44#	AGTL+ I/O
A13	D51#	AGTL+ I/O
A15	D47#	AGTL+ I/O
A17	D48#	AGTL+ I/O
A19	D57#	AGTL+ I/O
A21	D46#	AGTL+ I/O
A23	D53#	AGTL+ I/O
A25	D60#	AGTL+ I/O
A27	D61#	AGTL+ I/O
A29	Reserved	Reserved for future use
A31	Reserved	Reserved for future use
A33	Reserved	Reserved for future use
A35	PRDY#	AGTL+ Output
A37	GND	Power/Other
AA1	A27#	AGTL+ I/O
AA3	A30#	AGTL+ I/O
AA5	$V_{CC_{CORE}}$	Power/Other
AA33	Reserved	Reserved for future use
AA35	Reserved	Reserved for future use
AA37	$V_{CC_{CORE}}$	Power/Other
AB2	$V_{CC_{CORE}}$	Power/Other
AB4	A24#	AGTL+ I/O
AB6	A23#	AGTL+ I/O
AB32	GND	Power/Other
AB34	$V_{CC_{CORE}}$	Power/Other
AB36	$V_{CC_{CMOS}}$	Power/Other
AC1	Reserved	Reserved for future use
AC3	A20#	AGTL+ I/O
AC5	GND	Power/Other
AC33	GND	Power/Other
AC35	FERR#	CMOS Output
AC37	Reserved	Reserved for future use
AD2	GND	Power/Other
AD4	A31#	AGTL+ I/O
AD6	VREF5	Power/Other

Table 53. FC-PGA Signal Listing in Order by Pin Number

Pin No.	Pin Name	Signal Group
AD32	$V_{CC_{CORE}}$	Power/Other
AD34	GND	Power/Other
AD36	$V_{CC_{1.5}}$ [1]	Power/Other
AE1	A17#	AGTL+ I/O
AE3	A22#	AGTL+ I/O
AE5	$V_{CC_{CORE}}$	Power/Other
AE33	A20M#	CMOS Input
AE35	IERR#	CMOS Output
AE37	FLUSH#	CMOS Input
AF2	$V_{CC_{CORE}}$	Power/Other
AF4	Reserved	Reserved for future use
AF6	A25#	AGTL+ I/O
AF32	GND	Power/Other
AF34	$V_{CC_{CORE}}$	Power/Other
AF36	GND	Power/Other
AG1	EDGCTRL [2]	Power/Other
AG3	A19#	AGTL+ I/O
AG5	GND	Power/Other
AG33	INIT#	CMOS Input
AG35	STPCLK#	CMOS Input
AG37	IGNNE#	CMOS Input
AH2	GND	Power/Other
AH4	RESET#[6]	Power/Other
AH6	A10#	AGTL+ I/O
AH8	A5#	AGTL+ I/O
AH10	A8#	AGTL+ I/O
AH12	A4#	AGTL+ I/O
AH14	BNR#	AGTL+ I/O
AH16	REQ1#	AGTL+ I/O
AH18	REQ2#	AGTL+ I/O
AH20	Reserved	Reserved for future use
AH22	RS1#	AGTL+ Input
AH24	$V_{CC_{CORE}}$	Power/Other
AH26	RS0#	AGTL+ Input
AH28	THERMTRIP#	CMOS Output
AH30	SLP#	CMOS Input
AH32	$V_{CC_{CORE}}$	Power/Other
AH34	GND	Power/Other
AH36	$V_{CC_{CORE}}$	Power/Other

Table 53. FC-PGA Signal Listing in Order by Pin Number

Pin No.	Pin Name	Signal Group
AJ1	A21#	AGTL+ I/O
AJ3	GND	Power/Other
AJ5	$V_{CC_{CORE}}$	Power/Other
AJ7	GND	Power/Other
AJ9	$V_{CC_{CORE}}$	Power/Other
AJ11	GND	Power/Other
AJ13	$V_{CC_{CORE}}$	Power/Other
AJ15	GND	Power/Other
AJ17	$V_{CC_{CORE}}$	Power/Other
AJ19	GND	Power/Other
AJ21	$V_{CC_{CORE}}$	Power/Other
AJ23	GND	Power/Other
AJ25	$V_{CC_{CORE}}$	Power/Other
AJ27	GND	Power/Other
AJ29	$V_{CC_{CORE}}$	Power/Other
AJ31	BSEL1[5]	Power/Other
AJ33	BSEL0	CMOS I/O
AJ35	SMI#	CMOS Input
AJ37	VID3	Power/Other
AK2	$V_{CC_{CORE}}$	Power/Other
AK4	GND	Power/Other
AK6	A28#	AGTL+ I/O
AK8	A3#	AGTL+ I/O
AK10	A11#	AGTL+ I/O
AK12	$V_{REF}6$	Power/Other
AK14	A14#	AGTL+ I/O
AK16	Reserved	Reserved for future use
AK18	REQ0#	AGTL+ I/O
AK20	LOCK#	AGTL+ I/O
AK22	$V_{REF}7$	Power/Other
AK24	Reserved	Reserved for future use
AK26	PWRGOOD	CMOS Input
AK28	RS2#	AGTL+ Input
AK30	Reserved	Reserved for future use
AK32	TMS	TAP Input
AK34	$V_{CC_{CORE}}$	Power/Other
AK36	GND	Power/Other
AL1	GND	Power/Other
AL3	GND	Power/Other

Table 53. FC-PGA Signal Listing in Order by Pin Number

Pin No.	Pin Name	Signal Group
AL5	A15#	AGTL+ I/O
AL7	A13#	AGTL+ I/O
AL9	A9#	AGTL+ I/O
AL11	Reserved	Reserved for future use
AL13	Reserved	Reserved for future use
AL15	A7#	AGTL+ I/O
AL17	REQ4#	AGTL+ I/O
AL19	REQ3#	AGTL+ I/O
AL21	Reserved	Reserved for future use
AL23	HITM#	AGTL+ I/O
AL25	HIT#	AGTL+ I/O
AL27	DBSY#	AGTL+ I/O
AL29	THERMDN	Power/Other
AL31	THERMDP	Power/Other
AL33	TCK	TAP Input
AL35	VID0	Power/Other
AL37	VID2	Power/Other
AM2	Reserved[3]	Reserved for future use
AM4	$V_{CC_{CORE}}$	Power/Other
AM6	GND	Power/Other
AM8	$V_{CC_{CORE}}$	Power/Other
AM10	GND	Power/Other
AM12	$V_{CC_{CORE}}$	Power/Other
AM14	GND	Power/Other
AM16	$V_{CC_{CORE}}$	Power/Other
AM18	GND	Power/Other
AM20	$V_{CC_{CORE}}$	Power/Other
AM22	GND	Power/Other
AM24	$V_{CC_{CORE}}$	Power/Other
AM26	GND	Power/Other
AM28	$V_{CC_{CORE}}$	Power/Other
AM30	GND	Power/Other
AM32	$V_{CC_{CORE}}$	Power/Other
AM34	GND	Power/Other
AM36	VID1	Power/Other
AN3	GND	Power/Other
AN5	A12#	AGTL+ I/O
AN7	A16#	AGTL+ I/O
AN9	A6#	AGTL+ I/O

Table 53. FC-PGA Signal Listing in Order by Pin Number

Pin No.	Pin Name	Signal Group
AN11	Reserved	Reserved for future use
AN13	Reserved	Reserved for future use
AN15	Reserved	Reserved for future use
AN17	BPRI#	AGTL+ Input
AN19	DEFER#	AGTL+ Input
AN21	Reserved	Reserved for future use
AN23	Reserved	Reserved for future use
AN25	TRDY#	AGTL+ Input
AN27	DRDY#	AGTL+ I/O
AN29	BR0#	AGTL+ I/O
AN31	ADS#	AGTL+ I/O
AN33	TRST#	TAP Input
AN35	TDI	TAP Input
AN37	TDO	TAP Output
B2	D35#	AGTL+ I/O
B4	GND	Power/Other
B6	$V_{CC_{CORE}}$	Power/Other
B8	GND	Power/Other
B10	$V_{CC_{CORE}}$	Power/Other
B12	GND	Power/Other
B14	$V_{CC_{CORE}}$	Power/Other
B16	GND	Power/Other
B18	$V_{CC_{CORE}}$	Power/Other
B20	GND	Power/Other
B22	$V_{CC_{CORE}}$	Power/Other
B24	GND	Power/Other
B26	$V_{CC_{CORE}}$	Power/Other
B28	GND	Power/Other
B30	$V_{CC_{CORE}}$	Power/Other
B32	GND	Power/Other
B34	$V_{CC_{CORE}}$	Power/Other
B36	Reserved	Reserved for future use
C1	D33#	AGTL+ I/O
C3	$V_{CC_{CORE}}$	Power/Other
C5	D31#	AGTL+ I/O
C7	D34#	AGTL+ I/O
C9	D36#	AGTL+ I/O
C11	D45#	AGTL+ I/O
C13	D49#	AGTL+ I/O

Table 53. FC-PGA Signal Listing in Order by Pin Number

Pin No.	Pin Name	Signal Group
C15	D40#	AGTL+ I/O
C17	D59#	AGTL+ I/O
C19	D55#	AGTL+ I/O
C21	D54#	AGTL+ I/O
C23	D58#	AGTL+ I/O
C25	D50#	AGTL+ I/O
C27	D56#	AGTL+ I/O
C29	Reserved	Reserved for future use
C31	Reserved	Reserved for future use
C33	Reserved	Reserved for future use
C35	BPM0#	AGTL+ I/O
C37	CPUPRES#	Power/Other
D2	GND	Power/Other
D4	GND	Power/Other
D6	$V_{CC_{CORE}}$	Power/Other
D8	D38#	AGTL+ I/O
D10	D39#	AGTL+ I/O
D12	D42#	AGTL+ I/O
D14	D41#	AGTL+ I/O
D16	D52#	AGTL+ I/O
D18	GND	Power/Other
D20	$V_{CC_{CORE}}$	Power/Other
D22	GND	Power/Other
D24	$V_{CC_{CORE}}$	Power/Other
D26	GND	Power/Other
D28	$V_{CC_{CORE}}$	Power/Other
D30	GND	Power/Other
D32	$V_{CC_{CORE}}$	Power/Other
D34	GND	Power/Other
D36	$V_{CC_{CORE}}$	Power/Other
E1	D26#	AGTL+ I/O
E5	$V_{CC_{CORE}}$	Power/Other
E7	GND	Power/Other
E9	$V_{CC_{CORE}}$	Power/Other
E11	GND	Power/Other
E13	$V_{CC_{CORE}}$	Power/Other
E15	GND	Power/Other
E17	$V_{CC_{CORE}}$	Power/Other
E19	GND	Power/Other

Table 53. FC-PGA Signal Listing in Order by Pin Number

Pin No.	Pin Name	Signal Group
E21	VCORE_DET	Power/Other
E23	Reserved	Reserved for future use
E25	D62#	AGTL+ I/O
E27	SLEWCTRL	Power/Other
E29	Reserved	Reserved for future use
E3	D25#	AGTL+ I/O
E31	Reserved	Reserved for future use
E33	VREF0	Power/Other
E35	BPM1#	AGTL+ I/O
E37	BP3#	AGTL+ I/O
F2	VCC_{CORE}	Power/Other
F4	VCC_{CORE}	Power/Other
F6	D32#	AGTL+ I/O
F8	D22#	AGTL+ I/O
F10	Reserved	Reserved for future use
F12	D27#	AGTL+ I/O
F14	VCC_{CORE}	Power/Other
F16	D63#	AGTL+ I/O
F18	VREF1	Power/Other
F20	GND	Power/Other
F22	VCC_{CORE}	Power/Other
F24	GND	Power/Other
F26	VCC_{CORE}	Power/Other
F28	GND	Power/Other
F30	VCC_{CORE}	Power/Other
F32	GND	Power/Other
F34	VCC_{CORE}	Power/Other
F36	GND	Power/Other
G1	D21#	AGTL+ I/O
G3	D23#	AGTL+ I/O
G5	GND	Power/Other
G33	BP2#	AGTL+ I/O
G35	Reserved	Reserved for future use
G37	Reserved	Reserved for future use
H2	GND	Power/Other
H4	D16#	AGTL+ I/O
H6	D19#	AGTL+ I/O
H32	VCC_{CORE}	Power/Other
H34	GND	Power/Other

Table 53. FC-PGA Signal Listing in Order by Pin Number

Pin No.	Pin Name	Signal Group
H36	VCC_{CORE}	Power/Other
J1	D7#	AGTL+ I/O
J3	D30#	AGTL+ I/O
J5	VCC_{CORE}	Power/Other
J33	PICCLK	APIC Clock Input
J35	PICD0	APIC I/O
J37	PREQ#	CMOS Input
K2	VCC_{CORE}	Power/Other
K4	VREF2	Power/Other
K6	D24#	AGTL+ I/O
K32	VCC_{CORE}	Power/Other
K34	VCC_{CORE}	Power/Other
K36	GND	Power/Other
L1	D13#	AGTL+ I/O
L3	D20#	AGTL+ I/O
L5	GND	Power/Other
L33	Reserved	Reserved for future use
L35	PICD1	APIC I/O
L37	LINT1/NMI	CMOS Input
M2	GND	Power/Other
M4	D11#	AGTL+ I/O
M6	D3#	AGTL+ I/O
M32	VCC_{CORE}	Power/Other
M34	GND	Power/Other
M36	LINT0/INTR	CMOS Input
N1	D2#	AGTL+ I/O
N3	D14#	AGTL+ I/O
N5	VCC_{CORE}	Power/Other
N33	Reserved	Reserved for future use
N35	Reserved	Reserved for future use
N37	Reserved	Reserved for future use
P2	VCC_{CORE}	Power/Other
P4	D18#	AGTL+ I/O
P6	D9#	AGTL+ I/O
P32	GND	Power/Other
P34	VCC_{CORE}	Power/Other
P36	GND	Power/Other
Q1	D12#	AGTL+ I/O
Q3	D10#	AGTL+ I/O

Table 53. FC-PGA Signal Listing in Order by Pin Number

Pin No.	Pin Name	Signal Group
Q5	GND	Power/Other
Q33	Reserved	Reserved for future use
Q35	Reserved	Reserved for future use
Q37	Reserved	Reserved for future use
R2	Reserved	Reserved for future use
R4	D17#	AGTL+ I/O
R6	VREF3	Power/Other
R32	$V_{CC_{CORE}}$	Power/Other
R34	GND	Power/Other
R36	$V_{CC_{CORE}}$	Power/Other
S1	D8#	AGTL+ I/O
S3	D5#	AGTL+ I/O
S5	$V_{CC_{CORE}}$	Power/Other
S33	Reserved	Reserved for future use
S35	RTTCTRL	Power/Other
S37	Reserved	Reserved for future use
T2	$V_{CC_{CORE}}$	Power/Other
T4	D1#	AGTL+ I/O
T6	D6#	AGTL+ I/O
T32	GND	Power/Other
T34	$V_{CC_{CORE}}$	Power/Other
T36	GND	Power/Other
U1	D4#	AGTL+ I/O
U3	D15#	AGTL+ I/O
U5	GND	Power/Other
U33	PLL2	Power/Other
U35	Reserved	Reserved for future use
U37	Reserved	Reserved for future use
V2	GND	Power/Other
V4	Reserved	Reserved for future use
V6	VREF4	Power/Other
V32	$V_{CC_{CORE}}$	Power/Other
V34	GND	Power/Other
V36	$V_{CC_{CORE}}$	Power/Other
W1	D0#	AGTL+ I/O
W3	Reserved	Reserved for future use
W5	$V_{CC_{CORE}}$	Power/Other
W33	PLL1	Power/Other
W35	Reserved	Reserved for future use

Table 53. FC-PGA Signal Listing in Order by Pin Number

Pin No.	Pin Name	Signal Group
W37	BCLK	System Bus Clock
X4	RESET#[7]	Power/Other
X6	Reserved	Reserved for future use
X20	Reserved	Reserved for future use
X32	GND	Power/Other
X34	Reserved[8]	Reserved for future use
X36	GND	Power/Other
Y1	Reserved	Reserved for future use
Y3	A26#	AGTL+ I/O
Y5	GND	Power/Other
Y33	Reserved[4]	Reserved for future use
Y35	$V_{CC_{CORE}}$	Power/Other
Y37	GND	Power/Other
Z2	GND	Power/Other
Z4	A29#	AGTL+ I/O
Z6	A18#	AGTL+ I/O
Z32	$V_{CC_{CORE}}$	Power/Other
Z34	GND	Power/Other
Z36	$V_{CC_{2.5}}$	Power/Other

NOTES:

1. $VCC_{1.5}$ must be supplied by the same voltage source supplying V_{TT} on the motherboard.
2. Previously this pin functioned as the EDGCTRL signal.
3. Previously, PGA370 designs defined this pin as a GND. For flexible PGA370 designs, it must be left unconnected (N/C).
4. Previously, PGA370 designs defined this pin as a GND.
5. Celeron processor in the FC-PGA package does not make use of this pin.
6. This pin is only reset for processors with a CPUID of 0686h. For previous Celeron processors prior to 0686h (not including 0686h) this pin is reserved.
7. This pin is reserved for Celeron processors with a CPUID of 0686h.
8. For Celeron processors with a CPUID = 0683h, this pin is a CLKREF signal.

5.5 Heatsink Volumetric Keepout Zone Guidelines

When designing a system platform it is necessary to ensure sufficient space is left for a heatsink to be installed without mechanical interference. Due to the large number of proprietary heatsink designs, Intel cannot specify a keepout zone that covers all passive and active-fan heatsinks. It is the system designer’s responsibility to consider their own proprietary solution when designing the desired keepout zone in their system platform. Please refer to the *Intel® Celeron™ Processor (PPGA) at 466 MHz Thermal Solutions Guidelines* (Order Number 245156) for further guidance.

Note: The heatsink keepout zones found in Section 6.0, “Boxed Processor Specifications” on page 105 refer specifically to the Boxed Processor’s active-fan heatsink. This does not reflect the worst-case dimensions that may exist with other third party passive or active-fan heatsinks. Contact your vendor of choice for their passive or active-fan heatsink dimensions to ensure that mechanical interference with system platform components does not occur.

6.0 Boxed Processor Specifications

The Celeron processor is also offered as an Intel boxed processor in the FC-PGA, PPGA, and S.E.P. Package. Intel boxed processors are intended for system integrators who build systems from motherboards and standard components. The boxed Celeron processor in the S.E.P. Package is supplied with an attached fan heatsink. The boxed Celeron processors in FC-PGA and PPGA packages are supplied with unattached fan heatsinks.

This section documents motherboard and system requirements for the fan heatsink that is supplied with the boxed Intel Celeron processor. This section is particularly important for OEMs that manufacture motherboards for system integrators. Unless otherwise noted, all figures in this section are dimensioned in inches.

Note: Drawings in this section reflect only the specifications of the Intel boxed processor product. These dimensions should not be used as a generic keepout zone for all heatsinks. It is the system designer's responsibility to consider their proprietary solution when designing to the required keepout zone on their system platform and chassis. Refer to the package specific *Thermal / Mechanical Solution Functional Specifications* for further guidance. Contact your local Intel Sales Representative for these documents.

6.1 Mechanical Specifications for the Boxed Intel® Celeron™ Processor

6.1.1 Mechanical Specifications for the S.E.P. Package

This section documents the mechanical specifications of the boxed Celeron processor fan heatsink in the S.E.P. Package. The boxed processor in the S.E.P. Package ships with an attached fan heatsink. Figure 26 shows a mechanical representation of the boxed Intel Celeron processor in a S.E.P. Package in the retention mechanism, which is not shipped with the boxed Intel Celeron processor.

The space requirements and dimensions for the boxed processor in the S.E.P. Package are shown in Figure 27 and Figure 28. Also, a conceptual attachment interface to low profile retention mechanism is shown in Figure 34.

Note: The heatsink airflow keepout zones found in Table 54 and Figure 34 refer specifically to the boxed processor's active fan heatsink. This does not reflect the worst-case dimensions that may exist with other third party passive or active fan heatsinks.

Figure 26. Retention Mechanism for the Boxed Intel® Celeron™ Processor in the S.E.P. Package

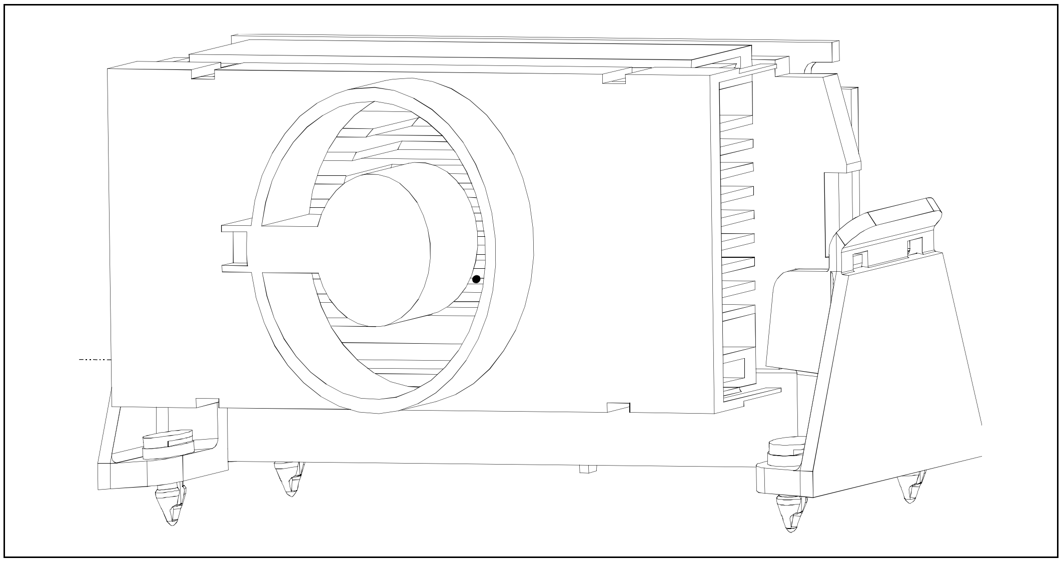


Figure 27. Side View Space Requirements for the Boxed Processor in the S.E.P. Package

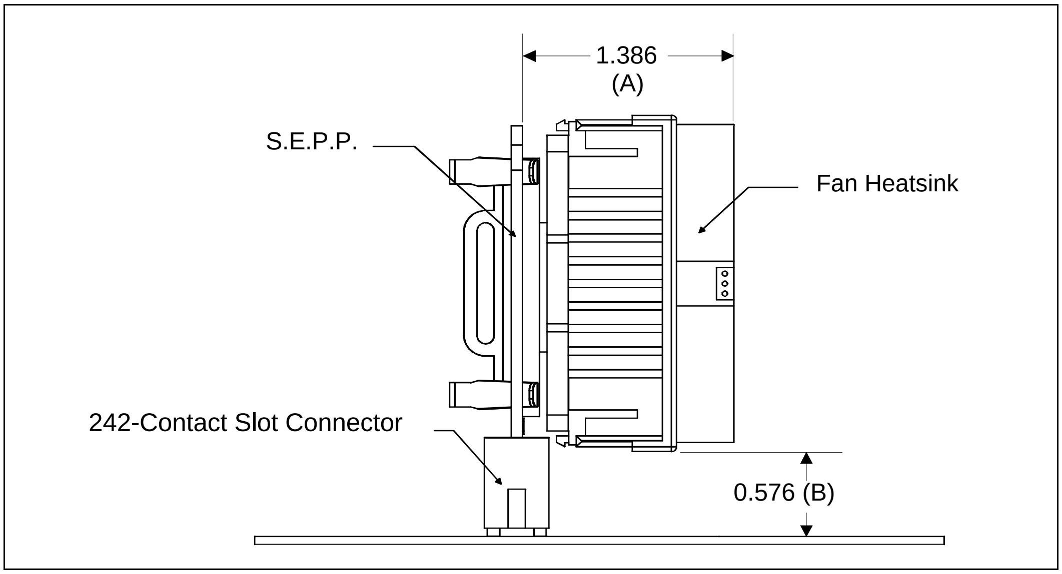


Figure 28. Front View Space Requirements for the Boxed Processor in the S.E.P. Package

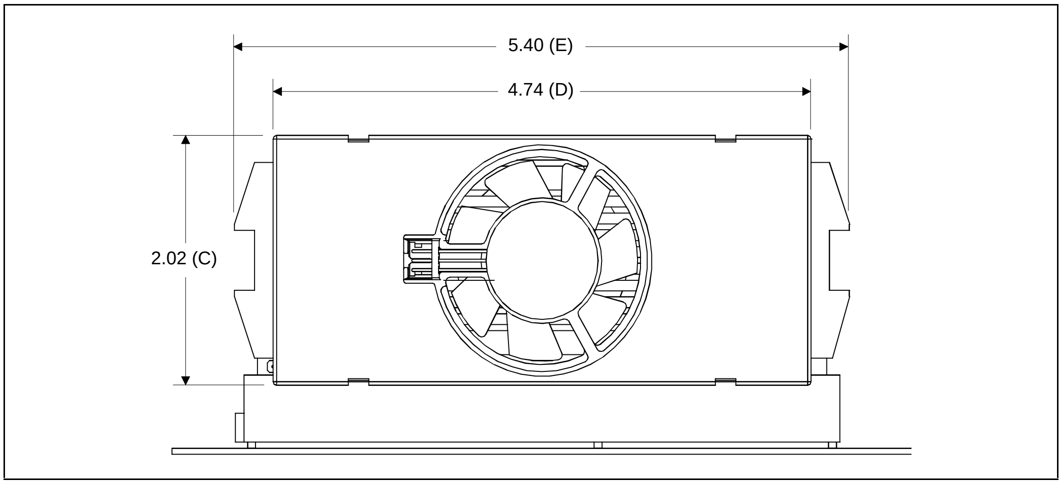


Table 54. Boxed Processor Fan Heatsink Spatial Dimensions for the S.E.P. Package

Fig. Ref. Label	Dimensions (Inches)	Min	Typ	Max
A	Fan Heatsink Depth (see Figure 25)			1.40
B	Fan Heatsink Height from Motherboard (see Figure 25)		0.58	
C	Fan Heatsink Height (see Figure 26)			2.00
D	Fan Heatsink Width (see Figure 26)			4.80
E	Fan Heatsink Base Width (see Figure 26)		5.4	
F	Airflow Keepout Zones from end of Fan Heatsink	0.4		
G	Airflow Keepout Zones from face of Fan Heatsink	0.2		

6.1.1.1 Boxed Processor Heatsink Weight

The heatsink for the boxed Intel Celeron processor in the S.E.P. Package will not weigh more than 225 grams.

6.1.1.2 Boxed Processor Retention Mechanism

The boxed Intel Celeron processor requires a S.E.P. Package retention mechanism to secure the processor in the 242-contact slot connector. A S.E.P. Package retention mechanism are provided with the boxed processor. Motherboards designed for use by system integrators should include a retention mechanism and appropriate installation instructions.

The boxed Intel Celeron processor does not require additional fan heatsink supports. Fan heatsink supports are not shipped with the boxed Intel Celeron processor.

Motherboards designed for flexible use by system integrators must still recognize the boxed Pentium II processor's fan heatsink clearance requirements, which are described in the *Pentium® II Processor at 233, 266, 300, and 333 MHz Datasheet* (Order Number 243335).

6.1.2 Mechanical Specifications for the PPGA Package

This section documents the mechanical specifications for the fan heatsink of the boxed Celeron processor in the PPGA package. The boxed processor in the PPGA package ships with an unattached fan heatsink which has an integrated clip. Figure 29 shows a mechanical representation of the boxed Intel Celeron processor in the PPGA package.

Note that the airflow of the fan heatsink is into the center and out of the sides of the fan heatsink. Clearance is required around the fan heatsink to ensure unimpeded airflow for proper cooling. The space requirements and dimensions for the boxed processor with an integrated fan heatsink are shown in Figure 30. All dimensions are in inches.

Note: The heatsink airflow keepout zones found in Figure 35 refer specifically to the boxed processor's active fan heatsink. This does not reflect the worst-case dimensions that may exist with other third party passive or active fan heatsinks.

Figure 29. Boxed Intel® Celeron™ Processor in the PPGA Package

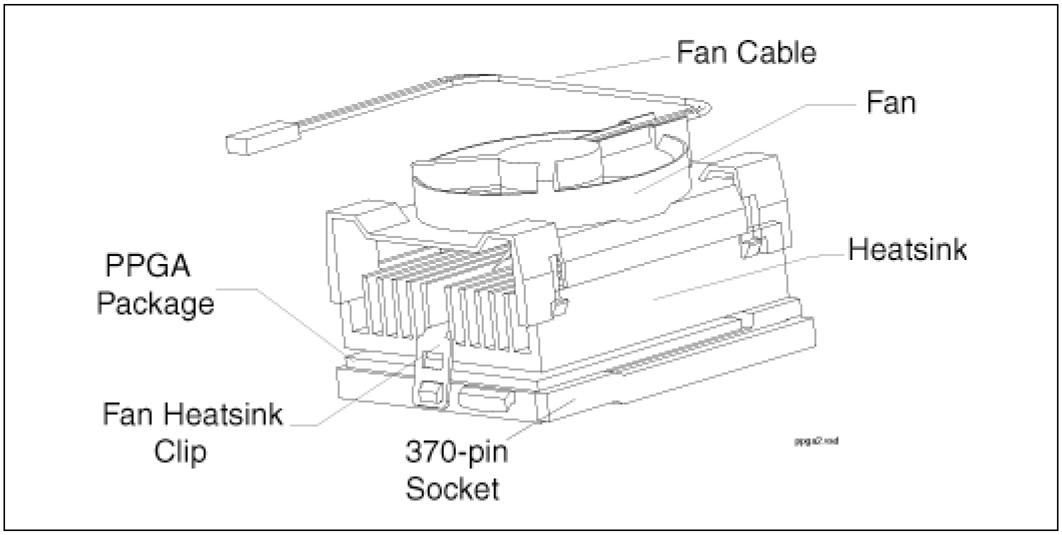
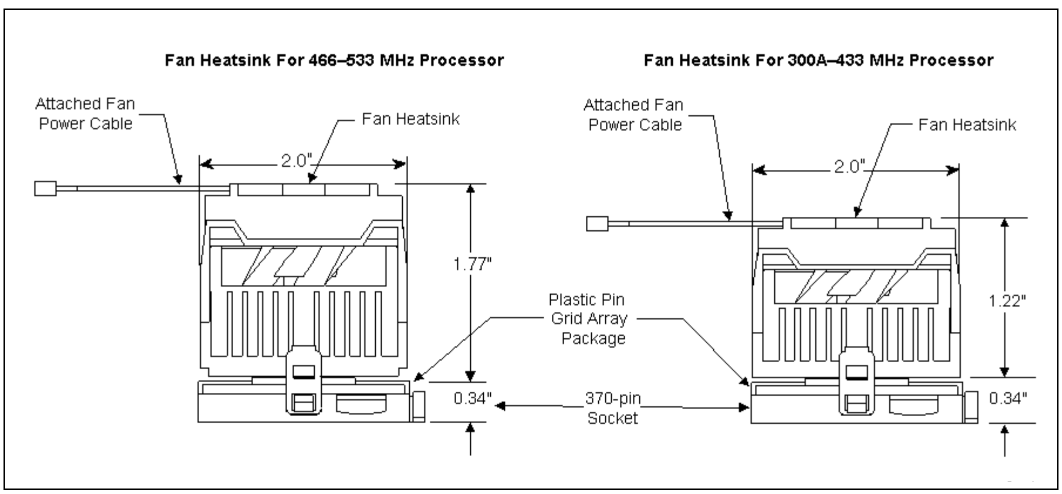


Figure 30. Side View Space Requirements for the Boxed Processor in the PPGA Package



6.1.2.1 Boxed Processor Heatsink Weight

The heatsink for the boxed Intel Celeron processor in the PPGA package will not weigh more than 180 grams.

6.1.3 Mechanical Specifications for the FC-PGA Package

This section documents the mechanical specifications of the fan heatsink for the boxed Intel Celeron processor in the FC-PGA (Flip-Chip Pin Grid Array) package. The boxed processor in the FC-PGA package ships with a fan heatsink which has an integrated clip. Figure 31 shows a mechanical representation of the boxed Intel Celeron processor in the FC-PGA package.

Figure 35 and Figure 37 show the REQUIRED keepout dimensions for the boxed processor thermal solution. The cooling fin orientation on the heatsink relative to the PGA-370 socket is subject to change. Contact your local Intel sales representative for documentation specific to the boxed fan heatsink orientation relative to the PGA-370 socket.

The fan heatsink is designed to allow visibility of the FC-PGA processor markings located on the top of the package. The FC-PGA processor markings are visible after installation of the fan heatsink due to notched sides of the heatsink base (See Figure 32). The boxed processor fan heatsink is also asymmetrical in that the mechanical step feature (specified in Figure 33) must sit over the socket's cam. The step allows the heatsink to securely interface with the processor in order to meet the processors thermal requirements.

Figure 31. Conceptual Drawing of the Boxed Intel® Celeron™ Processor in the 370-Pin Socket (FC-PGA Package)

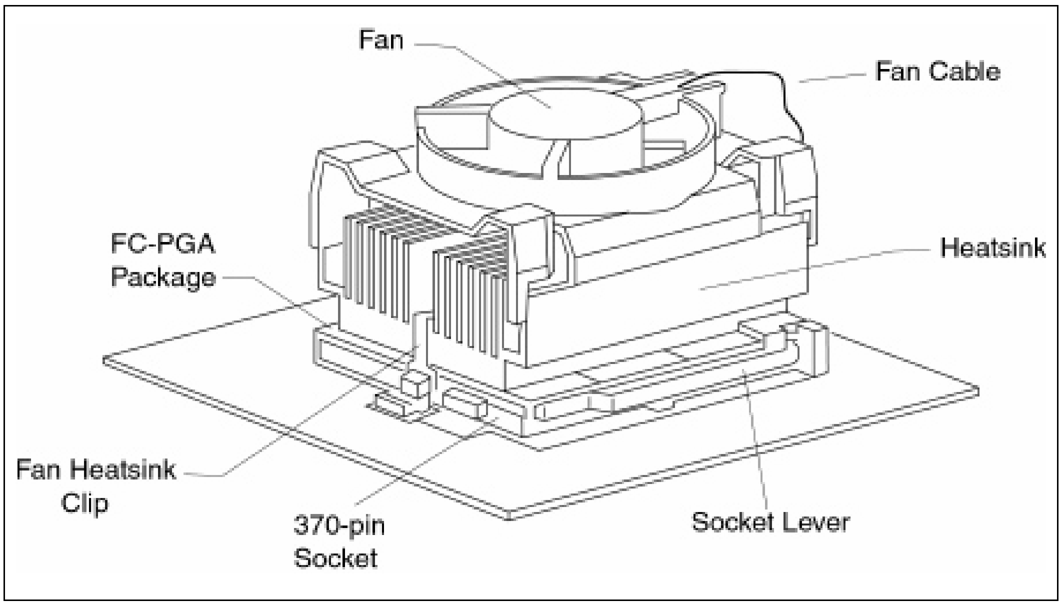


Figure 32. Dimensions of Notches in Heatsink Base

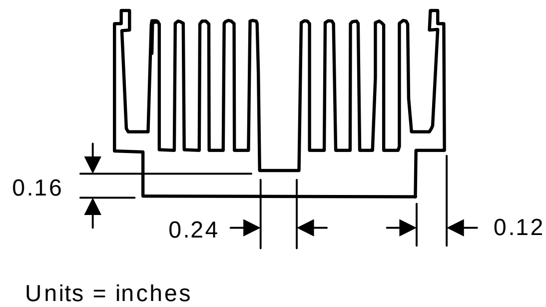
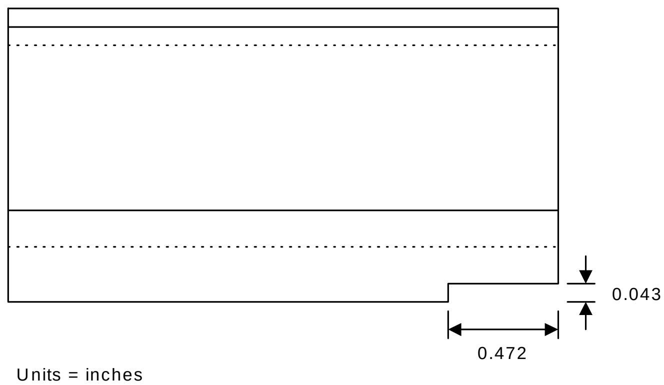


Figure 33. Dimensions of Mechanical Step Feature in Heatsink Base for the FC-PGA Package



6.1.3.1 Boxed Processor Heatsink Weight

The heatsink for the boxed Intel Celeron processor in the FC-PGA package will not weigh more than 180 grams.

6.2 Thermal Specifications

This section describes the cooling requirements of the fan heatsink solution utilized by the boxed processors.

6.2.1 Thermal Requirements for the Boxed Intel® Celeron™ Processor

6.2.1.1 Boxed Processor Cooling Requirements

The boxed processor is directly cooled with a fan heatsink. However, meeting the processor's temperature specification is also a function of the thermal design of the entire system, and ultimately the responsibility of the system integrator. The processor temperature specification is found in Section 4.0 of this document. The boxed processor fan heatsink is able to keep the processor temperature within the specifications (see Section 4.0) in chassis that provide good thermal management.

For the boxed processor fan heatsink to operate properly, it is critical that the airflow provided to the fan heatsink is unimpeded. Airflow of the fan heatsink is into the center and out of the sides of the fan heatsink. Airspace is required around the fan to ensure that the airflow through the fan heatsink is not blocked. Blocking the airflow to the fan heatsink reduces the cooling efficiency and decreases fan life. Figure 34 and Figure 35 illustrate an acceptable airspace clearance for the fan heatsink. It is also recommended that the air temperature entering the fan be kept below 45 °C. Again, meeting the processor's temperature specification is the responsibility of the system integrator. The processor temperature specification is found in Section 4.0 of this document.

Figure 34. Top View Airspace Requirements for the Boxed Processor in the S.E.P. Package

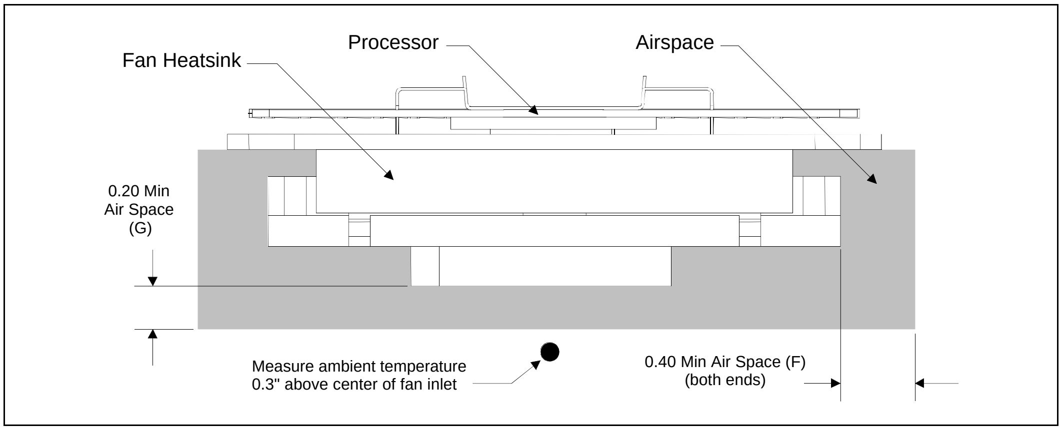


Figure 35. Side View Airspace Requirements for the Boxed Intel® Celeron™ Processor in the FC-PGA and PPGA Packages

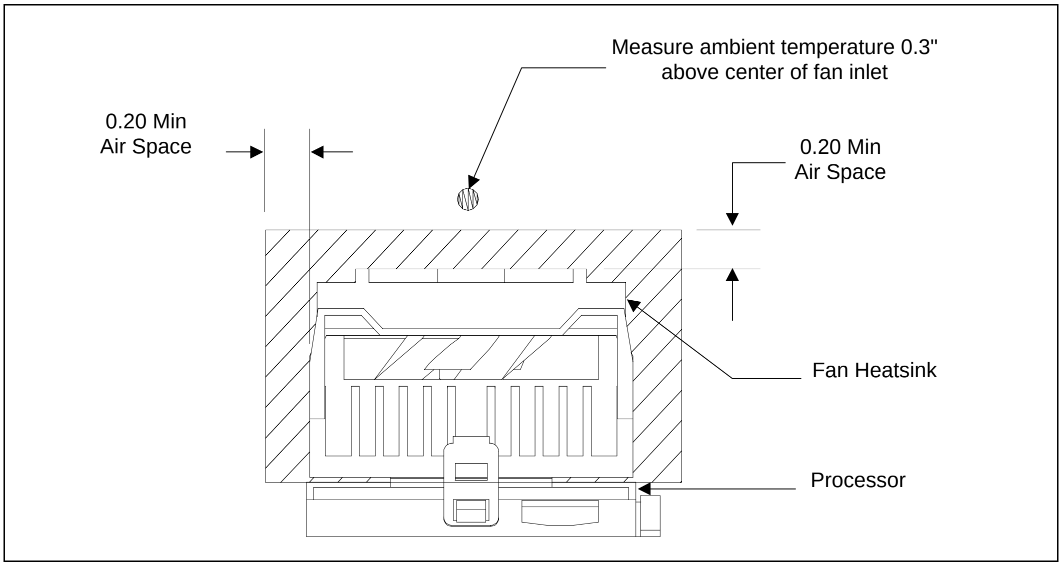
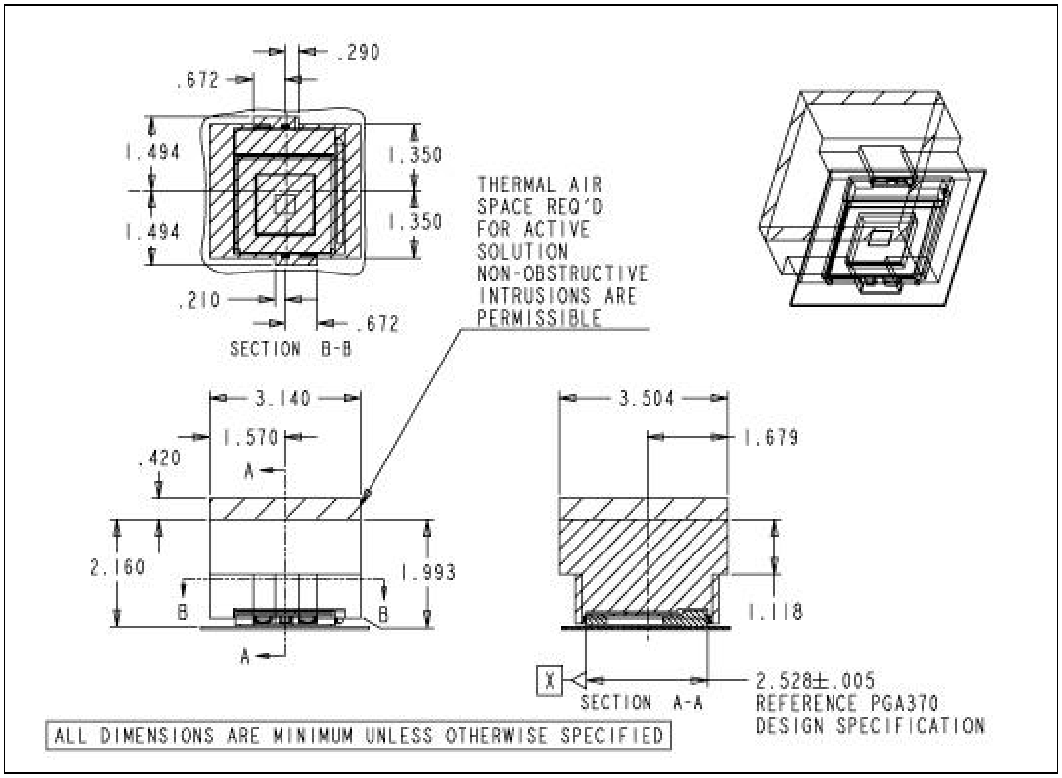


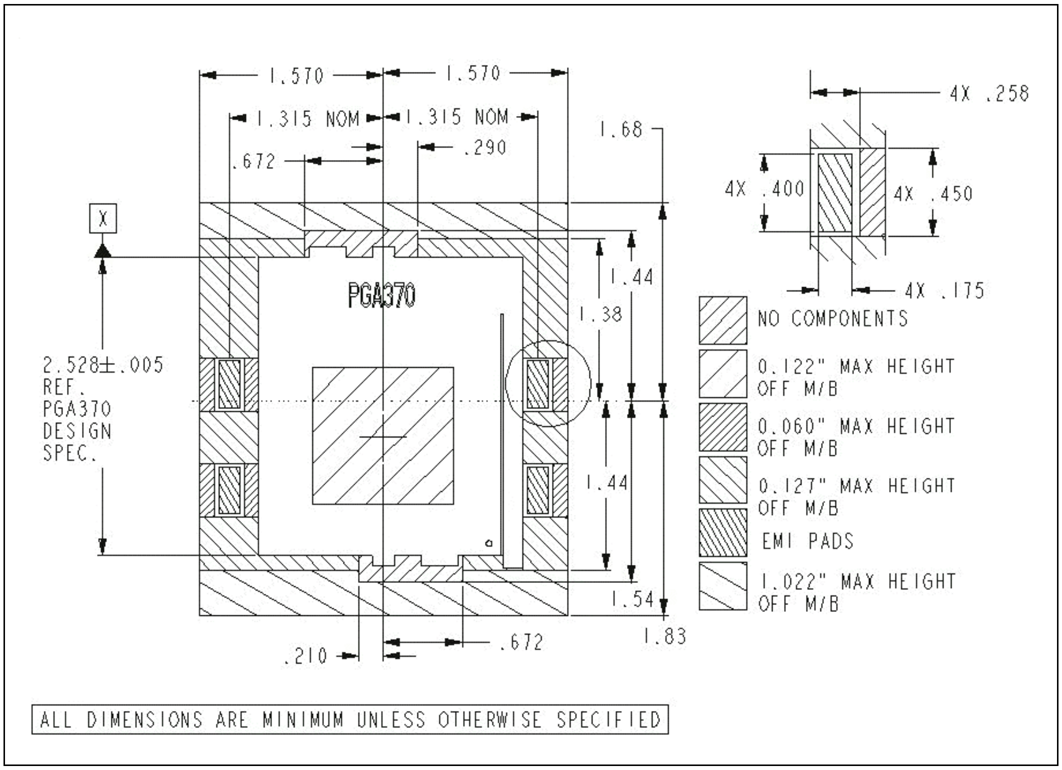
Figure 36. Volumetric Keepout Requirements for The Boxed Fan Heatsink



6.2.1.2 Boxed Processor Thermal Cooling Solution Clip

The boxed processor thermal solution requires installation by a system integrator to secure the thermal cooling solution to the processor after it is installed in the 370-pin socket ZIF socket. Motherboards designed for use by system integrators should take care to consider the implications of clip installation and potential scraping of the motherboard PCB underneath the 370-pin socket attach tabs. Motherboard components should not be placed too close to the 370-pin socket attach tabs in a way that interferes with the installation of the boxed processor thermal cooling solution (see Figure 37 for specifications).

Figure 37. Clip Keepout Requirements for the 370-Pin (Top View)



6.3 Electrical Requirements for the Boxed Intel® Celeron™ Processor

6.3.1 Electrical Requirements

The boxed processor's fan heatsink requires a +12 V power supply. A fan power cable is shipped with the boxed processor to draw power from a power header on the motherboard. The power cable connector and pin-out are shown in Figure 38. Motherboards must provide a matched power header to support the boxed processor. Table 55 contains specifications for the input and output signals at the fan heatsink connector. The fan heatsink outputs a SENSE signal (an open-collector output) that pulses at a rate of two pulses per fan revolution. A motherboard pull-up resistor provides V_{OH} to match the motherboard-mounted fan speed monitor requirements, if applicable. Use of the SENSE signal is optional. If the SENSE signal is not used, pin 3 of the connector should be tied to GND.

The boxed Intel Celeron processors in the PPGA package at 500 MHz and below are shipped with an unattached fan heatsink with two wire power-supply cables. These two wire fans do NOT support the motherboard-mounted fan speed monitor feature. The Intel Celeron processor at 533 MHz and above ship with unattached fan heatsinks that have three power-supply cables. These three wire fans DO support the motherboard-mounted fan speed monitor feature.

The power header on the baseboard must be positioned to allow the fan heatsink power cable to reach it. The power header identification and location should be documented in the motherboard documentation or on the motherboard. Figure 39 shows the recommended location of the fan power connector relative to the 242-contact slot connector. Figure 40 shows the recommended location of the fan power connector relative to the 370-pin socket. For the S.E.P. Package, the motherboard power header should be positioned within 4.75 inches (lateral) of the fan power connector. The motherboard power header should be positioned within 4.00 inches (lateral) of the fan power connector for the PPGA and FC-PGA packages.

Figure 38. Boxed Processor Fan Heatsink Power Cable Connector Description

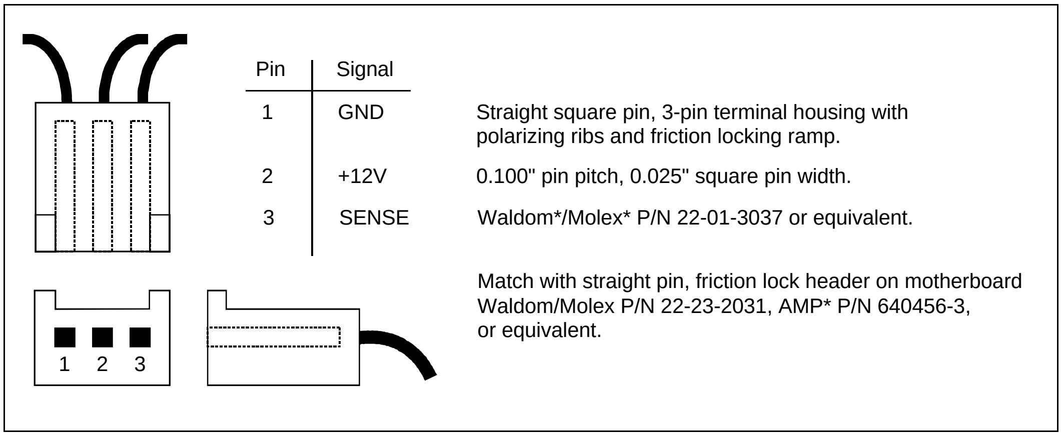


Table 55. Fan Heatsink Power and Signal Specifications

Description	Min	Typ	Max
+12V: 12 volt fan power supply	10.2V	12V	13.8V
IC: Fan current draw			100 mA
SENSE: SENSE frequency (motherboard should pull this pin up to appropriate Vcc with resistor)		2 pulses per fan revolution	

Figure 39. Motherboard Power Header Placement for the S.E.P. Package

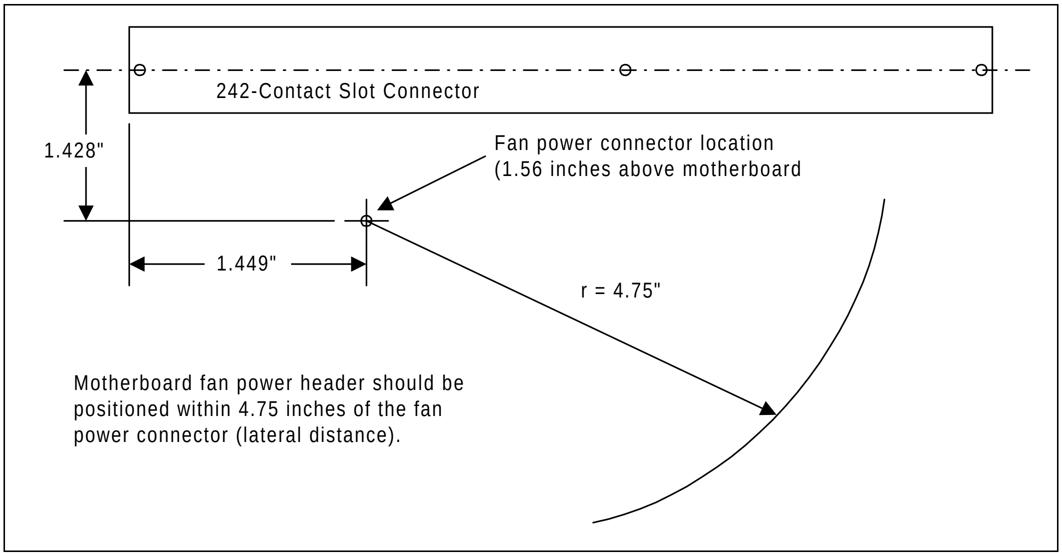
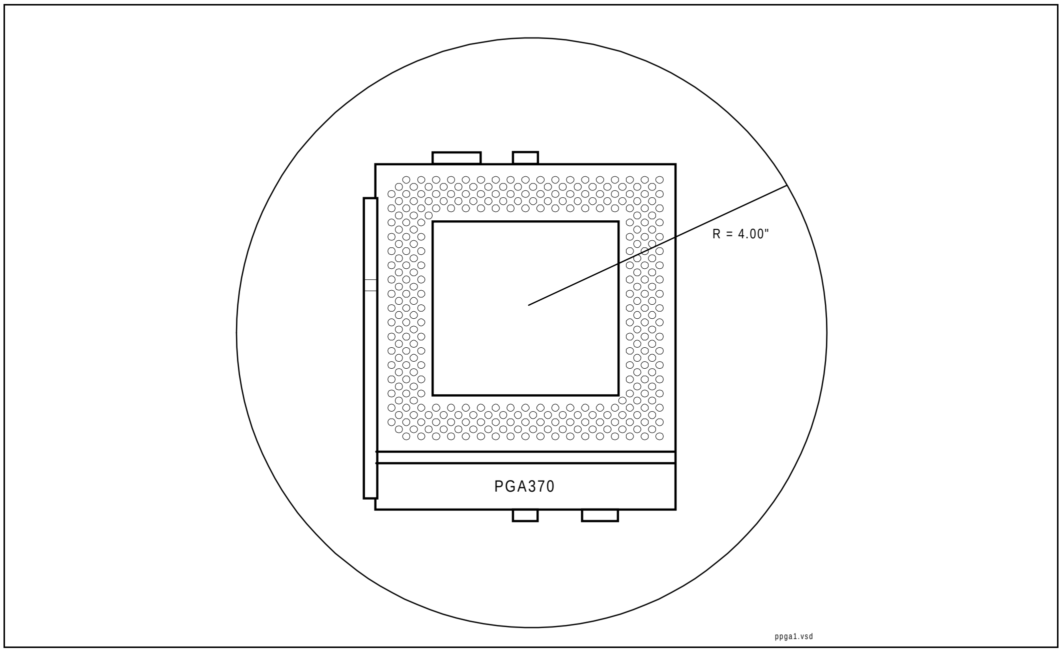


Figure 40. Motherboard Power Header Placement Relative to the 370-pin Socket



7.0 Processor Signal Description

Table 56 provides an alphabetical listing of all Celeron processor signals. The tables at the end of this section summarize the signals by direction (output, input, and I/O).

Note: Unless otherwise noted, the signals apply to S.E.P., PPGA, and FC-PGA Packages.

Table 56. Alphabetical Signal Reference (Sheet 1 of 7)

Signal	Type	Description
A[31:3]#	I/O	The A[31:3]# (Address) signals define a 2^{32}-byte physical memory address space. When ADS# is active, these pins transmit the address of a transaction; when ADS# is inactive, these pins transmit transaction type information. These signals must connect the appropriate pins of all agents on the Intel® Celeron™ processor system bus. The A[31:24]# signals are parity-protected by the AP1# parity signal, and the A[23:3]# signals are parity-protected by the AP0# parity signal. On the active-to-inactive transition of RESET#, the processors sample the A[31:3]# pins to determine their power-on configuration. See the *Pentium® II Processor Developer's Manual* (Order Number 243502) for details.
A20M#	I	If the A20M# (Address-20 Mask) input signal is asserted, the Intel Celeron processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1 MB boundary. Assertion of A20M# is only supported in real mode. A20M# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid along with the TRDY# assertion of the corresponding I/O Write bus transaction.
ADS#	I/O	The ADS# (Address Strobe) signal is asserted to indicate the validity of the transaction address on the A[31:3]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction. This signal must connect the appropriate pins on all Intel Celeron processor system bus agents.
BCLK	I	The BCLK (Bus Clock) signal determines the bus frequency. All Intel Celeron processor system bus agents must receive this signal to drive their outputs and latch their inputs on the BCLK rising edge. All external timing parameters are specified with respect to the BCLK signal.
BNR#	I/O	The BNR# (Block Next Request) signal is used to assert a bus stall by any bus agent who is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions. Since multiple agents might need to request a bus stall at the same time, BNR# is a wire-OR signal which must connect the appropriate pins of all Intel Celeron processor system bus agents. In order to avoid wire-OR glitches associated with simultaneous edge transitions driven by multiple drivers, BNR# is activated on specific clock edges and sampled on specific clock edges.
BP[3:2]#	I/O	The BP[3:2]# (Breakpoint) signals are outputs from the processor that indicate the status of breakpoints.
BPM[1:0]#	I/O	The BPM[1:0]# (Breakpoint Monitor) signals are breakpoint and performance monitor signals. They are outputs from the processor which indicate the status of breakpoints and programmable counters used for monitoring processor performance.

Table 56. Alphabetical Signal Reference (Sheet 2 of 7)

<table>
<tr><th>Signal</th><th>Type</th><th>Description</th></tr>
<tr><td>BPRI#</td><td>I</td><td>The BPRI# (Bus Priority Request) signal is used to arbitrate for ownership of the Intel Celeron processor system bus. It must connect the appropriate pins of all Intel Celeron processor system bus agents. Observing BPRI# active (as asserted by the priority agent) causes all other agents to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by deasserting BPRI#.</td></tr>
<tr><td>BSEL[1:0]</td><td>I/O</td><td>These signals are used to select the system bus frequency. The frequency is determined by the processor(s), chipset, and frequency synthesizer capabilities. All system bus agents must operate at the same frequency. Individual processors will only operate at their specified front side bus (FSB) frequency. On motherboards which support operation at either 66 MHz or 100 MHz, a BSEL[1:0] = “x1” will select a 100 MHz system bus frequency and a BSEL[1:0] = “x0” will select a 66 MHz system bus frequency.

These signals must be pulled up to 2.5 V or 3.3 V with 1 KΩ resistor and provided as a frequency selection signal to the clock driver/synthesizer. See Section 2.7.2 for implementation examples.

note: BSEL1 is not used by the Celeron processor.</td></tr>
<tr><td>BR0#</td><td>I/O</td><td>The BR0# (Bus Request) pin drives the BREQ[0]# signal in the system. During power-up configuration, the central agent asserts the BREQ0# bus signal in the system to assign the symmetric agent ID to the processor. The processor samples it’s BR0# pin on the active-to-inactive transition of RESET# to obtain it’s symmetric agent ID. The processor asserts BR0# to request the system bus.</td></tr>
<tr><td>CPUPRES#
(PPGA and FC-PGA only)</td><td>O</td><td>The CPUPRES# signal provides the ability for a system board to detect the presence of a processor. This pin is a ground on the processor indicating to the system that a processor is installed.

The CPUPRES# signal is defined to allow a system design to detect the presence of a terminator device or processor in a PGA370 socket. Combined with the VID combination of VID[3:0]= 1111 (see Section 2.5), a system can determine if a socket is occupied, and whether a processor core is present. See the table below for states and values for determining the presence of a device.

PGA370 Socket Occupation Truth Table
<table>
<tr><th>Signal</th><th>Value</th><th>Status</th></tr>
<tr><td>CPUPRES#
VID[3:0]</td><td>0
Anything other than ‘1111’</td><td>Processor core installed in the PGA370 socket.</td></tr>
<tr><td>CPUPRES#
VID[3:0]</td><td>0
1111</td><td>Terminator device installed in the PGA370 socket (i.e., no core present).</td></tr>
<tr><td>CPUPRES#
VID[3:0]</td><td>1
Any value</td><td>PGA370 socket not occupied.</td></tr>
</table></td></tr>
<tr><td>D[63:0]#</td><td>I/O</td><td>The D[63:0]# (Data) signals are the data signals. These signals provide a 64-bit data path between the Intel Celeron processor system bus agents, and must connect the appropriate pins on all such agents. The data driver asserts DRDY# to indicate a valid data transfer.</td></tr>
<tr><td>DBSY#</td><td>I/O</td><td>The DBSY# (Data Bus Busy) signal is asserted by the agent responsible for driving data on the Intel Celeron processor system bus to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must connect the appropriate pins on all Intel Celeron processor system bus agents.</td></tr>
<tr><td>DEFER#</td><td>I</td><td>The DEFER# signal is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or I/O agent. This signal must connect the appropriate pins of all Intel Celeron processor system bus agents.</td></tr>
</table>

Table 56. Alphabetical Signal Reference (Sheet 3 of 7)

Signal	Type	Description
DRDY#	I/O	The DRDY# (Data Ready) signal is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multicycle data transfer, DRDY# may be deasserted to insert idle clocks. This signal must connect the appropriate pins of all Intel Celeron processor system bus agents.
EDGCTRL	I	The EDGCTRL input provides AGTL+ edge control and should be pulled up to V_{CCCORE} with a 51 Ω ± 5% resistor. NOTE: This signal is NOT used on the FC-PGA package.
EMI (S.E.P.P. only)	I	EMI pins should be connected to motherboard ground and/or to chassis ground through zero ohm (0 Ω) resistors. The zero ohm resistors should be placed in close proximity to the Intel Celeron processor connector. The path to chassis ground should be short in length and have a low impedance. These pins are used for EMI management purposes.
FERR#	O	The FERR# (Floating-point Error) signal is asserted when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 387 coprocessor, and is included for compatibility with systems using MS-DOS*-type floating-point error reporting.
FLUSH#	I	When the FLUSH# input signal is asserted, the processor writes back all data in the Modified state from the internal cache and invalidates all internal cache lines. At the completion of this operation, the processor issues a Flush Acknowledge transaction. The processor does not cache any new data while the FLUSH# signal remains asserted. FLUSH# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid along with the TRDY# assertion of the corresponding I/O Write bus transaction. On the active-to-inactive transition of RESET#, the processor samples FLUSH# to determine its power-on configuration. See *Pentium® Pro Family Developer's Manual, Volume 1: Specifications* (Order Number 242690) for details.
HIT#, HITM#	I/O	The HIT# (Snoop Hit) and HITM# (Hit Modified) signals convey transaction snoop operation results, and must connect the appropriate pins of all Intel Celeron processor system bus agents. Any such agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.
IERR#	O	The IERR# (Internal Error) signal is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the Intel Celeron processor system bus. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#, BINIT#, or INIT#.
IGNNE#	I	The IGNNE# (Ignore Numeric Error) signal is asserted to force the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid along with the TRDY# assertion of the corresponding I/O Write bus transaction.
INIT#	I	The INIT# (Initialization) signal, when asserted, resets integer registers inside all processors without affecting their internal (L1) caches or floating-point registers. Each processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal and must connect the appropriate pins of all bus agents. If INIT# is sampled active on the active to inactive transition of RESET#, then the processor executes its Built-in Self-Test (BIST).

Table 56. Alphabetical Signal Reference (Sheet 4 of 7)

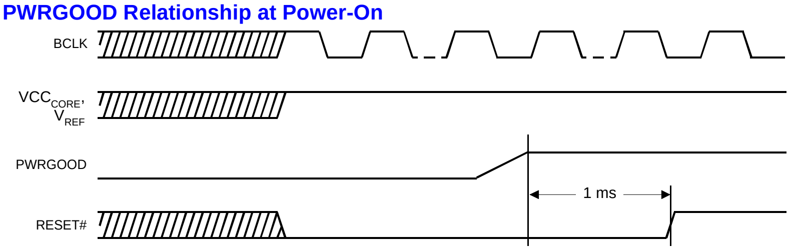
Signal	Type	Description
LINT[1:0]	I	The LINT[1:0] (Local APIC Interrupt) signals must connect the appropriate pins of all APIC Bus agents, including all processors and the core logic or I/O APIC component. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium® processor. Both signals are asynchronous. Both of these signals must be software configured via BIOS programming of the APIC register space to be used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.
LOCK#	I/O	The LOCK# signal indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of all system bus agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction end of the last transaction. When the priority agent asserts BPRI# to arbitrate for ownership of the system bus, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the system bus throughout the bus locked operation and ensure the atomicity of lock.
PICCLK	I	The PICCLK (APIC Clock) signal is an input clock to the processor and core logic or I/O APIC which is required for operation of all processors, core logic, and I/O APIC components on the APIC bus.
PICD[1:0]	I/O	The PICD[1:0] (APIC Data) signals are used for bidirectional serial message passing on the APIC bus, and must connect the appropriate pins of the Intel Celeron processor for proper initialization.
PLL1, PLL2 (PGA packages only)	I	All Intel Celeron processors have internal analog PLL clock generators that require quiet power supplies. PLL1 and PLL2 are inputs to the internal PLL and should be connected to $V_{CC_{CORE}}$ through a low-pass filter that minimizes jitter. See the platform design guide for implementation details.
PRDY#	O	The PRDY (Probe Ready) signal is a processor output used by debug tools to determine processor debug readiness.
PREQ#	I	The PREQ# (Probe Request) signal is used by debug tools to request debug operation of the processors.
PWRGOOD	I	The PWRGOOD (Power Good) signal is a 2.5 V tolerant processor input. The processor requires this signal to be a clean indication that the clocks and power supplies ($V_{CC_{CORE}}$, etc.) are stable and within their specifications. Clean implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high (2.5 V) state. Figure 39 illustrates the relationship of PWRGOOD to other system signals. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. It must also meet the minimum pulse width specification in Table 17 and Table 18, and be followed by a 1 ms RESET# pulse. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation. **PWRGOOD Relationship at Power-On** 

Table 56. Alphabetical Signal Reference (Sheet 5 of 7)

<table>
<tr><th>Signal</th><th>Type</th><th>Description</th></tr>
<tr><td>REQ[4:0]#</td><td>I/O</td><td>The REQ[4:0]# (Request Command) signals must connect the appropriate pins of all processor system bus agents. They are asserted by the current bus owner over two clock cycles to define the currently active transaction type.</td></tr>
<tr><td>RESET#</td><td>I</td><td>Asserting the RESET# signal resets the processor to a known state and invalidates the L1 cache without writing back any of the contents. RESET# must stay active for at least one millisecond after $V_{CC_{CORE}}$ and CLK have reached their proper specifications. On observing active RESET#, all system bus agents will deassert their outputs within two clocks.

A number of bus signals are sampled at the active-to-inactive transition of RESET# for power-on configuration. These configuration options are described in the Pentium® Pro Family Developer's Manual, Volume 1: Specifications (Order Number 242690).

The processor may have its outputs tristated via power-on configuration. Otherwise, if INIT# is sampled active during the active-to-inactive transition of RESET#, the processor will execute its Built-in Self-Test (BIST). Whether or not BIST is executed, the processor will begin program execution at the power on Reset vector (default 0_FFFF_FFF0h). RESET# must connect the appropriate pins of all processor system bus agents.</td></tr>
<tr><td>RS[2:0]#</td><td>I</td><td>The RS[2:0]# (Response Status) signals are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of all processor system bus agents.</td></tr>
<tr><td>RTTCTRL</td><td>I</td><td>The RTTCTRL input signal provides AGTL+ termination control. The Celeron FC-PGA processor samples this input to sense the presence of motherboard AGTL+ termination. See the platform design guide for implementation details.</td></tr>
<tr><td>SLEWCTRL</td><td>I</td><td>The SLEWCTRL input signal provides AGTL+ slew rate control. The Celeron FC-PGA processor samples this input to determine the slew rate for AGTL+ signals when it is the driving agent. See the platform design guide for implementation details.</td></tr>
<tr><td>SLOTOCC#
(S.E.P.P. only)</td><td>O</td><td>SLOTOCC# is defined to allow a system design to detect the presence of a terminator card or processor in a SC242 connector. This pin is not a signal; rather, it is a short to V_{SS}. Combined with the VID combination of VID[4:0]= 11111 (see Section 2.5), a system can determine if a SC242 connector is occupied, and whether a processor core is present. The states and values for determining the type of cartridge in the SC242 connector is shown below.

SC242 Occupation Truth Table
<table>
<tr><th>Signal</th><th>Value</th><th>Status</th></tr>
<tr><td>SLOTOCC#
VID[4:0]</td><td>0
Anything other than '11111'</td><td>Processor with core in SC242 connector.</td></tr>
<tr><td>SLOTOCC#
VID[4:0]</td><td>0
11111</td><td>Terminator cartridge in SC242 connector (i.e., no core present).</td></tr>
<tr><td>SLOTOCC#
VID[4:0]</td><td>1
Any value</td><td>SC242 connector not occupied.</td></tr>
</table>
</td></tr>
<tr><td>SLP#</td><td>I</td><td>The SLP# (Sleep) signal, when asserted in Stop-Grant state, causes processors to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will recognize only assertions of the SLP#, STPCLK#, and RESET# signals while in Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and APIC processor core units.</td></tr>
<tr><td>SMI#</td><td>I</td><td>The SMI# (System Management Interrupt) signal is asserted asynchronously by system logic. On accepting a System Management Interrupt, processors save the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler.</td></tr>
</table>

Table 56. Alphabetical Signal Reference (Sheet 6 of 7)

Signal	Type	Description
STPCLK#	I	The STPCLK# (Stop Clock) signal, when asserted, causes processors to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the bus and APIC units. The processor continues to snoop bus transactions and may latch interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units, resumes execution, and services any pending interrupt. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.
TCK	I	The TCK (Test Clock) signal provides the clock input for the Intel Celeron processor Test Access Port.
TDI	I	The TDI (Test Data In) signal transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.
TDO	O	The TDO (Test Data Out) signal transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.
TESTHI (S.E.P.P. only)	I	Refer to Section 2.6 for implementation details.
THERMDN	O	Thermal Diode p-n junction. Used to calculate core temperature. See Section 4.1.
THERMDP	I	Thermal Diode p-n junction. Used to calculate core temperature. See Section 4.1.
THERMTRIP#	O	The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when the junction temperature exceeds approximately 135 °C. This is signaled to the system by the THERMTRIP# (Thermal Trip) pin. Once activated, the signal remains latched, and the processor stopped, until RESET# goes active. There is no hysteresis built into the thermal sensor itself; as long as the die temperature drops below the trip level, a RESET# pulse will reset the processor and execution will continue. If the temperature has not dropped below the trip level, the processor will reassert THERMTRIP# and remain stopped. The system designer should not act upon THERMTRIP# until after the RESET# input is deasserted. Until this time, the THERMTRIP# is indeterminate.
TMS	I	The TMS (Test Mode Select) signal is a JTAG specification support signal used by debug tools.
TRDY#	I	The TRDY# (Target Ready) signal is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of all system bus agents.
TRST#	I	The TRST# (Test Reset) signal resets the Test Access Port (TAP) logic. Intel Celeron processors require this signal to be driven low during power on Reset. A 680 ohm resistor is the suggested value for a pull down resistor on TRST#.
$V_{CC1.5}$ (PGA packages only)	I	The V_{CCCMOS} pin provides the CMOS voltage for use by the platform. The 2.5 V must be provided to the $V_{CC2.5}$ input and 1.5 V must be provided to the $V_{CC1.5}$ input. The processor re-routes the 1.5 V input to the V_{CCCMOS} output via the package. The supply for $V_{CC1.5}$ must be the same one used to supply V_{TT}.
$V_{CC2.5}$ (PGA packages only)	I	The V_{CCCMOS} pin provides the CMOS voltage for use by the platform. The 2.5 V must be provided to the $V_{CC2.5}$ input and 1.5 V must be provided to the $V_{CC1.5}$ input. The processor re-routes the 2.5 V input to the V_{CCCMOS} output via the package.
V_{CCCMOS} (PGA packages only)	O	The V_{CCCMOS} pin provides the CMOS voltage for use by the platform. The 2.5 V must be provided to the $V_{CC2.5}$ input and 1.5 V must be provided to the $V_{CC1.5}$ input.
$V_{COREDET}$ (PGA packages only)	O	The $V_{COREDET}$ signal will float for 2.0 V core processors and will be grounded for Celeron™ FC-PGA processor with a 1.5V core voltage.

Table 56. Alphabetical Signal Reference (Sheet 7 of 7)

Signal	Type	Description
VID[4:0] (S.E.P.P.) VID[3:0] (PGA packages only)	O	The VID (Voltage ID) pins can be used to support automatic selection of power supply voltages. These pins are not signals, but are either an open circuit or a short circuit to V_{SS} on the processor. The combination of opens and shorts defines the voltage required by the processor. The VID pins are needed to cleanly support voltage specification variations on Intel Celeron processors. See Table 2 for definitions of these pins. The power supply must supply the voltage that is requested by these pins, or disable itself.
V_{REF}[7:0] (PGA packages only)	I	These input signals are used by the AGTL+ inputs as a reference voltage. AGTL+ inputs are differential receivers and will use this voltage to determine whether the signal is a logic high or logic low. For the FC-PGA package, V_{REF} is typically 2/3 of V_{TT}

7.1 Signal Summaries

Table 57 through Table 60 list attributes of the Celeron processor output, input, and I/O signals.

Table 57. Output Signals

Name	Active Level	Clock	Signal Group
CPUPRES# (PGA packages only)	Low	Asynch	Power/Other
FERR#	Low	Asynch	CMOS Output
IERR#	Low	Asynch	CMOS Output
PRDY#	Low	BCLK	AGTL+ Output
SLOTOCC# (S.E.P.P. only)	Low	Asynch	Power/Other
TDO	High	TCK	TAP Output
THERMDN	N/A	Asynch	Power/Other
THERMTRIP#	Low	Asynch	CMOS Output
$V_{CORE_{DET}}$ (PGA packages only)	High	Asynch	Power/Other
VID[4:0] (S.E.P.P.) VID[3:0] (PGA packages)	High	Asynch	Power/Other

Table 58. Input Signals

Name	Active Level	Clock	Signal Group	Qualified
A20M#	Low	Asynch	CMOS Input	Always [1]
BPRI#	Low	BCLK	AGTL+ Input	Always
BCLK	High	—	System Bus Clock	Always
DEFER#	Low	BCLK	AGTL+ Input	Always
FLUSH#	Low	Asynch	CMOS Input	Always [1]
IGNNE#	Low	Asynch	CMOS Input	Always [1]
INIT#	Low	Asynch	CMOS Input	Always [1]
INTR	High	Asynch	CMOS Input	APIC disabled mode
LINT[1:0]	High	Asynch	CMOS Input	APIC enabled mode
NMI	High	Asynch	CMOS Input	APIC disabled mode
PICCLK	High	—	APIC Clock	Always
PREQ#	Low	Asynch	CMOS Input	Always
PWRGOOD	High	Asynch	CMOS Input	Always
RESET#	Low	BCLK	AGTL+ Input	Always
RS[2:0]#	Low	BCLK	AGTL+ Input	Always
RTTCTRL	N/A	Asynch	Power/Other	
SLEWCTRL	N/A	Asynch	Power/Other	
SLP#	Low	Asynch	CMOS Input	During Stop-Grant state
SMI#	Low	Asynch	CMOS Input	
STPCLK#	Low	Asynch	CMOS Input	
TCK	High	—	TAP Input	
TDI	High	TCK	TAP Input	
TESTHI (S.E.P.P. only)	High	Asynch	Power/Other	Always
THERMDP	N/A	Asynch	Power/Other	
TMS	High	TCK	TAP Input	
TRST#	Low	Asynch	TAP Input	
TRDY#	Low	BCLK	AGTL+ Input	

NOTE:
1. Synchronous assertion with active TRDY# ensures synchronization.

Table 59. Input/Output Signals (Single Driver)

Name	Active Level	Clock	Signal Group	Qualified
BSEL[1:0]	Low	Asynch	Power/Other	Always
BP[3:2]	Low	BCLK	AGTL+ I/O	Always
BR0#	Low	BCLK	AGTL+I/O	Always
A[31:3]#	Low	BCLK	AGTL+ I/O	ADS#, ADS#+1
ADS#	Low	BCLK	AGTL+ I/O	Always
BPM[1:0]#	Low	BCLK	AGTL+ I/O	Always
D[63:0]#	Low	BCLK	AGTL+ I/O	DRDY#
DBSY#	Low	BCLK	AGTL+ I/O	Always
DRDY#	Low	BCLK	AGTL+ I/O	Always
LOCK#	Low	BCLK	AGTL+ I/O	Always
REQ[4:0]#	Low	BCLK	AGTL+ I/O	ADS#, ADS#+1

Table 60. Input/Output Signals (Multiple Driver)

Name	Active Level	Clock	Signal Group	Qualified
BNR#	Low	BCLK	AGTL+ I/O	Always
HIT#	Low	BCLK	AGTL+ I/O	Always
HITM#	Low	BCLK	AGTL+ I/O	Always
PICD[1:0]	High	PICCLK	APIC I/O	Always