Data Sheet May 2001 File Number 9014.1

Precision Dual PWM Controller And Linear Regulator for Notebook CPUs

The IPM6210 is a highly integrated power controller which provides a complete power management solution for mobile CPUs. The IC integrates two PWM controllers and a linear regulator as well as monitoring and protection circuitry into a single 28-lead plastic SSOP package. The two PWM controllers regulate the microprocessor core and I/O voltages with synchronous-rectified buck converters, while the linear regulator powers the CPU clock.

The IPM6210 includes 5-bit digital-to-analog converter (DAC) that adjusts the core PWM output voltage from $0.925V_{DC}$ to $2.0V_{DC}$ and conforms to the Intel Mobile VID specification. The DAC setting may be changed during operation to accommodate Dual-Mode processors. Special measures are taken to provide such a transition with controlled rate in a specified 100µs. A precision reference, remote sensing, and a proprietary architecture with integrated processor mode-compensated “droop” provide excellent static and dynamic core voltage regulation. The second PWM controller has a fixed 1.5V output voltage and powers the I/O circuitry. Both PWM controllers have integrated feedback loop compensation that dramatically reduces number of the external components. At nominal loads PWM controllers operate at a fixed frequency of 300kHz. At light loads when the filter inductor current becomes discontinuous, controllers operate in a hysteretic mode. Out-of-phase operation of two PWM controllers to reduce input current ripple is provide in both modes of operation. The linear regulator uses an internal pass device to provide 2.5V for the CPU clock generator.

The IPM6210 monitors all the output voltages. A single Power-Good signal is issued when soft start is completed and all outputs are within ±10% of their respective set points. A built-in overvoltage protection for the core and I/O outputs forces the lower MOSFETs on to prevent output voltages from going above 115% of their settings. Undervoltage protection latches the chip off when any of three outputs drops below 75% of the set value. The PWM controller's overcurrent circuitry monitors the output current by sensing the voltage drop across the lower MOSFETs. If precision overcurrent protection is required, an external current-sense resistor may optionally be used.

Ordering Information

PART NUMBER	TEMP. (^oC)	PACKAGE	PKG. NO.
IPM6210CA	-10 to 85	28 Ld SSOP	M28.15
IPM6210CA-T	-10 to 85	28 Ld SSOP, Tape and Reel	M28.15

Features

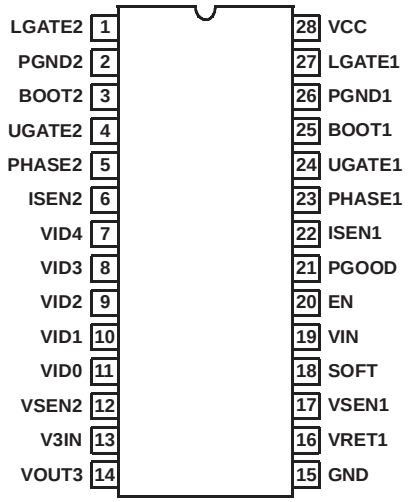
- Provides 3 Regulated Voltages
  - 0.9V to 2.0V Microprocessor Core (SpeedStep™ Enabled)
  - 1.5V Microprocessor I/O
  - 2.5V Microprocessor Clock Generator
- High Efficiency Over Wide Load Range
- Not Dissipative Current-Sense Scheme
  - Uses MOSFET’s $r_{DS(ON)}$
  - Optional Current-Sense Resistor for Precision Overcurrent
- Adaptive Dead-Time Drivers for N-Channel MOSFETs
- Operates from +5V, +3.3V and Battery (5.6-24V) Inputs
- Precision Core Voltage Control:
  - Remote “Kelvin” Sensing
  - Summing Current-Mode Control
  - On-Chip Mode-Compensated “Droop” for Optimum Transient Response and Lower Processor Power Dissipation
- TTL-Compatible 5-Bit Digital Output Voltage Selection
  - Wide Range - $0.925V_{DC}$ to $1.3V_{DC}$ in 25mV Steps, and from $1.3V_{DC}$ to $2.0V_{DC}$ in 50mV Steps
  - Programmable “On-the-Fly” VID Code Change with Customer Programmable Slew Rate and 100µs Settling Time
- Power-Good Output Voltage Monitor
- No Negative Voltage on Outputs at Turn-Off
- Overvoltage, Undervoltage and Overcurrent Fault Monitors
- 300kHz Fixed Switching Frequency
- Thermal Shutdown

Applications

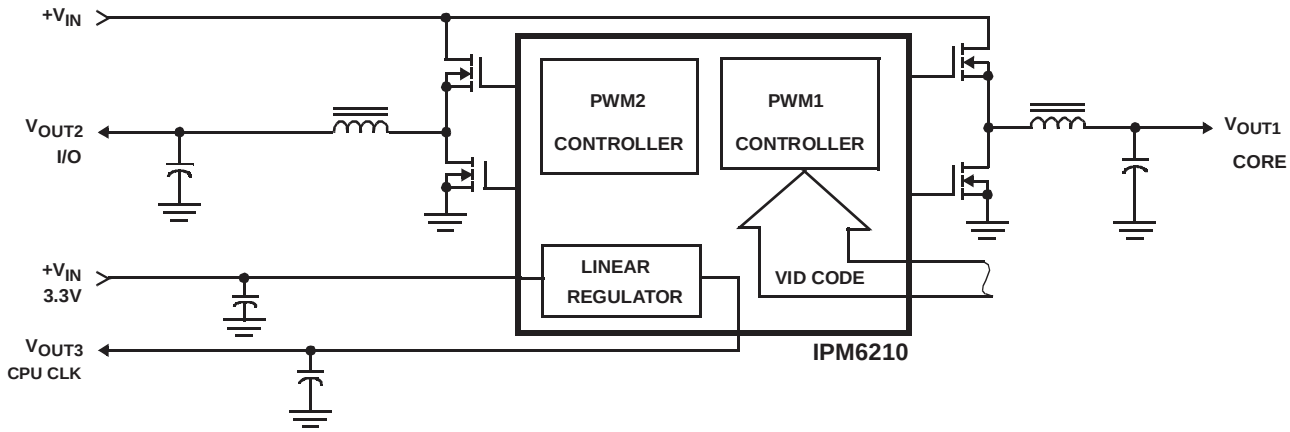
- Mobile PCs
- Web Tablets
- Internet Appliances

Pinout

IPM6210 (SSOP)
TOP VIEW



Simplified Power System Diagram



Absolute Maximum Ratings

Supply Voltage, V_{CC} . . . . . +6.5V
Input Voltage, V_{IN} . . . . . +27.0V
V3in . . . . . +6.5V
PHASE1,2 . . . . . +33.0V
BOOT1,2 . . . . . +33.0V
BOOT1,2 with respect to PHASE1,2 . . . . . +6.5V
PGOOD, RT/FAULT, and GATE Voltage . . . .GND - 0.3V to V_{CC} +0.3V
Core Output or I/O Voltage . . . . . GND - 0.3V to +6.5V
ESD Classification . . . . . Class 2

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . +5.0V ±5%
Input Voltage, V_{IN} . . . . . +7.5V to 24.0V
V3in . . . . . +3.3V ±10%
Ambient Temperature Range . . . . . -10^oC to 85^oC
Junction Temperature Range . . . . . -10^oC to 125^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
SSOP Package	100

Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SSOP - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

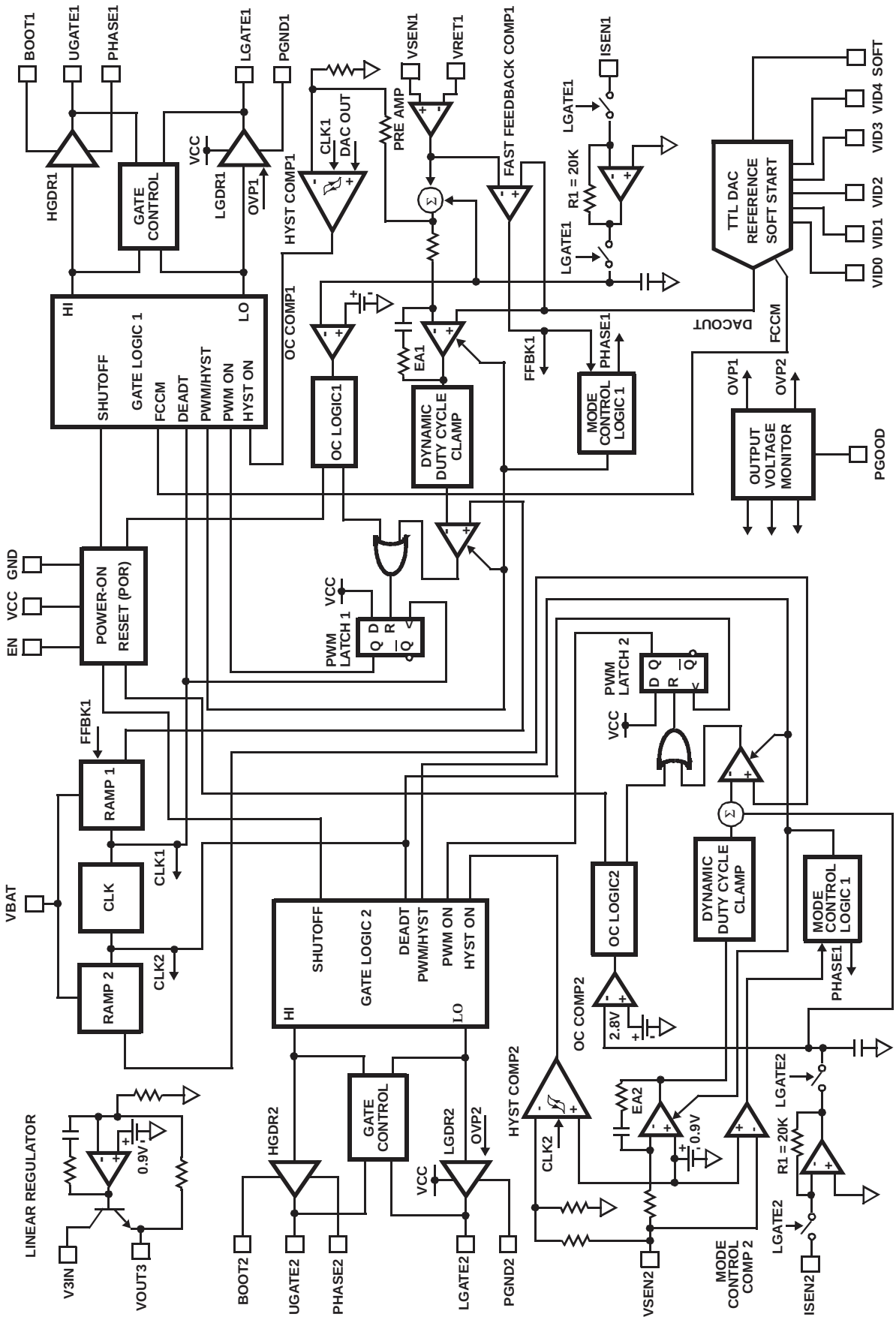
Recommended Operating Conditions, Unless Otherwise Noted. Refer to Figures 1, 2 and 3

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC SUPPLY						
Nominal Supply Current	I_{CC}	GATE1, GATE2 Open	-	2	2.5	mA
Shutdown Supply Current	I_{CCS}		-	30	-	µA
Battery Pin Supply Current	I_{VIN}		30	-	200	µA
Battery Pin Leakage Current at Shutdown	I_{VINSD}		-	-	1	µA
POWER-ON RESET						
Rising VCC Threshold			4.3	4.5	4.6	V
Falling VCC Threshold			3.9	4.1	4.3	V
OSCILLATOR						
Free Running Frequency			255	300	345	kHz
Ramp Amplitude, peak-to-peak		V_{BAT} = 16V	-	2	-	V
Ramp Offset			-	0.5	-	V
REFERENCE, DAC AND SOFT START						
VID0-VID4 Input Low Voltage			-	-	1.2	V
VID0-VID4 Input High Voltage			1.8	-	-	V
VID0-VID4 Pull-up Current to V_{CC}			-	1	-	µA
DAC Voltage Accuracy			-1.0	-	+1.0	%
Soft-Start Current During Start-Up	I_{SS}	V_{SS} = 0V...0.9V	18	25	32	µA
Soft-Start Current During Mode Change	I_{SSM}	V_{SS} = 0.925V...2.0V	350	500	650	µA
ENABLE						
Enable Voltage Low	V_{ENLOW}	IC Inhibited	-	-	1.2	V
Enable Voltage High	V_{ENHIGH}	IC Enabled Input has Internal Pull-up Current Source 2µA (Typ)	2.0	-	-	V
PWM 1 CONVERTER						
Output Voltage	VOUT1	Defined by the current VID code (Table 1)	0.925	-	2.0	V
Static Load Regulation		100mA < I_{VOUT1} < 15.0A	-2.0	-	+2.0	%

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted. Refer to Figures 1, 2 and 3 **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Undervoltage Shutdown Level	V_{UV1}	Percent of the voltage set by VID code. Disabled during dynamic VID code change.	72	75	78	%
Undervoltage Shutdown Delay	T_{DOC1}		1.2	-	1.6	µs
Overvoltage	V_{OVP1}	Percent of the voltage set by VID code.	112	115	120	%
Overvoltage Shutdown Delay	T_{DOV1}		1.6	-	3.2	µs
Overcurrent Comparator Threshold	I_{OC1}		100	135	170	µA
PWM 2 CONVERTER						
Output Voltage	VOUT2			1.5		V
Load Regulation		100mA < I_{VOUT3} < 2.1A	-2.0	-	+2.0	%
Undervoltage Shutdown Level	V_{UV2}		1.09	-	1.13	V
Undervoltage Shutdown Delay	T_{DOC2}		1.2	-	1.6	µs
Overvoltage Shutdown	V_{OVP2}		1.70	-	1.78	V
Overvoltage Shutdown Delay	T_{DOV2}		1.6	-	3.2	µs
Overcurrent Comparator Threshold	I_{OC2}		100	140	170	µA
LINEAR REGULATOR						
Output Voltage	VOUT3			2.5		V
Load Regulation		1mA < I_{VOUT3} < 100mA	-2.0	-	2.0	%
Undervoltage Shutdown Level	V_{UV3}		1.8	-	2.0	V
Current Limit	I_{oc3}		190	250	340	mA
PWM CONTROLLER ERROR AMPLIFIERS						
DC Gain		By Design	-	86	-	dB
Gain-Bandwidth Product	GBWP	By Design	-	2.7	-	MHz
Slew Rate	SR	By Design	-	1	-	V/µs
PWM 1 CONTROLLER GATE DRIVERS						
Upper Drive Pull-Up Resistance	R_{1UGPUP}		-	6	8	Ω
Upper Drive Pull-Down Resistance	R_{1UGPDN}		-	3	5	Ω
Lower Drive Pull-Up Resistance	R_{1LGPUP}		-	6	8	Ω
Lower Drive Pull-Down Resistance	R_{1LGPDN}		-	0.8	1.5	Ω
PWM 2 CONTROLLER GATE DRIVERS						
Upper Drive Pull-Up Resistance	R_{2UGPUP}		-	12	20	Ω
Upper Drive Pull-Down Resistance	R_{2UGPDN}		-	6	10	Ω
Lower Drive Pull-Up Resistance	R_{2LGPUP}		-	10	20	Ω
Lower Drive Pull-Down Resistance	R_{2LGPDN}		-	3	5	Ω
POWER GOOD						
V_{OUT1} Upper Threshold		Percent of the voltage defined by the VID code	108	-	114	%
V_{OUT1} Lower Threshold, Falling Edge		Percent of the voltage defined by the VID code	85	-	92	%
V_{OUT1} Lower Threshold, Rising Edge		Percent of the voltage defined by the VID code	87	-	94	%
V_{OUT2} Upper Threshold			1.63	-	1.7	V
V_{OUT2} Lower Threshold			1.32	-	1.38	V
V_{OUT3} Upper Threshold			2.7	-	2.9	V
V_{OUT3} Lower Threshold			2.18	-	2.32	V
PGOOD Voltage Low	V_{PGOOD}	I_{PGOOD} = -4mA	-	-	0.5	V
PGOOD Leakage Current	I_{PGILKG}	V_{PULLUP} = 5.0V	-	-	1.0	µA

Block Diagram



Functional Pin Descriptions

VID0, VID1, VID2, VID3, VID4 (Pins 11, 10, 9, 8 and 7 Respectively)

VID0-VID4 are the input pins to the 5-bit DAC. The states of these five pins program the internal voltage reference (DACOUT). The level of DACOUT sets the core converter output voltage (V_{OUT1}). It also sets the core PGOOD, UVP and OVP thresholds.

BOOT1, BOOT2 (Pins 25 and 3)

These pins provide power to the upper MOSFET drivers of the core and I/O converters. Connect these pins to their respective junctions of the bootstrap capacitors and the cathodes of the bootstrap diodes. The anodes of the bootstrap diodes are connected to pin 28, VCC.

PHASE1, PHASE2 (Pins 23 and 5)

The PHASE nodes are the junction points of the upper MOSFET sources, output filter inductors, and lower MOSFET drains. Connect the PHASE pins to the respective PWM converter's upper MOSFET source.

ISEN1, ISEN2 (Pins 22 and 6)

These pins are used to monitor the voltage drop across the lower MOSFETs for current feedback, output voltage droop and overcurrent protection. For precise current detection these inputs could be connected to optional current sense resistors placed in series with sources of the lower MOSFETs. To set the gain of the current sense amplifier, a resistor should be placed in series with each of these inputs.

UGATE1, UGATE2 (Pins 24 and 4)

These pins provide the gate drive for the upper MOSFETs.

LGATE1, LGATE 2 (Pin 27 and 1)

These pins provide the gate drive for the lower MOSFETs.

PGND1, PGND2 (Pin 26 and 2)

These are the power ground connection for the core and I/O converters, respectively. Tie each lower MOSFET source to the corresponding pin.

VSEN2 (Pin 12)

This pin is connected to the I/O output and provides voltage feedback to the I/O error amplifier. The PGOOD, UVP and OVP comparators use this signal.

V3IN (Pin 13)

This pin provides input power for the 2.5V linear regulator. The typical input voltage for that pin is 3.3V. Alternatively, 5.0V system rail can be used while efficiency will be proportionally lower.

VOUT3 (Pin 14)

Output of the 2.5V linear regulator. Supplies current up to 150mA. The output current on this pin is internally limited to 250mA.

VSEN1, VRTN1 (Pins 17 and 16)

These pins are connected to the core converter's output voltage to provide remote sensing. The PGOOD, UVP and OVP comparators use these pins for protection.

SOFT (Pin 18)

Connect a capacitor from this pin to the ground. This capacitor (typically 0.1mF), along with an internal 25mA current source, sets the soft-start interval of the converter. When voltage on this pin exceeds 0.9V, the soft start is completed. After the soft-start is completed, the pin function is changed. The internal circuit regulates voltage on this pin to the value commanded by VID code. The pin now has 500mA source/sink capability that allows to set desired slew rate for upward and downward VID code changes.

VIN (Pin 19)

VIN provides battery voltage to the oscillator for feed-forward rejection of input voltage variations.

EN (Pin 20)

This pin enables IC operation when left open or pulled-up to VCC. Also, it unlatches the chip after fault when being cycled.

PGOOD (Pin 21)

PGOOD is an open drain output used to indicate the status of the PWM converters' output voltages. This pin is pulled low when the core output is not within ±10% of the DACOUT reference voltage, or when any of the other outputs are not within their respective undervoltage and overvoltage thresholds.

The PGOOD output is pulled low for "01111" and '11111' VID code. See Table 1.

GND (Pin 15)

Signal ground for the IC. All voltage levels are measured with respect to this pin.

VCC (Pin 28)

Supplies all the power necessary to operate the chip. The IC starts to operate when the voltage on this pin exceeds 4.5V and shuts down when the voltage on this pin drops below 4.0V.

Description

Operation Overview

The IPM6210 three-in-one power management integrated circuit provides complete power solution for modern processors for notebook and sub-notebook PCs. The IC controls operation of two synchronous buck converters and one linear regulator. The output voltage of the core converter can be adjusted in the range from 0.925V to 2.0 by changing the DAC code settings (see Table 1). The output voltage of the I/O converter is fixed to 1.5V. The internal linear regulator provides fixed 2.5V for the CPU clock generator from the system +3.3V bus. The output voltage of the core converter

can be changed on-the-fly with programmable slew rate, which makes it especially suitable for the processors that feature modern power savings techniques as SpeedStep™ or PowerNow!™ .

Both, core and I/O converters can operate in two modes: fixed frequency PWM and variable frequency hysteretic depending on the load level. At loads lower than the critical where filter inductor current becomes discontinuous, hysteretic mode of operation is activated. Switchover from PWM to hysteretic operation at light loads improves the converters' efficiency and prolongs battery run time. In hysteretic mode, comparators are synchronized to the main clock that allows seamless transition between the operational modes and reduced channel-to-channel interaction. As the filter inductor resumes continuous current, the PWM mode of operation is restored.

The core converter incorporates Intersil's proprietary output voltage droop for optimum handling of fast load transients found in modern processors. The droop is compensated for the processor mode changes, which allows for relatively equal droop in any operation mode and to specify the droop as a fraction of the VID set voltage.

Initialization

The IPM6210 initializes upon receipt of input power assuming EN is high or not connected. The Power-On Reset (POR) function continually monitors the input supply voltage on the VCC pin and initiates soft-start operation after input supply voltage exceeds 4.5V. Should this voltage drop lower than 4.0V, POR disables the chip.

Soft-Start

When soft start is initiated, the voltage on the SOFT pin starts to ramp gradually due to the 25µA current sourced into the external capacitor.

When SOFT-pin voltage reaches 0.9V, the value of the sourcing current rapidly changes to 500µA charging the soft-start capacitor to the level determined by the DAC. This completes the soft start sequence, Figure 1. As long as the SOFT voltage is above 0.9V, the maximum value of the internal soft-start current is set to 500µA allowing fast rate-of-change in the core output voltage due to a VID code change. In this mode SOFT has both sourcing and sinking capabilities to maintain voltage across the soft-start capacitor conforming to the VID code.

This dual slope approach helps to provide safe rise of voltages and currents in the converters during initial start-up and at the same time sets a controlled speed of the core voltage change when the processor commands to do so.

Soft-start circuits for the I/O converter is slaved to the core output soft-start circuit and they complete their ramp-up when voltage on the SOFT pin reaches 0.9V.

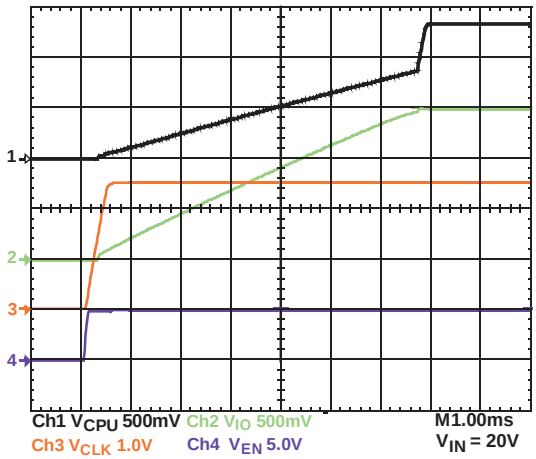


FIGURE 1. INITIAL STARTUP

The value of the soft-start capacitor can be estimated by the following equation:

$$Css = \frac{\Delta Issm}{\Delta Vdac}\Delta t$$

For the typical conditions when DVdac = 0.25V, Dt = 100µs:

$$Css = \frac{500mA}{0.25V}100\mu s = 0.2\mu F$$

With this value of the soft-start capacitor, soft start time will be equal to:

$$Tss = \frac{0.2\mu F x 0.9V}{25\mu A} = 7.2ms$$

OUT1 Voltage Program

This output of PWM1 converter is designated to supply the microprocessor core voltage. The OUT1 voltage is programmed to discrete levels between 0.925V_{DC} and 2.0V_{DC} as specified in Table 1. The voltage identification (VID) pins program an internal voltage reference (DAC) through a TTL-compatible 5-bit digital-to-analog converter. The level of the DAC voltage also sets the PGOOD, UVP and OVP thresholds. The VID pins can be left open for a logic 1 input due to internal 1µA pull-up to V_{CC}.

The ‘11111’ and ‘0111‘ VID codes, as shown in Table 1, shut the IC down and set PGOOD low.

Core Converter PWM Operation

At the nominal current core converter operates in a fixed frequency PWM mode. The output voltage is compared with a reference voltage set by the DAC. The derived error signal is amplified by an internally compensated error amplifier and applied to the inverting input of the PWM comparator. To provide output voltage droop for enhanced dynamic load regulation, a signal proportional to the output current is added to the voltage feedback signal. This feedback scheme in conjunction with a PWM ramp proportional to the input voltage allows for fast and stable loop response over a wide range of input voltage and output current variations. For the sake of efficiency and maximum simplicity, the current sense signal is derived from the voltage drop across the lower MOSFET during its conduction time.

TABLE 1.

PIN NAME					NOMINAL OUT1 VOLTAGE
VID4	VID3	VID2	VID1	VID0	
0	0	0	0	0	2.00
0	0	0	0	1	1.95
0	0	0	1	0	1.90
0	0	0	1	1	1.85
0	0	1	0	0	1.80
0	0	1	0	1	1.75
0	0	1	1	0	1.70
0	0	1	1	1	1.65
0	1	0	0	0	1.60
0	1	0	0	1	1.55
0	1	0	1	0	1.50
0	1	0	1	1	1.45
0	1	1	0	0	1.40
0	1	1	0	1	1.35
0	1	1	1	0	1.30
0	1	1	1	1	No CPU
1	0	0	0	0	1.275
1	0	0	0	1	1.250
1	0	0	1	0	1.225
1	0	0	1	1	1.200
1	0	1	0	0	1.175
1	0	1	0	1	1.150
1	0	1	1	0	1.125
1	0	1	1	1	1.100
1	1	0	0	0	1.075
1	1	0	0	1	1.050
1	1	0	1	0	1.025
1	1	0	1	1	1.000
1	1	1	0	0	0.975
1	1	1	0	1	0.950
1	1	1	1	0	0.925
1	1	1	1	1	No CPU

NOTE:

2. 0 = Connected to GND or V_{SS}, 1 = open or connected to 3.3V through pull-up resistors.

Mode-Compensated Droop

An output voltage ‘droop’ or an active voltage positioning is now widely used in the computer power applications. The technique is based on raising the converter voltage at light load in anticipation of the possible load current step. Inversely, the output voltage is lowered at high load in anticipation of possible load drop. The output voltage varies with the load like it is a resistor connected in series with the converter’s output. When done as a part of the feedback in a closed loop, the ‘droop’ is not associated with substantial power losses, though. There is no such a resistor in a real circuit, but the feature is rather emulated by the feedback.

The ‘droop’ allows a reduction in size and cost of the output capacitors required to handle the transient. Additionally, the CPU power dissipation is also slightly reduced as it is proportional to the applied voltage squared and even a slight voltage decrease translates to a measurable reduction in power dissipated.

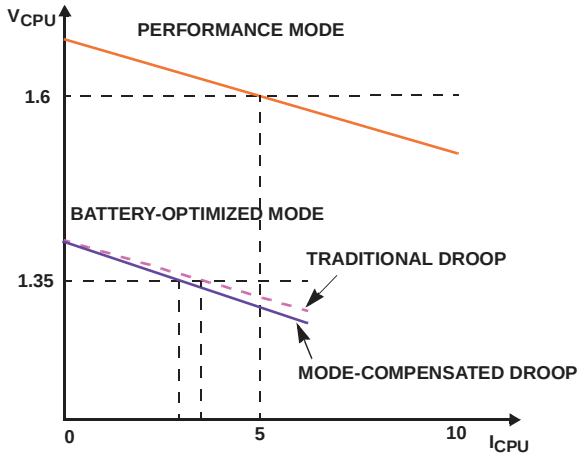


FIGURE 2. MODE-COMPENSATED DROOP

When powering the dual mode processor, it is desired to have an adequate “droop” (equal fractions of the programmed output voltage) in both performance and battery-optimized modes of operation. The traditional “droop” is normally tuned to the worse case load, which is associated with the performance mode. In the battery optimized mode, the CPU operating voltage and the clock frequency are both scaled down. Due to the constant gain in the current loop, the traditional ‘droop’ compensates only for the operating voltage change. The degree of the droop achieved in this case is not the same because the CPU current is significantly lower as it is illustrated by the following equation.

$$I_{CPU} = K_{CPU} x V_{CPUi} x F_{CPUi} x K_F \ ;$$

Where, K_{CPU} is a processor constant; V_{CPUi} is processor operating voltage; F_{CPUi} is processor clock frequency; K_F is a coefficient that varies from 0 to 1 and indicates how heavily the processor is engaged by the software; i is a denominator associated with the processor mode of operation (performance or battery optimized).

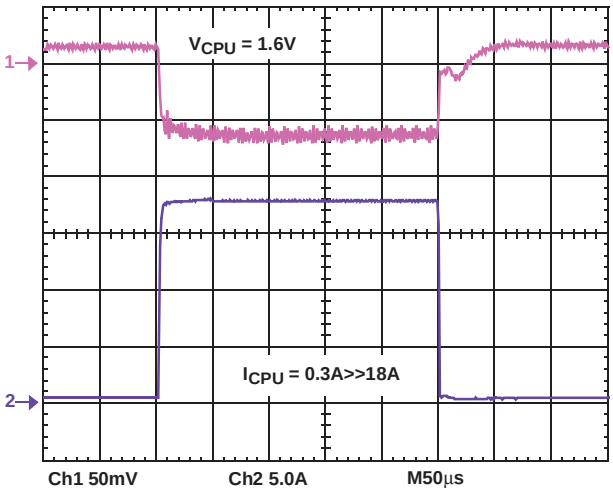


FIGURE 3.

This leads to deterioration of the droop benefits in the battery-optimized mode where they are mostly appreciable, Figure 2.

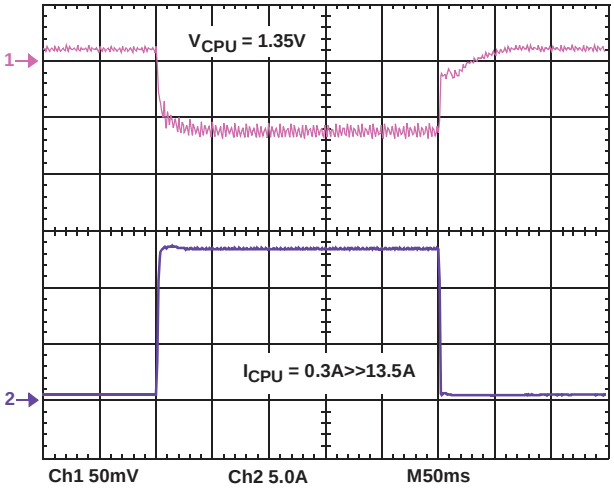


FIGURE 4.

The IPM6210 incorporates a new proprietary droop technique specially designed for the SpeedStep™ - enabled converters and provides mode-compensated, relatively equal droop in both, the performance and the battery-optimized modes. The droop is set as a fraction of the VID programmed voltage and the gain in the current loop is different for each VID combination. That makes the droop compensated for the voltage and the frequency changes associated with the different CPU modes of operation.

To accommodate the droop the output voltage of core converter is raised 2% at no load conditions. The resistor connected to ISEN1 pin programs the amount of droop.

$$R_{CS} = \frac{I_{MAX} x r_{DS(ON)}}{75\mu A} - 100\Omega$$

This resistor sets the gain in the current feedback loop. The droop is scaled to 5.5% of the VID code when current into ISEN1 pin equals 75µA.

The output voltage waveforms with droop subjected to load step are shown on Figures 3 through 5.

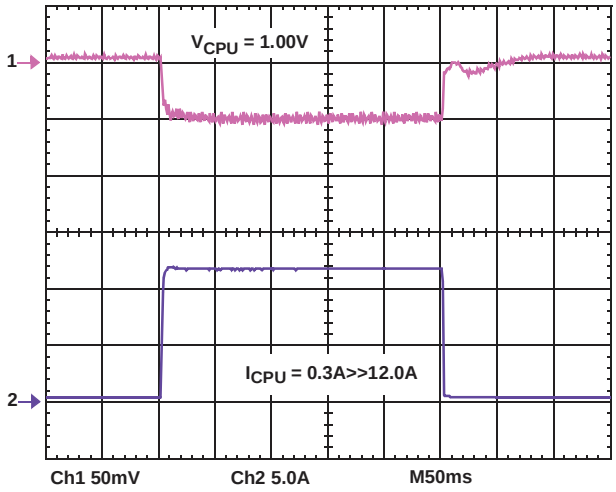


FIGURE 5.

Feedback Loop Compensation

Due to implemented average current mode control, the modulator has a single pole response with -1 slope at frequency determined by load:

$$F_{PO} = \frac{1}{2\pi x R_O x C_O},$$

where R_O is load resistance; C_O is load capacitance. For this type of modulator Type 2 compensation circuit is usually sufficient. To reduce number of external components and remove the burden at determining compensation components from a system designer, both PWM controllers have internally compensated error amplifiers.

Figure 6 shows Type 2 amplifier and its response along with responses of current mode modulator and the converter. The Type 2 amplifier, in addition to the pole at origin, has a zero-pole pair that causes a flat gain region at frequencies in between the zero and the pole.

$$F_Z = \frac{1}{2\pi x R_2 x C_1} = 6kHz;$$

$$F_P = \frac{1}{2\pi x R_1 x C_2} = 600kHz;$$

This region is also associated with phase ‘bump’ or reduced phase shift. The amount of phase shift reduction depends on how wide the region of flat gain is and has a maximum value of 90 degrees. To further simplify the converter compensation, the modulator gain is kept independent of the input voltage variation by providing feed-forward of V_{IN} to the oscillator ramp.

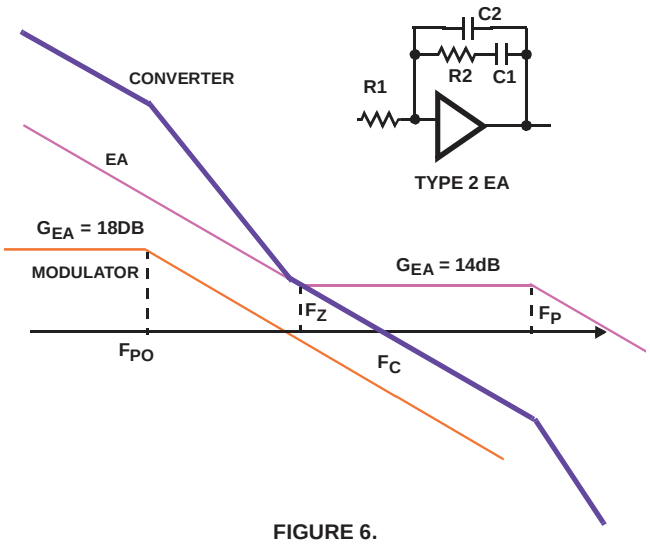


FIGURE 6.

The zero frequency, the amplifier high-frequency gain and the modulator gain are chosen to satisfy most of typical applications. The crossover frequency will appear at the point where the modulator attenuation equals the amplifier high frequency gain. The only task that the system designer has to complete is to specify the output filter capacitors to position the load main pole somewhere within one decade lower than the amplifier zero frequency. With this type of compensation plenty of phase margin is easily achieved due to zero-pole pair phase ‘boost’.

Conditional stability may occur only when the main load pole is positioned too much to the left side on the frequency axis due to excessive output filter capacitance. In this case, the ESR zero placed within 10kHz...50kHz range gives some additional phase ‘boost’. Fortunately, there is an opposite trend in mobile applications to keep the output capacitor as small as possible.

Automatic Operation Mode Control

The mode control circuit changes the converter’s mode of operation depending on the level of the load current. At nominal current the converter operates in a fixed frequency PWM mode. When the load current drops lower than the critical value, inductor current becomes discontinuous and the operation mode is changed to hysteretic.

The mode control circuit consists of a flip-flop which provides HYST and NORMAL signals. These signals inhibit normal PWM operation and activate hysteretic comparator and diode emulation mode of the synchronous MOSFET.

The inputs of the flip-flop are controlled by the outputs of two delay circuits that constantly monitor output of the phase node comparator. High level on the comparator output during $\overline{\text{PWM}}$ cycle is associated with continuous mode of operation. The low level -- corresponds to the discontinuous mode of operation. When the low level on the comparator output is detected eight times in a row, the mode control flip-flop is set and converter is commanded to operate in the hysteretic mode. If during this pulse counting process the comparator's output happens to be high, the counter of the delay circuit will be reset and circuit will continue to monitor for eight low-level pulses in a row, as shown in Figure 7.

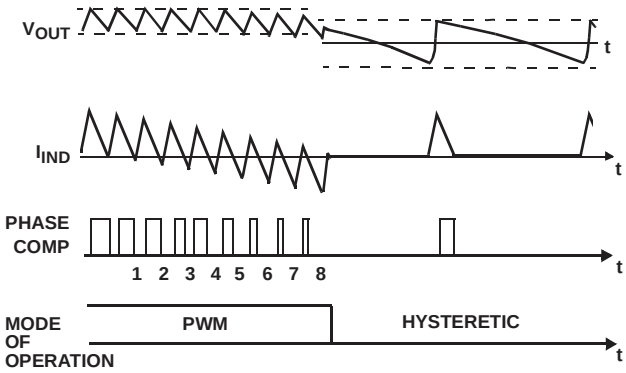


FIGURE 7. PWM TO HYSTERETIC TRANSITION

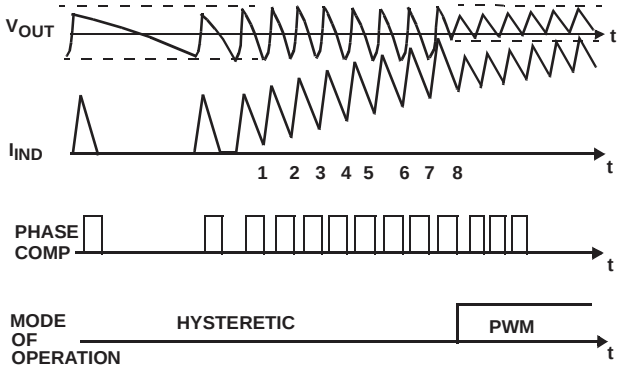


FIGURE 8. HYSTERETIC TO PWM TRANSITION

The circuit which restores normal PWM operation mode works in the same way and is looking for eight in a row high-level pulses on the comparator’s output. If during this counting process the comparator’s output happens to be low, the counter will be reset and the mode control flip-flop will not change the state. The operation mode will only be changed when eight pulses in a row fill the counter, see Figure 8. This technique prevents jitter and chatter of the operation mode control logic at the load levels close to the critical.

Hysteretic Operation

When discontinuous inductor current is detected, the mode control logic changes the way the signals in the chip are processed by entering hysteretic mode. The comparator and the error amplifier that provided control in the PWM mode are inhibited, and the hysteretic comparator is now activated. Changes are also made to the gate logic. The synchronous rectifier MOSFET is now controlled in diode emulation mode, hence conduction in the second quadrant is prohibited.

The converter output voltage is applied to the negative input of the hysteretic comparator. The voltage on the reference input of the hysteretic comparator is the DAC output voltage with a

small addition of the clock frequency pulses. Synchronization of the upper MOSFET turn-on pulses with the main clock enables seamless transition between the operation modes.

Operation During Processor Mode Changes

The PWM1 controller is specially designed to provide “on the fly” automatic core voltage changes required by some advanced processors for mobile applications. Dual core voltage and operation frequency scaling allows for significant power savings without sacrificing system performance in battery operation mode.

As processor mode changes can happen when chip is in PWM or hysteretic mode, measures were taken to provide equally fast response to these changes. As soon as a DAC code change is received, the chip is forced into PWM mode till transition completes regardless of the load level. Operating the controller in the synchronous PWM mode allows faster output voltage transitions especially when a downward output voltage change is commanded.

I/O Converter Architecture

The I/O converter architecture is close to that of the core converter. It has the same mode control logic and can operate in a constant frequency PWM mode or in hysteretic mode depending on the load level, but its structure is much simpler mainly because of absence of the differential input amplifier and the DAC. This controller is synchronized to the same clock as the core converter, but 180 degrees out-of-phase. Thus, some reduction of the input current ripple is achieved.

Some performance curves of I/O converter are shown on Figure 9 and Figure 10.

Gate Control Logic

The gate control logic translates generated PWM signals into the MOSFETs gate drive signals providing necessary amplification, level shift and shoot-trough protection. Also, it helps to optimize the IC performance over a wide range of the operational conditions. As MOSFET switching time can very dramatically from type to type and with input voltage variation, the gate control logic provides adaptive dead time by monitoring gate voltages of both upper and lower MOSFETs.

Protections

All three outputs are monitored and protected against extreme overload, short circuit and undervoltage conditions. Both PWM outputs are monitored and protected from overvoltage conditions. A sustained overload on any output latches-off all the converters and sets the PGOOD pin low. The chip operation can be restored by cycling VCC voltage or EN pin.

Overcurrent Protection

Both PWM controllers use the lower MOSFET’s on-resistance - $r_{DS(ON)}$ to monitor the current for protection against shorted outputs. The sensed voltage drop after amplification is compared with an internally set threshold.

Several scenarios of the current protection circuit behavior are possible.

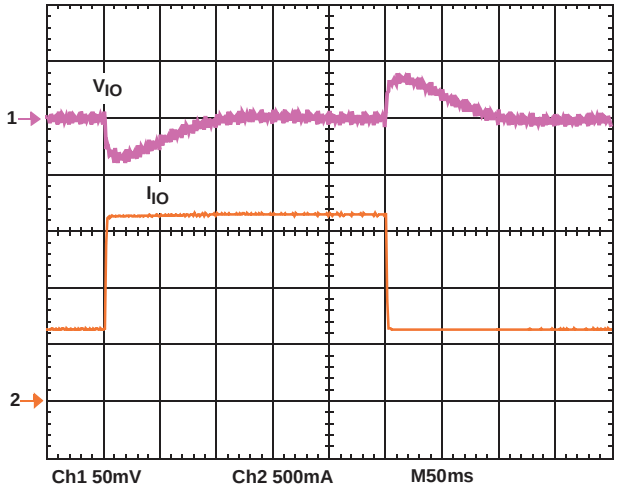


FIGURE 9. I/O CONVERTER LOAD TRANSIENT IN PWM MODE

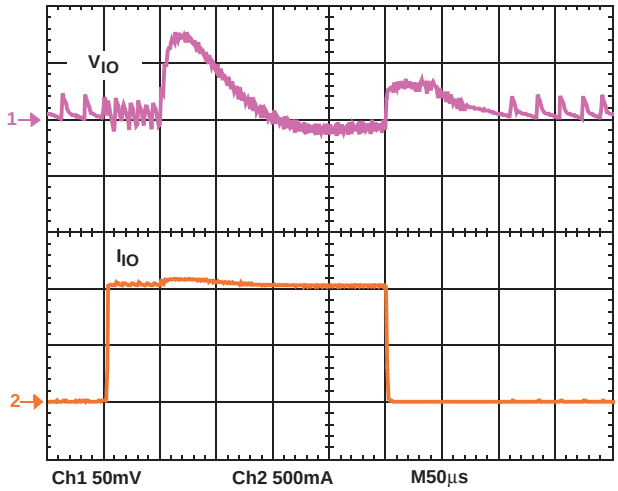


FIGURE 10. I/O CONVERTER LOAD TRANSIENT WITH MODE CHANGE

If load step is strong enough to pull output voltage lower than the undervoltage threshold, chip shuts down. If the output voltage sag does not reach the undervoltage threshold but the current exceeds the overcurrent threshold, the pulse skipping circuit is activated. This breaks the output voltage regulation and limits the current supplied to the load.

Because of the nature of the current sensing technique, and to accommodate a wide range of the $r_{DS(ON)}$ variation, the value of the threshold should represent overload current about 180% of the nominal value. To decrease current protection circuit noise susceptibility, a time delay circuit (8:1 counter which counts the clock cycles) is activated when the overcurrent condition is detected for the first time. If after the delay the overcurrent condition persists, the converter shuts down. If not - normal operation is restored.

The overcurrent protection circuit trips when the peak value of the lower MOSFET current is higher than the one obtained from the following equation.

$$I_{OC} = \frac{I_{th} \cdot (R_{CS} + 100\Omega)}{R_{DSON}}$$

where: R_{CS} is a resistor from ISEN pin to PHASE pin; I_{oc} is the desired overload current trip level; $r_{DS(ON)}$ is either $r_{DS(ON)}$ of the lower MOSFET, or the value of the optional current sense resistor; I_{th} is the threshold of the current protection circuitry (140µA).

In the linear regulator the maximum current of the integrated power device is actively limited to 250mA that eventually creates an undervoltage condition and sets the fault latch.

Overvoltage Protection

During operation, severe load dump or a short of an upper MOSFET can cause the output voltage to increase significantly over normal operation range. When the output exceeds the overvoltage threshold of 115% of the DAC voltage (1.7V for PWM2), the overvoltage comparator forces the lower gate driver high and turns the lower MOSFET on. This will pull down the output voltage and eventually blow the battery fuse. As soon as output voltage drops below the threshold, OVP comparator is disengaged.

Such an OVP scheme provides soft crowbar function and does not interfere with on-the-fly VID code changes. During downward changes in the converter output voltage, the condition where the OVP threshold is set before the new value of the output voltage is reached is permissible and harmless. Also, it does not invert output voltage when activated, a common problem for OVP schemes with a latch.

Overvoltage protection is not provided for the linear regulator.

Shutdown

When EN (pin 20) is pulled down, the chip is disabled and enters a low-current state. Both high-side and low-side gate drivers are turned off. This control scheme produces no negative output voltage at shutdown, as shown in Figure 11. A rising edge on EN clears the fault latch.

Thermal Shutdown

The chip incorporates an over temperature protection circuit that shuts all the outputs down when the die temperature of 150^{o}C is reached. Normal operation restores at die temperatures below 125^{o}C through the full soft-start cycle.

Design Procedure and Component Selection Guidelines

As an initial step, define operating voltage range, minimum and maximum load currents for each controller.

Output Inductor Selection

The minimum practical output inductor value is the one that keeps inductor current just on the boundary of continuous conduction at some minimum load. The industry standard practice is to choose the minimum current somewhere from 10% to 25% of the nominal current. At light load, IPM6210 PWM controllers automatically switch to a hysteretic mode of operation to sustain high efficiency. It is suggested that transition to hysteretic mode occur before inductor current becomes discontinuous. The following equations help to choose proper value of the output filter inductor.

$$\Delta I = 2 \times I_{min}$$

$$\Delta I = \frac{\Delta Vout}{ESR}$$

$$L = \frac{Vin - Vout}{Fs \times \Delta I} \times \frac{Vout}{Vin}$$

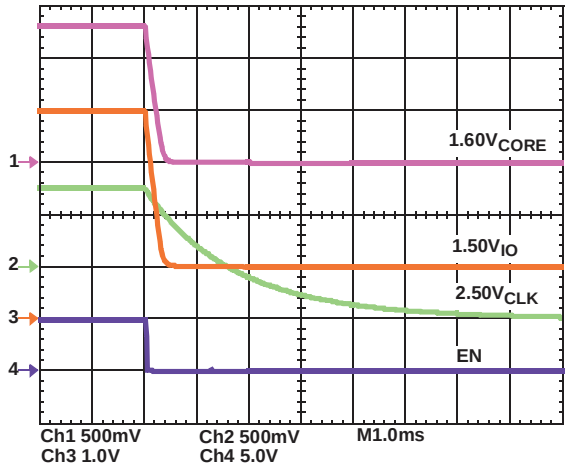


FIGURE 11. SHUTDOWN WAVEFORMS

Output Capacitor Selection

An output capacitor serves two major functions in a switching power supply. Along with an inductor it filters the sequence of pulses produced by the switcher and supply the load transient currents. The filtering requirements are a function of the switching frequency and the ripple current allowed, and are usually easy to satisfy in high frequency converters.

The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. Modern microprocessors produce transient load rates in excess of 10A/µs. High frequency ceramic capacitors placed beneath the processor socket initially supply the transient and reduce the slew rate seen by the bulk capacitors. The bulk capacitor values are generally determined by the total allowable ESR rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the processor power pins as physically possible. Consult with the processor manufacturer for specific decoupling requirements. Use only specialized low-ESR electrolytic capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR will determine the

output ripple voltage and the initial voltage drop after a transient. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

MOSFET Selection and Considerations

Requirements for the upper and lower MOSFETs are different in mobile applications. The reason for that is the 10:1 difference in conduction time of the lower and the upper MOSFETs driven by a difference between the input voltage which is nominally in the range from 8V to 20V, while nominal output voltage is about 1.5V.

Requirements for the lower MOSFET are simpler than those to the upper one. The lower the $r_{DS(ON)}$ of this device, the lower the conduction losses, the higher the converter's efficiency. Switching losses and gate drive losses are not significant because of zero-voltage switching conditions inherent for this device in the buck converter. Low reverse recovery charge of the body diode is important because it causes shoot-trough current spikes when the upper MOSFET turns on. Also, important is to verify that the lower MOSFET gate voltage does not reach threshold when high dV/dt transition occurs on the phase node. To minimize this effect, IPM6210 has a low, 0.8Ω typical, low side driver pull-down resistance.

Requirements to the upper MOSFET $r_{DS(ON)}$ are less stringent than to the lower MOSFET because its conduction time is significantly shorter so switching losses can dominate especially at higher input voltages. It is recommended to have equal conduction and switching losses in the upper MOSFET at the nominal input voltage and load current. Then the maximum of the converter efficiency is tuned to the operating point where it is most desired. Also, this provides the most cost effective solution.

Precise calculation of power dissipation in the MOSFETs is very complex because many parameters affecting turn-on and turn-off times such as gate reverse transfer charge, gate internal resistance, body diode reverse recovery charge, package and layout impedances and their variation with the operation conditions are not available to a designer. The following equations are provided only for rough estimation of the power losses and should be accompanied by a detailed breadboard evaluation. Attention should be paid to the input voltage extremes where power dissipation in the MOSFETs is usually higher.

$$P_{UPPER} = \frac{Io^2 \times r_{DS(ON)}(V_{OUT})}{V_{IN}} + \frac{Io \times V_{IN} x Fs \times ton + toff}{2}$$

$$P_{LOWER} = Io^2 \times r_{DS(ON)} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Table 2 provides some component information for several typical applications.

Layout Considerations

Switching converters, even during normal operation, produce short pulses of current which could cause substantial ringing and be a source of EMI pollution if layout constrains are not observed.

TABLE 2

COMPONENT	CIRCUIT 1	CIRCUIT 2	CIRCUIT 3
Maximum CPU Current	8.0A	12.0A	18.0A
Inductor	2.0µH Panasonic ETQP6F2R0BFA	1.0µH Panasonic ETQP6F2R0BFA	0.8µH Panasonic ETQP6F2R0BFA
Output Capacitor	3x270µF Panasonic EEFUE0D271R or Sanyo 4x2R5TPC220M	5x270µF Panasonic EEFUE0D271R or Sanyo 6x2R5TPC220M	6x270µF Panasonic EEFUE0D271R
High-Side MOSFET	HUF76112SK8	HUF76112SK8	2x HUF76112SK8
Low-Side MOSFET	ITF86130SK8T	2x ITF86130SK8T	2x ITF86130SK8T
Current-Input Resistor for ~6% Droop At V_O = 1.6V	1.27kΩ	1.00kΩ	1.50kΩ

There are two sets of critical components in a DC-DC converter. The switching power components process large amounts of energy at high rate and though, usually appear to be a source of a noise, end a low power components responsible for bias and feedback functions, though appear to be mainly recipients of the noise. The situation with the IPM6210 control IC is even more critical as it provides control functions for two independent converters and poor layout design could lead to cross talk between the converters and result in degradation in the performance.

A multi-layer printed circuit board is recommended.

Dedicate one solid layer for a ground plane. Dedicate another solid layer as a power plane and break this plane into smaller island of common voltage levels.

Notice all the nodes that are subjected to high dV/dt voltage swing as PHASE1,2 nodes, for example. All surrounding circuitry will tend to couple the noise from these nodes trough stray capacitance. Do not oversize copper traces connected to these nodes. Do not place traces connected to the feedback components adjacent to these traces.

Keep the wiring traces from the control IC to the MOSFET gate and source as short as possible and capable to handle peak currents up to 2A. Minimize the area within the gate-source path to reduce stray inductance and eliminate parasitic ringing at the gate.

Locate small critical components like the soft-start capacitor and current sense resistors as close, as possible to the respective pins of the IC.

IPM6210 DC-DC Converter Application Circuit

Figure 12 shows an application circuit of a power supply for a notebook PC microprocessor system. The power supply provides the microprocessor core voltage (V_{CORE}), the I/O voltage ($V_{I/O}$) and the clock generator voltage (V_{CLK}) from +5.6-24V_{DC}, +5V_{DC} and +3.3V_{DC}.

Visit Intersil's web site (www.intersil.com) for the latest information.

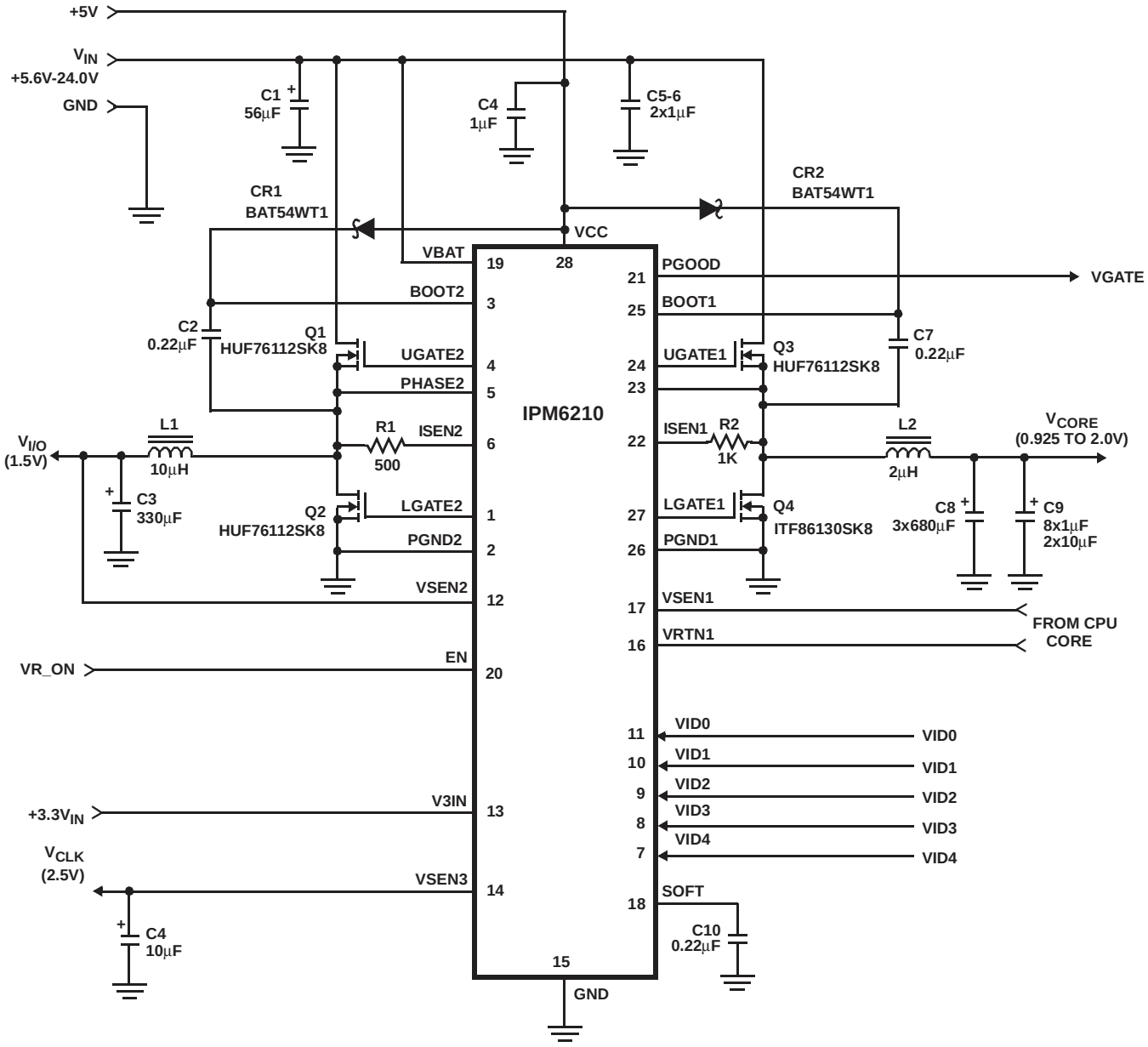
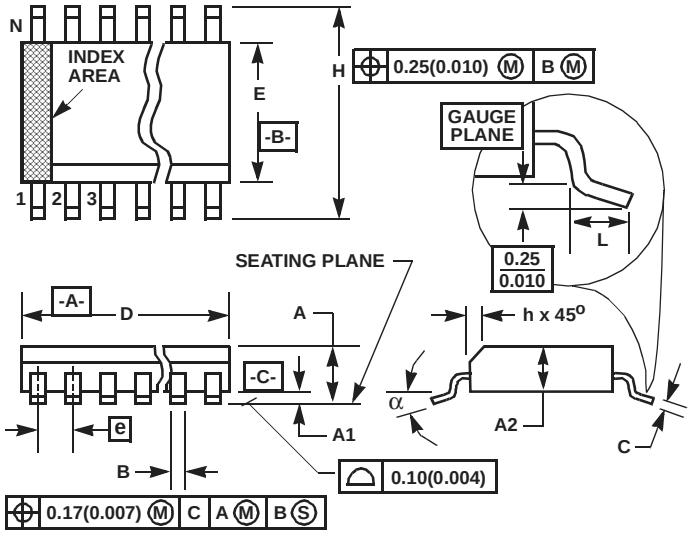


FIGURE 12. APPLICATION CIRCUIT

Shrink Small Outline Plastic Packages (SSOP)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “B” does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm (0.004 inch) total in excess of “B” dimension at maximum material condition.
10. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

M28.15

28 LEAD SHRINK NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.053	0.069	1.35	1.75	-
A1	0.004	0.010	0.10	0.25	-
A2	-	0.061	-	1.54	-
B	0.008	0.012	0.20	0.30	9
C	0.007	0.010	0.18	0.25	-
D	0.386	0.394	9.81	10.00	3
E	0.150	0.157	3.81	3.98	4
e	0.025 BSC		0.635 BSC		-
H	0.228	0.244	5.80	6.19	-
h	0.0099	0.0196	0.26	0.49	5
L	0.016	0.050	0.41	1.27	6
N	28		28		7
α	0^o	8^o	0^o	8^o	-

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