# IR2151

## SELF-OSCILLATING HALF-BRIDGE DRIVER

### Features

- Floating channel designed for bootstrap operation
  Fully operational to +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Undervoltage lockout
- Programmable oscillator frequency

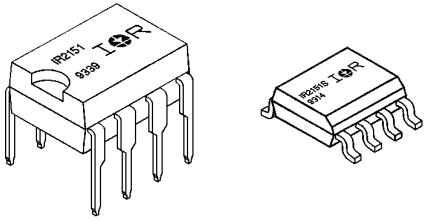
$$f = \frac{1}{1.4 \times (R_T + 75\Omega) \times C_T}$$

- Matched propagation delay for both channels
- Low side output in phase with $R_T$

### Product Summary

| | |
|---|---|
| $V_{OFFSET}$ | 600V max. |
| Duty Cycle | 50% |
| $I_O$+/- | 100 mA / 210 mA |
| $V_{OUT}$ | 10 - 20V |
| Deadtime (typ.) | 1.2 µs |

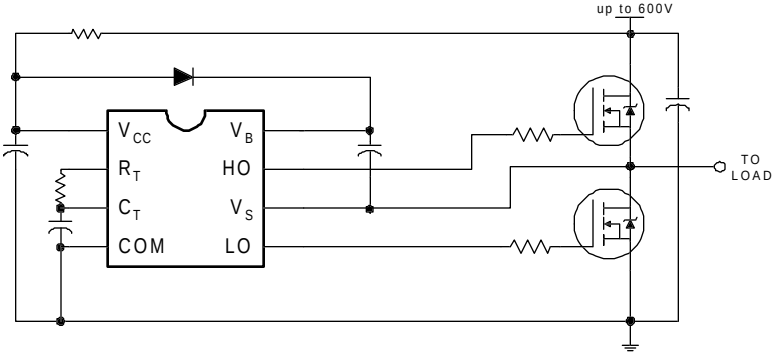
### Packages



### Description

The IR2151 is a high voltage, high speed, self-oscillating power MOSFET and IGBT driver with both high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The front end features a programmable oscillator which is similar to the 555 timer. The output drivers feature a high pulse current buffer stage and an internal deadtime designed for minimum driver cross-conduction. Propagation delays for the two channels are matched to simplify use in 50% duty cycle applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration that operates off a high voltage rail up to 600 volts.

### Typical Connection



## Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

| Parameter | | Value | | |
|---|---|---|---|---|
| Symbol | Definition | Min. | Max. | Units |
| $V_B$ | High Side Floating Supply Voltage | -0.3 | 625 | V |
| $V_S$ | High Side Floating Supply Offset Voltage | $V_B$ - 25 | $V_B$ + 0.3 | |
| $V_{HO}$ | High Side Floating Output Voltage | $V_S$ - 0.3 | $V_B$ + 0.3 | |
| $V_{LO}$ | Low Side Output Voltage | -0.3 | $V_{CC}$ + 0.3 | |
| $V_{RT}$ | $R_T$ Voltage | -0.3 | $V_{CC}$ + 0.3 | |
| $V_{CT}$ | $C_T$ Voltage | -0.3 | $V_{CC}$ + 0.3 | |
| $I_{CC}$ | Supply Current (Note 1) | — | 25 | mA |
| $I_{RT}$ | $R_T$ Output Current | -5 | 5 | |
| $dV_S/dt$ | Allowable Offset Supply Voltage Transient | — | 50 | V/ns |
| $P_D$ | Package Power Dissipation @ $T_A \leq +25°C$ (8 Lead DIP) | — | 1.0 | W |
| | (8 Lead SOIC) | — | 0.625 | |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (8 Lead DIP) | — | 125 | °C/W |
| | (8 Lead SOIC) | — | 200 | |
| $T_J$ | Junction Temperature | — | 150 | °C |
| $T_S$ | Storage Temperature | -55 | 150 | |
| $T_L$ | Lead Temperature (Soldering, 10 seconds) | — | 300 | |

## Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The $V_S$ offset rating is tested with all supplies biased at 15V differential.

| Parameter | | Value | | |
|---|---|---|---|---|
| Symbol | Definition | Min. | Max. | Units |
| $V_B$ | High Side Floating Supply Absolute Voltage | $V_S$ + 10 | $V_S$ + 20 | V |
| $V_S$ | High Side Floating Supply Offset Voltage | — | 600 | |
| $V_{HO}$ | High Side Floating Output Voltage | $V_S$ | $V_B$ | |
| $V_{LO}$ | Low Side Output Voltage | 0 | $V_{CC}$ | |
| $I_{CC}$ | Supply Current (Note 1) | — | 5 | mA |
| $T_A$ | Ambient Temperature | -40 | 125 | °C |

Note 1: Because of the IR2151's application specificity toward off-line supply systems, this IC contains a zener clamp structure between the chip $V_{CC}$ and COM which has a nominal breakdown voltage of 15.6V. Therefore, the IC supply voltage is normally derived by forcing current into the supply lead (typically by means of a high value resistor connected between the chip $V_{CC}$ and the rectified line voltage and a local decoupling capacitor from $V_{CC}$ to COM) and allowing the internal zener clamp circuit to determine the nominal supply voltage. Therefore, this circuit should not be driven by a DC, low impedance power source of greater than $V_{CLAMP}$.

## Dynamic Electrical Characteristics

$V_{BIAS}$ ($V_{CC}$, $V_{BS}$) = 12V, $C_L$ = 1000 pF and $T_A$ = 25°C unless otherwise specified.

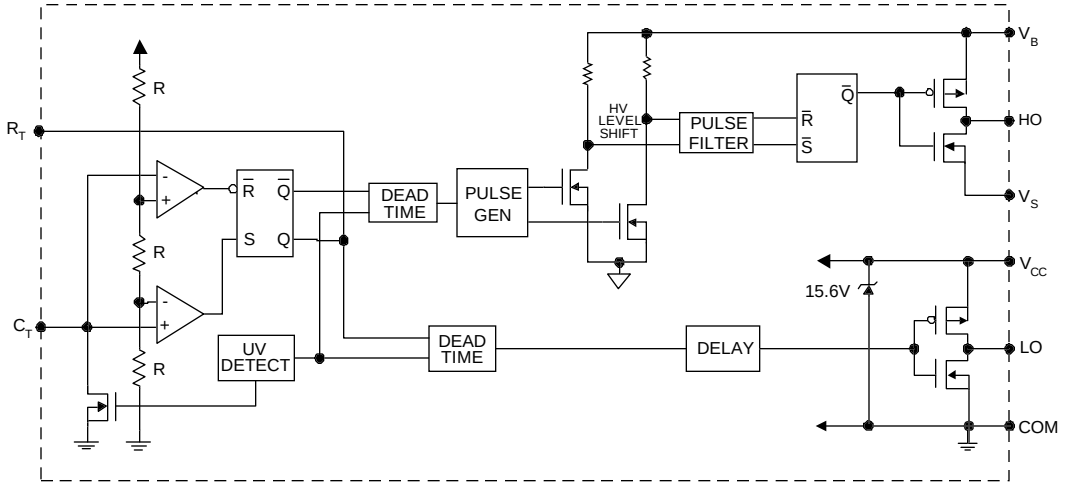
| Parameter | | Value | | | | |
|---|---|---|---|---|---|---|
| Symbol | Definition | Min. | Typ. | Max. | Units | Test Conditions |
| $t_r$ | Turn-On Rise Time | — | 80 | 120 | ns | |
| $t_f$ | Turn-Off Fall Time | — | 40 | 70 | | |
| DT | Deadtime | 0.50 | 1.20 | 2.25 | µs | |
| D | $R_T$ Duty Cycle | 48 | 50 | 52 | % | |

## Static Electrical Characteristics

$V_{BIAS}$ ($V_{CC}$, $V_{BS}$) = 12V, $C_L$ = 1000 pF, $C_T$ = 1 nF and $T_A$ = 25°C unless otherwise specified. The $V_{IN}$, $V_{TH}$ and $I_{IN}$ parameters are referenced to COM. The $V_O$ and $I_O$ parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

| Parameter | | Value | | | | |
|---|---|---|---|---|---|---|
| Symbol | Definition | Min. | Typ. | Max. | Units | Test Conditions |
| $f_{OSC}$ | Oscillator Frequency | 19.4 | 20.0 | 20.6 | kHz | $R_T$ = 35.7 kΩ |
| | | 94 | 100 | 106 | | $R_T$ = 7.04 kΩ |
| $V_{CLAMP}$ | $V_{CC}$ Zener Shunt Clamp Voltage | 14.4 | 15.6 | 16.8 | V | $I_{CC}$ = 5 mA |
| $V_{CT+}$ | 2/3 $V_{CC}$ Threshold | 7.8 | 8.0 | 8.2 | | |
| $V_{CT-}$ | 1/3 $V_{CC}$ Threshold | 3.8 | 4.0 | 4.2 | | |
| $V_{CTUV}$ | $C_T$ Undervoltage Lockout | — | 20 | 50 | mV | 2.5V<$V_{CC}$<$V_{CCUV+}$ |
| $V_{RT+}$ | $R_T$ High Level Output Voltage, $V_{CC}$ - $R_T$ | — | 0 | 100 | | $I_{RT}$ = -100 µA |
| | | — | 200 | 300 | | $I_{RT}$ = -1 mA |
| $V_{RT-}$ | $R_T$ Low Level Output Voltage | — | 20 | 50 | | $I_{RT}$ = 100 µA |
| | | — | 200 | 300 | | $I_{RT}$ = 1 mA |
| $V_{RTUV}$ | $R_T$ Undervoltage Lockout, $V_{CC}$ - $R_T$ | — | 0 | 100 | | 2.5V<$V_{CC}$<$V_{CCUV+}$ |
| $V_{OH}$ | High Level Output Voltage, $V_{BIAS}$ - $V_O$ | — | — | 100 | | $I_O$ = 0A |
| $V_{OL}$ | Low Level Output Voltage, $V_O$ | — | — | 100 | | $I_O$ = 0A |
| $I_{LK}$ | Offset Supply Leakage Current | — | — | 50 | µA | $V_B$ = $V_S$ = 600V |
| $I_{QBS}$ | Quiescent $V_{BS}$ Supply Current | — | 10 | 50 | | |
| $I_{QCC}$ | Quiescent $V_{CC}$ Supply Current | — | 400 | 950 | | |
| $I_{CT}$ | $C_T$ Input Current | — | 0.001 | 1.0 | | |
| $V_{CCUV+}$ | $V_{CC}$ Supply Undervoltage Positive Going Threshold | 7.7 | 8.4 | 9.2 | V | |
| $V_{CCUV-}$ | $V_{CC}$ Supply Undervoltage Negative Going Threshold | 7.4 | 8.1 | 8.9 | | |
| $V_{CCUVH}$ | $V_{CC}$ Supply Undervoltage Lockout Hysteresis | 200 | 500 | — | mV | |
| $I_{O+}$ | Output High Short Circuit Pulsed Current | 100 | 125 | — | mA | $V_O$ = 0V |
| $I_{O-}$ | Output Low Short Circuit Pulsed Current | 210 | 250 | — | | $V_O$ = 15V |

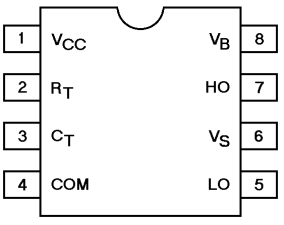
## Functional Block Diagram




## Lead Definitions

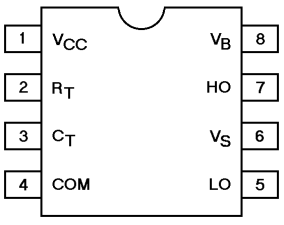
| Lead Symbol | Description |
|---|---|
| $R_T$ | Oscillator timing resistor input,in phase with LO for normal IC operation |
| $C_T$ | Oscillator timing capacitor input, the oscillator frequency according to the following equation: $f = \frac{1}{1.4 \times (R_T + 75\Omega) \times C_T}$ where 75Ω is the effective impedance of the $R_T$ output stage |
| $V_B$ | High side floating supply |
| HO | High side gate drive output |
| $V_S$ | High side floating supply return |
| $V_{CC}$ | Low side and logic fixed supply |
| LO | Low side gate drive output |
| COM | Low side return |

## Lead Assignments




8 Lead DIP

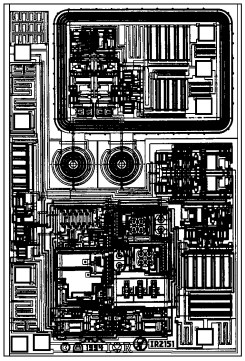
**IR2151**




SO-8

**IR2151S**

## Device Information

| | | |
|---|---|---|
| Process & Design Rule | | HVDCMOS 4.0 µm |
| Transistor Count | | 231 |
| Die Size | | 68 X 101 X 26 (mil) |
| Die Outline | |  |
| Thickness of Gate Oxide | | 800Å |
| Connections | Material | Poly Silicon |
| First Layer | Width | 5 µm |
| | Spacing | 6 µm |
| | Thickness | 5000Å |
| Second Layer | Material | Al - Si - Cu (Si: 1.0%, Cu ±0.5%) |
| | Width | 6 µm |
| | Spacing | 9 µm |
| | Thickness | 20,000Å |
| Contact Hole Dimension | | 5 µm X 5 µm |
| Insulation Layer | Material | PSG ($SiO_2$) |
| | Thickness | 1.7 µm |
| Passivation | Material | PSG ($SiO_2$) |
| | Thickness | 1.7 µm |
| Method of Saw | | Full Cut |
| Method of Die Bond | | Ablebond 84 - 1 |
| Wire Bond | Method | Thermo Sonic |
| | Material | Au (1.0 mil / 1.3 mil) |
| Leadframe | Material | Cu |
| | Die Area | Ag |
| | Lead Plating | Pb : Sn (37 : 63) |
| Package | Types | 8 Lead PDIP / SO-8 |
| | Materials | EME6300 / MP150 / MP190 |
| Remarks: | | |

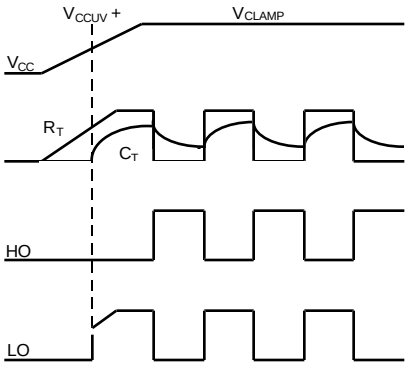



Figure 1. Input/Output Timing Diagram

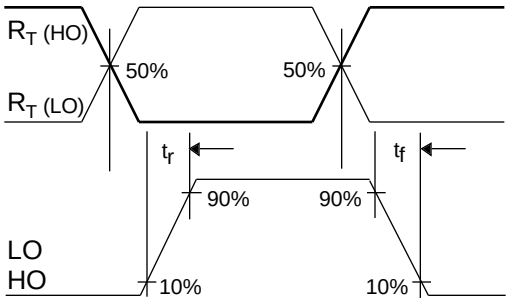



Figure 2. Switching Time Waveform Definitions

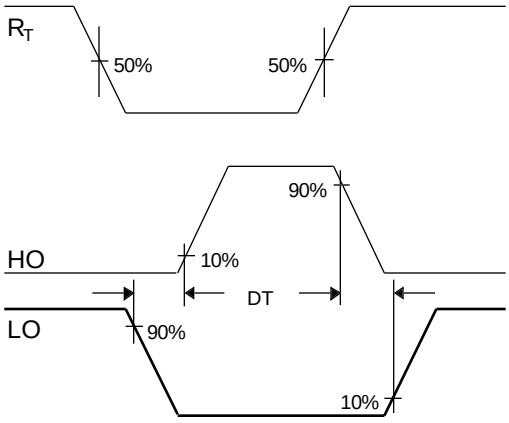



Figure 3. Deadtime Waveform Definitions