# International IR Rectifier

# IR3086

## PRELIMINARY DATA SHEET

## *XPHASE*[TM] PHASE IC WITH OVP, FAULT AND OVERTEMP DETECT

## DESCRIPTION

The IR3086 Phase IC combined with an IR *XPhase*[TM] Control IC provides a full featured and flexible way to implement power solutions for the latest high performance CPUs and ASICs. The "Control" IC provides overall system control and interfaces with any number of "Phase" ICs which each drive and monitor a single phase of a multiphase converter. The *XPhase*[TM] architecture results in a power supply that is smaller, less expensive, and easier to design while providing higher efficiency than conventional approaches.

## FEATURES

- 2.5A Average Gate Drive Current
- Loss-Less Inductor Current Sense
- Internal Inductor DCR Temperature Compensation
- Programmable Phase Delay
- Programmable Feed-Forward Voltage Mode PWM Ramp
- Sub 100ns Minimum Pulse Width supports 1MHz per-phase operation
- Current Sense Amplifier drives a single wire Average Current Share Bus
- Current Share Amplifier reduces PWM Ramp slope to ensure sharing between phases
- *Body Braking*[TM] disables Synchronous MOSFET for improved transient response and prevents negative output voltage at converter turn-off
- OVP comparator with 150ns response
- Phase Fault Detection
- Programmable Phase Over-Temperature Detection
- Small thermally enhanced 20L MLPQ package

## PACKAGE PINOUT

# International IR Rectifier

**IR3086**
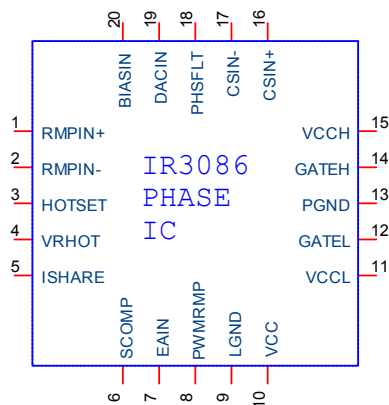
## ABSOLUTE MAXIMUM RATINGS

Operating Junction Temperature……………..150°C
Storage Temperature Range………………….-65°C to 150°C
ESD Rating……………………………………HBM Class 1C JEDEC standard

| PIN # | PIN NAME | $V_{MAX}$ | $V_{MIN}$ | $I_{SOURCE}$ | $I_{SINK}$ |
|---|---|---|---|---|---|
| 1 | RMPIN+ | 27V | -0.3V | 1mA | 1mA |
| 2 | RMPIN- | 27V | -0.3V | 1mA | 1mA |
| 3 | HOTSET | 27V | -0.3V | 1mA | 1mA |
| 4 | VRHOT | 27V | -0.3V | 1mA | 30mA |
| 5 | ISHARE | 27V | -0.3V | 5mA | 5mA |
| 6 | SCOMP | 27V | -0.3V | 1mA | 1mA |
| 7 | EAIN | 27V | -0.3V | 1mA | 1mA |
| 8 | PWMRMP | 27V | -0.3V | 1mA | 20mA |
| 9 | LGND | n/a | n/a | 50mA | n/a |
| 10 | VCC | 27V | -0.3V | n/a | 50mA |
| 11 | VCCL | 27V | -0.3V | n/a | 3A for 100ns, 200mA DC |
| 12 | GATEL | 27V | -0.3V DC, -2V for 100ns | 3A for 100ns, 200mA DC | 3A for 100ns, 200mA DC |
| 13 | PGND | 0.3V | -0.3V | 3A for 100ns, 200mA DC | n/a |
| 14 | GATEH | 27V | -0.3V DC, -2V for 100ns | 3A for 100ns, 200mA DC | 3A for 100ns, 200mA DC |
| 15 | VCCH | 27V | -0.3V | n/a | 3A for 100ns, 200mA DC |
| 16 | CSIN+ | 27V | -0.3V | 1mA | 1mA |
| 17 | CSIN- | 27V | -0.3V | 1mA | 1mA |
| 18 | PHSFLT | 27V | -0.3V | 1mA | 20mA |
| 19 | DACIN | 27V | -0.3V | 1mA | 1mA |
| 20 | BIASIN | 27V | -0.3V | 1mA | 1mA |

# ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over: $8.4V \leq V_{CC} \leq 14V$, $6V \leq V_{CCH} \leq 25V$, $6V \leq V_{CCL} \leq 25V$, and $0\,^{o}C \leq T_J \leq 125\,^{o}C$, $C_{GATEH} = 3.3nF$, $C_{GATEL} = 6.8nF$

| PARAMETER | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **Gate Drivers** | | | | | |
| GATEH Rise Time | VCCH = 12V, Measure 2V to 9V transition time | | 22 | 50 | ns |
| GATEH Fall Time | VCCH = 12V, Measure 9V to 2V transition time | | 22 | 50 | ns |
| GATEL Rise Time | VCCL = 12V, Measure 2V to 9V transition time | | 50 | 75 | ns |
| GATEL Fall Time | VCCL = 12V, Measure 9V to 2V transition time | | 50 | 75 | ns |
| GATEL low to GATEH high delay | VCCH = VCCL = 12V, Measure the time from GATEL falling to 1V to GATEH rising to 1V | 10 | 25 | 50 | ns |
| GATEH low to GATEL high delay | VCCH = VCCL = 12V, Measure the time from GATEH falling to 1V to GATEL rising to 1V | 10 | 25 | 50 | ns |
| Disable Pull-Down Current | Force GATH or GATEL = 2V with BIASIN = 0V | 15 | 25 | 40 | $\mu$A |
| **Current Sense Amplifier** | | | | | |
| CSIN+ Bias Current | | -0.5 | -0.25 | 0 | $\mu$A |
| CSIN- Bias Current | | -1 | -0.4 | 0 | $\mu$A |
| Input Offset Voltage | CSIN+ = CSIN- = DACIN. Measure input referred offset from DACIN | -3 | 0.5 | 5 | mV |
| Gain at $T_J = 25\,^{o}C$ | | 32 | 34 | 36 | V/V |
| Gain at $T_J = 125\,^{o}C$ | | 27 | 29 | 31 | V/V |
| Bandwidth (-3dB) | Note 1 | TBD | TBD | | kHz |
| Slew Rate | Current Sense Amp output is an internal node. Slew rate at the ISHARE pin will be set by the internal 10k$\Omega$ resistor and any stray external capacitance | | 12.5 | | V/$\mu$s |
| Differential Input Range | | -20 | | 100 | mV |
| Common Mode Input Range | | 0 | | 4 | V |
| Rout at $T_J = 25\,^{o}C$ | | 7.9 | 10.5 | 13.1 | k$\Omega$ |
| Rout at $T_J = 125\,^{o}C$ | | 9.3 | 12.4 | 15.5 | k$\Omega$ |
| **Ramp Discharge Clamp** | | | | | |
| Clamp Voltage | Force I(PWMRMP) = 500$\mu$A. Measure V(PWMRMP) – V(DACIN) | -10 | 5 | 20 | mV |
| Clamp Discharge Current | | 4 | 8 | | mA |

| PARAMETER | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **Ramp Comparator** | | | | | |
| Input Offset Voltage | | 20 | 40 | 80 | mV |
| Hysteresis | Note 1 | -10 | 0 | 10 | mV |
| RMPIN+, RMPIN- Bias Current | | -1 | 0 | 1 | μA |
| Propagation Delay | VCCH = 12V. Measure time from RMPIN input (50mV overdrive) to GATEL transition to <11V. | 100 | 150 | 240 | ns |
| **PWM Comparator** | | | | | |
| PWM Comparator Input Offset Voltage | | -5 | 5 | 15 | mV |
| EAIN & PWMRMP Bias Current | Clamp and Current Share Adjust OFF | -1 | -0.4 | 1 | μA |
| Propagation Delay | VCCH = 12V. Measure time from PWMRMP input (50mV overdrive) to GATEH transition to < 11V. | | 70 | 150 | ns |
| Common Mode Input Range | Exceeding the Common Mode input range results in 100% duty cycle | | | 5 | V |
| **Share Adjust Error Amplifier** | | | | | |
| Input Offset Voltage | | 10 | 20 | 30 | mV |
| PWMRMP Adjust Current | | 4 | 8 | | mA |
| Transconductance | 10μA < I(PWMRMP) > 100μA, Note 1 | 0.9 | 1.6 | 2.3 | A/V |
| SCOMP Source/Sink Current | Note 1 | 20 | 30 | 40 | μA |
| SCOMP Activation Voltage | Amount SCOMP must increase from its minimum voltage until the Ramp Slope Adjust current equals = 10μA | 60 | 150 | 300 | mV |
| PWMRMP Min Voltage | I(PWMRMP) = 500μA | 150 | 225 | 350 | mV |
| **0% Duty Cycle Comparator** | | | | | |
| Threshold Voltage | Compare to V(DACIN) | 88 | 91 | 94 | % |
| Propagation Delay | VCCL = 12V. Measure time from EAIN < 0.9 x V(DACIN) (200mV overdrive) to GATEL transition to < 11V. Note 1. | | 100 | 150 | ns |
| **OVP Comparator** | | | | | |
| Threshold Voltage | Compare to V(DACIN) | 100 | 125 | 160 | mV |
| Propagation Delay | VCCL = 12V. Measure time from CSIN > V(DACIN) (200mV overdrive) to GATEL transition to <11V. | | 150 | 250 | ns |
| **Phase Fault Comparator** | | | | | |
| Threshold Voltage | Compare to V(DACIN) | 88 | 91 | 94 | % |
| Output Voltage | I(PHSFLT) = 4mA | | 300 | 400 | mV |
| PHSFLT Leakage Current | V(PHSFLT) = 5.5V | | 0 | 10 | μA |

| PARAMETER | TEST CONDITION | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **General** | | | | | | |
| VCC Supply Current | | | | 8 | 12 | mA |
| VCCL Supply Current | | | | 4 | 6 | mA |
| VCCH Supply Current | $6V \leq V_{CCH} \leq 14V$ | | | 6 | 7.5 | mA |
| | $14V \leq V_{CCH} \leq 25V$ | | | 7 | 10 | mA |
| BIASIN Bias Current | | | -5 | -2.5 | 1 | $\mu$A |
| DACIN Bias Current | | | -2 | -0.5 | 1 | $\mu$A |
| **VRHOT Comparator** | | | | | | |
| HOTSET Bias Current | | | -2 | -0.5 | 1 | $\mu$A |
| Output Voltage | I(VRHOT) = 24mA | | | 150 | 400 | mV |
| VRHOT Leakage Current | V(VRHOT) = 5.5V | | | 0 | 10 | $\mu$A |
| Threshold Hysteresis | $T_J \geq 85\,^{o}C$ | | 3.0 | 7.0 | 9.0 | $^{o}C$ |
| | | MIN | TYP | | MAX | |
| Threshold Voltage | $T_J \geq 85\,^{o}C$ | $4.73mV/\,^{o}C \times T_J + 1.176V$ | $4.73mV/\,^{o}C \times T_J + 1.241V$ | | $4.73mV/\,^{o}C \times T_J + 1.356V$ | V |

**Note 1:** Guaranteed by design, but not tested in production

# International IR Rectifier

# IR3086

## PIN DESCRIPTION

| PIN# | PIN SYMBOL | PIN DESCRIPTION |
|------|-----------|-----------------|
| 1 | RMPIN+ | Non-inverting input to Ramp Comparator |
| 2 | RMPIN- | Inverting input to Ramp Comparator |
| 3 | HOTSET | Inverting input to VRHOT comparator. Connect resistor divider from VBIAS to LGND to program VRHOT threshold. Diode or thermistor may be substituted for lower resistor for enhanced/remote temperature sensing. |
| 4 | VRHOT | Open Collector output of the VRHOT comparator which drives low if IC junction temperature exceeds the user programmable limit. Connect external pull-up. |
| 5 | ISHARE | Output of the Current Sense Amplifier and input to the Share Adjust Error Amplifier. Voltage on this pin is equal to $V(DACIN) + 34 [V(CSIN+) – V(CSIN-)]$. Connecting ISHARE pins creates a Share Bus enabling current sharing between Phase ICs. The Share bus is also used by the Control IC for voltage positioning and Over-Current protection. |
| 6 | SCOMP | Compensation for the Current Share control loop. Connect a capacitor to ground to set the control loop's bandwidth. |
| 7 | EAIN | PWM comparator input from the Control IC. Both Gate Driver outputs drive low if the voltage on this pin is less than 91% of V(DACIN). |
| 8 | PWMRMP | PWM comparator ramp input. Connect a resistor from this pin to the converter input voltage and a capacitor to LGND to program the PWM ramp. |
| 9 | LGND | Signal ground and IC substrate connection |
| 10 | VCC | Power for internal circuitry |
| 11 | VCCL | Power for Low-Side Gate Driver |
| 12 | GATEL | Low-Side Gate Driver Output and input to GATEH non-overlap comparator |
| 13 | PGND | Return for Gate Drivers |
| 14 | GATEH | High-Side Gate Driver Output and input to GATEL non-overlap comparator |
| 15 | VCCH | Power for High-Side Gate Driver |
| 16 | CSIN+ | Non-inverting input to the Current Sense Amplifier |
| 17 | CSIN- | Inverting input to the Current Sense Amplifier and non-inverting input to the OVP comparator |
| 18 | PHSFLT | Open Collector output of the Phase Fault comparator. Drives low if Phase current is unable to match the level of the SHARE bus due to an external fault. Connect external pull-up. |
| 19 | DACIN | Reference voltage input from the Control IC and inverting input to the OVP comparator. Current sensing and PWM operation referenced to this pin. |
| 20 | BIASIN | System reference voltage for internal circuitry |

# SYSTEM THEORY OF OPERATION

## *XPhase*<sup>TM</sup> Architecture

The *XPhase*<sup>TM</sup> architecture is designed for multiphase interleaved buck converters which are used in applications requiring small size, design flexibility, low voltage, high current and fast transient response. The architecture can be used in any multiphase converter ranging from 1 to 16 or more phases where flexibility facilitates the design trade-off of multiphase converters. The scalable architecture can be applied to other applications which require high current or multiple output voltages.

As shown in Figure 1, the *XPhase*<sup>TM</sup> architecture consists of a Control IC and a scalable array of phase converters each using a single Phase IC. The Control IC communicates with the Phase ICs through a 5-wire analog bus, i.e. bias voltage, phase timing, average current, error amplifier output, and VID voltage. The Control IC incorporates all the system functions, i.e. VID, PWM ramp oscillator, error amplifier, bias voltage, and fault protections etc. The Phase IC implements the functions required by the converter of each phase, i.e. the gate drivers, PWM comparator and latch, over-voltage protection, and current sensing and sharing.

There is no unused or redundant silicon with the *XPhase*<sup>TM</sup> architecture compared to others such as a 4 phase controller that can be configured for 2, 3, or 4 phase operation.  PCB Layout is easier since the 5 wire bus eliminates the need for point-to-point wiring between the Control IC and each Phase. The critical gate drive and current sense connections are short and local to the Phase ICs. This improves the PCB layout by lowering the parasitic inductance of the gate drive circuits and reducing the noise of the current sense signal.
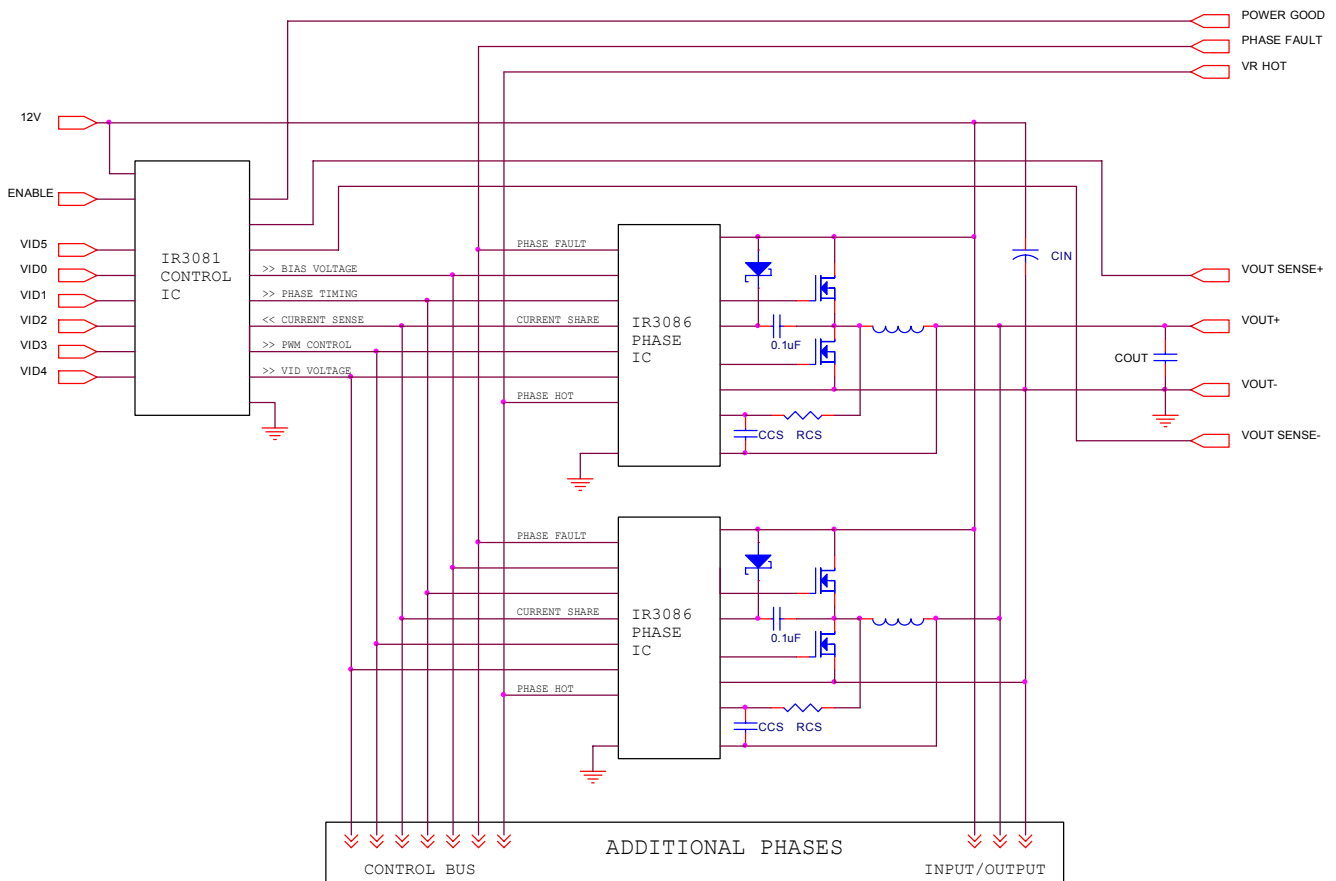


Figure 1 – System Block Diagram

**PWM Control Method**

The PWM block diagram of the *XPhase*[TM] architecture is shown in Figure 2. Feed-forward voltage mode control with trailing edge modulation is used. A high-gain wide-bandwidth voltage type error amplifier in the Control IC is used for the voltage control loop. An external RC circuit connected to the input voltage and ground is used to program the slope of the PWM ramp and to provide the feed-forward control at each phase. The PWM ramp slope will change with the input voltage and automatically compensate for changes in the input voltage. The input voltage can change due to variations in the silver box output voltage or due to drops in the PCB related to changes in load current.
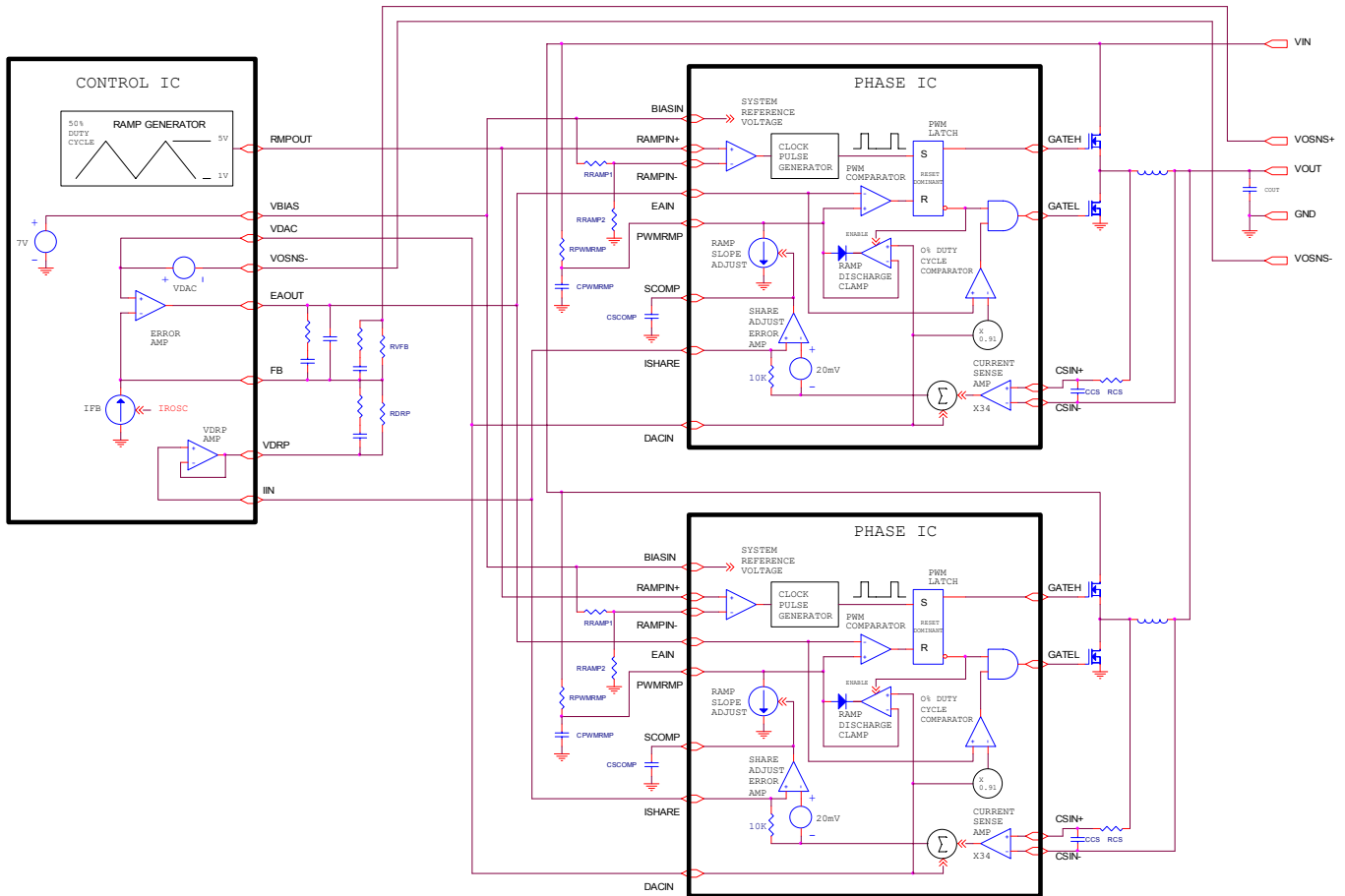


Figure 2 – PWM Block Diagram

**Frequency and Phase Timing Control**

The oscillator is located in the Control IC and its frequency is programmable from 100kHz to 1MHZ by an external resistor. The output of the oscillator is a 50% duty cycle triangle waveform with peak and valley voltages of approximately 5V and 1V. This signal is used to program both the switching frequency and phase timing of the Phase ICs. The Phase IC is programmed by resistor divider RRAMP1 and RRAMP2 connected between the VBIAS reference voltage and the Phase IC LGND pin. A comparator in the Phase ICs detects the crossing of the oscillator waveform with the voltage generated by the resistor divider and triggers a clock pulse that starts the PWM cycle. The peak and valley voltages track the VBIAS voltage reducing potential Phase IC timing errors. Figure 3 shows the Phase timing for an 8 phase converter. Note that both slopes of the triangle waveform can be used for synchronization by swapping the RAMP + and – pins.
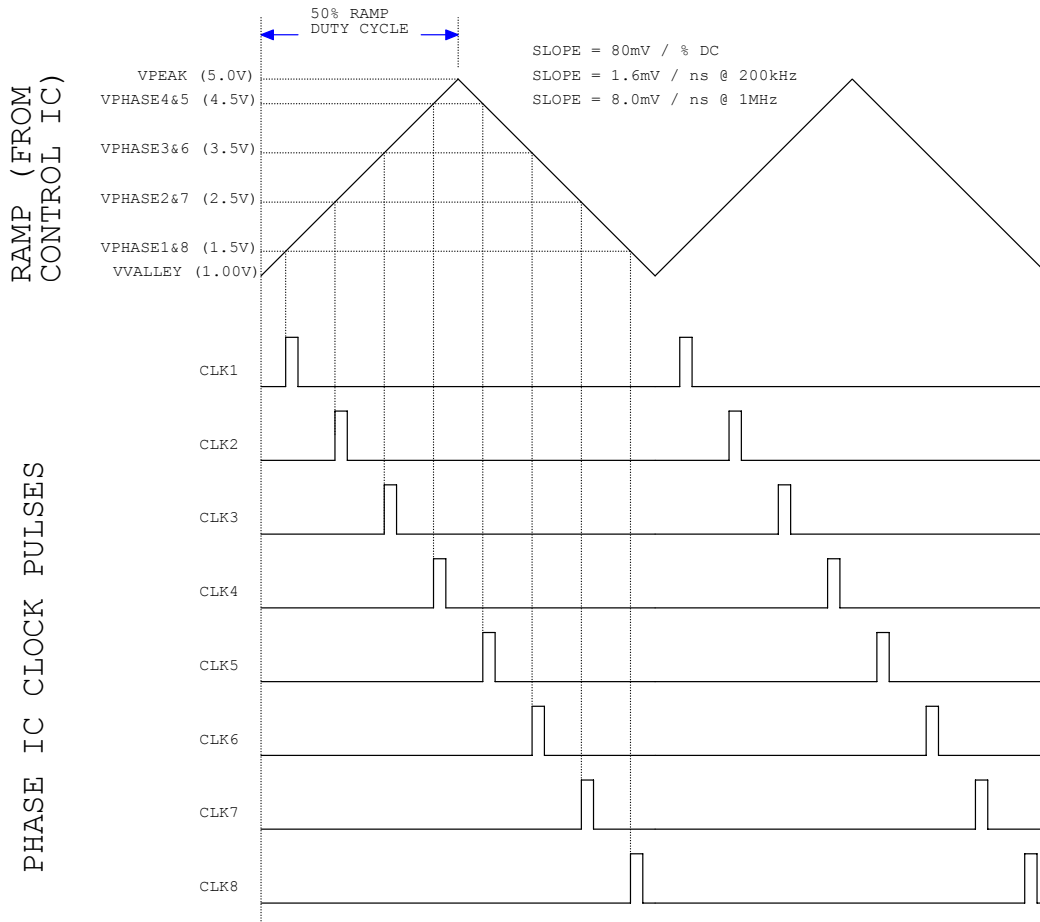
Figure 3 – 8 Phase Oscillator Waveforms

**PWM Operation**

The PWM comparator is located in the Phase IC. Upon receiving a clock pulse, the PWM latch is set, the PWMRMP voltage begins to increase, the low side driver is turned off, and the high side driver is then turned on. When the PWMRMP voltage exceeds the Error Amp's output voltage the PWM latch is reset. This turns off the high side driver, turns on the low side driver, and activates the Ramp Discharge Clamp. The clamp quickly discharges the PWMRMP capacitor to the VDAC voltage of the Control IC until the next clock pulse.

The PWM latch is reset dominant allowing all phases to go to zero duty cycle within a few tens of nanoseconds in response to a load step decrease. Phases can overlap and go to 100% duty cycle in response to a load step increase with turn-on gated by the clock pulses. An Error Amp output voltage greater than the common mode input range of the PWM comparator results in 100% duty cycle regardless of the voltage of the PWM ramp. This arrangement guarantees the Error Amp is always in control and can demand 0 to 100% duty cycle as required. It also favors response to a load step decrease which is appropriate given the low output to input voltage ratio of most systems. The inductor current will increase much more rapidly than decrease in response to load transients.

This control method is designed to provide "single cycle transient response" where the inductor current changes in response to load transients within a single switching cycle maximizing the effectiveness of the power train and minimizing the output capacitor requirements. An additional advantage is that differences in ground or input voltage at the phases have no effect on operation since the PWM ramps are referenced to VDAC.

## Body Braking$^{TM}$

In a conventional synchronous buck converter, the minimum time required to reduce the current in the inductor in response to a load step decrease is;

$$T_{SLEW} = [L \times (I_{MAX} - I_{MIN})] / Vout$$

The slew rate of the inductor current can be significantly increased by turning off the synchronous rectifier in response to a load step decrease. The switch node voltage is then forced to decrease until conduction of the synchronous rectifier's body diode occurs. This increases the voltage across the inductor from Vout to Vout + V$_{BODY\ DIODE}$. The minimum time required to reduce the current in the inductor in response to a load transient decrease is now;

$$T_{SLEW} = [L \times (I_{MAX} - I_{MIN})] / (Vout + V_{BODY\ DIODE})$$

Since the voltage drop in the body diode is often higher than output voltage, the inductor current slew rate can be increased by 2X or more. This patent pending technique is referred to as "body braking" and is accomplished through the "0% Duty Cycle Comparator" located in the Phase IC. If the Error Amp's output voltage drops below 91% of the VDAC voltage this comparator turns off the low side gate driver.

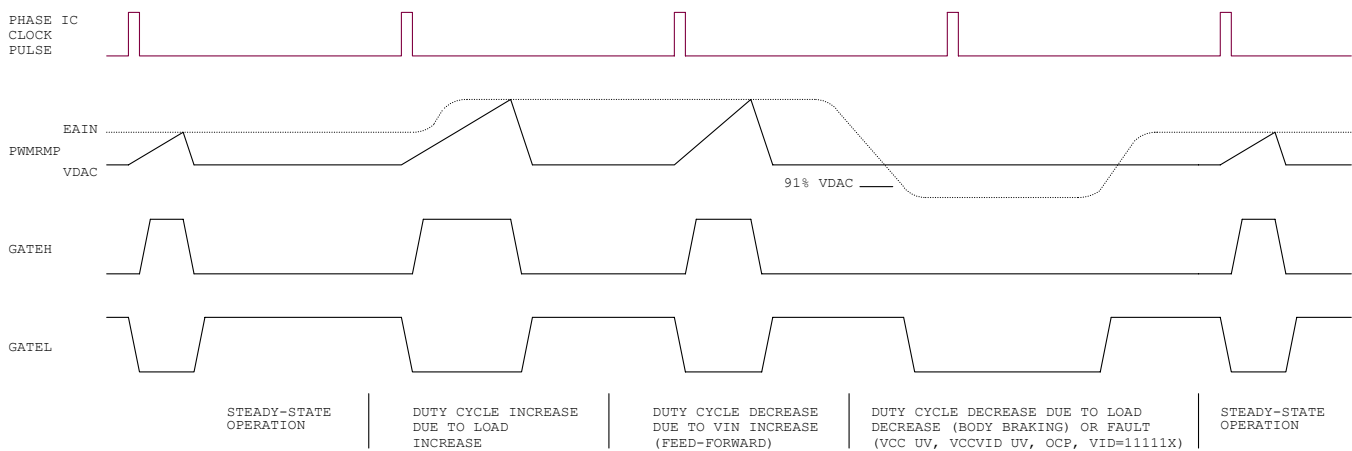Figure 4 depicts PWM operating waveforms under various conditions



Figure 4 – PWM Operating Waveforms

## Lossless Average Inductor Current Sensing

Inductor current can be sensed by connecting a resistor and a capacitor in parallel with the inductor and measuring the voltage across the capacitor. The equation of the sensing network is,

$$v_C(s) = v_L(s)\frac{1}{1 + sR_SC_S} = i_L(s)\frac{R_L + sL}{1 + sR_SC_S}$$

Usually the resistor Rcs and capacitor Ccs are chosen so that the time constant of Rcs and Ccs equals the time constant of the inductor which is the inductance L over the inductor DCR. If the two time constants match, the voltage across Ccs is proportional to the current through L, and the sense circuit can be treated as if only a sense resistor with the value of R$_L$ was used. The mismatch of the time constants does not affect the measurement of inductor DC current, but affects the AC component of the inductor current.

The advantage of sensing the inductor current versus high side or low side sensing is that actual output current being delivered to the load is obtained rather than peak or sampled information about the switch currents. The output voltage can be positioned to meet a load line based on real time information. Except for a sense resistor in series with inductor, this is the only sense method that can support a single cycle transient response. Other methods provide no information during either load increase (low side sensing) or load decrease (high side sensing).

An additional problem associated with peak or valley current mode control for voltage positioning is that they suffer from peak-to-average errors. These errors will show in many ways but one example is the effect of frequency variation. If the frequency of a particular unit is 10% low, the peak to peak inductor current will be 10% larger and the output impedance of the converter will drop by about 10%. Variations in inductance, current sense amplifier bandwidth, PWM prop delay, any added slope compensation, input voltage, and output voltage are all additional sources of peak-to-average errors.

**Current Sense Amplifier**

A high speed differential current sense amplifier is located in the Phase IC, as shown in figure 5. Its gain decreases with increasing temperature and is nominally 34 at 25ºC and 29 at 125ºC (-1470 ppm/ºC). This reduction of gain tends to compensate the 3850 ppm/ºC increase in inductor DCR. Since in most designs the Phase IC junction is hotter than the inductor these two effects tend to cancel such that no additional temperature compensation of the load line is required.

The current sense amplifier can accept positive differential input up to 100mV and negative up to -20mV before clipping. The output of the current sense amplifier is summed with the DAC voltage and sent to the Control IC and other Phases through an on-chip 10KΩ resistor connected to the ISHARE pin. The ISHARE pins of all the phases are tied together and the voltage on the share bus represents the total current being delivered to the load and is used by the Control IC for voltage positioning and current limit protection.
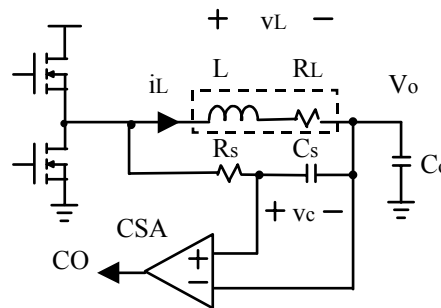


Figure 5 – Inductor Current Sensing and Current Sense Amplifier

**Average Current Share Loop**

Current sharing between phases of the converter is achieved by the average current share loop in each Phase IC. The output of the current sense amplifier is compared with the share bus less a 20mV offset. If current in a phase is smaller than the average current, the share adjust error amplifier of the phase will activate a current source that reduces the slope of its PWM ramp thereby increasing its duty cycle and output current. The crossover frequency of the current share loop can be programmed with a capacitor at the SCOMP pin so that the share loop does not interact with the output voltage loop.

# IR3086 THEORY OF OPERATION

### Block Diagram

The Block diagram of the IR3086 is shown in figure 6 and specific features discussed in the following section.
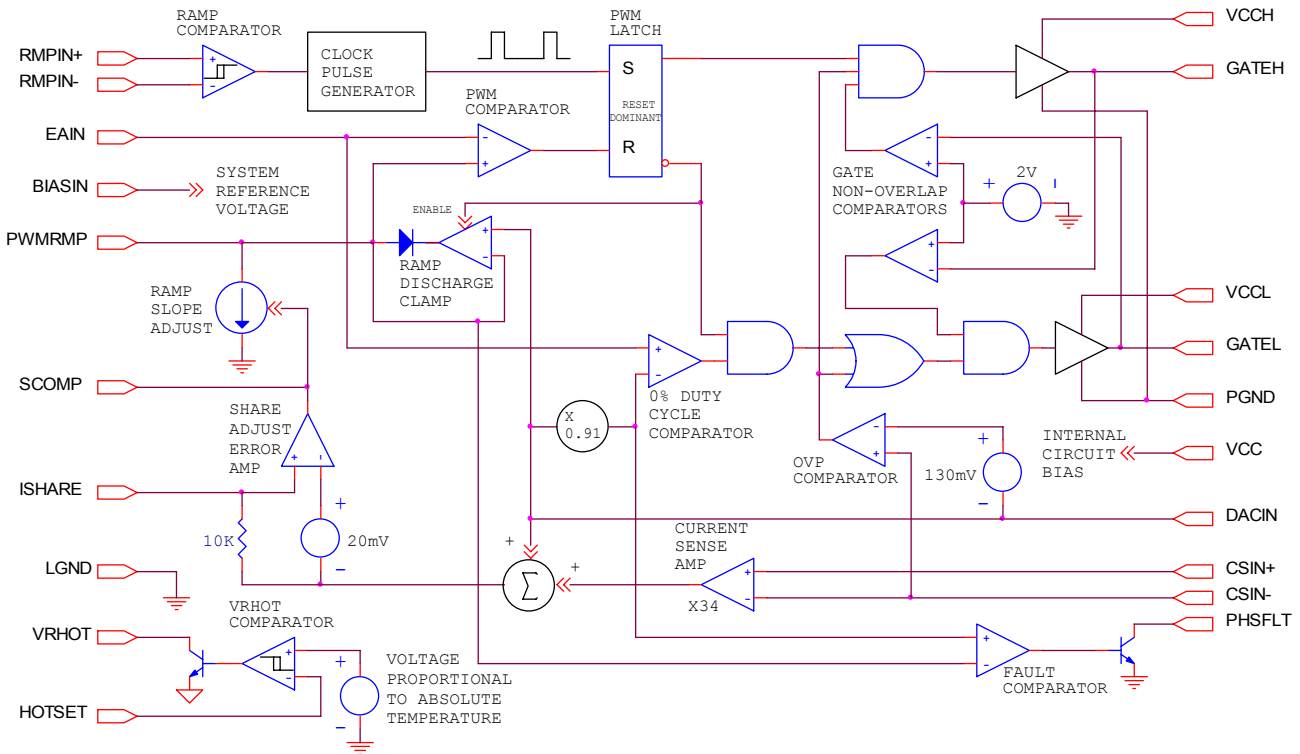


Figure 6 – IR3086 Block Diagram

### Tri-State Gate Drivers

The gate drivers can deliver up to 3A peak current. An adaptive non-overlap circuit monitors the voltage on the GATEH and GATEL pins to prevent MOSFET shoot-through current while minimizing body diode conduction.

An Enable signal is provided by the Control IC to the Phase IC without the additional of a dedicated signal line. The Error Amplifier output of the Control IC drives low in response to any fault condition such as input under voltage or output overload. The IR3086 0% duty cycle comparator detects this and drives both gate outputs low. This tri-state operation prevents negative inductor current and negative output voltage during power-down.

The Gate Drivers revert to a high impedance "off" state at VCCL and VCCH supply voltages below the normal operating range. An 80kΩ resistor is connected across the GATEX and PGND pins to prevent the GATEX voltage from rising due to leakage or other cause under these conditions.

**Over Voltage Protection (OVP)**

The IR3086 includes over-voltage protection that turns on the low side MOSFET to protect the load in the event of a shorted high-side MOSFET or connection of the converter output to an excessive output voltage. A comparator monitors the voltage at the CSIN+ pin which is usually connected directly to the converter output. If the voltage exceeds the DACIN voltage plus 130mV the GATEL pin drives high. The OVP circuit over-rides the normal PWM operation and will fully turn-on the low side MOSFET within approximately 150ns. The low side MOSFET will remain ON until the over-voltage condition ceases.

When designing for OVP the overall system must be considered. In many cases the over-current protection of the AC-DC or DC-DC converter supplying the multiphase converter will be triggered thus providing effective protection without damage as long as all PCB traces and components are sized to handle the worst-case maximum current. If this is not possible a fuse can be added in the input supply to the multiphase converter. One scenario to be careful of is where the input voltage to the multiphase converter may be pulled below the level where the ICs can provide adequate voltage to the low side MOSFET thus defeating OVP.

Dynamic changes in the VID code to a lower output voltage may trigger OVP. For example; a 250mV decrease in output voltage combined with a light load condition will cause the low side MOSFETs to turn on and interfere with Body Braking$^{TM}$. This will not cause a problem however as Body Braking$^{TM}$ will resume once the output voltage is less than 130mV above the VID voltage.

Excessive distribution impedance between the converter and load or programming of the converter output voltage above the VID voltage may trigger OVP during normal operation. If the voltage dropped across the distribution impedance exceeds the minimum OVP comparator threshold of 100mV plus any voltage positioning the IR3086 can not be used. For example; a converter having 25mV of VID offset, 125mV of AVP at full load, and 75mV of drop in the distribution path at full load would be OK since 100mV + 25mV + 125mV = 250mV which is greater than 75mV. The IR3088 Phase IC without OVP should be used in applications with excessive distribution impedance.

**Thermal Monitoring (VRHOT)**

The IR3086 senses its own die temperature and produces a voltage at the input of the VRHOT comparator that is proportional to temperature. An external resistor divider connected from VBIAS to the HOTSET pin and ground can be used to program the thermal trip point of the VRHOT comparator. The VRHOT pin is an open-collector output and should be pulled up to a voltage source through a resistor. If the thermal trip point is reached the VRHOT output drives low.

**Phase Fault**

Its possible for multiphase converters to appear to be working correctly with one or more phases not functioning. The output voltage can still be regulated and the full load current may still be delivered. However, the remaining phase(s) will be stressed far beyond their intended design limits and are likely to fail. Loss of a phase can occur due to poor solder connections or mounting during the manufacturing process, or can occur in the field. The most common failure mode of a buck converter is failure of the high side MOSFET.

The IR3086 has the ability to detect if a phase stops switching and can provide this information to the system through the PHSFLT output pin. If a phase stops switching its output current will drop to zero and the output of its IR3086 current sense amp will be the DACIN voltage. The Share Adjust Amplifier reacts to this by increasing the Ramp Slope Adjust current until it exceeds the externally programmable PWM Ramp bias current. This will cause the voltage at the PWMRMP pin to drop below its normal operating range. The Fault Comparator trips and drives the PHSFLT output to ground when the voltage on the PWMRMP pin falls below 91% of the DACIN voltage. PHSFLT is an open-collector output and should be pulled up to a voltage source through a resistor.

# APPLICATIONS INFORMATION



Figure 7 – 5 Phase IR3081/3086 EVRD10 Converter

## TYPICAL PERFORMANCE CHARACTERISTICS

**To be added:**

1. Switching Frequency vs RT and CT for 1V ramp amplitude at 10% Duty Cycle with Vcc=12V, VDAC=1.35V

2. Gate Rise and Fall Times versus Load Capacitance and Supply Voltage

3. Non-Overlap Time vs Load Capacitance and Supply Voltage (Measured at GATEX = 1V).

4. Current Sense Amp Gain versus temperature

5. Current Sense Amp Gain distribution data

6. Current Sense Input Offset distribution data

7. VRHOT Thresholds versus temperature

**PACKAGE INFORMATION**

**20L MLPQ (4 x 4mm Body) – $\theta_{JA}$ = 32$^o$C/W, $\theta_{JC}$ = 3$^o$C/W**
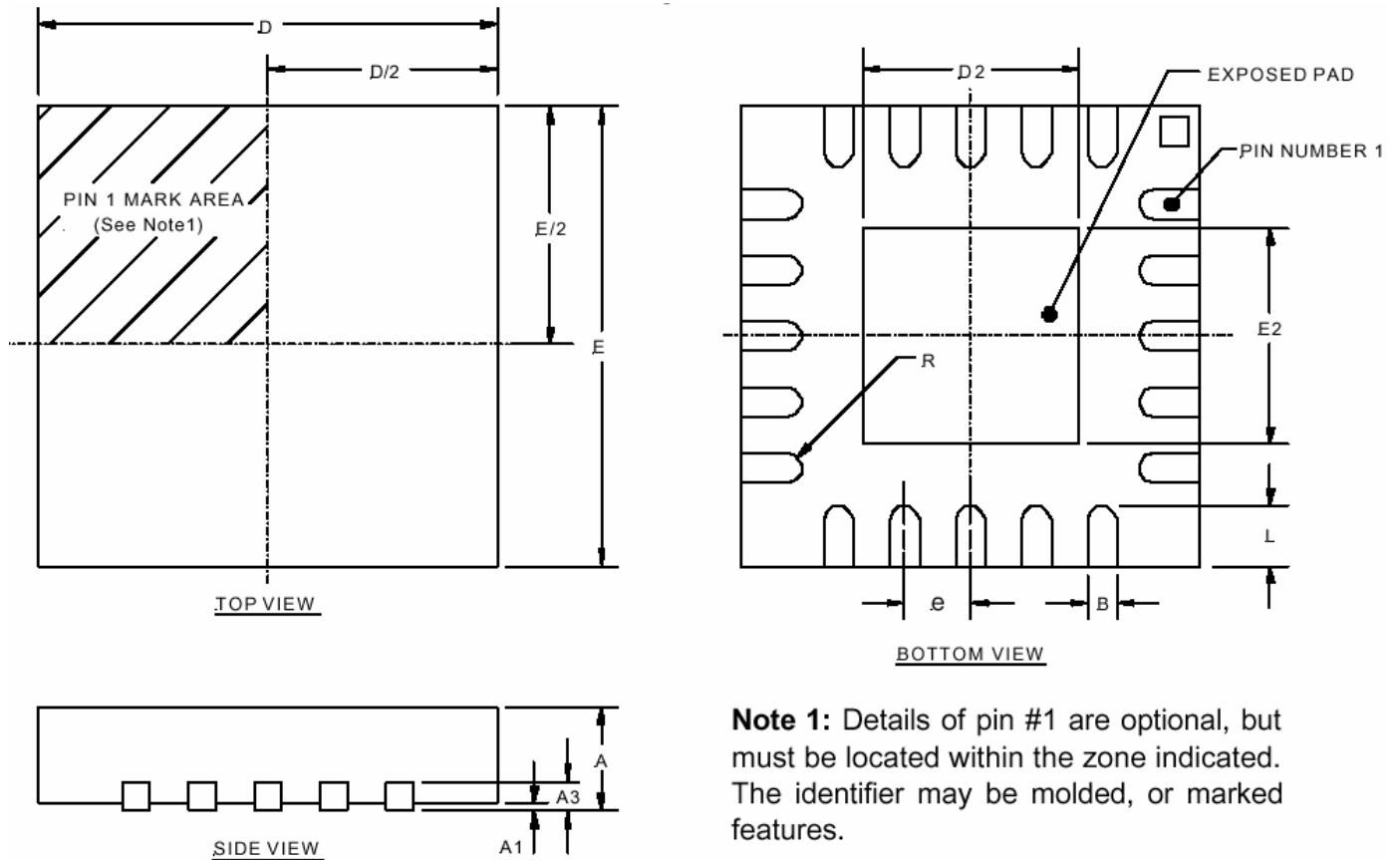


**Note 1:** Details of pin #1 are optional, but must be located within the zone indicated. The identifier may be molded, or marked features.

| SYMBOL | 20-PIN 4x4 | | |
|---|---|---|---|
| DESIG | MIN | NOM | MAX |
| A | 0.80 | 0.90 | 1.00 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | 0.20 REF | | |
| B | 0.18 | 0.23 | 0.30 |
| D | 4.00 BSC | | |
| D2 | 2.00 | 2.15 | 2.25 |
| E | 4.00 BSC | | |
| E2 | 2.00 | 2.15 | 2.25 |
| e | 0.50 BSC | | |
| L | 0.45 | 0.55 | 0.65 |
| R | 0.09 | --- | --- |

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.