## Multi-Output Low Dropout Linear Regulator with Integrated Microprocessor Reset Circuit

The ISL6411 integrates three ultra low noise, low dropout linear regulators providing a highly integrated single-chip solution for wireless chipset architectures. It operates from 2.7V to 3.8V input. The device provides preset output voltages - LDO1 is set at 1.8V, LDO2 and LDO3 are set at 2.84V.

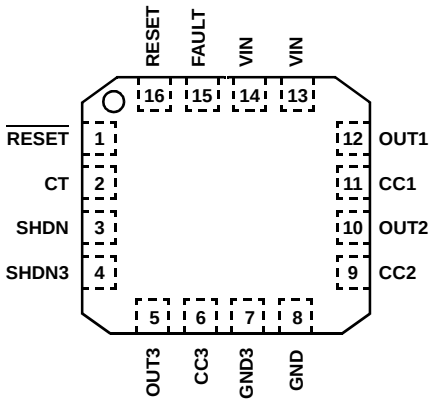
The device features specific power sequencing for wireless chipsets. A regulator is sequenced such that LDO1, the 1.8V core regulator voltage, is always stabilized before LDO2, the 2.84V output LDO, is sequenced on. When powering down, power to the 2.84V LDO2 is removed before the 1.8V LDO1 core regulator is sequenced off.

Designed with an internal P-channel MOSFET pass transistor, the ISL6411 has a low supply current. An output fault detection circuit indicates loss of regulation on any of the three outputs. Other features include a logic controlled shutdown mode, short circuit and thermal shutdown protection, and reverse battery protection.

The ISL6411 also includes a RESET function. Integration of this function into the ISL6411 eliminates the additional RESET IC and external support components required in wireless chipset power supply applications. The IC asserts a RESET signal whenever the $V_{CC}$ (IN) supply voltage drops below a preset threshold, keeping it asserted for at least 100mS after $V_{CC}$ (IN) has risen above the reset threshold. Two RESET outputs are provided; $\overline{\text{RESET}}$ is a push-pull active-LOW output, while RESET is an active-HIGH output.

## Pinout

**ISL6411 (QFN)**
TOP VIEW




## Features

- High Output Current
  - LDO1, 1.8V . . . . . 500mA
  - LDO2, 2.84V . . . . . 300mA
  - LDO3, 2.84V . . . . . 200mA
- Low Output Voltage Noise . . . . . $20\mu V_{RMS}$
- Low Dropout Voltage
  - LDO2 and LDO3 . . . . . 105mV at 200mA
- Low No-Load Supply Current
  - LDO2 and LDO3 . . . . . 120µA
  - LDO1 . . . . . 80µA
- Integrated Microprocessor RESET Circuit
  - Power-On RESET Pulse Width . . . . . 25msec(Min.)
  - Push-Pull Active-LOW and Active-HIGH Outputs
  - Power Supply Transient Immunity
  - No External Components Needed
- Thermal-Overload and Short Circuit Protection
- Reverse Battery Protection
- Logic Controlled Shutdown
- FAULT Indicator
- Space-Saving, Low Profile MLF Packaging
- Small Output Capacitors Save Space and Cost
- QFN Package
  - Compliant to JEDEC PUB95 MO-220 QFN-Quad Flat No Leads-Product Outline
  - Near Chip-Scale Package Footprint; Improves PCB Efficiency and Thinner in Profile

## Applications

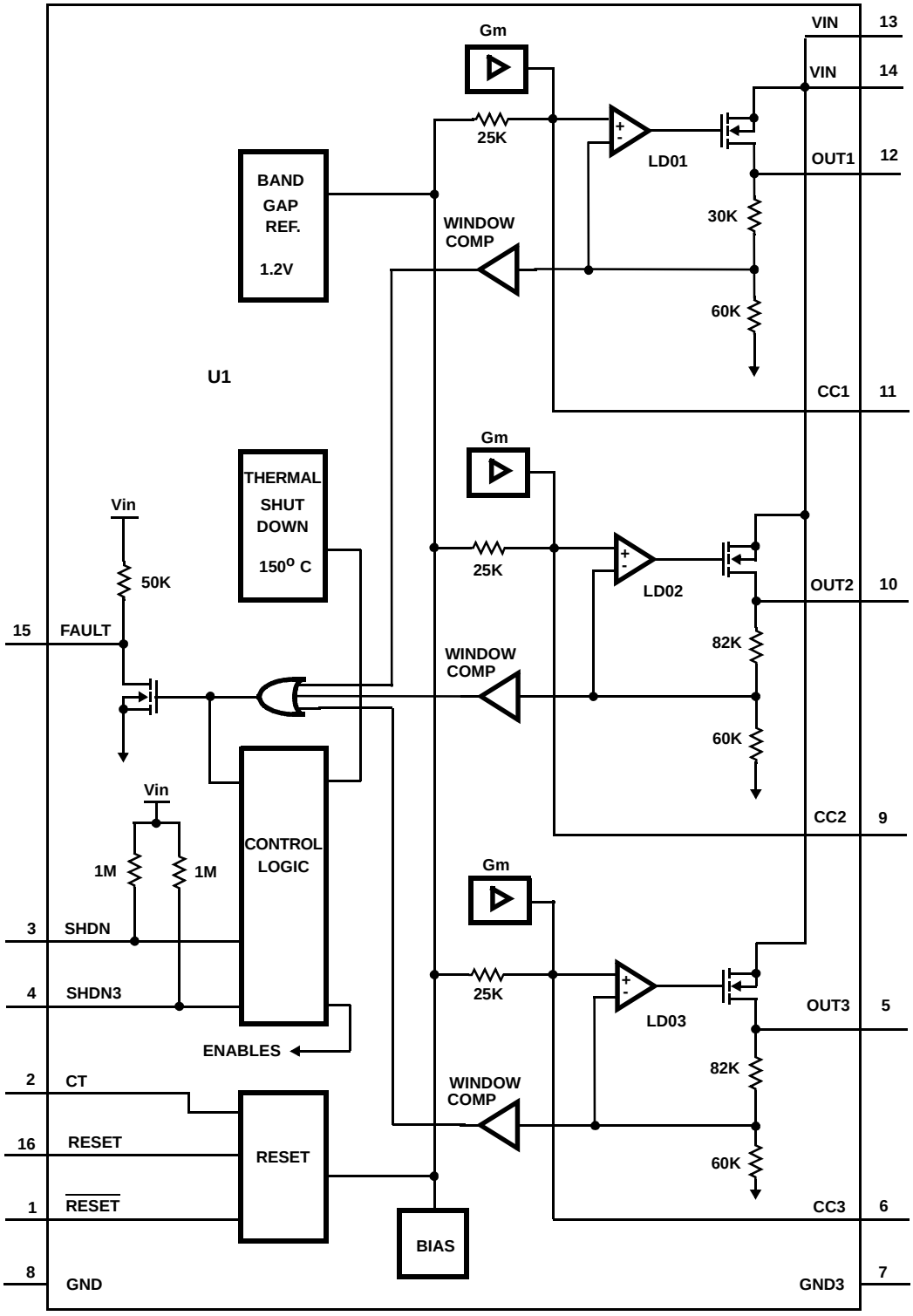
- Wireless Chipsets
- Cardbus 32
- PCMCIA Cards
- Wireless Handsets
- DSP Core Power
- Palmtop Computers
- Electronic Planners
- Hand-Held Instruments

## Ordering Information

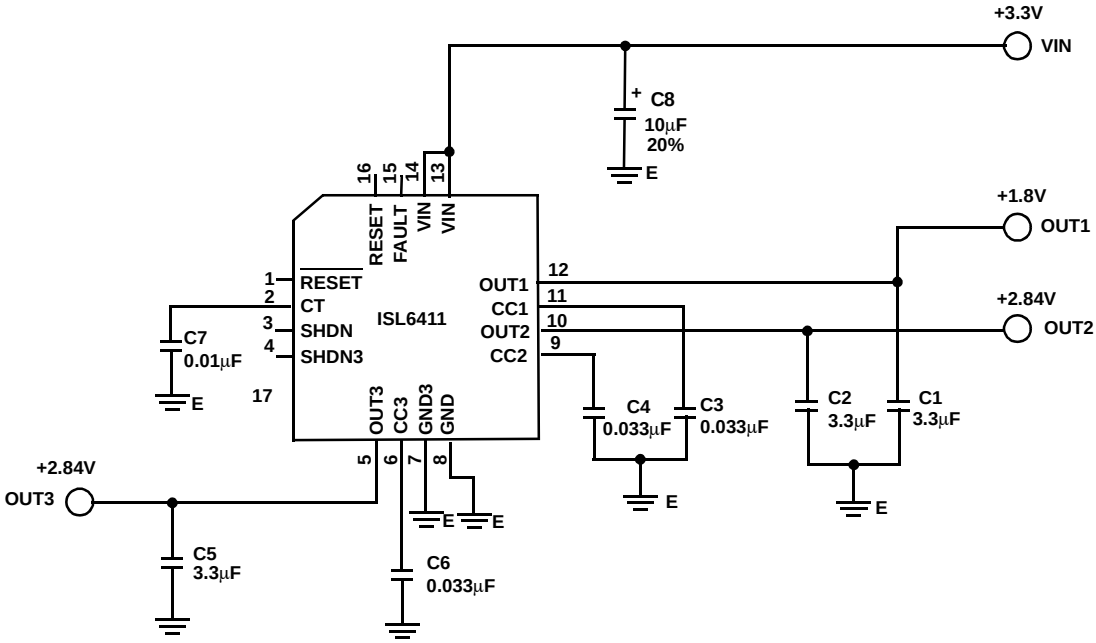
| PART NUMBER | TEMP. RANGE ($^oC$) | PACKAGE | PKG. NO. |
|---|---|---|---|
| ISL6411IR (Note) | -40 to 85 | 16 Ld QFN | L16.4x4 |

NOTE: All specifications are subject to change.

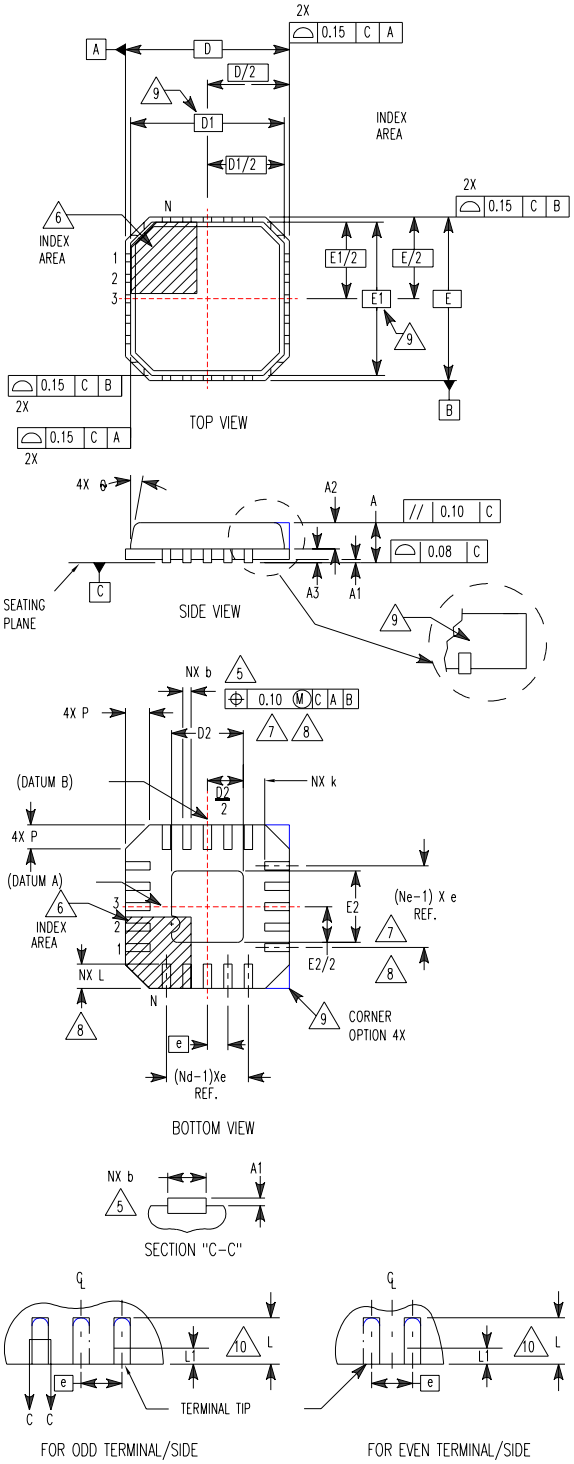
## Functional Block Diagram



## Typical Application Schematic



## *Quad Flat No-Lead Plastic Package (QFN)*
## *Micro Lead Frame Plastic Package (MLFP)*




## L16.4x4

**16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220-VGGC ISSUE C)**

| SYMBOL | MILLIMETERS | | | NOTES |
|---|---|---|---|---|
| | MIN | NOMINAL | MAX | |
| A | 0.80 | 0.90 | 1.00 | - |
| A1 | - | - | 0.05 | - |
| A2 | - | - | 1.00 | 9 |
| A3 | | 0.20 REF | | 9 |
| b | 0.23 | 0.28 | 0.38 | 5, 8 |
| D | | 4.00 BSC | | - |
| D1 | | 3.75 BSC | | 9 |
| D2 | 1.95 | 2.10 | 2.25 | 7, 8 |
| E | | 4.00 BSC | | - |
| E1 | | 3.75 BSC | | 9 |
| E2 | 1.95 | 2.10 | 2.25 | 7, 8 |
| e | | 0.65 BSC | | - |
| k | 0.25 | - | - | - |
| L | 0.35 | 0.60 | 0.75 | 8 |
| L1 | - | - | 0.15 | 10 |
| N | | 16 | | 2 |
| Nd | | 4 | | 3 |
| Ne | | 4 | | 3 |
| P | - | - | 0.60 | 9 |
| θ | - | - | 12 | 9 |

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NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.