PRELIMINARY | Data Sheet | November 2002 | FN9098.0

Multi-Phase PWM Controller with Precision Rds, On or DCR Current Sensing

The ISL6561 controls microprocessor core voltage regulation by driving up to 4 synchronous-rectified buck channels in parallel. Multi-phase buck converter architecture uses interleaved timing to multiply channel ripple frequency and reduce input and output ripple currents. Lower ripple results in fewer components, lower component cost, reduced power dissipation, and smaller implementation area.

Microprocessor loads can generate load transients with extremely fast edge rates. The ISL6561 features a high bandwidth control loop and ripple frequencies of >4MHz to provide optimal response to the transients.

Today's microprocessors require a tightly regulated output voltage position versus load current (droop). The ISL6561 senses current by utilizing patented techniques to measure the voltage across the on resistance, $r_{DS(on)}$, of the lower MOSFETs or DCR of output inductor during their conduction intervals. Current sensing provides the needed signals for precision droop, channel-current balancing, and over-current protection.

The accuracy of the $r_{DS(on)}$ current-sensing method is enhanced by the ISL6561's temperature compensation function. Droop accuracy can be affected by increasing $r_{DS(on)}$ or DCR with elevated temperature. The ISL6561 uses an internal temperature-sensing element to provide programmable temperature compensation. Correctly applied, temperature compensation can completely nullify the effect of $r_{DS(on)}$ temperature sensitivity.

A unity gain, differential amplifier is provided for remote voltage sensing. Any potential difference between remote and local grounds can be completely eliminated using the remote-sense amplifier. Eliminating ground differences improves regulation and protection accuracy. The threshold-sensitive enable input is available to accurately coordinate the start up of the ISL6561 with any other voltage rail. Dynamic-VID™ technology allows seamless on-the-fly VID changes. The offset pin allows accurate voltage offset settings that are independent of VID setting. The ISL6561 uses a 5V bias and has a built-in shunt regulator to allow 12V bias using only a small external limiting resistor.

Applications

- Computer DC/DC converter VRM/VRD10.0.
- Computer DC/DC Converter VRM/VRD9.X with 5-bit VID code up to 1.6V.
- Telecom DC/DC converter.

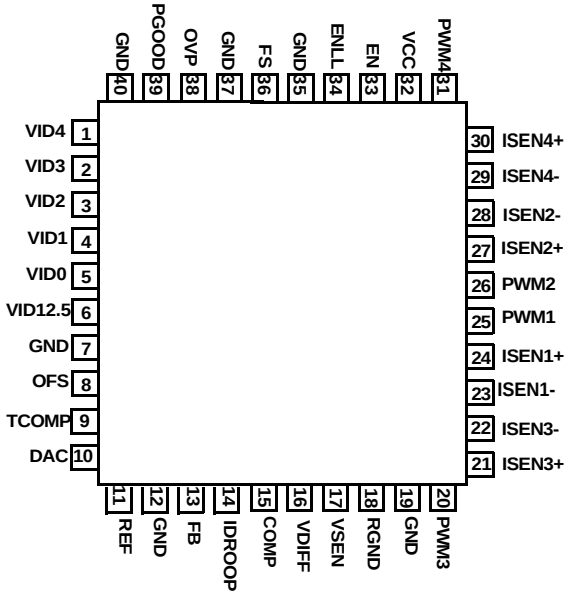
Features

- Precision Multi-Phase Core Voltage Regulation
  - Differential Remote Voltage Sensing
  - ±0.5% System Accuracy Over Life, Load, Line and Temperature
  - Adjustable Reference-Voltage Offset
- Precision $R_{DS(on)}$ or DCR Current Sensing
  - Integrated Programmable Temperature Compensation
  - Accurate Load-Line Programming
  - Accurate Channel-Current Balancing
  - Differential Current Sense
  - Low-Cost, Lossless Current Sensing
- Internal Shunt Regulator for 5V or 12V Biasing
- Microprocessor Voltage Identification Input
  - Dynamic VID™ technology
  - 6-Bit VID Input
  - .8375V to 1.600V in 12.5mV Steps
- Threshold-Sensitive Enable Function for synchronizing with driver POR
- Over Current Protection
- Over-Voltage Protection
  - No Additional External Components Needed
  - OVP Pin to drive Crowbar Device
- 2, 3, or 4 Phase Operation
- Greater Than 1MHz Operation (> 4MHz Ripple)

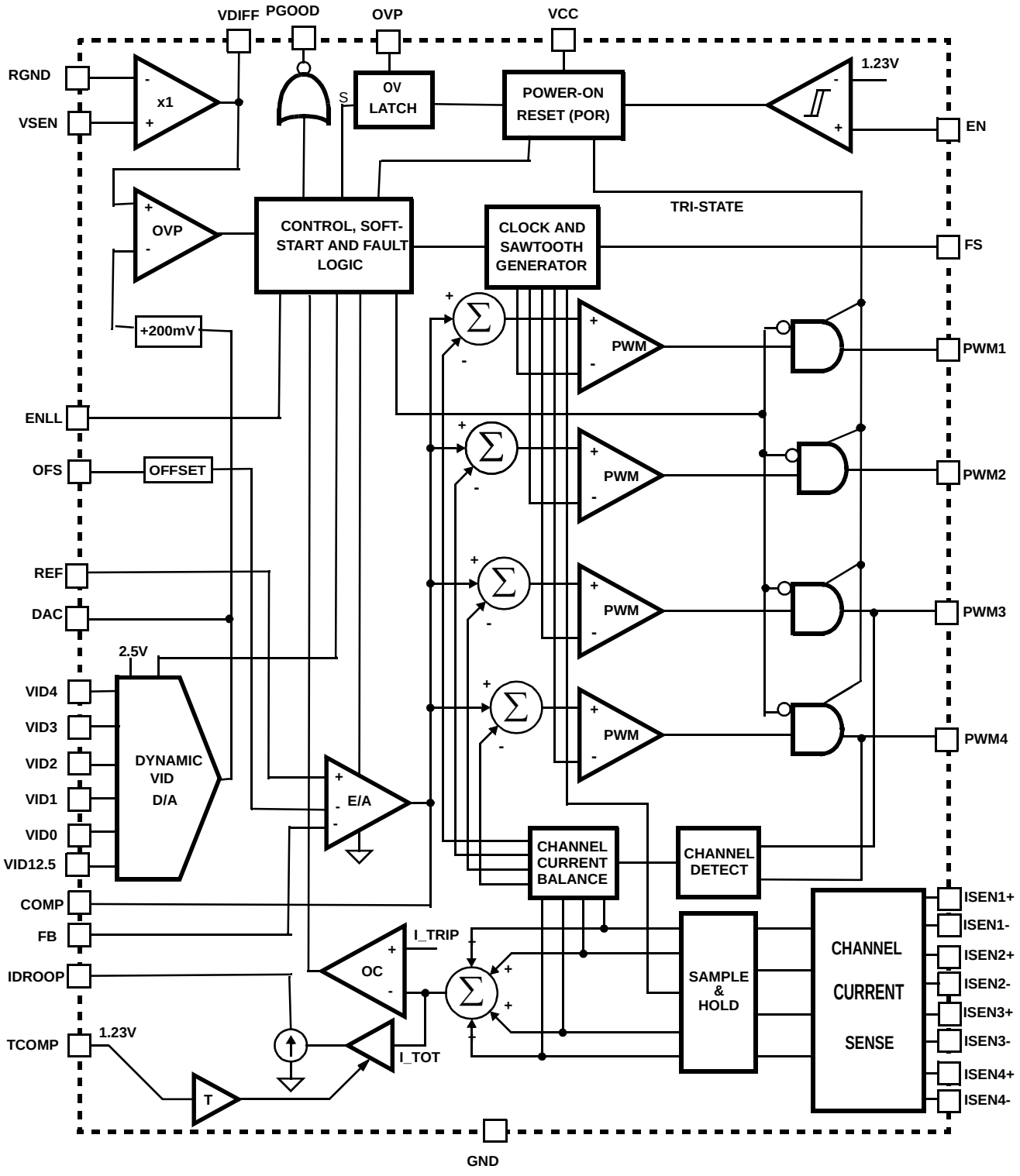
Ordering Information

PART NUMBER	TEMP. (^{o}C)	PACKAGE	PKG. NO.
ISL6561	0 to 70	40 Ld QFN	L40.6X6

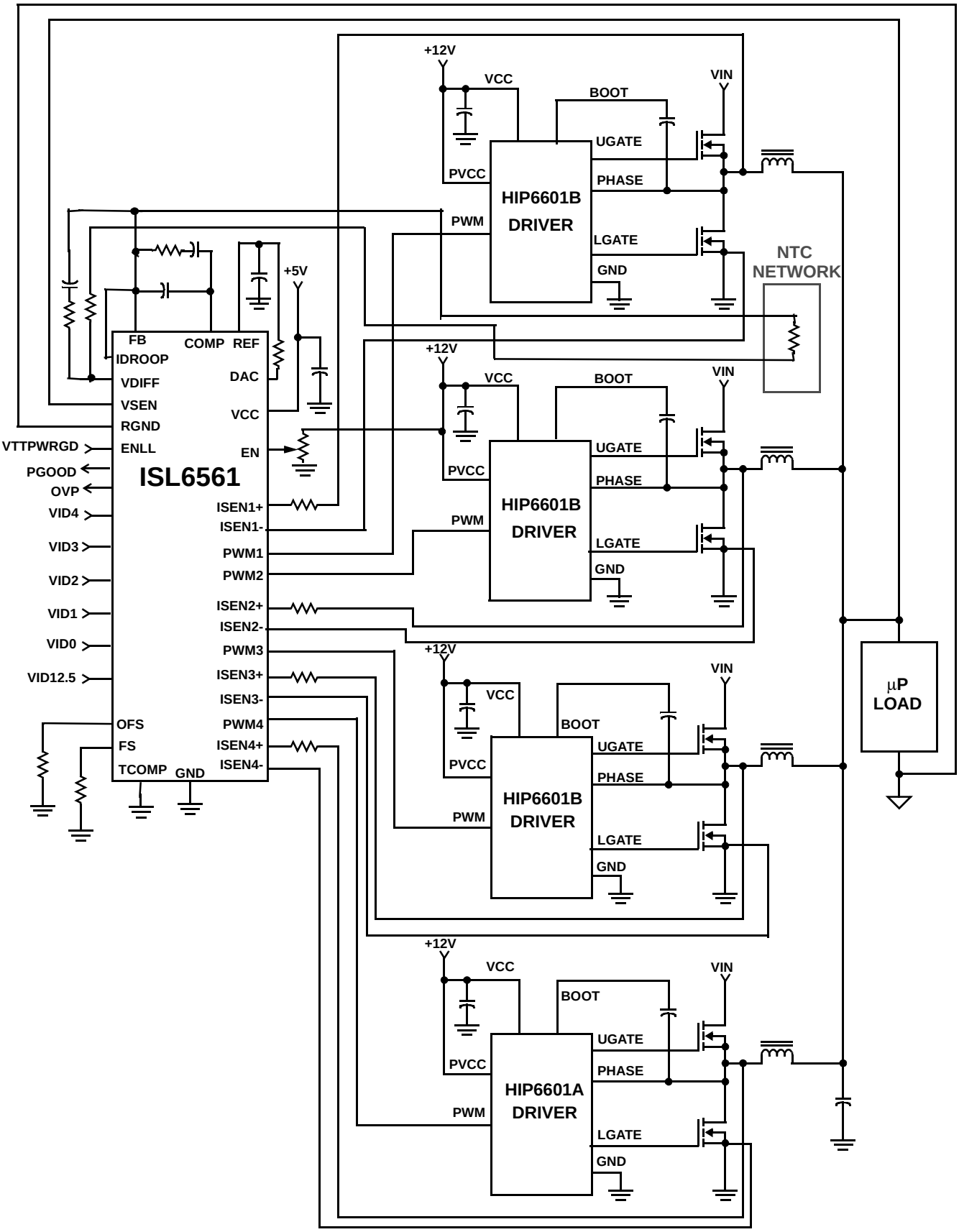
ISL6561 (40-PIN MLFP)
TOP VIEW



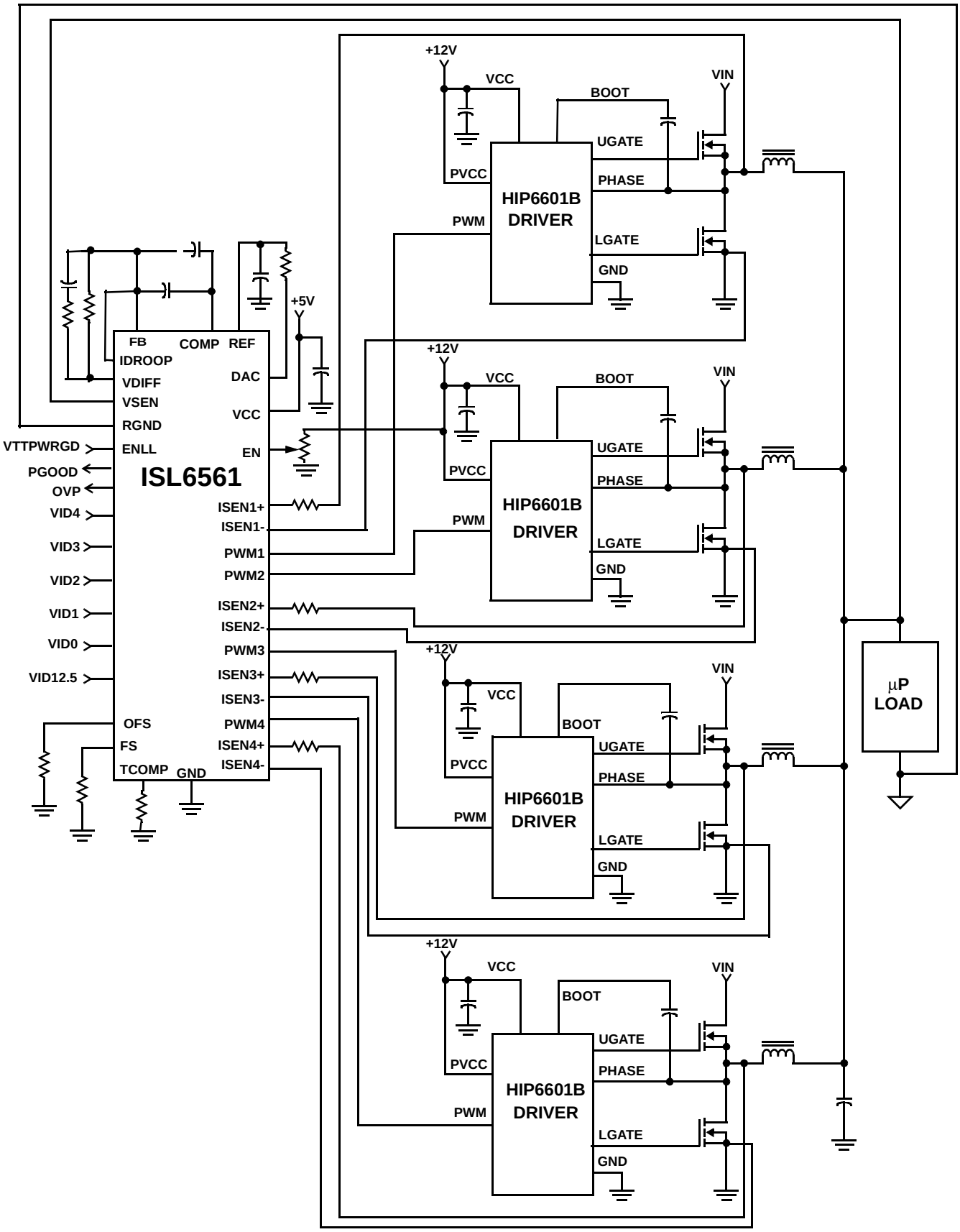
Block Diagram



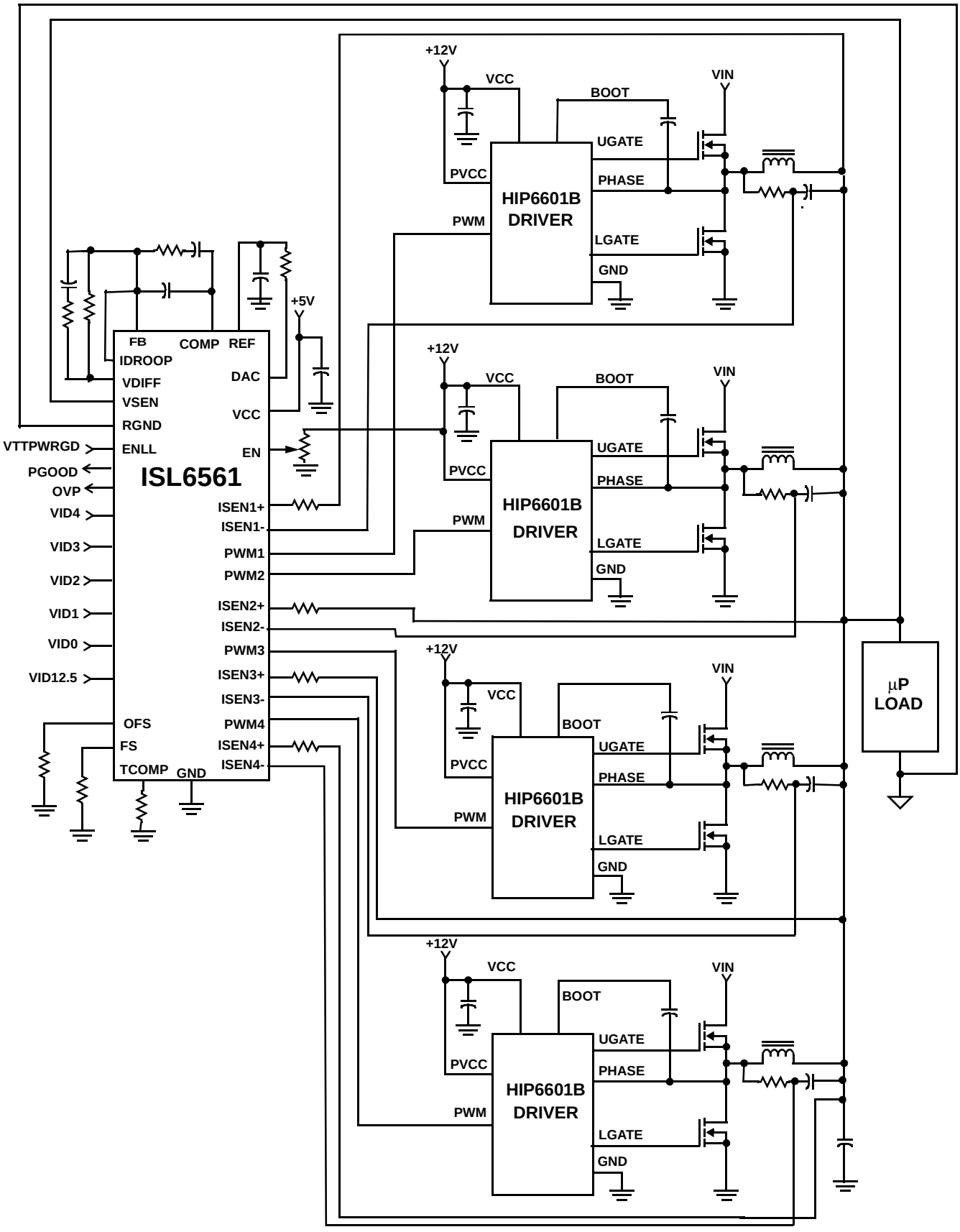
Typical Application - 4-Phase Buck Converter with Rds, On Sensing and External NTC



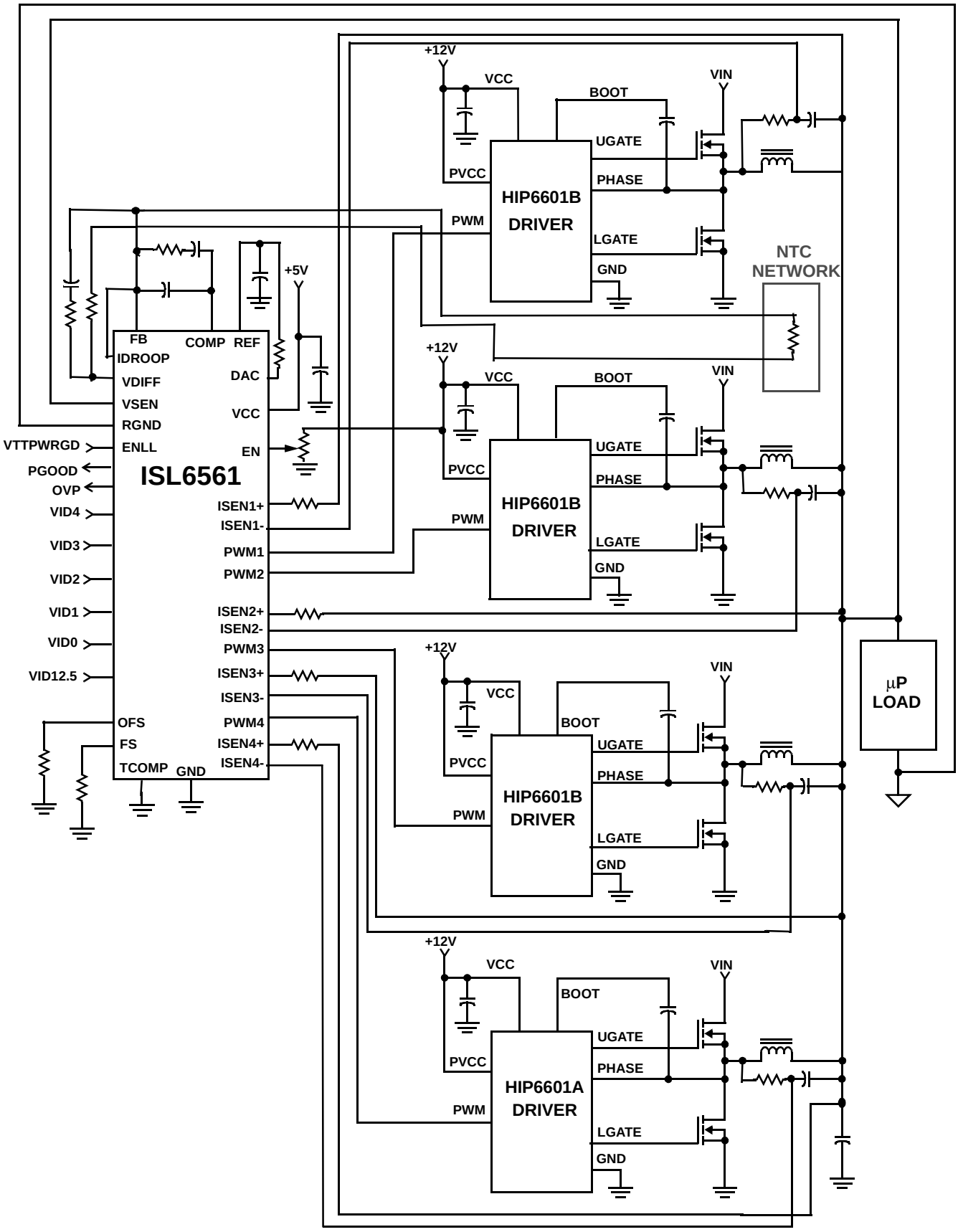
Typical Application - 4-Phase Buck Converter with Rdes, On Sensing and Internal PTC



Typical Application - 4-Phase Buck Converter with DCR Sensing and Internal PTC



Typical Application - 4-Phase Buck Converter with DCR Sensing and External NTC



OFS

The OFS pin provides a programmable means to introduce a DC offset voltage to the DAC reference. The offset is generated via an external resistor and precision internal voltage references. The polarity of the offset is selected by connecting the resistor to GND or VCC. For no offset, the OFS pin should be left unterminated. The current which flows through the resistor is output on the FB pin. The magnitude of the offset is determined by the reference voltage and the ratio of the OFS programming resistor to the DC impedance from VDIFF to FB. OFS is intended for introducing offsets in a range within ±50mV of the DAC setting.

OVP

A latched over-voltage indicator. Once tripped OVP remains set until power is cycled.

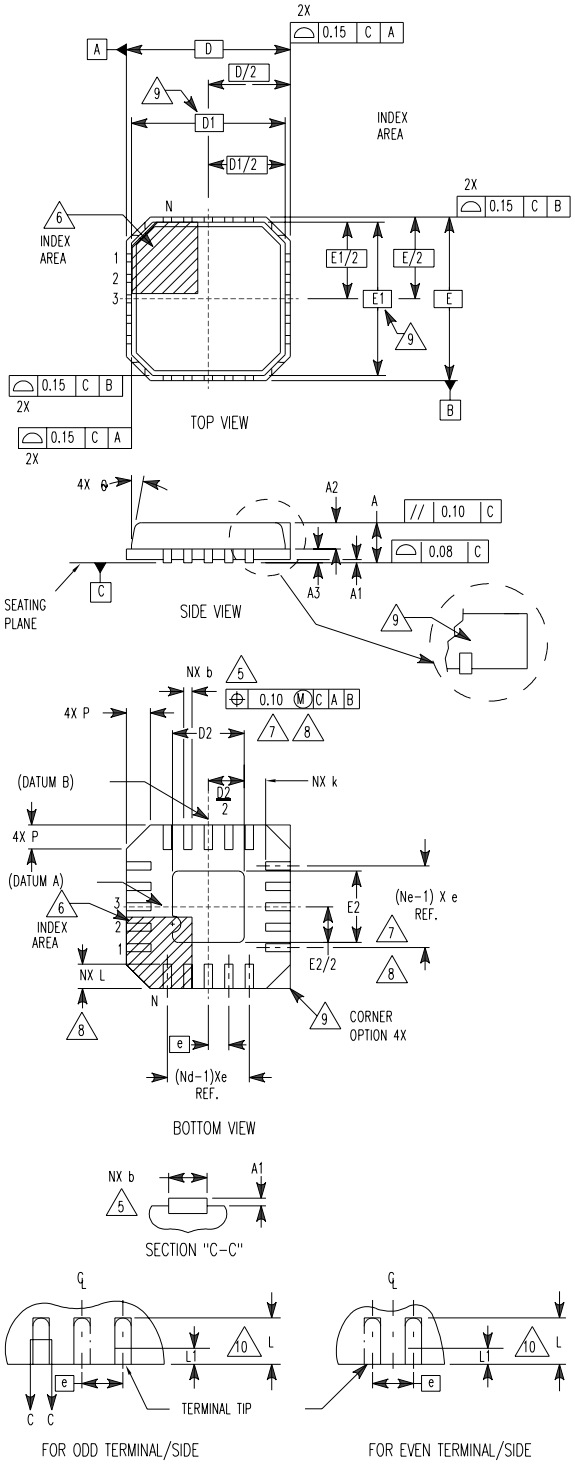
TABLE 1. VOLTAGE IDENTIFICATION CODES

VID4	VID3	VID2	VID1	VID0	VID12.5	VDAC
0	1	0	1	0	0	0.8375V
0	1	0	0	1	1	0.8500V
0	1	0	0	1	0	0.8625V
0	1	0	0	0	1	0.8750V
0	1	0	0	0	0	0.8875V
0	0	1	1	1	1	0.9000V
0	0	1	1	1	0	0.9125V
0	0	1	1	0	1	0.9250V
0	0	1	1	0	0	0.9375V
0	0	1	0	1	1	0.9500V
0	0	1	0	1	0	0.9625V
0	0	1	0	0	1	0.975V0
0	0	1	0	0	0	0.9875V
0	0	0	1	1	1	1.0000V
0	0	0	1	1	0	1.0125V
0	0	0	1	0	1	1.0250v
0	0	0	1	0	0	1.0375V
0	0	0	0	1	1	1.0500V
0	0	0	0	1	0	1.0625V
0	0	0	0	0	1	1.0750V
0	0	0	0	0	0	1.0875V
1	1	1	1	1	1	OFF
1	1	1	1	1	0	OFF
1	1	1	1	0	1	1.1000V
1	1	1	1	0	0	1.1125V
1	1	1	0	1	1	1.1250V
1	1	1	0	1	0	1.1375V
1	1	1	0	0	1	1.1500V
1	1	1	0	0	0	1.1625V
1	1	0	1	1	1	1.1750V
1	1	0	1	1	0	1.1875V
1	1	0	1	0	1	1.2000V
1	1	0	1	0	0	1.2125V
1	1	0	0	1	1	1.2250V
1	1	0	0	1	0	1.2375V

TABLE 1. VOLTAGE IDENTIFICATION CODES (Continued)

VID4	VID3	VID2	VID1	VID0	VID12.5	VDAC
1	1	0	0	0	1	1.2500V
1	1	0	0	0	0	1.2625V
1	0	1	1	1	1	1.2750V
1	0	1	1	1	0	1.2875V
1	0	1	1	0	1	1.3000V
1	0	1	1	0	0	1.3125V
1	0	1	0	1	1	1.3250V
1	0	1	0	1	0	1.3375V
1	0	1	0	0	1	1.3500V
1	0	1	0	0	0	1.3625V
1	0	0	1	1	1	1.3750V
1	0	0	1	1	0	1.3875V
1	0	0	1	0	1	1.4000V
1	0	0	1	0	0	1.4125V
1	0	0	0	1	1	1.4250V
1	0	0	0	1	0	1.4375V
1	0	0	0	0	1	1.4500V
1	0	0	0	0	0	1.4625V
0	1	1	1	1	1	1.4750V
0	1	1	1	1	0	1.4875V
0	1	1	1	0	1	1.5000V
0	1	1	1	0	0	1.5125V
0	1	1	0	1	1	1.5250V
0	1	1	0	1	0	1.5375V
0	1	1	0	0	0	1.5625V
0	1	0	1	1	1	1.5750V
0	1	0	1	1	0	1.5875V
0	1	0	1	0	1	1.600V

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L40.6x6

40 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220VJJD-2 ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.18	0.23	0.30	5, 8
D		6.00 BSC		-
D1		5.75 BSC		9
D2	3.95	4.10	4.25	7, 8
E		6.00 BSC		-
E1		5.75 BSC		9
E2	3.95	4.10	4.25	7, 8
e		0.50 BSC		-
k	0.25	-	-	-
L	0.30	0.40	0.50	8
L1	-	-	0.15	10
N		40		2
Nd		10		3
Ne		10		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 1 10/02

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.