

## ISO7240CF-Q1, ISO7240C-Q1 ISO7241C-Q1, ISO7242C-Q1

SLLSE40A – SEPTEMBER 2010–REVISED SEPTEMBER 2011

# HIGH-SPEED QUAD DIGITAL ISOLATORS

Check for Samples: ISO7240CF-Q1, ISO7241C-Q1

**4 kV ESD Protection** 

**Operate With 3.3-V or 5-V Supplies** 

High Electromagnetic Immunity (see application report SLLA181)

-40°C to 125°C Operating Range

## **FEATURES**

- Qualified for Automotive Applications
- Selectable Failsafe Output (ISO7240CF)
- 25 and 150-Mbps Signaling Rate Options
  - Low Channel-to-Channel Output Skew;
     1 ns Max
  - Low Pulse-Width Distortion (PWD);
     2 ns Max
  - Low Jitter Content; 1 ns Typ at 150 Mbps
- Typical 25-Year Life at Rated Working Voltage (see application note SLLA197 and Figure 17)
- 4000-V<sub>peak</sub> Isolation, 560-V<sub>peak</sub> V<sub>IORM</sub>
  - UL 1577, IEC 60747-5-2 (VDE 0884, Rev 2), IEC 61010-1, IEC 60950-1 and CSA Approved

## DESCRIPTION

The ISO7240, ISO7241 and ISO7242 are quad-channel digital isolators with multiple channel configurations and output enable functions. These devices have logic input and output buffers separated by TI's silicon dioxide (SiO<sub>2</sub>) isolation barrier. Used in conjunction with isolated power supplies, these devices block high voltage, isolate grounds, and prevent noise currents from entering the local ground and interfering with or damaging sensitive circuitry.

The ISO7240 has all four channels in the same direction while the ISO7241 has three channels the same direction and one channel in opposition. The ISO7242 has two channels in each direction.

The C option devices have TTL input thresholds and a noise-filter at the input that prevents transient pulses from being passed to the output of the device. The M option devices have CMOS  $V_{CC}/2$  input thresholds and do not have the input noise-filter or the additional propagation delay.

The ISO7240CF has an input disable function on pin 7, and a selectable high or low failsafe-output function with the CTRL pin (pin 10). The failsafe-output is a logic high when a logic-high is placed on the CTRL pin or it is left unconnected. If a logic-low signal is applied to the CTRL pin, the failsafe-output becomes a logic-low output state. The ISO7240CF input disable function prevents data from being passed across the isolation barrier to the output. When the inputs are disabled, the outputs are set by the CTRL pin.

These devices may be powered from either 3.3-V or 5-V supplies on either side in any 3.3-V / 3.3-V / 5-V / 5-V / 5-V / 3.3-V, or 3.3-V / 5-V combination. Note that the signal input pins are 5-V tolerant regardless of the voltage supply level being used.

These devices are characterized for operation over the ambient temperature range of -40°C to 125°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

## ISO7240CF-Q1, ISO7240C-Q1 ISO7241C-Q1, ISO7242C-Q1

SLLSE40A - SEPTEMBER 2010-REVISED SEPTEMBER 2011

TEXAS INSTRUMENTS

www.ti.com



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

#### ORDERING INFORMATION<sup>(1)</sup>

| T <sub>A</sub> | PACKAGE <sup>(2)</sup> |              | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------------------|--------------|-----------------------|------------------|
|                |                        |              | ISO7240CFQDWRQ1       | ISO7240CFQ       |
| 40°C to 405°C  |                        | Reel of 2000 | ISO7240CQDWRQ1        | Product Preview  |
| –40°C to 125°C | SOIC – DW              |              | ISO7241CQDWRQ1        | ISO7241CQ        |
|                |                        |              | ISO7242CQDWRQ1        | ISO7242CQ        |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

| ISO7240CF  | ISO7240   | ISO7241   | ISO7242   |
|--|---|---|---|
| V <sub>CC1</sub> □ 1 ● !! 16 □ V <sub>CC2</sub>            | V <sub>CC1</sub> □ 1 ● !! 16 □ V <sub>CC2</sub> | V <sub>CC1</sub> □ 1 ● !! 16 □ V <sub>CC2</sub>   | V <sub>CC1</sub> □ 1 ● !! 16 □ V <sub>CC2</sub>                 |
| GND1 - 2    15 - GND2                                      | $GND1 \square 2$ $15 \square GND2$              |   | GND1 □ 2    15 □ GND2   |
|  |   | IN <sub>A</sub> ा 3 - 2 4 - 14 □ OUT <sub>A</sub> | IN <sub>A</sub> ा 3 - → 14 □ OUT <sub>A</sub>                   |
| IN <sub>B</sub> - 4 13 - 13 - 0UT <sub>B</sub>             |   |   | IN <sub>B</sub> □ 4 - → + + 13 □ OUT <sub>B</sub>               |
|  |   |   | OUT <sub>C</sub> □===5{}+ +{}+{}+{}+12 == IN <sub>C</sub>       |
| IN <sub>D</sub> 11 → 6 → + + + + + + + + + + + + + + + + + |   |   | OUT <sub>D</sub> □====6{}+i +-{}+{}+{}+{}+11 == IN <sub>D</sub> |
|  | NC ഥ 7    └─10 ่่ ── EN                         | EN <sub>1</sub> œ 7─┘ ¦¦ └──10⊨□ EN <sub>2</sub>  | EN <sub>1</sub> œ 7— ↓ ↓ ↓ ↓ EN <sub>2</sub>                    |
| GND1 = 8 ; 9 = GND2  | $GND1 \square 8$ '' $9 \square GND2$            | GND1 = 8 $1$ $9 = GND2$                           | GND1 🖂 8 🤫 9 🖽 GND2   |

#### Table 1. ISO724xC Function Table<sup>(1)</sup>

| INPUT V <sub>CC</sub> | OUTPUT V <sub>CC</sub> | INPUT<br>(IN) | OUTPUT ENABLE<br>(EN) | OUTPUT<br>(OUT) |
|-----------------------|------------------------|---------------|-----------------------|-----------------|
|                       |                        | Н             | H or Open             | Н               |
| PU                    | PU                     | L             | H or Open             | L               |
| PU                    | PU                     | Х             | L                     | Z               |
|                       |                        | Open          | H or Open             | Н               |
| PD                    | PU                     | Х             | X H or Open           |                 |
| PD                    | PU                     | Х             | L                     | Z               |

(1) PU = Powered Up; PD = Powered Down ; X = Irrelevant; H = High Level; L = Low Level

#### Table 2. ISO7240CF Function Table

| V <sub>CC1</sub> | V <sub>CC2</sub> | DATA INPUT<br>(IN) | DISABLE INPUT<br>(DISABLE) | FAILSAFE CONTROL INPUT<br>(CTRL) | DATA OUTPUT<br>(OUT) |
|------------------|------------------|--------------------|----------------------------|----------------------------------|----------------------|
| PU               | PU               | Н                  | L or Open                  | X                                | Н                    |
| PU               | PU               | L                  | L or Open                  | X                                | L                    |
| Х                | PU               | Х                  | Н                          | H or Open                        | Н                    |
| Х                | PU               | Х                  | Н                          | L                                | L                    |
| PD               | PU               | Х                  | Х                          | H or Open                        | Н                    |
| PD               | PU               | Х                  | Х                          | L                                | L                    |

SLLSE40A - SEPTEMBER 2010-REVISED SEPTEMBER 2011

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

|                |   |  |          | VALUE     | UNIT |
|----------------|---|--|----------|-----------|------|
| $V_{CC}$       | Supply voltag                           | e <sup>(2)</sup> , V <sub>CC1</sub> , V <sub>CC2</sub> |          | –0.5 to 6 | V    |
| VI             | Voltage at IN, OUT, EN, DISABLE, CTRL - |  |          |           | V    |
| I <sub>O</sub> | Output currer                           | it   |          | ±15       | mA   |
|                |   | Human-Body Model                                       |          | ±4        | kV   |
| ESD            | Electrostatic<br>discharge              | Field-Induced-Charged Device Model                     | All pins | ±1        | ĸv   |
|                | alsonargo                               | Machine Model  |          | ±200      | V    |
| TJ             | Maximum jun                             | ction temperature                                      |          | 150       | °C   |

Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings (1) only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

All voltage values are with respect to network ground terminal and are peak voltage values. (2)

#### **RECOMMENDED OPERATING CONDITIONS**

|                   |   | MIN  | TYP               | MAX      | UNIT |
|-------------------|---|------|-------------------|----------|------|
| $V_{CC}$          | Supply voltage <sup>(1)</sup> , V <sub>CC1</sub> , V <sub>CC2</sub>                         | 3.15 |                   | 5.5      | V    |
| I <sub>OH</sub>   | High-level output current   |      |                   | 4        | mA   |
| I <sub>OL</sub>   | Low-level output current  | -4   |                   |          | mA   |
| t <sub>ui</sub>   | Input pulse width   | 40   |                   |          | ns   |
| 1/t <sub>ui</sub> | Signaling rate  | 0    | 30 <sup>(2)</sup> | 25       | Mbps |
| VIH               | High-level input voltage (IN, DISABLE, CTRL, EN)  | 2    |                   | $V_{CC}$ | V    |
| VIL               | Low-level input voltage (IN, DISABLE, CTRL, EN)   | 0    |                   | 0.8      | V    |
| T <sub>A</sub>    | Operating free-air temperature  | -40  |                   | 125      | °C   |
| н                 | External magnetic field-strength immunity per IEC 61000-4-8 and IEC 61000-4-9 certification |      |                   | 1000     | A/m  |

For the 5-V operation, V<sub>CC1</sub> or V<sub>CC2</sub> is specified from 4.5 V to 5.5 V. For the 3-V operation, V<sub>CC1</sub> or V<sub>CC2</sub> is specified from 3.15 V to 3.6 V. Typical value at room temperature and well-regulated power supply. (1)

(2)

# IEC 60747-5-2 INSULATION CHARACTERISTICS<sup>(1)</sup>

over recommended operating conditions (unless otherwise noted)

|                   | PARAMETER                          | TEST CONDITIONS   | SPECIFICATIONS   | UNIT |
|-------------------|------------------------------------|---|------------------|------|
| VIORM             | Maximum working insulation voltage |   | 560              | V    |
|                   |                                    | After Input/Output Safety Test Subgroup 2/3<br>$V_{PR} = V_{IORM} \times 1.2$ , t = 10 s,<br>Partial discharge < 5 pC | 672              | V    |
| V <sub>PR</sub>   | Input to output test voltage       | Method a, $V_{PR} = V_{IORM} \times 1.6$ ,<br>Type and sample test with t = 10 s,<br>Partial discharge < 5 pC         | 896              | V    |
|                   |                                    | Method b1, $V_{PR} = V_{IORM} \times 1.875$ ,<br>100 % Production test with t = 1 s,<br>Partial discharge < 5 pC      | 1050             | V    |
| V <sub>IOTM</sub> | Transient overvoltage              | t = 60 s  | 4000             | V    |
| R <sub>S</sub>    | Insulation resistance              | $V_{IO} = 500 \text{ V at } T_S$  | >10 <sup>9</sup> | Ω    |
|                   | Pollution degree                   |   | 2                |      |

(1) Climatic Classification 40/125/21

SLLSE40A - SEPTEMBER 2010-REVISED SEPTEMBER 2011

www.ti.com

STRUMENTS

EXAS

## ELECTRICAL CHARACTERISTICS: $V_{CC1}$ and $V_{CC2}$ at 5-V<sup>(1)</sup> OPERATION

, over recommended operating conditions (unless otherwise noted)

|                     | PARAMETER   |  | TEST CONDITIONS  | MIN            | TYP | MAX  | UNIT  |
|---------------------|---|--|--|----------------|-----|------|-------|
| SUPPLY              | CURRENT   |  |  |                |     |      |       |
|                     | 10072400  | Quiescent                                | $V_{I} = V_{CC}$ or 0 V, All channels, no load,        |                | 1   | 3    |       |
|                     | ISO7240C  | 25 Mbps                                  | EN <sub>2</sub> at 3 V                                 |                | 7   | 10.5 | mA    |
|                     | ISO7241C  | Quiescent                                | $V_{I} = V_{CC}$ or 0 V, All channels, no load,        |                | 6.5 | 11   | mA    |
| I <sub>CC1</sub>    | 13072410  | 25 Mbps                                  | $EN_1$ at 3 V, $EN_2$ at 3 V                           |                | 12  | 18   | ША    |
|                     | ISO7242C  | Quiescent                                | $V_{I} = V_{CC}$ or 0 V, All channels, no load,        |                | 10  | 16   | mA    |
|                     | 13072420  | 25 Mbps                                  | $EN_1$ at 3 V, $EN_2$ at 3 V                           |                | 15  | 24   | ШA    |
|                     | ISO7240C  | Quiescent $V_I = V_{CC}$ or 0 V, All cha | $V_I = V_{CC}$ or 0 V, All channels, no load,          |                | 15  | 22   | mA    |
|                     |   | 25 Mbps                                  | EN <sub>2</sub> at 3 V                                 |                | 17  | 25   | mA    |
| I <sub>CC2</sub>    | ISO7241C  | Quiescent                                | $V_{I} = V_{CC}$ or 0 V, All channels, no load,        |                | 13  | 20   | mA    |
|                     | 13072410  | 25 Mbps                                  | $EN_1$ at 3 V, $EN_2$ at 3 V                           |                | 18  | 28   | ША    |
|                     | ISO7242C  | Quiescent                                | $V_{I} = V_{CC}$ or 0 V, All channels, no load,        |                | 10  | 16   | mA    |
|                     | 15072420  | 25 Mbps                                  | 25 Mbps EN <sub>1</sub> at 3 V, EN <sub>2</sub> at 3 V |                | 15  | 24   | ША    |
| ELECTR              | RICAL CHARACTERISTICS                               |  |  |                |     |      |       |
| I <sub>OFF</sub>    | Sleep mode output currer                            | nt                                       | EN at 0 V, Single channel                              |                | 0   |      | μA    |
| V                   | High-level output voltage                           |  | I <sub>OH</sub> = –4 mA, See Figure 1                  | $V_{CC} - 0.8$ |     |      | V     |
| V <sub>OH</sub>     | nigh-level output voltage                           |  | $I_{OH} = -20 \ \mu A$ , See Figure 1                  | $V_{CC} - 0.1$ |     |      | v     |
|                     |   |  | I <sub>OL</sub> = 4 mA, See Figure 1                   |                |     | 0.4  | V     |
| V <sub>OL</sub>     | Low-level output voltage                            |  | $I_{OL} = 20 \ \mu A$ , See Figure 1                   |                |     | 0.1  | v     |
| V <sub>I(HYS)</sub> | Input voltage hysteresis                            |  |  |                | 150 |      | mV    |
| I <sub>IH</sub>     | High-level input current<br>Low-level input current |  | IN from 0 \/ to \/                                     |                |     | 10   |       |
| IIL                 |   |  | IN from 0 V to V <sub>CC</sub>                         | -10            |     |      | μA    |
| CI                  | Input capacitance to grou                           | nd                                       | IN at $V_{CC}$ , $V_I = 0.4 \sin (4E6\pi t)$           |                | 2   |      | pF    |
| СМТІ                | Common-mode transient                               | immunity                                 | $V_{I} = V_{CC}$ or 0 V, See Figure 5                  | 25             | 50  |      | kV/µs |

(1) For the 5-V operation, V<sub>CC1</sub> or V<sub>CC2</sub> is specified from 4.5 V to 5.5 V. For the 3-V operation, V<sub>CC1</sub> or V<sub>CC2</sub> is specified from 3.15 V to 3.6 V.

4



## SWITCHING CHARACTERISTICS: $V_{CC1}$ and $V_{CC2}$ at 5-V OPERATION

over recommended operating conditions (unless otherwise noted)

|                                     | PARAMETER  | TEST CONDITIONS    | MIN | TYP | MAX | UNIT |
|-------------------------------------|--|--------------------|-----|-----|-----|------|
| t <sub>PLH</sub> , t <sub>PHL</sub> | Propagation delay  | See Figure 1       | 18  |     | 45  | 20   |
| PWD                                 | Pulse-width distortion <sup>(1)</sup>  t <sub>PHL</sub> – t <sub>PLH</sub> | See Figure 1       |     |     | 5   | ns   |
| t <sub>sk(pp)</sub>                 | Part-to-part skew <sup>(2)</sup>   |                    |     |     | 8   | ns   |
|                                     | Observations and and a start of an (3)                                     | ISO7240C, ISO7241C |     |     | 3   |      |
| t <sub>sk(o)</sub>                  | Channel-to-channel output skew <sup>(3)</sup>                              | ISO7242C           |     |     | 4   | ns   |
| t <sub>r</sub>                      | Output signal rise time  |                    | 2   |     |     |      |
| t <sub>f</sub>                      | Output signal fall time  | See Figure 1       |     | 2   |     | ns   |
| t <sub>PHZ</sub>                    | Propagation delay, high-level-to-high-impedance output                     |                    |     | 15  | 25  |      |
| t <sub>PZH</sub>                    | Propagation delay, high-impedance-to-high-level output                     |                    |     | 15  | 25  |      |
| t <sub>PLZ</sub>                    | Propagation delay, low-level-to-high-impedance output                      | See Figure 2       |     | 15  | 25  | ns   |
| t <sub>PZL</sub>                    | Propagation delay, high-impedance-to-low-level output                      |                    |     | 15  | 25  |      |
| t <sub>fs</sub>                     | Failsafe output delay time from input power loss                           | See Figure 3       |     | 12  |     | μs   |
| t <sub>wake</sub>                   | Wake time from input disable   | See Figure 4       |     | 15  |     | μs   |

(1)

Also referred to as pulse skew.  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices (2)  $t_{sk(o)}$  is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the

(3) same direction while driving identical specified loads. SLLSE40A - SEPTEMBER 2010-REVISED SEPTEMBER 2011

TEXAS INSTRUMENTS

www.ti.com

## ELECTRICAL CHARACTERISTICS: $V_{CC1}$ at 5-V, $V_{CC2}$ at 3.3-V<sup>(1)</sup> OPERATION

over recommended operating conditions (unless otherwise noted)

|                     | PARAMET              | FER   | TEST CONDIT  | IONS                             | MIN                   | TYP  | MAX        | UNIT  |
|---------------------|----------------------|---|--|----------------------------------|-----------------------|------|------------|-------|
| SUPPL               | YCURRENT             |   | 1  |                                  | 1                     |      | 1          |       |
|                     | ISO7240C             | Quiescent   |  |                                  |                       | 1    | 3          |       |
|                     | 15072400             | 25 Mbps   | - V <sub>I</sub> = V <sub>CC</sub> or 0 V, All channels, n       | 10 10ad, $EN_2$ at 3 V           |                       | 7    | 10.5       | mA    |
|                     | IS07241C             | Quiescent   | $V_{I} = V_{CC}$ or 0 V, All channels, n                         | lo load, EN₁ at 3 V,             |                       | 6.5  | 11         |       |
| I <sub>CC1</sub>    | 15072410             | 25 Mbps   | EN <sub>2</sub> at 3 V   |                                  |                       | 12   | 18         | mA    |
|                     | IS07242C             | Quiescent   | $V_{I} = V_{CC}$ or 0 V, All channels, n                         | io load, EN <sub>1</sub> at 3 V, |                       | 10   | 16         | mA    |
| 13072420            |                      | 25 Mbps   | EN <sub>2</sub> at 3 V   |                                  |                       | 15   | 24         | ШA    |
|                     | ISO7240C             | Quiescent   | V = V or $0 V$ All channels in                                   | a load ENL at 2 V                |                       | 9.5  | 15         | m۸    |
| 15072400            |                      | 25 Mbps   | $V_{I} = V_{CC}$ or 0 V, All channels, n                         | $1010a0$ , $EN_2 at 3 V$         |                       | 10.5 | 17         | mA    |
|                     | IS07241C             | Quiescent   | $V_{I} = V_{CC}$ or 0 V, All channels, n                         | o load, EN₁ at 3 V,              |                       | 8    | 13         | mA    |
| I <sub>CC2</sub>    | 15072410             | 25 Mbps   | EN <sub>2</sub> at 3 V   |                                  | 11.5                  | 18   | mA         |       |
|                     | ISO7242C             | Quiescent $V_I = V_{CC}$ or 0 V, All channels, no load, EN <sub>1</sub> | o load, EN₁ at 3 V,  |                                  | 6                     | 10   | <b>س</b> ۸ |       |
|                     | 15072420             | 25 Mbps   | $EN_2$ at 3 V  |                                  |                       | 9    | 14         | mA    |
| ELECT               | RICAL CHARACT        | ERISTICS  |  |                                  |                       |      |            |       |
| I <sub>OFF</sub>    | Sleep mode out       | put current   | EN at 0 V, Single channel  |                                  |                       | 0    |            | μA    |
|                     |                      |   |  | ISO7240                          | $V_{CC} - 0.4$        |      |            |       |
| V <sub>OH</sub>     | High-level outpu     | ut voltage  | $I_{OH} = -4$ mA, See Figure 1 ISO724x (5-V side) $V_{CC} - 0.8$ | $V_{CC} - 0.8$                   |                       |      | V          |       |
|                     |                      |   | $I_{OH} = -20 \ \mu A$ , See Figure 1                            |                                  | V <sub>CC</sub> – 0.1 |      |            |       |
| V                   |                      | t voltogo   | I <sub>OL</sub> = 4 mA, See Figure 1                             |                                  |                       |      | 0.4        | V     |
| V <sub>OL</sub>     | Low-level outpu      | t voltage   | $I_{OL}$ = 20 µA, See Figure 1                                   |                                  |                       |      | 0.1        | v     |
| V <sub>I(HYS)</sub> | Input voltage hy     | steresis  |  |                                  |                       | 150  |            | mV    |
| I <sub>IH</sub>     | High-level input     | current   |  |                                  |                       |      | 10         |       |
| IIL                 | Low-level input      | current   | IN from 0 V to V <sub>CC</sub>                                   |                                  | -10                   |      |            | μA    |
| CI                  | Input capacitand     | ce to ground  | IN at $V_{CC}$ , $V_I = 0.4 \sin (4E6\pi t)$                     |                                  |                       | 2    |            | pF    |
| CMTI                | Common-mode immunity | transient   | $V_{I} = V_{CC}$ or 0 V, See Figure 5                            |                                  | 25                    | 50   |            | kV/µs |

(1) For the 5-V operation, V<sub>CC1</sub> or V<sub>CC2</sub> is specified from 4.5 V to 5.5 V. For the 3-V operation, V<sub>CC1</sub> or V<sub>CC2</sub> is specified from 3.15 V to 3.6 V.

6



SLLSE40A - SEPTEMBER 2010-REVISED SEPTEMBER 2011

## SWITCHING CHARACTERISTICS: V<sub>CC1</sub> at 5-V, V<sub>CC2</sub> at 3.3-V OPERATION

over recommended operating conditions (unless otherwise noted)

|                                     | PARAMETER  | TEST CONDITIONS    | MIN   | TYP | MAX | UNIT |
|-------------------------------------|--|--------------------|-------|-----|-----|------|
| t <sub>PLH</sub> , t <sub>PHL</sub> | Propagation delay  | See Figure 1       | 20    |     | 50  |      |
|                                     | Pulse-width distortion <sup>(1)</sup>  t <sub>PHL</sub> – t <sub>PLH</sub> | ISO7240C, ISO7241C |       |     | 3   | ns   |
| PWD                                 |  | ISO7242C           |       |     | 4   |      |
| t <sub>sk(pp)</sub>                 | Part-to-part skew <sup>(2)</sup>   |                    |       |     | 10  | ns   |
|                                     | <b>O</b> han and the share of a structure (3)                              | ISO7240C, ISO7241C |       |     | 3   |      |
| t <sub>sk(o)</sub>                  | Channel-to-channel output skew <sup>(3)</sup>                              | ISO7242C           |       |     | 4   | ns   |
| t <sub>r</sub>                      | Output signal rise time  | 0                  | 2     |     |     |      |
| t <sub>f</sub>                      | Output signal fall time  | See Figure 1       |       |     |     | ns   |
| t <sub>PHZ</sub>                    | Propagation delay, high-level-to-high-impedance output                     |                    |       | 15  | 25  |      |
| t <sub>PZH</sub>                    | Propagation delay, high-impedance-to-high-level output                     |                    |       | 15  | 25  |      |
| t <sub>PLZ</sub>                    | Propagation delay, low-level-to-high-impedance output                      | See Figure 2       |       | 15  | 25  | ns   |
| t <sub>PZL</sub>                    | Propagation delay, high-impedance-to-low-level output                      |                    | 15 25 |     | 25  |      |
| t <sub>fs</sub>                     | Failsafe output delay time from input power loss                           | See Figure 3       |       | 18  |     | μs   |
| t <sub>wake</sub>                   | Wake time from input disable   | See Figure 4       |       | 15  |     | μs   |

(1) Also known as pulse skew

tsk(pp) is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices (2)

operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.  $t_{sk(o)}$  is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the (3) same direction while driving identical specified loads.

SLLSE40A - SEPTEMBER 2010-REVISED SEPTEMBER 2011

www.ti.com

STRUMENTS

EXAS

## ELECTRICAL CHARACTERISTICS: $V_{CC1}$ at 3.3-V, $V_{CC2}$ at 5-V<sup>(1)</sup> OPERATION

over recommended operating conditions (unless otherwise noted)

|                     | PARAMET  | ER   | TEST CONDI   | TIONS                            | MIN                   | TYP | MAX   | UNIT |
|---------------------|--|--|--|----------------------------------|-----------------------|-----|-------|------|
| SUPPL               | Y CURRENT  |  |  |                                  |                       |     |       |      |
|                     | 10070400   | Quiescent  | $V_I = V_{CC}$ or 0 V, All channels,   | no load, EN <sub>2</sub> at 3 V  |                       | 0.5 | 1     |      |
|                     | ISO7240C   | 25 Mbps  |  |                                  |                       | 3   | 5     | mA   |
|                     | $\label{eq:scent} ISO7241C \qquad \qquad$ |  | no load, EN <sub>1</sub> at 3 V,   |                                  | 4                     | 7   | mA    |      |
| I <sub>CC1</sub>    |  | 25 Mbps  |  |                                  |                       | 6.5 | 11    |      |
|                     | ISO7242C   | Quiescent  | $V_{I} = V_{CC}$ or 0 V, All channels,<br>EN <sub>2</sub> at 3 V               | no load, EN <sub>1</sub> at 3 V, |                       | 6   | 10    | mA   |
|                     |  | 25 Mbps  |  |                                  |                       | 9   | 14    |      |
|                     | 10070400   | Quiescent $V_1 = V_{CC}$ or 0 V, All channels, no load, EN <sub>2</sub> at 3 V | no load, EN <sub>2</sub> at 3 V  |                                  | 15                    | 22  |       |      |
|                     | ISO7240C   | 25 Mbps  |  |                                  |                       | 17  | 25    | mA   |
| I <sub>CC2</sub>    | ISO7241C Quiescent $V_1 = V_{CC}$ or 0 V, All channels,<br>EN <sub>2</sub> at 3 V  |  | no load, EN <sub>1</sub> at 3 V,   |                                  | 13                    | 20  | mA    |      |
|                     |  | 25 Mbps  |  |                                  |                       | 18  | 28    |      |
|                     | ISO7242C Quiescent   | Quiescent  | $V_{\rm I}$ = $V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V |                                  |                       | 10  | 16    | mA   |
|                     |  | 25 Mbps  |  |                                  | 15                    | 24  |       |      |
| ELECTR              | RICAL CHARACTE   | RISTICS  |  |                                  |                       |     |       |      |
| I <sub>OFF</sub>    | Sleep mode out   | put current  | EN at 0 V, Single channel  |                                  |                       | 0   |       | μA   |
|                     |  |  | I <sub>OH</sub> = –4 mA, See Figure 1  | ISO7240                          | $V_{CC} - 0.4$        |     |       |      |
| V <sub>OH</sub>     | High-level outpu   | it voltage   | $I_{OH} = -4 \text{ mA}, \text{ See Figure 1}$                                 | ISO724x (5-V side)               | $V_{CC} - 0.8$        |     |       | V    |
|                     |  |  | $I_{OH} = -20 \ \mu A$ , See Figure 1  |                                  | V <sub>CC</sub> – 0.1 |     |       |      |
| V <sub>OL</sub>     | Low-level outpu  | t voltago  | I <sub>OL</sub> = 4 mA, See Figure 1   |                                  |                       |     | 0.4   | V    |
| VOL                 |  | t voltage  | I <sub>OL</sub> = 20 μA, See Figure 1  |                                  |                       |     | 0.1   | v    |
| V <sub>I(HYS)</sub> | Input voltage hy   | steresis   |  |                                  |                       | 150 |       | mV   |
| I <sub>IH</sub>     | High-level input   | gh-level input current   |  |                                  |                       | 10  | ıιΔ   |      |
| IIL                 | Low-level input current IN from 0 V to V <sub>CC</sub>   |  | –10  |                                  |                       | μA  |       |      |
| CI                  | Input capacitant   | ce to ground   | IN at $V_{CC}$ , $V_I = 0.4 \sin (4E6\pi t)$                                   | )                                |                       | 2   |       | pF   |
| CMTI                | Common-mode transient<br>immunity $V_1 = V_{CC}$ or 0 V, See Figure 5  |  |  | 25                               | 50                    |     | kV/µs |      |

(1) For the 5-V operation, V<sub>CC1</sub> or V<sub>CC2</sub> is specified from 4.5 V to 5.5 V. For the 3-V operation, V<sub>CC1</sub> or V<sub>CC2</sub> is specified from 3.15 V to 3.6 V.

8



## SWITCHING CHARACTERISTICS: $V_{cc1}$ at 3.3-V and $V_{cc2}$ at 5-V OPERATION

over recommended operating conditions (unless otherwise noted)

| PARAMETER                              |  | TEST CONDITIONS    |                       |    | ТҮР | MA<br>X | UNIT |
|--|--|--------------------|-----------------------|----|-----|---------|------|
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Propagation delay  | See Figure 1       |                       | 20 |     | 51      |      |
| PWD                                    | Pulse-width distortion $^{(1)}$  t <sub>PHL</sub> – t <sub>PLH</sub> | See Figure 1       | ISO7240C,<br>ISO7241C |    |     | 3       | ns   |
|  |  |                    | ISO7242C              |    |     | 4       |      |
| t <sub>sk(pp)</sub>                    | Part-to-part skew <sup>(2)</sup>                                     |                    |                       |    |     | 10      | ns   |
|  | Channel to channel output allow (3)                                  | ISO7240C, ISO72410 | 2                     |    |     | 3       | ns   |
| t <sub>sk(o)</sub>                     | Channel-to-channel output skew <sup>(3)</sup>                        | ISO7242C           |                       |    |     |         |      |
| t <sub>r</sub>                         | Output signal rise time  | See Figure 1       |                       |    | 2   |         | 20   |
| t <sub>f</sub>                         | Output signal fall time  | See Figure 1       |                       |    | 2   |         | ns   |
| t <sub>PHZ</sub>                       | Propagation delay,<br>high-level-to-high-impedance output            |                    |                       |    | 15  | 25      |      |
| t <sub>PZH</sub>                       | Propagation delay,<br>high-impedance-to-high-level output            |                    |                       |    | 15  | 25      | 20   |
| t <sub>PLZ</sub>                       | Propagation delay, low-level-to-high-impedance output                | See Figure 2       |                       |    | 15  | 25      | ns   |
| t <sub>PZL</sub>                       | Propagation delay, high-impedance-to-low-level output                |                    |                       |    | 15  | 25      |      |
| t <sub>fs</sub>                        | Failsafe output delay time from input power loss                     | See Figure 3       |                       |    | 12  |         | μs   |
| t <sub>wake</sub>                      | Wake time from input disable   | See Figure 4       |                       |    | 15  |         | μs   |

(1) Also known as pulse skew

t<sub>sk(pp)</sub> is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices (2)

 $t_{sk(0)}$  is the same supply voltages, at the same temperature, and have identical packages and test circuits.  $t_{sk(0)}$  is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads. (3)

SLLSE40A - SEPTEMBER 2010-REVISED SEPTEMBER 2011

www.ti.com

# ELECTRICAL CHARACTERISTICS: $V_{\text{CC1}}$ and $V_{\text{CC2}}$ at 3.3 $V^{(1)}$ OPERATION

over recommended operating conditions (unless otherwise noted)

|                     | PARAMETER  |           | TEST CONDITIONS                                 | MIN TYF               | MAX  | UNIT  |
|---------------------|--|-----------|---|-----------------------|------|-------|
| SUPPLY              | CURRENT  |           |   |                       |      |       |
|                     | 18070400   | Quiescent | $V_{I} = V_{CC}$ or 0 V, all channels, no load, | 0.5                   | 5 1  | ~^^   |
|                     |  |           | EN <sub>2</sub> at 3 V                          | ;                     | 3 5  | mA    |
|                     | ISO7241C   | Quiescent | $V_{I} = V_{CC}$ or 0 V, all channels, no load, | 4                     | ¥ 7  |       |
| I <sub>CC1</sub>    |  | 25 Mbps   | $EN_1$ at 3 V, $EN_2$ at 3 V                    | 6.5                   | 5 11 | mA    |
|                     | ISO7242C   | Quiescent | $V_{I} = V_{CC}$ or 0 V, all channels, no load, | (                     | 6 10 | ШA    |
|                     |  | 25 Mbps   | EN <sub>1</sub> at 3 V, EN <sub>2</sub> at 3 V  | 9                     | 9 14 |       |
| 10070400            |  | Quiescent | $V_{I} = V_{CC}$ or 0 V, all channels, no load, | 9.8                   | 5 15 | mA    |
|                     | ISO7240C   | 25 Mbps   | EN <sub>2</sub> at 3 V                          | 10.8                  | 5 17 | mA    |
| 1                   | ISO7241C   | Quiescent | $V_{I} = V_{CC}$ or 0 V, all channels, no load, | 8                     | 3 13 |       |
| I <sub>CC2</sub>    |  | 25 Mbps   | $EN_1$ at 3 V, $EN_2$ at 3 V                    | 11.5                  | 5 18 | mA    |
|                     | ISO7242C   | Quiescent | $V_{I} = V_{CC}$ or 0 V, all channels, no load, |                       | 6 10 | ШA    |
|                     |  | 25 Mbps   | $EN_1$ at 3 V, $EN_2$ at 3 V                    | 9                     | 9 14 |       |
| ELECTR              | RICAL CHARACTERISTICS                            |           |   |                       |      |       |
| I <sub>OFF</sub>    | Sleep mode output current                        |           | EN at 0 V, single channel                       | (                     | )    | μA    |
| V <sub>он</sub>     | High-level output voltage                        |           | I <sub>OH</sub> = -4 mA, See Figure 1           | $V_{CC} - 0.4$        |      | V     |
| VОН                 | Tilgit-level output voltage                      |           | $I_{OH} = -20 \ \mu A$ , See Figure 1           | V <sub>CC</sub> – 0.1 |      | v     |
| V <sub>OL</sub>     | Low-level output voltage                         |           | I <sub>OL</sub> = 4 mA, See Figure 1            |                       | 0.4  | V     |
| VOL                 | L Low-level output voltage                       |           | $I_{OL}$ = 20 µA, See Figure 1                  |                       | 0.1  | v     |
| V <sub>I(HYS)</sub> | Input voltage hysteresis                         |           |   | 150                   | )    | mV    |
| I <sub>IH</sub>     | High-level input current Low-level input current |           | IN from 0 V or V <sub>CC</sub>                  |                       | 10   |       |
| IIL                 |  |           |   | -10                   |      | μA    |
| CI                  | Input capacitance to ground                      | d         | IN at $V_{CC}$ , $V_I = 0.4 \sin (4E6\pi t)$    |                       | 2    | pF    |
| CMTI                | Common-mode transient in                         | nmunity   | $V_{I} = V_{CC}$ or 0 V, See Figure 5           | 25 50                 | )    | kV/μs |

(1) For the 5-V operation, V<sub>CC1</sub> or V<sub>CC2</sub> is specified from 4.5 V to 5.5 V. For the 3-V operation, V<sub>CC1</sub> or V<sub>CC2</sub> is specified from 3.15 V to 3.6 V.

Copyright © 2010–2011, Texas Instruments Incorporated





## SWITCHING CHARACTERISTICS: $V_{CC1}$ and $V_{CC2}$ at 3.3-V OPERATION

over recommended operating conditions (unless otherwise noted)

| PARAMETER                              |  | TEST                               | MI<br>N               | TY<br>P | MAX | UNIT |     |
|--|--|------------------------------------|-----------------------|---------|-----|------|-----|
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Propagation delay  | See Figure 1                       |                       | 25      |     | 56   | ns  |
| PWD                                    | Pulse-width distortion  t <sub>PHL</sub> – t <sub>PLH</sub>   <sup>(1)</sup> |                                    |                       |         |     | 4    |     |
| t <sub>sk(pp)</sub>                    | Part-to-part skew <sup>(2)</sup>   |                                    |                       |         |     | 10   | ns  |
| •                                      | Channel-to-channel output skew (3)   | ISO7240C, ISO7241C                 | ;                     |         |     | 3.5  | ns  |
| t <sub>sk(o)</sub>                     |  | ISO7242C                           |                       |         |     | 4    | 115 |
| t <sub>r</sub>                         | Output signal rise time  | See Figure 1                       |                       |         | 2   |      | ns  |
| t <sub>f</sub>                         | Output signal fall time  | See Figure 1                       |                       |         | 2   |      | ns  |
| t <sub>PHZ</sub>                       | Propagation delay,<br>high-level-to-high-impedance output                    |                                    | ISO7240C,<br>ISO7241C |         | 15  | 20   |     |
|  |  |                                    | ISO7242C              |         | 15  | 25   |     |
| t <sub>PZH</sub>                       | Propagation delay,<br>high-impedance-to-high-level output                    |                                    | ISO7240C,<br>ISO7241C |         | 15  | 20   |     |
|  |  |                                    | ISO7242C              |         | 15  | 25   |     |
| t <sub>PLZ</sub>                       | Propagation delay, low-level-to-high-impedance output                        | See Figure 2 ISO7240C,<br>ISO7241C |                       |         | 15  | 20   | ns  |
|  |  |                                    | ISO7242C              |         | 15  | 25   |     |
| t <sub>PZL</sub> Propagati<br>output   | Propagation delay, high-impedance-to-low-level output                        | *                                  | ISO7240C,<br>ISO7241C | 15      |     | 20   |     |
|  |  |                                    | ISO7242C              |         | 15  | 25   |     |
| t <sub>fs</sub>                        | Failsafe output delay time from input power loss                             | See Figure 3                       |                       |         | 18  |      | μs  |
| t <sub>wake</sub>                      | Wake time from input disable   | See Figure 4                       |                       |         | 15  |      | μs  |

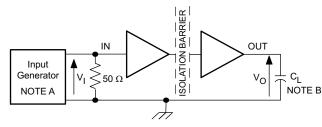
(1) Also referred to as pulse skew.

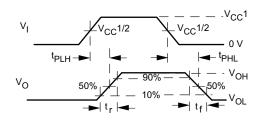
(2) t<sub>sk(pp)</sub> is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

(3)  $t_{sk(o)}$  is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.



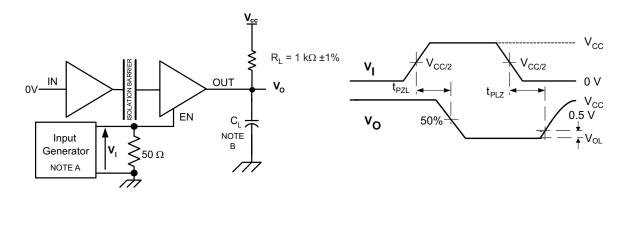
#### PARAMETER MEASUREMENT INFORMATION

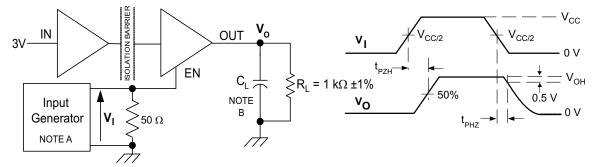




- A. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  50 kHz, 50% duty cycle, t<sub>r</sub>  $\leq$  3 ns, t<sub>f</sub>  $\leq$  3 ns, Z<sub>O</sub> = 50 $\Omega$ .
- B.  $C_L = 15 \text{ pF}$  and includes instrumentation and fixture capacitance within ±20%.

#### Figure 1. Switching Characteristic Test Circuit and Voltage Waveforms



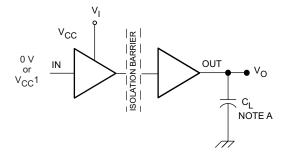


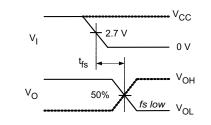
- A. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  50 kHz, 50% duty cycle, t<sub>r</sub>  $\leq$  3 ns, t<sub>f</sub>  $\leq$  3 ns, Z<sub>O</sub> = 50 $\Omega$ .
- B.  $C_L = 15 \text{ pF}$  and includes instrumentation and fixture capacitance within ±20%.

#### Figure 2. Enable/Disable Propagation Delay Time Test Circuit and Waveform



#### PARAMETER MEASUREMENT INFORMATION (continued)





- A.  $C_L = 15 \text{ pF}$  and includes instrumentation and fixture capacitance within ±20%.
- B. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  50 kHz, 50% duty cycle, t<sub>r</sub>  $\leq$  3 ns, t<sub>f</sub>  $\leq$  3 ns, Z<sub>O</sub> = 50 $\Omega$ .

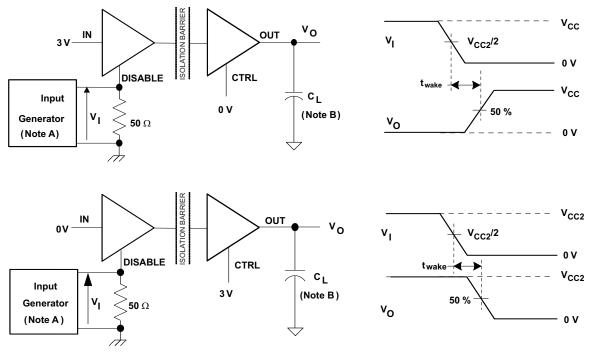


Figure 3. Failsafe Delay Time Test Circuit and Voltage Waveforms

NOTE: Which ever test yields the longest time is used in this data sheet

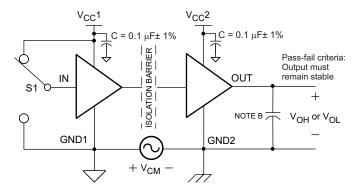
A. Whichever test yields the longest time is used in this data sheet.

Figure 4. Wake Time From Input Disable Test Circuit and Voltage Waveforms

TEXAS INSTRUMENTS

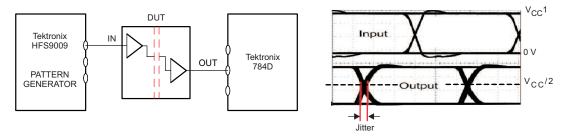
www.ti.com

#### PARAMETER MEASUREMENT INFORMATION (continued)



- A.  $C_L = 15 \text{ pF}$  and includes instrumentation and fixture capacitance within ±20%.
- B. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  50 kHz, 50% duty cycle, t<sub>r</sub>  $\leq$  3 ns, t<sub>f</sub>  $\leq$  3 ns, Z<sub>O</sub> = 50 $\Omega$ .

Figure 5. Common-Mode Transient Immunity Test Circuit and Voltage Waveform



NOTE: PRBS bit pattern run length is 2<sup>16</sup> – 1. Transition time is 800 ps. NRZ data input has no more than five consecutive 1s or 0s.

Figure 6. Peak-to-Peak Eye-Pattern Jitter Test Circuit and Voltage Waveform



## SLLSE40A – SEPTEMBER 2010–REVISED SEPTEMBER 2011

#### **DEVICE INFORMATION**

#### PACKAGE CHARACTERISTICS

|                 | PARAMETER  | TEST CONDITIONS  | MIN   | TYP               | MAX | UNIT |
|-----------------|--|--|-------|-------------------|-----|------|
| L(I01)          | Minimum air gap (Clearance)                      | Shortest terminal-to-terminal distance through air   | 8.34  |                   |     | mm   |
| L(I02)          | Minimum external tracking (Creepage)             | Shortest terminal-to-terminal distance across the package surface  | 8.1   |                   |     | mm   |
| C <sub>TI</sub> | Tracking resistance (comparative tracking index) | DIN IEC 60112/VDE 0303 Part 1  | ≥ 175 |                   |     | V    |
|                 | Minimum Internal Gap (Internal<br>Clearance)     | Distance through the insulation  | 0.008 |                   |     | mm   |
| R <sub>IO</sub> | Isolation resistance                             | Input to output, $V_{IO}$ = 500 V, all pins on each side of the barrier tied together creating a two-terminal device |       | >10 <sup>12</sup> |     | Ω    |
| C <sub>IO</sub> | Barrier capacitance Input to output              | V <sub>I</sub> = 0.4 sin (4E6πt)   |       | 2                 |     | pF   |
| CI              | Input capacitance to ground                      | V <sub>I</sub> = 0.4 sin (4E6πt)   |       | 2                 |     | pF   |

#### IEC 60664-1 RATINGS TABLE

| PARAMETER                   | TEST CONDITIONS               | SPECIFICATION |
|-----------------------------|-------------------------------|---------------|
| Basic isolation group       | Material group                | Illa          |
| Installation classification | Rated mains voltage ≤150 VRMS | I-IV          |
|                             | Rated mains voltage ≤300 VRMS | I-III         |

#### **REGULATORY INFORMATION**

| VDE                                  | CSA   | UL   |
|--------------------------------------|---|--|
| Certified according to IEC 60747-5-2 | Approved under CSA Component<br>Acceptance Notice | Recognized under 1577 Component Recognition Program <sup>(1)</sup> |
| File Number: 40016131                | File Number: 1698195                              | File Number: E181974   |

(1) Production tested  $\geq$  3000 Vrms for 1 second in accordance with UL 1577.

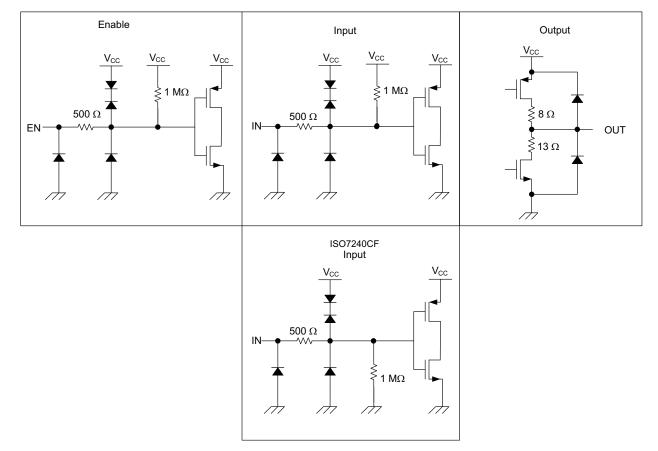
## ISO7240CF-Q1, ISO7240C-Q1 ISO7241C-Q1, ISO7242C-Q1

SLLSE40A - SEPTEMBER 2010-REVISED SEPTEMBER 2011



www.ti.com

## **DEVICE I/O SCHEMATICS**



## THERMAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

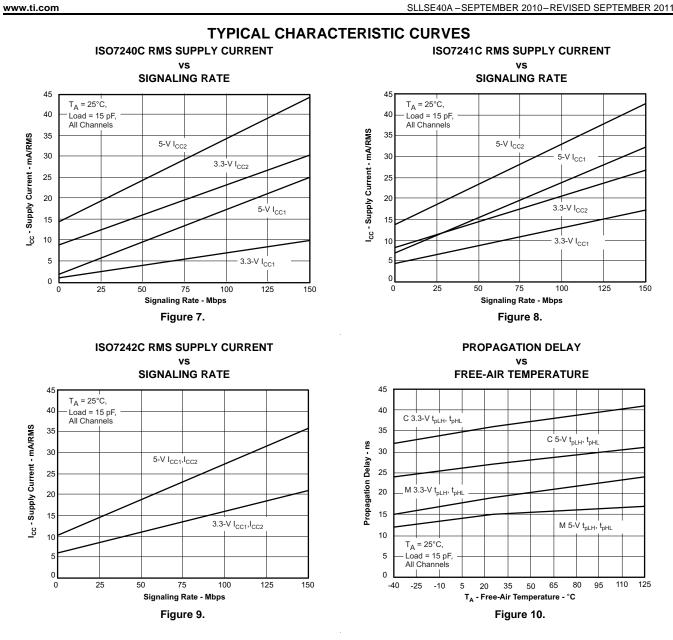
|                      | PARAMETER                            | TEST CONDITIONS  | MIN | TYP | MAX  | UNIT |
|----------------------|--------------------------------------|--|-----|-----|------|------|
| 0                    | lunction to air                      | Low-K Thermal Resistance <sup>(1)</sup>  | 168 |     |      | °C/W |
| $\theta_{JA}$        | Junction-to-air                      | High-K Thermal Resistance 96.1   |     |     | C/vv |      |
| $\theta_{JB}$        | Junction-to-Board Thermal Resistance |  |     | 61  |      | °C/W |
| $\theta_{\text{JC}}$ | Junction-to-Case Thermal Resistance  |  |     | 48  |      | °C/W |
| P <sub>D</sub>       | Device Power Dissipation             | $V_{CC1} = V_{CC2} = 5.5 \text{ V}, \text{ T}_{J} = 150^{\circ}\text{C}, \text{ C}_{L} = 15 \text{ pF},$<br>Input a 50% duty cycle square wave |     |     | 220  | mW   |

(1) Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface mount packages.



## ISO7240CF-Q1, ISO7240C-Q1 IS07241C-Q1, IS07242C-Q1

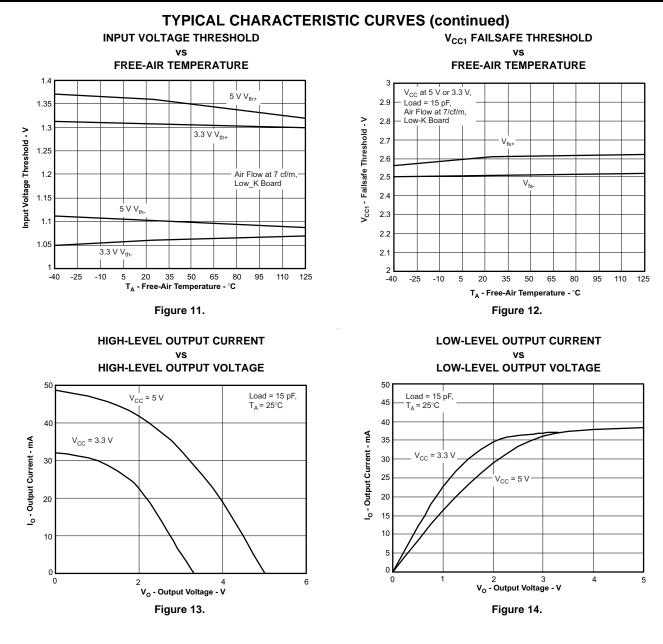
SLLSE40A - SEPTEMBER 2010-REVISED SEPTEMBER 2011



## ISO7240CF-Q1, ISO7240C-Q1 ISO7241C-Q1, ISO7242C-Q1 SLLSE40A-SEPTEMBER 2010-REVISED SEPTEMBER 2011



www.ti.com



Copyright © 2010-2011, Texas Instruments Incorporated



#### **APPLICATION INFORMATION**

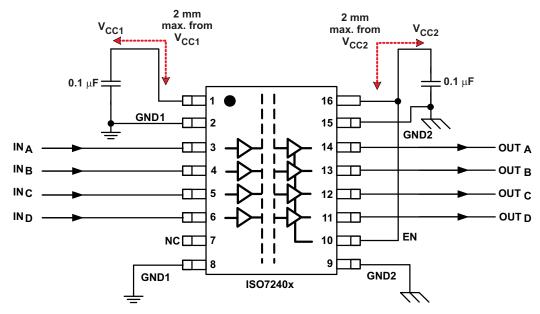


Figure 15. Typical ISO7240x Application Circuit

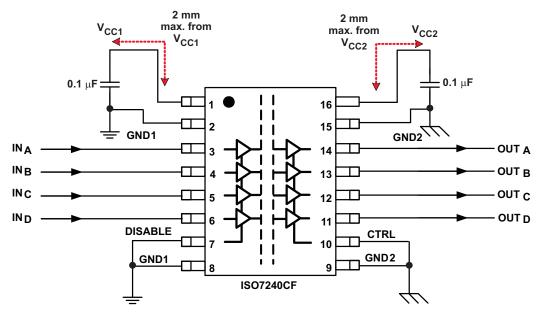


Figure 16. Typical ISO7240CF Failsafe-Low Application Circuit

SLLSE40A - SEPTEMBER 2010-REVISED SEPTEMBER 2011

# STRUMENTS

EXAS

#### LIFE EXPECTANCY vs WORKING VOLTAGE

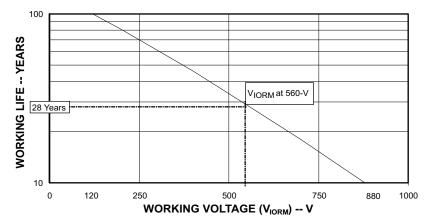


Figure 17. Time-Dependant Dielectric Breakdown Testing Results



#### **PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package<br>Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup>    | Lead/<br>Ball Finish | MSL Peak Temp <sup>(3)</sup> | Samples<br>(Requires Login) |
|------------------|-----------------------|--------------|--------------------|------|-------------|----------------------------|----------------------|------------------------------|-----------------------------|
| ISO7240CFQDWRQ1  | ACTIVE                | SOIC         | DW                 | 16   | 2000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-3-260C-168 HR          |                             |
| ISO7241CQDWRQ1   | ACTIVE                | SOIC         | DW                 | 16   | 2000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-3-260C-168 HR          |                             |
| ISO7242CQDWRQ1   | ACTIVE                | SOIC         | DW                 | 16   | 2000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-3-260C-168 HR          |                             |

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between

the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

#### OTHER QUALIFIED VERSIONS OF ISO7240CF-Q1, ISO7241C-Q1, ISO7242C-Q1 :

• Catalog: ISO7240CF, ISO7241C, ISO7242C





20-Mar-2012

NOTE: Qualified Version Definitions:

• Catalog - TI's standard catalog product

# PACKAGE MATERIALS INFORMATION

www.ti.com

Texas Instruments

## TAPE AND REEL INFORMATION





## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



| *All dimensions are nominal |                 |                    |    |      |                          |                          |            |            |            |            |           |                  |
|-----------------------------|-----------------|--------------------|----|------|--------------------------|--------------------------|------------|------------|------------|------------|-----------|------------------|
| Device                      | Package<br>Type | Package<br>Drawing |    | SPQ  | Reel<br>Diameter<br>(mm) | Reel<br>Width<br>W1 (mm) | A0<br>(mm) | B0<br>(mm) | K0<br>(mm) | P1<br>(mm) | W<br>(mm) | Pin1<br>Quadrant |
| ISO7240CFQDWRQ1             | SOIC            | DW                 | 16 | 2000 | 330.0                    | 16.4                     | 10.75      | 10.7       | 2.7        | 12.0       | 16.0      | Q1               |
| ISO7242CQDWRQ1              | SOIC            | DW                 | 16 | 2000 | 330.0                    | 16.4                     | 10.75      | 10.7       | 2.7        | 12.0       | 16.0      | Q1               |

TEXAS INSTRUMENTS

www.ti.com

# PACKAGE MATERIALS INFORMATION

6-Nov-2012



\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| ISO7240CFQDWRQ1 | SOIC         | DW              | 16   | 2000 | 367.0       | 367.0      | 38.0        |
| ISO7242CQDWRQ1  | SOIC         | DW              | 16   | 2000 | 367.0       | 367.0      | 38.0        |

DW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MS-013 variation AA.



# LAND PATTERN DATA



NOTES:

A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



#### **IMPORTANT NOTICE**

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have *not* been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components which meet ISO/TS16949 requirements, mainly for automotive use. Components which have not been so designated are neither designed nor intended for automotive use; and TI will not be responsible for any failure of such components to meet such requirements.

| Products                     |                          | Applications                  |                                   |
|------------------------------|--------------------------|-------------------------------|-----------------------------------|
| Audio                        | www.ti.com/audio         | Automotive and Transportation | www.ti.com/automotive             |
| Amplifiers                   | amplifier.ti.com         | Communications and Telecom    | www.ti.com/communications         |
| Data Converters              | dataconverter.ti.com     | Computers and Peripherals     | www.ti.com/computers              |
| DLP® Products                | www.dlp.com              | Consumer Electronics          | www.ti.com/consumer-apps          |
| DSP                          | dsp.ti.com               | Energy and Lighting           | www.ti.com/energy                 |
| Clocks and Timers            | www.ti.com/clocks        | Industrial                    | www.ti.com/industrial             |
| Interface                    | interface.ti.com         | Medical                       | www.ti.com/medical                |
| Logic                        | logic.ti.com             | Security                      | www.ti.com/security               |
| Power Mgmt                   | power.ti.com             | Space, Avionics and Defense   | www.ti.com/space-avionics-defense |
| Microcontrollers             | microcontroller.ti.com   | Video and Imaging             | www.ti.com/video                  |
| RFID                         | www.ti-rfid.com          |                               |                                   |
| OMAP Applications Processors | www.ti.com/omap          | TI E2E Community              | e2e.ti.com                        |
| Wireless Connectivity        | www.ti.com/wirelessconne | ctivity                       |                                   |

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2012, Texas Instruments Incorporated