Low Power Quad Channels Digital Isolators

Check for Samples: ISO7640FM, ISO7641FM

FEATURES

- **Signaling Rate: 150 Mbps**
- **Low Power Consumption, Typical I_{CC} per Channel (3.3 V Supplies):**
  - **ISO7640FM: 2 mA at 25 Mbps**
  - **ISO7641FM: 2.4 mA at 25 Mbps**
- **Low Propagation Delay: 7 ns Typical**
- **Output Defaults to Low-state in fail-safe mode**
- **Wide Temperature Range: –40°C to 125°C**
- **50 KV/µs Transient Immunity, Typical**
- **Long Life with SiO_2 Isolation barrier**
- **Operates From 2.7V, 3.3 V and 5 V Supply and Logic Levels**
- **Wide Body SOIC-16 Package**

APPLICATIONS

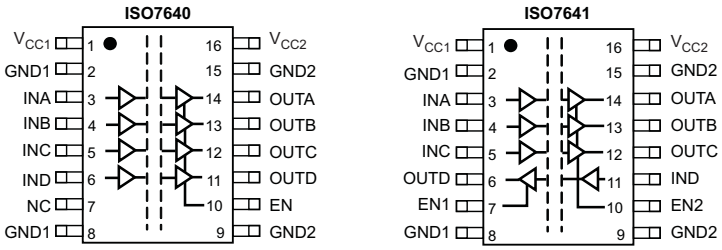
- **Optocoupler Replacement in:**
  - **Industrial Fieldbus**
    - **Profibus**
    - **Modbus**
    - **DeviceNet™ Data Buses**
  - **Servo Control Interface**
  - **Motor Control**
  - **Power Supplies**
  - **Battery Packs**

SAFETY AND REGULATORY APPROVALS

- **6000 V_{PK} / 4243 V_{RMS} for 1 Minute per UL 1577 (approved)**
- **VDE Approval for DIN EN 60747-5-2 (VDE 0884 Rev. 2), 1414 V_{PK} Working Voltage (approved)**
- **CSA Component Acceptance Notice 5A, IEC 60601-1 Medical Standard (approved)**
- **5 KV_{RMS} Reinforced Insulation per TUV for EN/UL/CSA 60950-1 and EN/UL/CSA 61010-1 (approved)**

DESCRIPTION

ISO7640FM and ISO7641FM provide galvanic isolation up to 6 KV_{PK} for 1 minute per UL and VDE. These devices are also certified up to 5 KV_{RMS} Reinforced isolation at a working voltage of 400 V_{RMS} per end equipment standards EN/UL/CSA 60950-1 and 61010-1. ISO7640F and ISO7641F are quad channel isolators; ISO7640F has four forward and ISO7641F has three forward and one reverse direction channels. Suffix F indicates that output defaults to Low-state in fail-safe conditions (see Table 1). M-Grade devices are high speed isolators capable of 150 Mbps data rate with fast propagation delays



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION CONTINUED

Each isolation channel has a logic input and output buffer separated by a silicon dioxide (SiO_2) insulation barrier. Used in conjunction with isolated power supplies, these devices prevent noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. The devices have TTL input thresholds and can operate from 2.7 V, 3.3 V and 5 V supplies. All inputs are 5 V tolerant when supplied from 3.3 V or 2.7 V supplies.

PIN DESCRIPTIONS

PIN			I/O	DESCRIPTION
NAME	ISO7640	ISO7641		
INA	3	3	I	Input, channel A
INB	4	4	I	Input, channel B
INC	5	5	I	Input, channel C
IND	6	11	I	Input, channel D
OUTA	14	14	O	Output, channel A
OUTB	13	13	O	Output, channel B
OUTC	12	12	O	Output, channel C
OUTD	11	6	O	Output, channel D
EN	10	-	I	Enables (when input is High or Open) or Disables (when input is Low) OUTA, OUTB, OUTC and OUTD of ISO7640
EN1	-	7	I	Enables (when input is High or Open) or Disables (when input is Low) OUTD of ISO7641
EN2	-	10	I	Enables (when input is High or Open) or Disables (when input is Low) OUTA, OUTB, and OUTC of ISO7641
V_{CC1}	1	1	–	Power supply, V_{CC1}
V_{CC2}	16	16	–	Power supply, V_{CC2}
GND1	2,8	2,8	–	Ground connection for V_{CC1}
GND2	9,15	9,15	–	Ground connection for V_{CC2}
NC	7	-	-	No Connect pins are floating with no internal connection

Table 1. FUNCTION TABLE(1)

INPUT V_{CC}	OUTPUT V_{CC}	INPUT (INx)	OUTPUT ENABLE (ENx)	OUTPUT (OUTx)
PU	PU	H	H or Open	H
		L	H or Open	L
		X	L	Z
		Open	H or Open	L
PD	PU	X	H or Open	L
PD	PU	X	L	Z
PU	PD	X	X	Undetermined

(1) PU = Powered Up(V_{CC} ≥ 2.7 V); PD = Powered Down (V_{CC} ≤ 2.1 V); X = Irrelevant; H = High Level; L = Low Level; Z = High Impedance

AVAILABLE OPTIONS

PRODUCT	RATED ISOLATION	PACKAGE	INPUT THRESHOLD	DATA RATE and FILTER	CHANNEL DIRECTION	MARKED AS	ORDERING NUMBER
ISO7640FM	6 KV_{PK} / 5 KV_{RMS} (1)	DW-16	1.5 V TTL (CMOS Compatible)	150 Mbps, No Noise Filter	4 Forward, 0 Reverse	ISO7640FM	ISO7640FMDW (rail)
							ISO7640FMDWR (reel)
ISO7641FM					3 Forward, 1 Reverse	ISO7641FM	ISO7641FMDW (rail)
							ISO7641FMDWR (reel)

(1) See the Regulatory Information table for detailed isolation ratings.

ABSOLUTE MAXIMUM RATINGS(1)

PARAMETER				VALUE MIN	VALUE MAX	UNIT
Supply voltage(2)	V_{CC1}, V_{CC2}			–0.5	6	V
Voltage	INx, OUTx, ENx			–0.5	6	V
Output Current, I_O					±15	mA
Electrostatic discharge	Human Body Model	ESDA, JEDEC JS-001-2012	All pins		±4	kV
	Field-Induced Charged Device Model	JEDEC JESD22-C101E			±1.5	kV
	Machine Model	JEDEC JESD22-A115-A			±200	V
Maximum junction temperature, T_J					150	°C
Storage temperature, T_{STG}				-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.

RECOMMENDED OPERATING CONDITIONS

PARAMETER			MIN	TYP	MAX	UNIT
Supply voltage	V_{CC1}, V_{CC2}		2.7		5.5	V
High-level output current	I_{OH}		-4			mA
Low-level output current	I_{OL}				4	mA
High-level input voltage	V_{IH}		2		V_{CC}	V
Low-level input voltage	V_{IL}		0		0.8	V
Input pulse duration	t_{ui}	≥3V-Operation	6.67			ns
		<3V-Operation	10			
Signaling rate	1 / t_{ui}	≥3V-Operation	0		150	Mbps
		<3V-Operation	0		100	
Junction temperature	T_J		-40		136	°C
Ambient temperature	T_A		-40	25	125	°C

THERMAL INFORMATION

THERMAL METRIC(1)			ISO76xx DW (16 Pins)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance		72	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance		38	
θ_{JB}	Junction-to-board thermal resistance		39	
ψ_{JT}	Junction-to-top characterization parameter		9.4	
ψ_{JB}	Junction-to-board characterization parameter		n/a	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance		n/a	
P_D	Maximum Device Power Dissipation	V_{CC1} = V_{CC2} = 5.5V, T_J = 150°C, C_L = 15pF Input a 75 MHz 50% duty cycle square wave	399	mW

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS

V_{CC1} and V_{CC2} at 5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 1	V_{CCx}(1) – 0.8	4.8		V
		I_{OH} = –20 µA; see Figure 1	V_{CCx}(1) – 0.1	5		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 1		0.2	0.4	V
		I_{OL} = 20 µA; see Figure 1		0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis			450		mV
I_{IH}	High-level input current	V_{IH} = V_{CC} at INx or ENx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx	-10			
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see Figure 4	25	75		kV/µs

(1) V_{CCx} is the supply voltage, V_{CC1} or V_{CC2}, for the output channel that is being measured.

SWITCHING CHARACTERISTICS

V_{CC1} and V_{CC2} at 5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 1	3.5	7	10.5	ns
PWD(1)	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$				2	
$t_{sk(o)}$(2)	Channel-to-channel output skew time	Same-direction Channels			2	
		Opposite-direction Channels			3	
$t_{sk(pp)}$(3)	Part-to-part skew time				4.5	
t_r	Output signal rise time	See Figure 1		1.6		ns
t_f	Output signal fall time			1		
t_{PHZ}	Disable Propagation Delay, high-to-high impedance output	See Figure 2		5	16	ns
t_{PLZ}	Disable Propagation Delay, low-to-high impedance output			5	16	
t_{PZH}	Enable Propagation Delay, high impedance-to-high output			4	16	
t_{PZL}	Enable Propagation Delay, high impedance-to-low output			4	16	
t_{fs}	Fail-safe output delay time from input data or power loss	See Figure 3		9.5		µs

(1) Also known as Pulse Skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

SUPPLY CURRENT

V_{CC1} and V_{CC2} at 5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
ISO7640FM						
I_{CC1}	Disable	EN = 0 V		0.6	1.2	mA
I_{CC2}				4.5	6.6	
I_{CC1}	DC to 1 Mbps	DC Signal: V_I = V_{CC} or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF		0.7	1.3	
I_{CC2}				4.6	6.7	
I_{CC1}	10 Mbps			1.1	2	
I_{CC2}				6.6	10.5	
I_{CC1}	25 Mbps			1.9	3	
I_{CC2}				9.7	14.7	
I_{CC1}	150 Mbps			8.2	14.5	
I_{CC2}				35	58	
ISO7641FM						
I_{CC1}	Disable	EN1 = EN2 = 0 V		2.6	4.2	mA
I_{CC2}				4.2	6.8	
I_{CC1}	DC to 1 Mbps	DC Signal: V_I = V_{CC} or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF		2.7	4.3	
I_{CC2}				4.3	6.9	
I_{CC1}	10 Mbps			3.6	4.9	
I_{CC2}				6	8.2	
I_{CC1}	25 Mbps			5.1	6.6	
I_{CC2}				8.8	11.4	
I_{CC1}	150 Mbps			17	22	
I_{CC2}				31	42	

ELECTRICAL CHARACTERISTICS

V_{CC1} at 5 V ± 10% and V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 1	OUTx on V_{CC1} (5V) side	V_{CC1} – 0.8	4.8		V
			OUTx on V_{CC2} (3.3V) side	V_{CC2} - 0.4	3		
		I_{OH} = –20 µA; see Figure 1	OUTx on V_{CC1} (5V) side	V_{CC1} – 0.1	5		
			OUTx on V_{CC2} (3.3V) side	V_{CC2} – 0.1	3.3		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 1			0.2	0.4	V
		I_{OL} = 20 µA; see Figure 1			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				430		mV
I_{IH}	High-level input current	V_{IH} = V_{CC} at INx or ENx				10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx		-10			
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see Figure 4		25	50		kV/µs

SWITCHING CHARACTERISTICS

V_{CC1} at 5 V ± 10% and V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 1	4	8	13	ns
PWD(1)	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$				2	
$t_{sk(o)}$(2)	Channel-to-channel output skew time	Same-direction Channels			2.5	
		Opposite-direction Channels			3.5	
$t_{sk(pp)}$(3)	Part-to-part skew time				6	
t_r	Output signal rise time	See Figure 1		2		ns
t_f	Output signal fall time			1.2		
t_{PHZ}	Disable Propagation Delay, high-to-high impedance output	See Figure 2		6.5	17	ns
t_{PLZ}	Disable Propagation Delay, low-to-high impedance output			6.5	17	
t_{PZH}	Enable Propagation Delay, high impedance-to-high output			5.5	17	
t_{PZL}	Enable Propagation Delay, high impedance-to-low output			5.5	17	
t_{fs}	Fail-safe output delay time from input data or power loss	See Figure 3		9.5		µs

(1) Also known as Pulse Skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

SUPPLY CURRENT

V_{CC1} at 5 V ± 10% and V_{CC2} at 3.3V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
ISO7640FM						
I_{CC1}	Disable	EN = 0 V		0.6	1.2	mA
I_{CC2}				3.6	5.1	
I_{CC1}	DC to 1 Mbps	DC Signal: V_I = V_{CC} or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF		0.7	1.3	
I_{CC2}				3.7	5.2	
I_{CC1}	10 Mbps			1.1	2	
I_{CC2}				5	7.1	
I_{CC1}	25 Mbps			1.9	3	
I_{CC2}				6.9	11	
I_{CC1}	150 Mbps			8.2	14.5	
I_{CC2}				24	40	
ISO7641FM						
I_{CC1}	Disable	EN1 = EN2 = 0 V		2.6	4.2	mA
I_{CC2}				3.2	4.9	
I_{CC1}	DC to 1 Mbps	DC Signal: V_I = V_{CC} or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF		2.7	4.3	
I_{CC2}				3.3	5	
I_{CC1}	10 Mbps			3.6	4.9	
I_{CC2}				4.4	5.8	
I_{CC1}	25 Mbps			5.1	6.6	
I_{CC2}				6.1	7.6	
I_{CC1}	150 Mbps			17	22	
I_{CC2}				20.6	26.5	

ELECTRICAL CHARACTERISTICS

V_{CC1} at 3.3 V ± 10% and V_{CC2} at 5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 1	OUTx on V_{CC1} (3.3 V) side	V_{CC1}–0.4	3		V
			OUTx on V_{CC2} (5 V) side	V_{CC2}–0.8	4.8		
		I_{OH} = –20 µA; see Figure 1	OUTx on V_{CC1} (3.3 V) side	V_{CC1}–0.1	3.3		
			OUTx on V_{CC2} (5 V) side	V_{CC2}–0.1	5		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 1			0.2	0.4	V
		I_{OL} = 20 µA; see Figure 1			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				430		mV
I_{IH}	High-level input current	V_{IH} = V_{CC} at INx or ENx				10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx		-10			
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see Figure 4		25	50		kV/µs

SWITCHING CHARACTERISTICS

V_{CC1} at 3.3 V ± 10% and V_{CC2} at 5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 1	4	7.5	12.5	ns
PWD(1)	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$				2	
$t_{sk(o)}$(2)	Channel-to-channel output skew time	Same-direction Channels			2.5	
		Opposite-direction Channels			3.5	
$t_{sk(pp)}$(3)	Part-to-part skew time				6	
t_r	Output signal rise time	See Figure 1		1.7		ns
t_f	Output signal fall time			1.1		
t_{PHZ}	Disable Propagation Delay, high-to-high impedance output	See Figure 2		5.5	17	ns
t_{PLZ}	Disable Propagation Delay, low-to-high impedance output			5.5	17	
t_{PZH}	Enable Propagation Delay, high impedance-to-high output			4.5	17	
t_{PZL}	Enable Propagation Delay, high impedance-to-low output			4.5	17	
t_{fs}	Fail-safe output delay time from input data or power loss	See Figure 3		9.5		µs

(1) Also known as Pulse Skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

SUPPLY CURRENT

V_{CC1} at 3.3 V ± 10% and V_{CC2} at 5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
ISO7640FM						
I_{CC1}	Disable	EN = 0 V		0.35	0.7	mA
I_{CC2}				4.5	6.6	
I_{CC1}	DC to 1 Mbps	DC Signal: $V_I = V_{CC}$ or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF		0.4	0.8	
I_{CC2}				4.6	6.7	
I_{CC1}	10 Mbps			0.7	1.2	
I_{CC2}				6.6	10.5	
I_{CC1}	25 Mbps			1.1	2	
I_{CC2}				9.7	14.7	
I_{CC1}	150 Mbps			5	8.5	
I_{CC2}				35	58	
ISO7641FM						
I_{CC1}	Disable	EN1 = EN2 = 0 V		1.9	2.9	mA
I_{CC2}				4.2	6.8	
I_{CC1}	DC to 1 Mbps	DC Signal: $V_I = V_{CC}$ or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF		2	3	
I_{CC2}				4.3	6.9	
I_{CC1}	10 Mbps			2.5	3.5	
I_{CC2}				6	8.2	
I_{CC1}	25 Mbps			3.4	4.5	
I_{CC2}				8.8	11.4	
I_{CC1}	150 Mbps			10.5	14.5	
I_{CC2}				31	42	

ELECTRICAL CHARACTERISTICS

V_{CC1} and V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 1	V_{CCx} (1) – 0.4	3		V
		I_{OH} = –20 µA; see Figure 1	V_{CCx} (1) – 0.1	3.3		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 1		0.2	0.4	V
		I_{OL} = 20 µA; see Figure 1		0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis			425		mV
I_{IH}	High-level input current	V_{IH} = V_{CC} at INx or ENx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx	-10			
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see Figure 4	25	50		kV/µs

(1) V_{CCx} is the supply voltage, V_{CC1} or V_{CC2}, for the output channel that is being measured.

SWITCHING CHARACTERISTICS

V_{CC1} and V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 1	4	8.5	14	ns
PWD (1)	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$				2	
$t_{sk(o)}$ (2)	Channel-to-channel output skew time	Same-direction Channels			3	
		Opposite-direction Channels			4	
$t_{sk(pp)}$ (3)	Part-to-part skew time				6.5	
t_r	Output signal rise time	See Figure 1		2		ns
t_f	Output signal fall time			1.3		
t_{PHZ}	Disable Propagation Delay, high-to-high impedance output	See Figure 2		6.5	17	ns
t_{PLZ}	Disable Propagation Delay, low-to-high impedance output			6.5	17	
t_{PZH}	Enable Propagation Delay, high impedance-to-high output			5.5	17	
t_{PZL}	Enable Propagation Delay, high impedance-to-low output			5.5	17	
t_{fs}	Fail-safe output delay time from input data or power loss	See Figure 3		9.2		µs

(1) Also known as Pulse Skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

SUPPLY CURRENT

V_{CC1} and V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
ISO7640FM						
I_{CC1}	Disable	EN = 0 V		0.35	0.7	mA
I_{CC2}				3.6	5.1	
I_{CC1}	DC to 1 Mbps	DC Signal: $V_I = V_{CC}$ or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF		0.4	0.8	
I_{CC2}				3.7	5.2	
I_{CC1}	10 Mbps			0.7	1.2	
I_{CC2}				5	7.1	
I_{CC1}	25 Mbps			1.1	2	
I_{CC2}				6.9	11	
I_{CC1}	150 Mbps			5	8.5	
I_{CC2}				24	40	
ISO7641FM						
I_{CC1}	Disable	EN1 = EN2 = 0 V		1.9	2.9	mA
I_{CC2}				3.2	4.9	
I_{CC1}	DC to 1 Mbps	DC Signal: $V_I = V_{CC}$ or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF		2	3	
I_{CC2}				3.3	5	
I_{CC1}	10 Mbps			2.5	3.5	
I_{CC2}				4.4	5.8	
I_{CC1}	25 Mbps			3.4	4.5	
I_{CC2}				6.1	7.6	
I_{CC1}	150 Mbps			10.5	14.5	
I_{CC2}				20.6	26.5	

ELECTRICAL CHARACTERISTICS

V_{CC1} and V_{CC2} at 2.7 V[1] (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 1	V_{CC}[2] – 0.5	2.4		V
		I_{OH} = –20 µA; see Figure 1	V_{CC}[2] – 0.1	2.7		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 1		0.2	0.4	V
		I_{OL} = 20 µA; see Figure 1		0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis			350		mV
I_{IH}	High-level input current	V_{IH} = V_{CC} at INx or ENx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx	-10			
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see Figure 4	25	50		kV/µs

(1) For 2.7 V-operation, max data rate is 100 Mbps.
(2) V_{CCx} is the supply voltage, V_{CC1} or V_{CC2}, for the output channel that is being measured.

SWITCHING CHARACTERISTICS

V_{CC1} and V_{CC2} at 2.7 V (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 1	5	8	16	ns
PWD[1]	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$				2.5	
$t_{sk(o)}$[2]	Channel-to-channel output skew time	Same-direction Channels			4	
		Opposite-direction Channels			5	
$t_{sk(pp)}$[3]	Part-to-part skew time				8	
t_r	Output signal rise time	See Figure 1		2.3		ns
t_f	Output signal fall time			1.8		
t_{PHZ}	Disable Propagation Delay, high-to-high impedance output	See Figure 2		8	18	ns
t_{PLZ}	Disable Propagation Delay, low-to-high impedance output			8	18	
t_{PZH}	Enable Propagation Delay, high impedance-to-high output			7	18	
t_{PZL}	Enable Propagation Delay, high impedance-to-low output			7	18	
t_{fs}	Fail-safe output delay time from input data or power loss	See Figure 3		8.5		µs

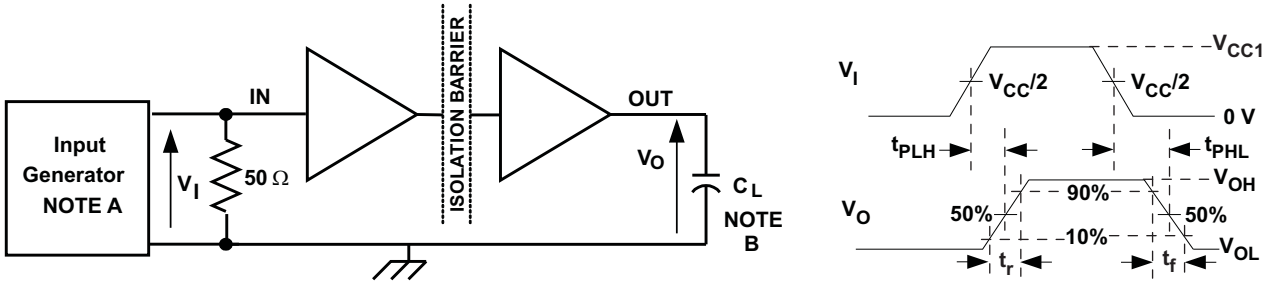
(1) Also known as Pulse Skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

SUPPLY CURRENT

V_{CC1} and V_{CC2} at 2.7 V (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
ISO7640FM						
I_{CC1}	Disable	EN = 0 V		0.2	0.6	mA
I_{CC2}				3.3	5	
I_{CC1}	DC to 1 Mbps	DC Signal: $V_I = V_{CC}$ or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF		0.2	0.7	
I_{CC2}				3.4	5.1	
I_{CC1}	10 Mbps			0.4	1.1	
I_{CC2}				4.4	6.8	
I_{CC1}	25 Mbps			0.8	1.8	
I_{CC2}				6	9.5	
I_{CC1}	100 Mbps			2.7	5	
I_{CC2}				14.2	21	
ISO7641FM						
I_{CC1}	Disable	EN1 = EN2 = 0 V		1.6	2.4	mA
I_{CC2}				2.8	4.1	
I_{CC1}	DC to 1 Mbps	DC Signal: $V_I = V_{CC}$ or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF		1.7	2.5	
I_{CC2}				2.9	4.2	
I_{CC1}	10 Mbps			2.1	3	
I_{CC2}				3.8	5	
I_{CC1}	25 Mbps			2.8	3.8	
I_{CC2}				5.2	6.7	
I_{CC1}	100 Mbps			6.4	7.5	
I_{CC2}				11.8	15.5	

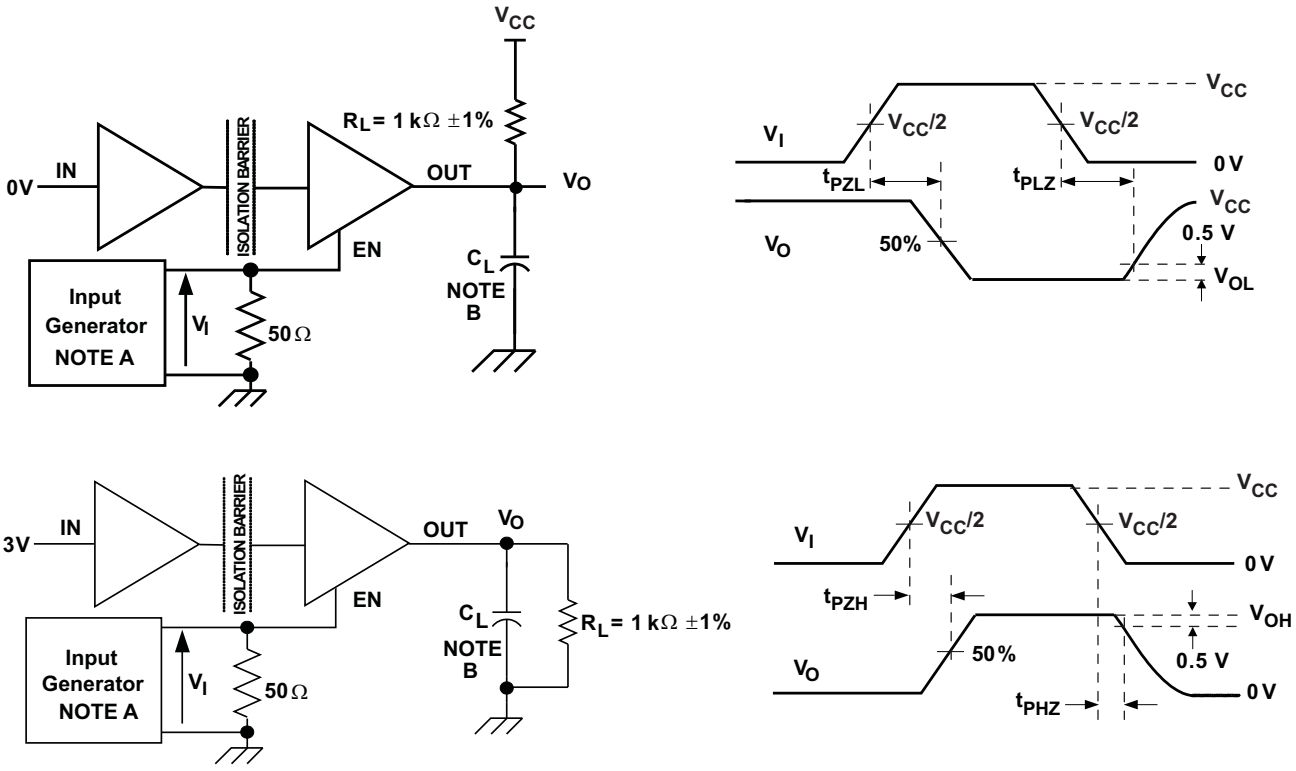
PARAMETER MEASUREMENT INFORMATION



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3ns, Z_O = 50 Ω. At the input, 50 Ω resistor is required to terminate Input Generator signal. It is not needed in actual application.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 1. Switching Characteristics Test Circuit and Voltage Waveforms

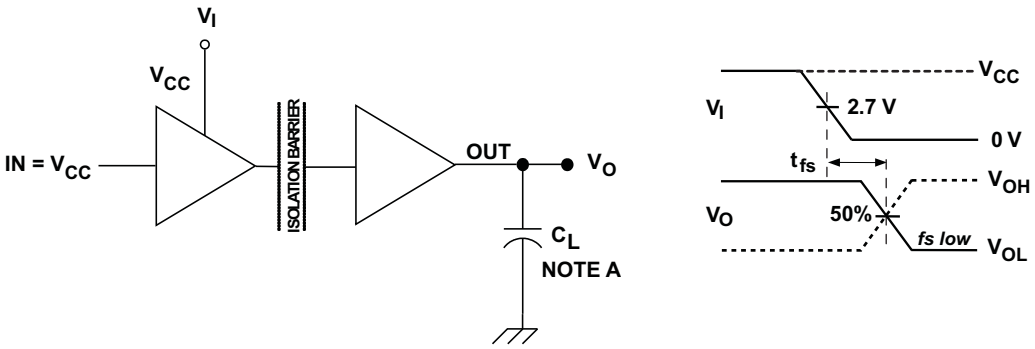


A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 10 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

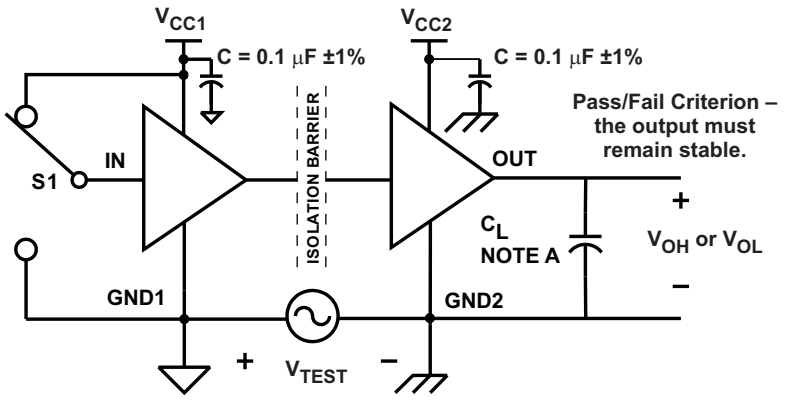
Figure 2. Enable/Disable Propagation Delay Time Test Circuit and Waveform

PARAMETER MEASUREMENT INFORMATION (continued)



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 3. Failsafe Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 4. Common-Mode Transient Immunity Test Circuit

DEVICE INFORMATION

IEC INSULATION AND SAFETY-RELATED SPECIFICATIONS FOR DW-16 PACKAGE

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (Clearance)	Shortest terminal to terminal distance through air	8.3			mm
L(I02) (1)	Minimum external tracking (Creepage)	Shortest terminal to terminal distance across the package surface	8.1			mm
CTI	Tracking resistance (Comparative Tracking Index)	DIN IEC 60112 / VDE 0303 Part 1	≥400			V
	Minimum Internal Gap (Internal Clearance)	Distance through the insulation	0.014			mm
R_{IO} (2)	Isolation resistance, Input to Output	V_{IO} = 500 V, T_A < 100°C		$>10^{12}$		Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ max		$>10^{11}$		
C_{IO} (2)	Barrier capacitance, Input to Output	V_I = 0.4 sin (2πft), f = 1MHz		2		pF
C_I (3)	Input capacitance	V_I = V_{CC}/2 + 0.4 sin (2πft), f = 1MHz, V_{CC} = 5 V		2		pF

(1) Per JEDEC package dimensions.
(2) All pins on each side of the barrier tied together creating a two-terminal device.
(3) Measured from input pin to ground.

NOTE

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board do not reduce this distance.

Creepage and clearance on a printed circuit board become equal according to the measurement techniques shown in the Isolation Glossary. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

DIN EN 60747-5-2 (VDE 0884 TEIL 2) INSULATION CHARACTERISTICS (4)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
V_{IORM}	Maximum working insulation voltage (1)		1414	V_{PEAK}
V_{PR}	Input-to-output test voltage	After Input/Output safety test subgroup 2/3, V_{PR} = V_{IORM} x 1.2, t = 10 s, Partial discharge < 5 pC	1697	V_{PEAK}
		Method a, After environmental tests subgroup 1, V_{PR} = V_{IORM} x 1.6, t = 10 s, Partial Discharge < 5 pC	2262	
		Method b1, 100% Production test V_{PR} = V_{IORM} x 1.875, t = 1 s Partial discharge < 5 pC	2652	
V_{IOTM}	Maximum transient overvoltage	V_{TEST} = V_{IOTM} t = 60 sec (Qualification) t = 1 sec (100% Production)	6000	V_{PEAK}
R_S	Insulation resistance	V_{IO} = 500 V at T_S	$>10^9$	Ω
	Pollution degree		2	

(4) Climatic Classification 40/125/21
(1) For applications that require DC working voltages between GND1 and GND2, please contact Texas Instruments for further details.

IEC 60664-1 RATINGS TABLE

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic Isolation Group	Material Group	II
Installation classification	Rated mains voltage ≤ 300 V_{RMS}	I–IV
	Rated mains voltage ≤ 600 V_{RMS}	I–III
	Rated mains voltage ≤ 1000 V_{RMS}	I–II

REGULATORY INFORMATION

VDE	TUV	CSA	UL
Certified according to DIN EN 60747-5-2	Certified according to EN/UL/CSA 60950-1 and 61010-1	Approved under CSA Component Acceptance Notice #5A	Recognized under 1577 Component Recognition Program
Basic Insulation Maximum Transient Overvoltage, 6000 V_{PK} Maximum Working Voltage, 1414 V_{PK}	5000 V_{RMS} Reinforced Insulation, 400 V_{RMS} maximum working voltage 5000 V_{RMS} Basic Insulation, 600 V_{RMS} maximum working voltage	5000 V_{RMS} Reinforced Insulation 2 Means of Patient Protection at 125 V_{RMS} per IEC 60601-1 (3rd Ed.)	Single Protection, 4243 V_{RMS} (1)
File Number: 40016131	Certificate Number: U8V 11 08 77311 005	File Number: 220991	File Number: E181974

(1) Production tested ≥ 5092 V_{RMS} for 1 second in accordance with UL 1577.

IEC SAFETY LIMITING VALUES

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the IO can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	DW-16	θ_{JA} = 72 °C/W, V_I = 5.5V, T_J = 150°C, T_A = 25°C			316	mA
			θ_{JA} = 72 °C/W, V_I = 3.6V, T_J = 150°C, T_A = 25°C			482	
			θ_{JA} = 72 °C/W, V_I = 2.7V, T_J = 150°C, T_A = 25°C			643	
T_S	Maximum case temperature					150	°C

The safety-limiting constraint is the absolute maximum junction temperature specified in the absolute maximum ratings table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed on a High-K Test Board for Leaded Surface Mount Packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

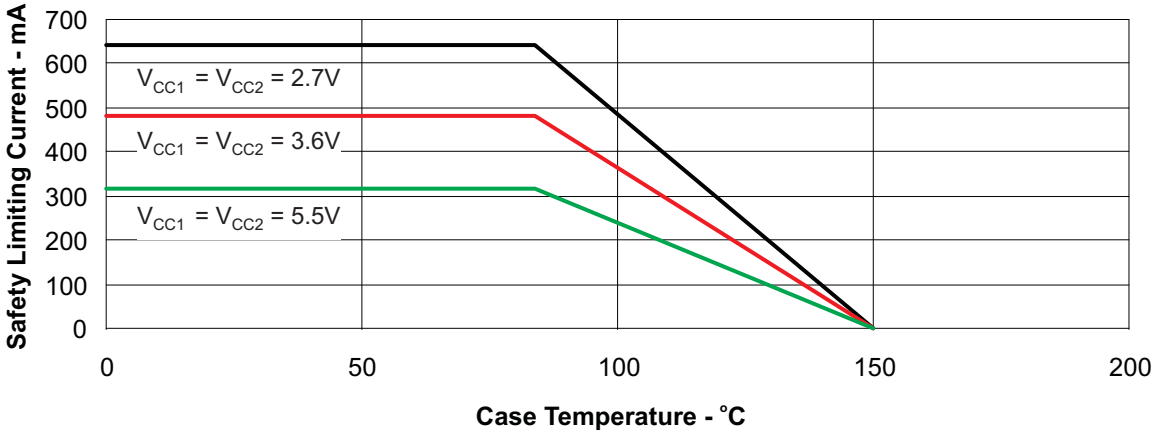


Figure 5. DW-16 θ_{JC} Thermal Derating Curve per IEC 60747-5-2

APPLICATION INFORMATION

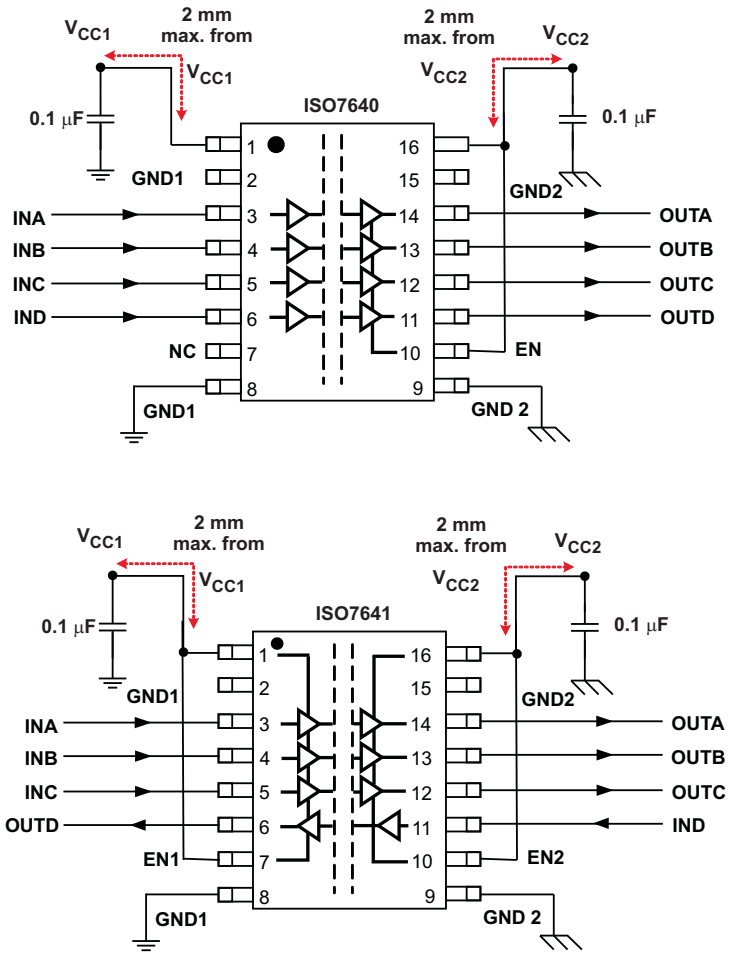


Figure 6. Typical ISO7640FM and ISO7641FM Application Circuit

Note: For detailed layout recommendations, see Application Note SLLA284, *Digital Isolator Design Guide*.

TYPICAL SUPPLY CURRENT EQUATIONS

(Calculated based on room temperature and typical Silicon process)

ISO7640FM:

At $V_{CC1} = V_{CC2} = 3.3V$

$I_{CC1} = 0.388 + 0.0312 \times f$

$I_{CC2} = 3.39 + 0.03561 \times f + 0.006588 \times f \times C_L$

At $V_{CC1} = V_{CC2} = 5V$

$I_{CC1} = 0.584 + 0.05349 \times f$

$I_{CC2} = 4.184 + 0.05597 \times f + 0.009771 \times f \times C_L$

ISO7641FM:

At $V_{CC1} = V_{CC2} = 3.3V$

$I_{CC1} = 1.848 + 0.03233 \times f + 0.001645 \times f \times C_L$

$I_{CC2} = 3.005 + 0.03459 \times f + 0.0049395 \times f \times C_L$

At $V_{CC1} = V_{CC2} = 5V$

$I_{CC1} = 2.369 + 0.05385 \times f + 0.002448 \times f \times C_L$

$I_{CC2} = 3.857 + 0.05506 \times f + 0.007348 \times f \times C_L$

I_{CC1} and I_{CC2} are typical supply currents measured in mA; f is data rate measured in Mbps; C_L is the capacitive load on each channel measured in pF.

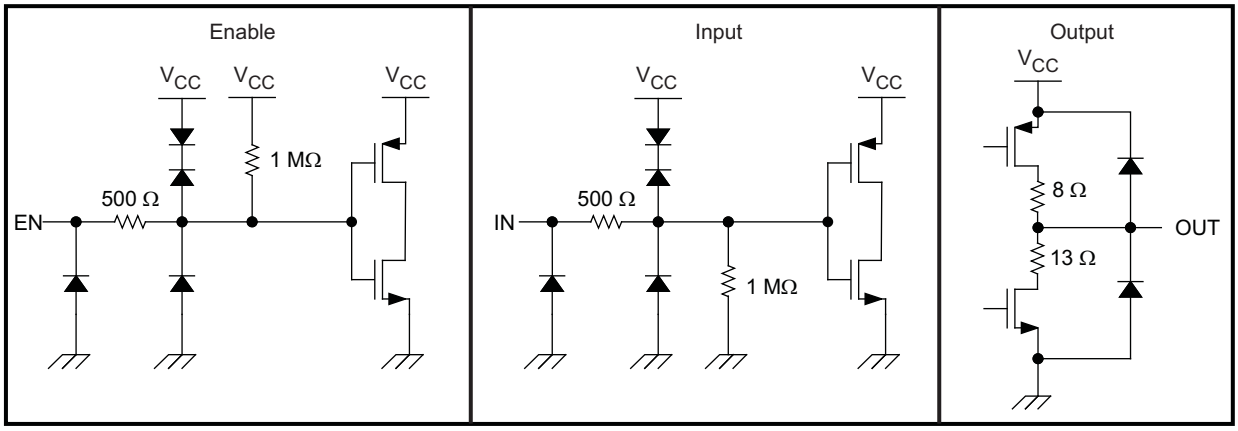


Figure 7. Device I/O Schematics

TYPICAL CHARACTERISTICS

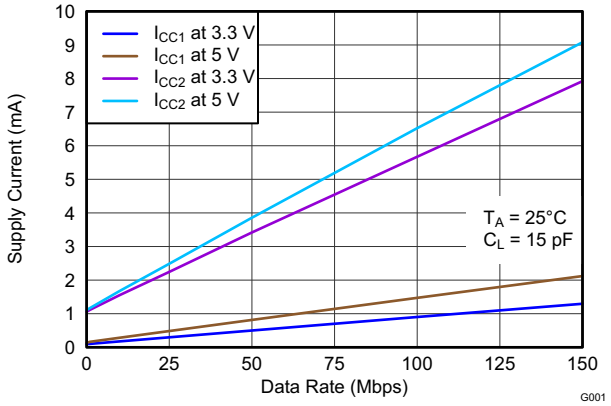


Figure 8. ISO7640FM Supply Current Per Channel vs Data Rate

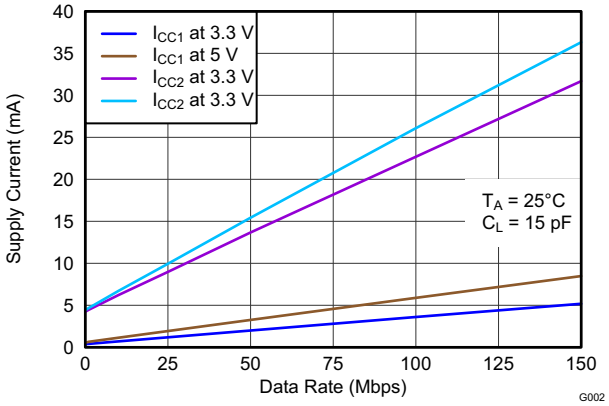


Figure 9. ISO7640FM Supply Current For All Channels vs Data Rate

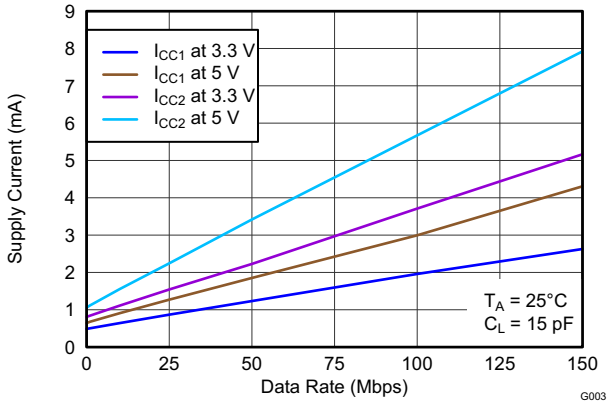


Figure 10. ISO7641FM Supply Current Per Channel vs Data Rate

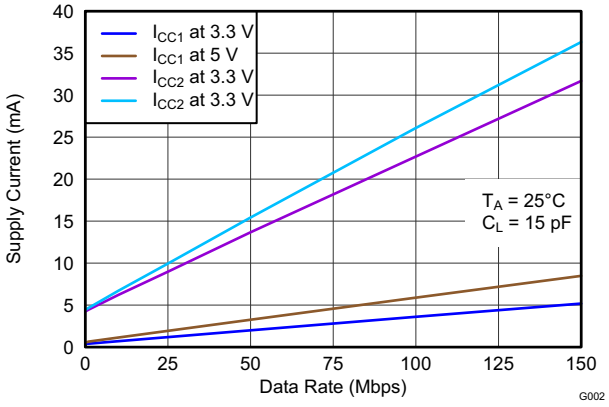


Figure .

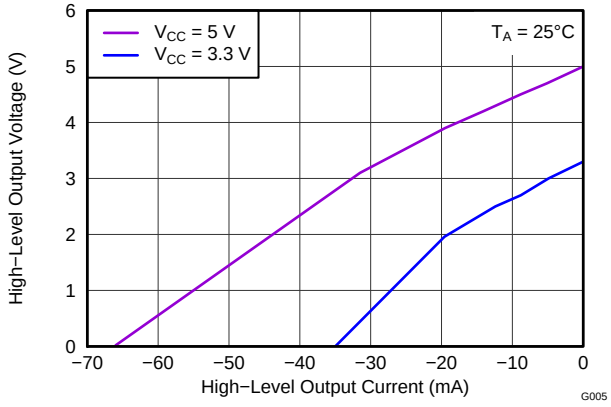


Figure 11. High-Level Output Voltage vs High-Level Output Current

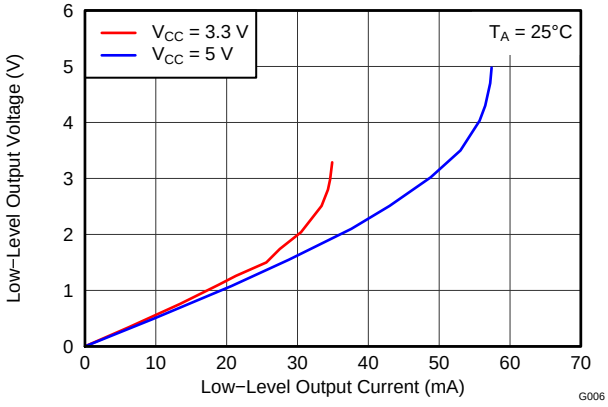


Figure 12. Low-Level Output Voltage vs Low-Level Output Current

TYPICAL CHARACTERISTICS (continued)

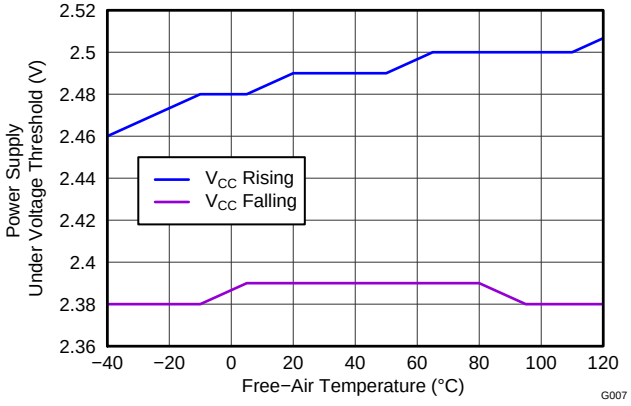


Figure 13. V_{CC} Undervoltage Threshold vs Free Air Temperature

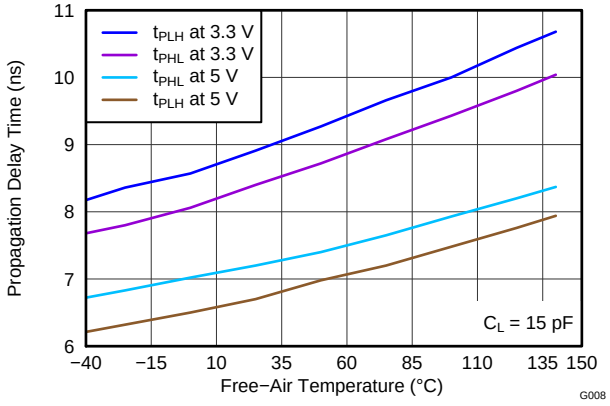


Figure 14. Propagation Delay Time vs Free Air Temperature

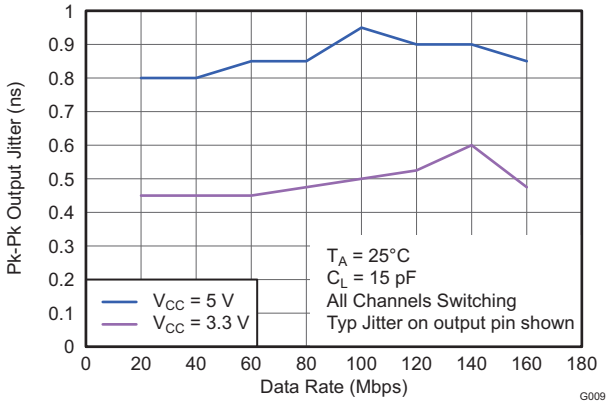


Figure 15. Output Jitter vs Data Rate

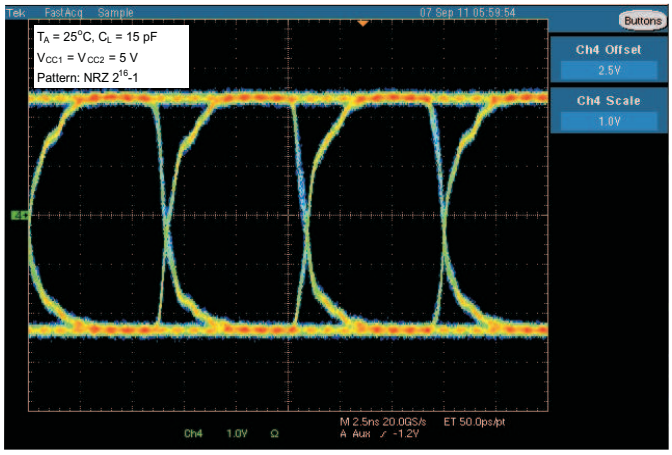


Figure 16. Typical Eye Diagram at 150 Mbps, 5 V Operation

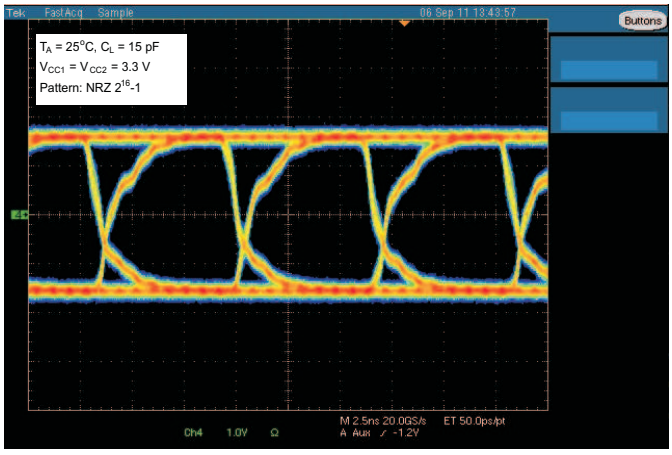


Figure 17. Typical Eye Diagram at 150 Mbps, 3.3 V Operation

REVISION HISTORY

Changes from Original (September 2011) to Revision A **Page**

- Changed Figure 3 - From: 0 V or V_{CC} To: IN = V_{CC} 15
- Added Note (1) "Per JEDEC package dimensions" to the IEC INSULATION AND SAFETY-RELATED SPECIFICATIONS FOR DW-16 PACKAGE table 16
- Changed L(I01) Min Value From: 8 mm To: 8.3 mm 16
- Changed L(I02) Min Value From: 7.8 mm To: 8.1 mm 16
- Added pinout for ISO7641 and ISO7631 to Figure 6 18

Changes from Revision A (October 2011) to Revision B **Page**

- Changed feature bullet From: ISO7641FC: 1.2 mA at 10 Mbps To: ISO7641FC: 1.3 mA at 10 Mbps 1
- Changed Safety and Regulatory Approvals bullet From: 6 KV_{PK} for 1 Minute per UL1577 and VDE (Pending) To: 6000 V_{PK} / 4243 V_{RMS} for 1 Minute per UL 1577 (pending) 1
- Changed Safety and Regulatory Approvals bullet From: To: 6000 V_{PK} / 4243 V_{RMS} for 1 Minute per UL 1577 (approved) 1
- Changed Safety and Regulatory Approvals bullet From: CSA Component Acceptance Notice 5A, IEC 60601-1 Medical Standard (pending) To: CSA Component Acceptance Notice 5A, IEC 60601-1 Medical Standard (approved) 1
- Changed all the ELECTRICAL CHARACTERISTICS tables 4
- Changed all the SWITCHING CHARACTERISTICS tables 4
- Changed the SWITCHING CHARACTERISTICS table ISO7640F and ISO7641F C-Grade values 5
- Changed the SWITCHING CHARACTERISTICS table ISO7640F and ISO7641F C-Grade values 7
- Changed the SWITCHING CHARACTERISTICS table ISO7640F and ISO7641F C-Grade values 9
- Changed the SWITCHING CHARACTERISTICS table ISO7640F and ISO7641F C-Grade values 11
- Changed the SWITCHING CHARACTERISTICS table ISO7640F and ISO7641F C-Grade values 13
- Changed the IEC 60664-1 Ratings Table 17

Changes from Revision B (December 2011) to Revision C **Page**

- Changed Safety and Regulatory Approvals bullet From: 6000 V_{PK} / 4243 V_{RMS} for 1 Minute per UL1577 (pending) To: 6000 V_{PK} / 4243 V_{RMS} for 1 Minute per UL 1577 (approved) 1
- Changed Description text From: The devices have TTL input thresholds and can operate from 2.7 V, 3.3 V and 5 V supplies. To: The devices have TTL input thresholds and can operate from 2.7 V (M-Grade), 3.3 V and 5 V supplies. 2
- Deleted the Product Preview Note From the Available Options Table 3
- Changed the ESD standards 3
- Changed UL in the REGULATORY INFORMATION Table From: File Number: E181974 (Approval Pending) To: File Number: E181974 17
- Changed the typical characteristics section 20

Changes from Revision C (January 2012) to Revision D **Page**

- Deleted devices: ISO7631FM, ISO7631FC, ISO7640FC, ISO7641FC from the data sheet 1
- Changed the Title From: Low Power Triple and Quad Channels Digital Isolators To: Low Power Quad Channels Digital Isolators 1
- Deleted devices from the Features List 1
- Changed the DESCRIPTION 1
- Changed EN1 and EN2 Pin Descriptions 2
- Deleted device from the Available Options Table 3
- Changed the ELECTRICAL, SWITCHING, and SUPPLY CURRENT CHARACTERISTICS tables 4
- Changed the ELECTRICAL, SWITCHING, and SUPPLY CURRENT CHARACTERISTICS tables 6
- Changed the ELECTRICAL, SWITCHING, and SUPPLY CURRENT CHARACTERISTICS tables 8
- Changed the ELECTRICAL, SWITCHING, and SUPPLY CURRENT CHARACTERISTICS tables 10
- Changed the ELECTRICAL, SWITCHING, and SUPPLY CURRENT CHARACTERISTICS tables 12
- Deleted devices from the TYPICAL SUPPLY CURRENT EQUATIONS section 19
- Changed the TYPICAL CHARACTERISTICS section 20

Changes from Revision D (July 2012) to Revision E **Page**

- Changed Z to Undetermined in the OUTPUT (OUTx) column of the FUNCTION TABLE 2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
ISO7640FMDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7640FM	Samples
ISO7640FMDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7640FM	Samples
ISO7641FMDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7641FM	Samples
ISO7641FMDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7641FM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

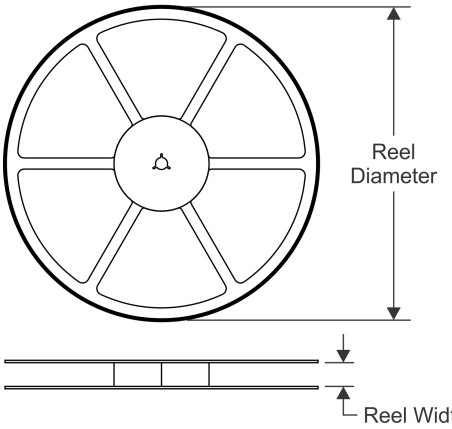
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

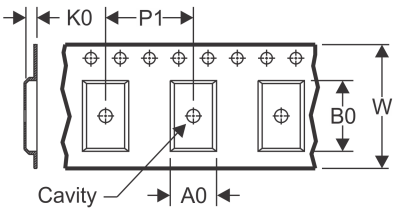
(4) Only one of markings shown within the brackets will appear on the physical device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

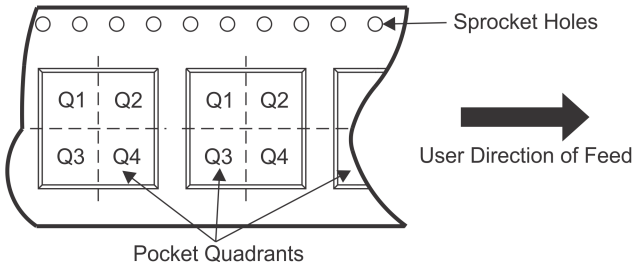


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

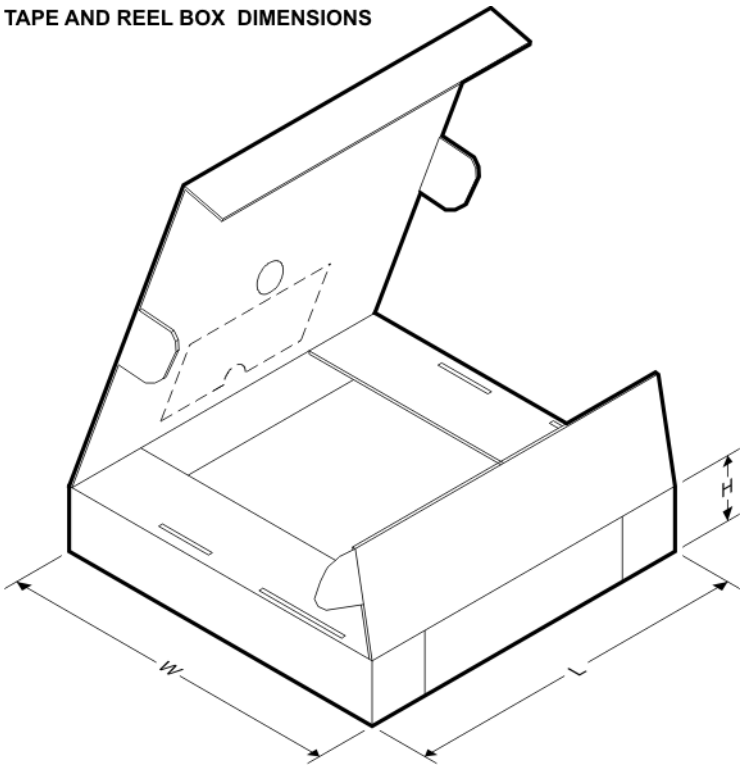
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7640FMDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7641FMDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

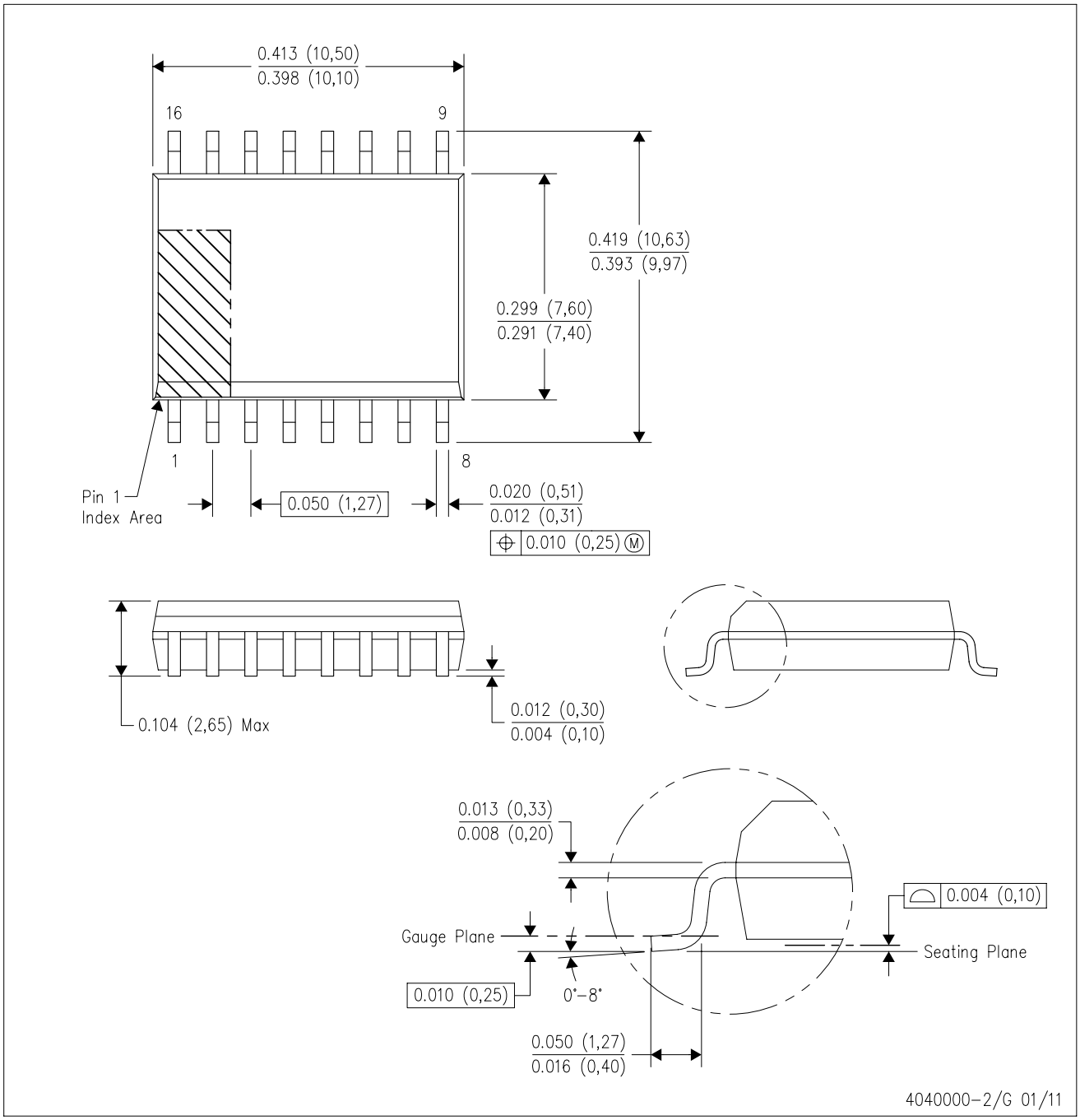
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

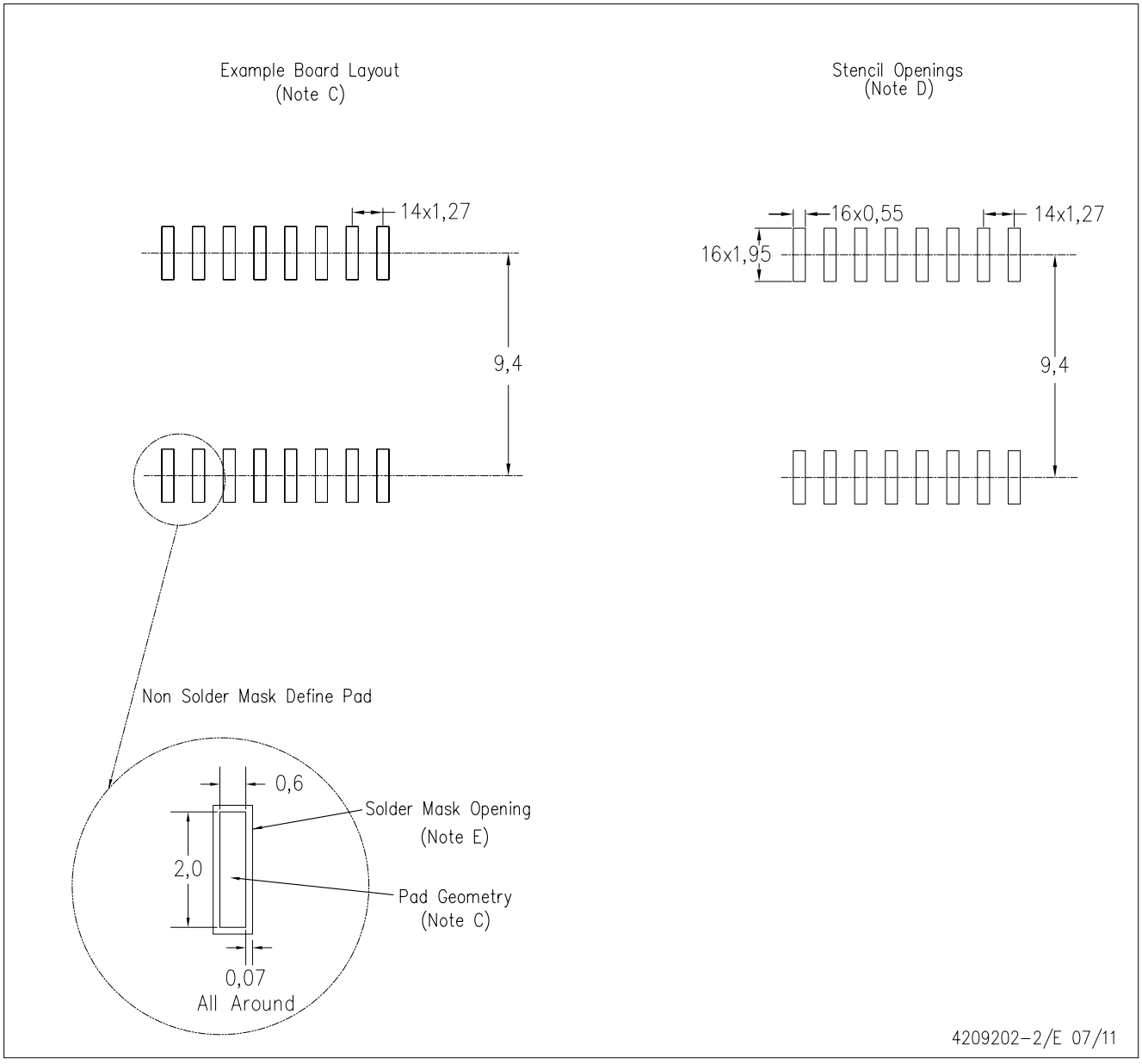
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7640FMDWR	SOIC	DW	16	2000	367.0	367.0	38.0
ISO7641FMDWR	SOIC	DW	16	2000	533.4	186.0	36.0

DW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AA.

DW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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