

TV VERTICAL OUTPUT CIRCUIT

The KA2131 is a monolithic integrated circuit designed for the vertical output stage in color television receivers.

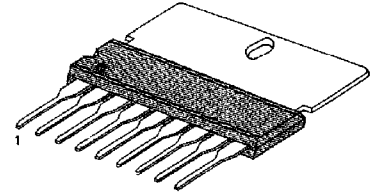
FUNCTIONS

- Driver stage.
- Output stage.
- Flyback generators.
- Pulse shapers.

FEATURES

- Low power consumption, direct deflection coil driving capability (Flyback voltage is two times as high as the supply voltage is supplied during flyback period only).
- High breakdown voltage: 60V.

9 SIP H/S



ORDERING INFORMATION

Device	Package	Operating Temperature
KA2131	9 SIP H/S	-20 ~ +70°C

BLOCK DIAGRAM

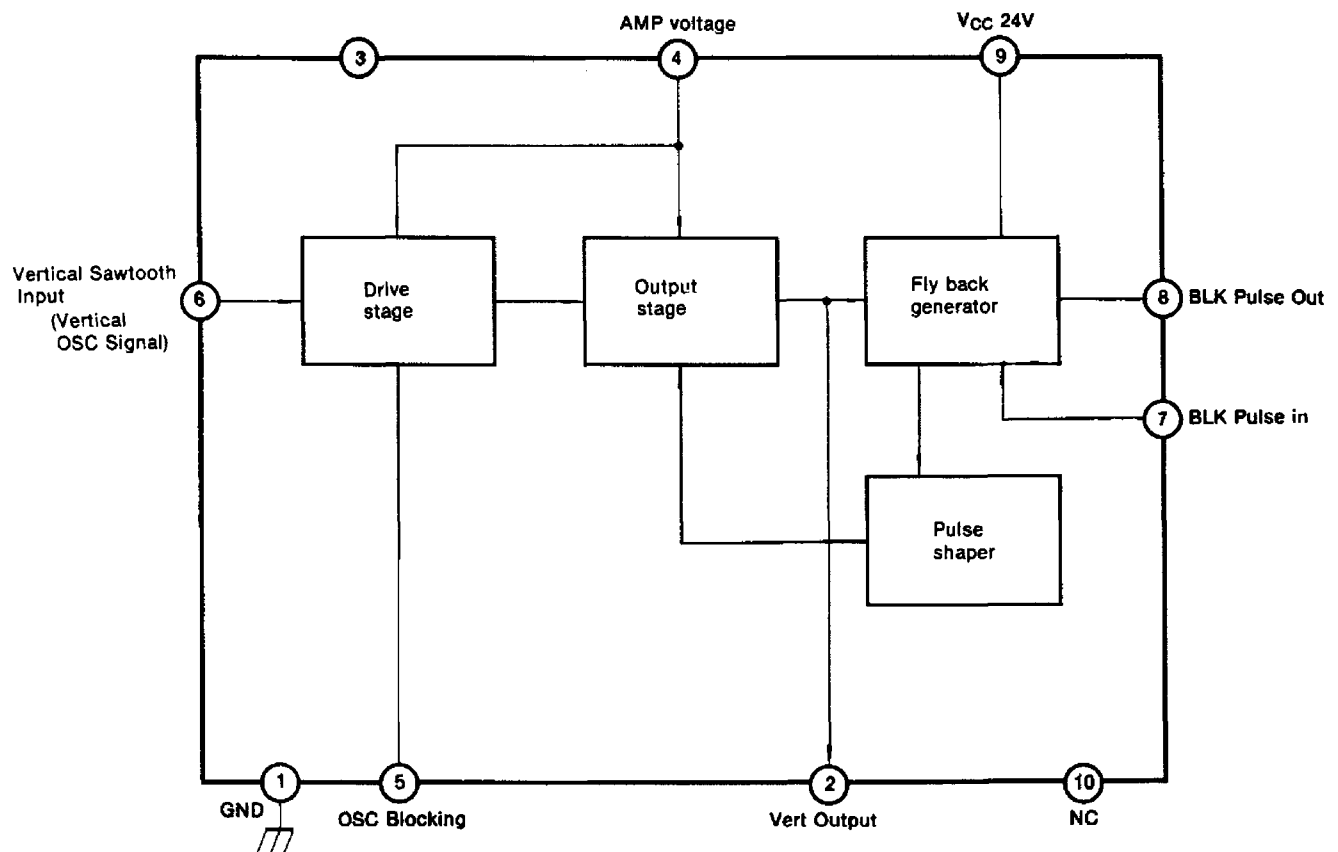
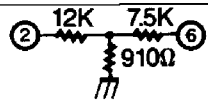


Fig. 1

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	27.6	V
Circuit Voltage	V_4	60	V
	V_6	2.5	V
	V_7	1.3	V
Supply Current	I_{CC}	250	mA
Power Dissipation	P_D	6.66	W
Circuit Current	I_2	- 1000 ~ + 1000	mA _{P-P}
	I_8	- 1000 ~ + 1000	mA _{P-P}
Operating Temperature	T_{OPR}	- 20 ~ + 70	°C
Storage Temperature	T_{STG}	- 55 ~ + 150	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Deflection Current	I_{Y-P-P}	SW:2	860	930	1000	mA _{P-P}
Deflection Current Linearity	$\Delta I_Y (+)$	SW: 1	25	—	75	mA _{P-P}
	$\Delta I_Y (-)$	SW:1	22	—	85	mA _{P-P}
Deflection Current vs. Operating Temperature	$\Delta I_Y/T_A$	$T_a = -20 \sim +70^\circ\text{C}$	-1.5	—	1.5	%
Center Voltage	V_{MID}	SW: 1	12.1	12.6	13.1	V
Flyback Pulse Amplitude	$V(\text{FBP})$	SW: 1	47			V
Flyback Pulse Width	t_{FBP}	SW: 1	850	920	980	μsec
Quiescent Circuit Current	I_{CO}	$V_4 = 24\text{V}$ $V_9 = 24\text{V}$ $V_7 = 0\text{V}$ 	7	13	22	mA
Output TR Saturation Voltage	V_{4-2}	$V_4 = V_9 = 24\text{V}$, $\text{pin}_{2-1} = 56\Omega$ $V_6 = 0.3\text{V}$, $V_7 = 0\text{V}$	—	2.7	3.7	V
	V_2	$V_4 = V_9 = 24\text{V}$, $\text{pin}_{2-4} = 56\Omega$ $V_6 = 1.3\text{V}$, $V_7 = 0\text{V}$	—	0.6	1.0	V
Saturation Voltage	V_8	$V_9 = 24\text{V}$, $R_{\text{pin}_{9-8}} = 1.2\text{K}\Omega$ $V_7 = 0\text{V}$	—	—	0.5	V
Thermal Resistance	$R_{\text{TH (J-C)}}$		—	—	12	°C/W

TYPICAL APPLICATION CIRCUIT

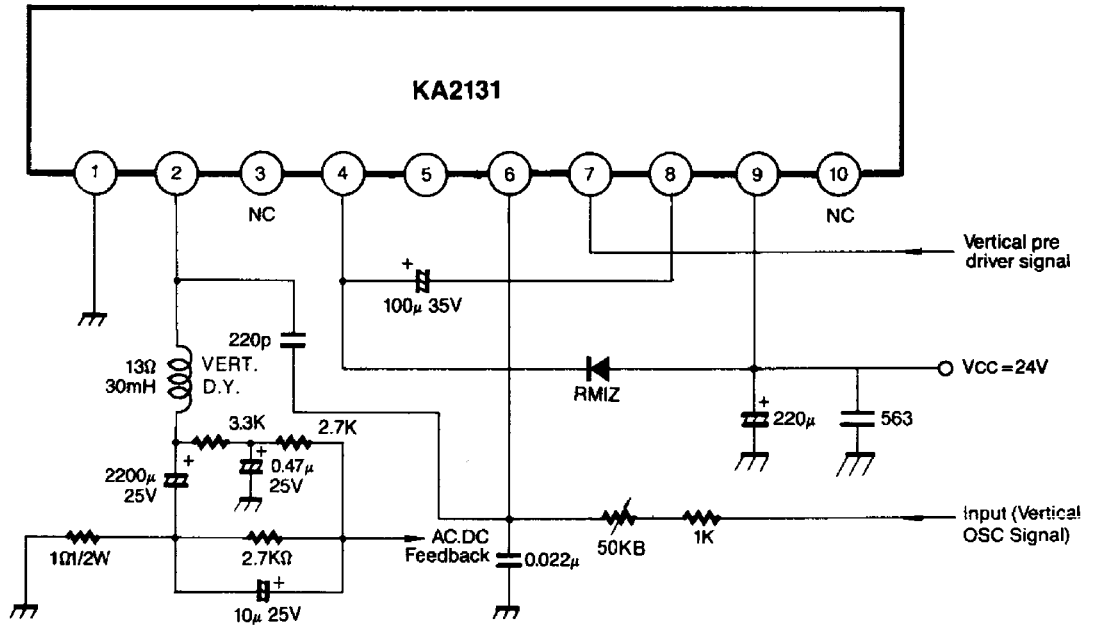


Fig. 2

TEST CIRCUIT

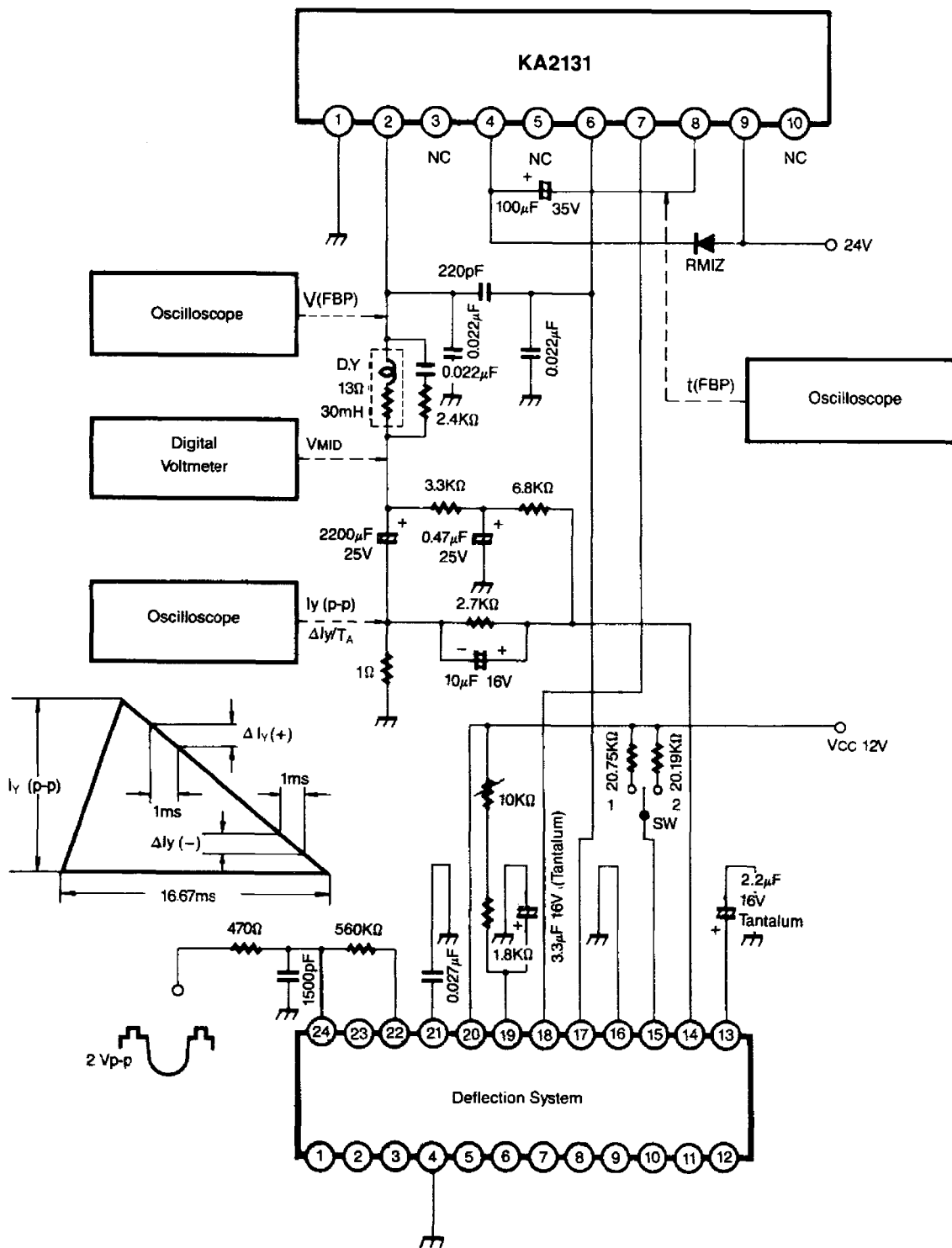


Fig. 3