
Chapter 1

Introduction to KS9245 ATAPI Automated CD-ROM Controller

1.0 Introduction

The KS9245 is a high performance single-chip CD-ROM decoder with an ATAPI interface. The KS9245 integrates a Buffer Manager which supports a high performance 16-bit DRAM interface, CD-ROM decoder, ECC engine, microcontroller interface, and ATAPI host interface logic. The chip decodes CD-ROM media according to the Sony-Philips® CD-ROM, CD-DA™, CD-ROM/XA, CD-I and CD Enhanced formats, and is designed for operation in a cost effective CD-ROM drive system with industry standard DRAMs, DSPs, and microcontrollers. The KS9245 has sufficient data rates to support up to 50X speed CD-ROM drives which can be daisy-chained to a hard drive through the IDE/ATA interface. Thus, the KS9245 will continue to promote the CD-ROM drive as a new standard device in multimedia PCs.

The Host Interface logic supports ATAPI protocols and handles ATAPI packet commands all from hardware to maximize system performance and reduce firmware overhead. The ATAPI Command and Control Block registers are included in the KS9245's register set, allowing both the host and local microcontroller access. The KS9245 supports PIO modes 3 and 4, DMA modes 1 and 2, and UltraDMA modes 1 and 2, allowing for super fast host transfers. In addition, the KS9245 also supports command overlapping to prevent the slower CD-ROM drive from becoming a bottleneck at the system level when daisy-chained to a faster EIDE/ATA device.

The Buffer Manager controls data flow between the host and a CD DSP. The buffer manager supports Fast Page Mode and EDO DRAMs for high performance application. The buffer manager is programmable and provides all the necessary address and control signals for up to 512K bytes of DRAM. Additionally, the Buffer Manager provides up to 42 MB/sec memory bandwidth with Fast Page DRAM and up to 80 MB/sec with EDO DRAM for host transfers such as PIO mode-3/4 and high speed CD-ROM data access.

The KS9245 uniquely integrates and automates the ATAPI sequences, CD Cache Manager, DRQ Packet handler and Scatter/Gather features. This allows Multiple Block Transfers of up to 1024K bytes in single burst and auto data transfers up to 128M bytes. The entire data transfer for ATAPI Read, and Read CD commands are completely processed by the KS9245 without firmware intervention. As a result, low CPU utilization is achieved in high speed CD-ROM applications.

The CD-DA copy and audio data buffering is supported for audio application. The raw P-W subcode buffering and Q-subcode de-interweaving with CRC check are automated in the KS9245. The audio playback in CAV mode is fully supported by KS9245. With superior CD-DA concatenated techniques and Audio Hardware Buffer Manager, the KS9245 guarantees that the audio data can be played without losing audio frames during CAV playback.

The microcontroller Interface supports high speed, low cost Intel® and Motorola® microcontrollers, such as the 8051 or 68HC11. It supports multiplexed address and data buses. Thus, external glue logic previously required may be removed and system cost minimized. For further flexibility, four general purpose I/O pins are provided by the KS9245, which may be used for various control purposes, such as tray and volume control, etc.

1.0.1 Features Summary

- **General**

- Fully compatible with ATAPI Specification SFF-8020i.
- ATAPI command and control registers contained in the KS9245 register set.
- Automatic power-down on interfaces when idle.
- Supports up to 50X CD-ROM drive.
- 0.5 micron, low-power CMOS technology.
- 100-pin PQFP package.
- low power consumption 0.6W typical.
- System Clock running at 33.868 / 50.8 MHz.

- **Buffer Manager**

- Advanced CD Cache Manger for low CPU utilization rate and auto data transfer.
- Advanced priority arbitration scheme to maximize buffer bandwidth for all requests.
- Multiple Block Transfer Up to 1M bytes.
- Auto data transfer for Read, Read CD command Up to 128M bytes.
- External 16-bit wide DRAM supports up to 512K-bytes with EDO option.
- Supports both physical or block addressing modes for microcontroller DRAM access.
- Scatter/Gather host transfer for Read CD command.
- Up to 42 MB/sec buffer bandwidth with Fast Page DRAM.
- Up to 80 MB/sec buffer bandwidth with EDO DRAM.
- Up to 64 K bytes direct host transfer for TOC data.

- **ATAPI Host Interface**

- Support Industry Standard UltraDMA Mode 0, 1 and Mode 2.
- True real-time hardware/firmware ATAPI compatibility.
- Hardware implementation of ATAPI packet command receiving.
- Automated ATA shadow command process.
- Automated ATAPI Signature response.
- Automated protocol control on block transfers for ATAPI read commands.
- Automated command completion control for all ATAPI commands.
- Automated DRQ Packet handler to obtain the best CPU utilization.
- Hardware Service/Release process for overlap command.
- Supports PIO modes 3 and 4 bus transfer rate.
- Supports DMA modes 0, 1 and 2 transfer rate.
- Provision for daisy-chaining two ATA/IDE or ATAPI-embedded drives.
- Supports automatic DASP handshake based on master or slave mode.

- **CD-ROM DSP interface**

- Supports Sony-Philips® CD-ROM, CD-DA™, CD-I and CD Enhanced formats.
- Supports various compact DSP controllers such as Philips, Toshiba, Sanyo, Matsushita.
- Supports erasure correction up to 2 errors per Codeword.
- Supports P,Q correction up to 1 error per Codeword.
- Repeated error correction support.
- On-The-Fly™ EDC correction up to 50X data rate.
- C2PO error flags, Raw subcode, and CD-DA buffering support.
- Supports automatic sync pattern search and protection for DRAM data.
- Sector header validity check done by hardware during data transfer.
- Supports real-time de-interleaved Q-subcode buffering and CRC error checking.

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- Supports serial DSP programming interface.
 - CD-to-DSP data transfer rates up to 50X drive speed.
 - Audio Playback in CAV Mode support.

- **Microcontroller Interface**

- Supports high speed Intel® and Motorola® microcontrollers, such as 8051 & 68HC11.
- Supports multiplexed address and data buses.
- Supports separate host/buffer and disk interrupt signals.
- Four General Purpose I/O pins are provided.
- Interrupt or polled-microcontroller interface.
- Automatic power-down when idle; automatic power-up when command is received.
- Direct register access to facilitate low CPU utilization.

1.0.2 Description of Block Diagram

There are six key functional blocks integrated in the KS9245:

- 1) CD-ROM DSP Interface
- 2) Buffer Manager
- 3) Host Interface
- 4) Microcontroller Interface
- 5) ECC Data Corrector
- 6) EDC-CRC Checker.

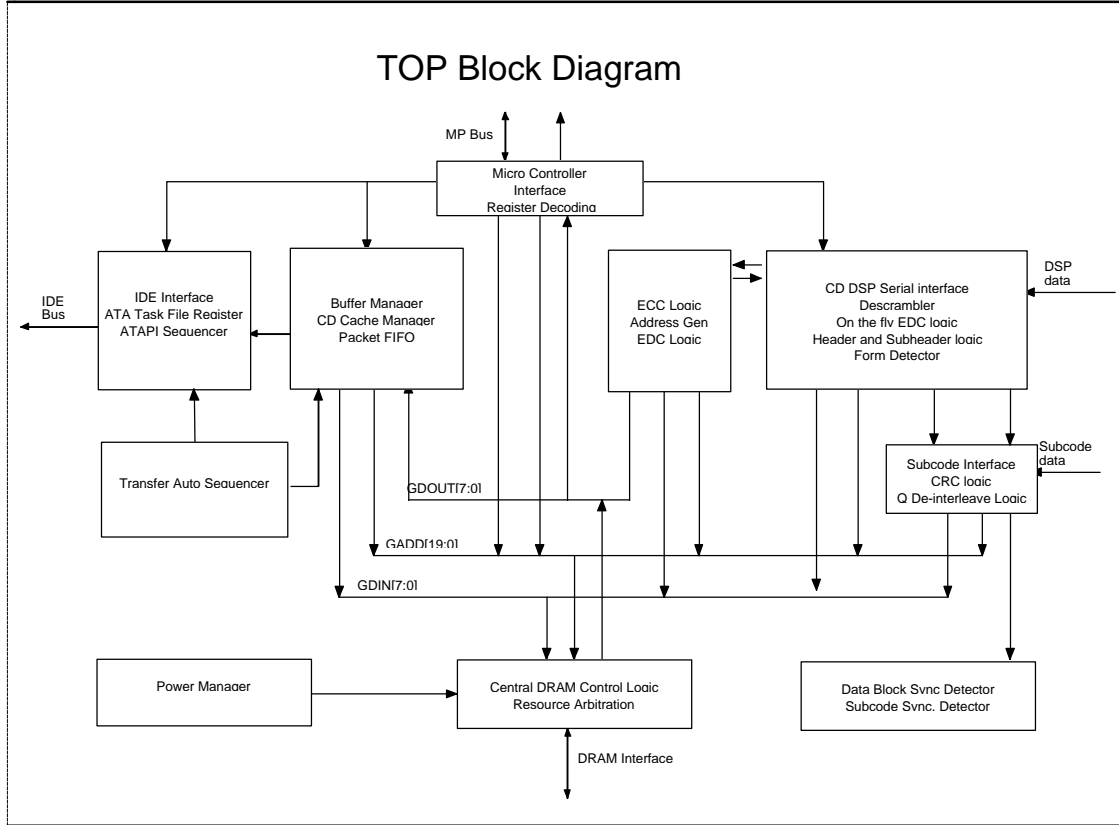
The CD-ROM DSP Interface logic performs sync-mark detection and insertion for CD-ROM sector synchronization. After descrambling and assembling data from the CD-DSP, the KS9245 sends the data through the On-The-Fly-EDC™ EDC Data Checker before storing the data into buffer DRAM.

The On-The-Fly-EDC™ logic then verifies the CD-DSP incoming data stream. If an error is encountered, the On-The-Fly-EDC™ logic invokes the ECC logic to correct the error. If no error is encountered, the ECC logic remains idle.

The ECC Correction Code circuit performs CIRC Error Correction on each data block. The EDC-CRC Checker then performs a cyclic redundancy check on the corrected data. All ECC correction, including erasure pointer correction, are done in real-time without microcontroller. This reduces firmware overhead and complexity, and minimizes microcontroller performance requirements.

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1.0.3 KS9245 Functional Block Diagram



The Buffer Manager controls the data flow between the IDE and DSP interfaces. These interfaces store and retrieve data to / from the external DRAM buffer memory using interleaved access cycles.

The Host Interface supports ATAPI protocol, and provides the control for the corrected data to be transferred from the DRAM to the host CPU. Diagnostic data can be transferred from the host CPU to the DRAM to allow testing of the ECC, EDC, and Host Interface logic.

The Microcontroller Interface logic allows the KS9245 to be controlled by the microcontroller through an 8-bit bus. The chip also provides registers and control functions for transferring data between the microcontroller and DRAM through Microcontroller Interface.

1.1. Functional and Features Description

1.1.1 Microprocessor Interface Functional Descriptions

- **Intel and Motorola microprocessor interface support**

The KS9245 supports both Intel and Motorola type microprocessor interfaces with multiplexed addressing mode. In this mode, the microprocessor address and data lines are shared in AD0-7 pins. Addresses are latched on the trailing edge of the ALE signal. The RDB/WRB pins are used as read and write strobes respectively. Supporting both Intel and Motorola type microprocessors directly enhances the flexibility of the KS9245.

- **Combined host/buffer and disk interrupt circuit**

The KS9245 supports host/buffer interrupts via the HINTB pin and decoder/disk interrupts via the DINTB pin. Using separate interrupt signals, the interrupt priorities are easily realized. This increases the real-time firmware processing capabilities for high speed CD-ROM applications.

Also, all interrupts can be combined onto the HINTB pin by clearing the *IntMode* bit in the *Interface Configuration Control Register* (0Bh, bit 7). When power-on or reset occurs, the combined interrupt on the HINTB pin is the default configuration.

The host/buffer interrupt includes host command received, reset, or data transfer completed interrupts. The decoder interrupt includes CD decoder or subcode interrupts. The interrupt status is reported in the *Host Interrupt Status Register* (10h) and the *Decoder Interrupt Status Register* (11h).

Both HINTB and DINTB are active low, level triggered signals. With the organized interrupt control in the *Host Interrupt Clear/Mask Register* (10h) and *Disk Interrupt Clear/Mask Register* (11h), the firmware is ensured of obtaining interrupts without accidentally clearing or disabling of the interrupts. As a result, reliability of real-time process is achieved.

Polling mode for interrupt processing is also supported in the KS9245 by clearing the mask bits in *Host Interrupt Mask Register* (10h) and *Disk Interrupt Mask Register* (11h).

- **Direct register access from microprocessor**

The KS9245 supports direct register accesses. Normally, no external glue logic is required to use this feature. Using direct register access, firmware overhead is minimized and system performance enhanced.

- **General purpose IO pins support**

Four General purpose I/O pins are supported in the KS9245. They are the GPIO0-3 pins. Also, these pins are shared with Audio Output pins AWCK/ABCK/ADAT. When the APCE bit in the *Global Configuration Register* (2F, Bit 3) is set, these pins are configured as general purpose Input or Output functions. These pins can be configured as Input or Output by programming the *Port Control Register* (44h, Bit 7, Bit 6, Bit 5, Bit 4). These pins may be used for Eject, CD tray, and volume, etc. controls without external glue logic.

- **Power Management/Auto wake-up support**

The Sleep Mode power management is supported by KS9245. In this mode, the Decoder, Buffer Manager, and host interface circuits are in power savings mode. During Sleep Mode, the buffer DRAM contents are sustained by the KS9245's internal refresh logic and the ATA Task File Registers are available to the host. The Sleep Mode is enabled by setting *SSleep* bit in *Global Control Register* (2Fh,

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Bit7). Sleep Mode will automatically wake up and switch into the normal operation mode if the host has written a command to the *ATAPI Command Register* (07h) or ATA Reset occurs. The auto wake up is performed transparently and automatically. The Sleep Mode can only be applied when there is no host transfers and the decoder is in Stop Mode. Thus, the KS9245's power management features provides good solutions for power restricted environments.

1.1.2 ATAPI Host Interface Functional Descriptions

The ATAPI interface logic is completely automated. The KS9245 can receive the ATAPI Packet Command and store the 12-byte command packet in a Packet FIFO. During data transfer stage, the ATAPI transfer protocols are processed by KS9245 without firmware intervention. When the total number of host requested blocks are transferred, the ATAPI command completion is posted if automatic command completion is enabled.

- **Automated DASP handle to increase Master/Slave Compatibility**

The KS9245 will assert the DASP pin of the ATA interface signals in the slave mode when Power-on Reset, Hardware Reset, or ATA SRST command is received. By asserting the DASP pin, it allows the master drive to identify the existence of the KS9245 as a slave drive. In some cases, the DASP signal is sampled by master drive as soon as the above event occurs. If the DASP signal does not assert fast enough, some master drives cannot recognize the existence of the slave drive. This feature is provided to insure the most compatibility in the Master/Slave handshaking sequence. The master or slave drive is configured by the MSTB pin. The KS9245 will sample this pin when the above events occur. If the KS9245 is configured as a master drive, the PDIAGB and DASP signals will be negated and left the slave drive to control these signals. Additionally, the PDIAGB and DASP pins can be asserted or negated by setting *SetDASP*, *SetPDIAGB*, *ClrDASP*, *ClrPDIAGB* bits in *Host Interface Control Register* (0Ah, bit 6,5,2,1). The microprocessor can read *DASP* and *PDIAGB* bits in the *Host Interface Signal Value Register* (0Ah, bit 2, 1) to get the values of the DASP and PDIAGB signals of the ATA interface.

- **Automated ATAPI Signature process**

The ATAPI Signature is the required information for host to identify an ATAPI device. The ATAPI Signature is reported in the *ATAPI Byte Count Registers* (04h, 05h) as 14h/EBh. The KS9245 will initialize the ATA Task File Registers and setup the ATAPI Signature automatically. Moreover, the KS9245 supports the ATAPI Signature for ATA Read and ATA Identify commands. The ATAPI Signature is reported and command abort sequence will be posted by the KS9245 if the shadow feature is enabled.

- **Automated Packet Command Receiving**

The KS9245 will process the ATAPI Packet Command (A0h) and receive 12-byte command packet after host has written the command packet into the ATAPI Data Register. The 12-byte command packet is stored in a Packet FIFO. The firmware is able to retrieve 12-byte command packet by consecutively reading the *Packet FIFO Register* (00h). The 12-byte Packet FIFO is protected from over-run if more than twelve bytes have written. Also, the data pointer of the Packet FIFO is reset whenever a new ATAPI command is received. The Packet Command Interrupt mode assertion of the INTRQ line with the assertion of command packet DRQ is supported. This is enabled by setting the *PcmdInt* bit in the *Interface Configuration Control Register* (0Bh, bit 1).

- **Automated DRQ Packet Handle**

The KS9245 is able to calculate the transfer byte count and load it into the *ATAPI Byte Count Registers* (04h, 05h) when host transfer occurs. Moreover, the KS9245 will break the block-oriented transfers in the Buffer Manager into byte-oriented transfers in the ATAPI interface without firmware intervention. Before a DRQ packet transfer starts, the ATAPI Byte Count Registers are calculated and the ATAPI data transfer protocol are processed by the KS9245.

- **Automated BSY bit handle**

The *BSY* bit of ATAPI Task File Register is controlled by KS9245. It ensures that the protocol is in compliance with the ATA Specification. Using this feature, the firmware is assured to be compatible with the Win 95/OS2/Win NT Operating Systems.

Also, the *BSY* bit can be set or cleared by firmware as manual mode by setting *SetBSY* or *ClrBSY* bits in *Host Interface Control Register* (0Ah, bit 7, 3), respectively.

- **Automated DRQ bit handle**

The *DRQ* bit in ATAPI Status Register is automated by the KS9245. The *DRQ* bit in the ATAPI Status Register is set automatically where appropriate.

- **Automated DSC bit handle**

The *DSC* bit in the ATAPI Status Register is fully automated. This is used to post overlap seek command completion. This sequence starts by setting the *SDSC* bit in the *Host Sequence Command Register* (0Eh, bit 0).

- **Automated command completion handle**

The command with either Successful or Error Completion sequence is supported by the KS9245. The sequence starts by setting the *SCpl* or *SCplChk* bits in the *Host Sequence Command Register* (0Eh, bit 2, 1) for ATAPI error or successful conditions, respectively. Also, the automated command completion is extended into data transfers. With the completion of an entire host transfer, the ATAPI completion status is posted to the host if the *ACplE* bit in the *Transfer Sequence Command Register* is set (0Fh, bit 6).

- **ATAPI Overlap Command - Service/Release support**

Overlap command operations are supported by the KS9245. The ATAPI Release and Service protocols are implemented by the KS9245. The Release sequence starts by setting the *Srelease* bit in the *Host Sequence Command Register* (0Eh, Bit 4). The Service sequence starts by setting the *Sservice* bit in the *Host Sequence Command Register* (0Eh, Bit 5). Both interrupts on Release or Service can be disabled by setting the *DisSerInt* or *DisRelInt* bits in the *Host Interface Diagnostic Control 2 Register* (51h, bit 7, 6).

- **Automated ATA Shadow command support**

The shadow command is used when the drive is in the master mode and there is no slave drive connected. The KS9245 will abort the command without firmware intervention when the host has issued the command to a non-existent slave drive. The sequence is enabled by clearing the *DisShaR* bit in the *Interface Configuration Control Register* (0Bh, bit 2) when the *CDRV* bit is cleared (0Bh, bit 4) and the *SShadow* (0Bh, bit 3) bit is set in the *Interface Configuration Control Register*.

1.1.3 Buffer Interface/Manager Functional Descriptions

The CD Cache Manager is supported by hardware in the KS9245. With the automated and integrated architecture, the data transfers for entire Read and Read CD command are achieved. The Buffer Manager state machine will monitor the buffer block count. The maximum number of blocks that can be automatically transferred is 64K blocks, or about 128M bytes. With the powerful DRQ packet handling of the KS9245, the host transfers are realized with very high performance. As a result, low CPU utilization for high speed CD-ROM is achieved and code size minimized. The KS9245 supports up to 512K bytes of 16-bit Fast Page mode and EDO (Extended Data Output) DRAMs. The CD data block are organized in either 2.5K bytes or 3K bytes per block. The CD data and subcode can be chosen to be buffered in both configurations. In the latter case, the buffering for C2PO error flags and Block Error flags are included.

All data blocks are linearly arranged without separating as auxiliary or data block. With the straight addressing mechanism, firmware overhead and programming mistakes are minimized.

- **Multiple Block Transfer support**

Multiple Block Transfer is supported by the KS9245. The transfer block is specified in the *Current Host Transfer Block Length Registers* (18h, 19h). For Multiple Block Transfers, up to 256 blocks, or 512K bytes, can be burst to the host without firmware intervention. In the ATAPI specification, the maximum host transfer in a single DRQ packet is 64K bytes. The KS9245 will send the maximum number of bytes in a DRQ packet transfer.

- **Automated transfer for entire Read command**

The KS9245, with its advanced hardware CD Cache Manager, supports host transfers for entire Read or Read CD commands of up to 64K blocks, or 128M bytes, without firmware intervention. When the *ACache* bit in the *Transfer Sequence Command Register* (0Fh, bit 7) is set, the CD Cache Manager is enabled. At the completion of the total transfers specified in the *Total Host Transfer Block Length Registers* (16h, 17h), the ATAPI completion status will be posted to the host if the *ACPIE* bit in the *Transfer Sequence Command Register* (0Fh, bit 6) is set. Also, the *TxfrDone* bit in the *Host Interrupt Status Register* (10h, bit 7) will be set and a microprocessor interrupt will be generated if the *TxfrDoneE* bit in the *Host Interrupt Mask Register* (12h, bit 7) is set.

- **Scatter/Gather Support**

The KS9245 provides two sets of segment registers which specify the start offset address and the transfer byte lengths within a data block. When the transfer is completed in the first segment, the hardware will automatically chain the second segment and continue the host transfers. The advantage to using Scatter/Gather feature is to avoid breaking transfer into two or more sub-transfers if data is scattered within a block. Two segment registers are specified in the *Transfer Offset Length Low/High 1/2* (1Eh, 1Fh, 22h, 23h) and *Host Block Offset Address Low/High 1/2 Registers* (1Ch, 1Dh, 20h, 21h). In a Read CD command, the host requested data may not be in a contiguous location. For example, the 2048-byte data block and 294-byte C2PO error flags are requested in the same transfer. The firmware can utilize this Scatter/Gather feature to chain these transfers together.

- **CD Cache Manager**

A hardware CD Cache Manager is supported in KS9245. When the *ACache* bit in the *Transfer Sequence Command Register* (0Fh, bit 7) is set, the CD Cache Manager initiates the host transfer as soon as data is available in the cache. That is, the *Valid Cache Block Count Registers* (14h, 15h) are not equal to zero, until the *Total Host Transfer Block Length Registers* (16h, 17h) is decreased to zero. The host transfer process is continuously monitored by hardware until all data are transferred.

- **Block Address support**

All data blocks can be addressed by a sequential block number which starts from zero at the top of the buffer DRAM and ends at the last or bottom of the block address specified in the *Buffer Bottom Block Address Register* (2Ch). Before starting host transfers, the *Host Transfer Block Address Low/High Registers* (1Ah, 1Bh) must be loaded with the starting block address. Before starting the decoder transfers, the *Disk Transfer Block Address Register* (38h) must be loaded with the starting block address. Both host and disk address pointers are automatically increased by one when a block of data is transferred to host or from the disk. When these registers reach the values of *Buffer Bottom Block Address Register* plus one, they are wrapped around to the top of the buffer DRAM.

- **Microprocessor Physical and Block access DRAM support**

Both the physical and block addressing modes for accessing DRAM by the microprocessor are supported. The *PAMb* bit in the *Buffer Access Control Register* (29h, bit 2) is used to specify the addressing mode. Using Physical Address Mode (PAM), the DRAM physical address must be loaded into

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the *MP Access Physical Address LSB/MID/MSB registers* (24h, 25h, 26h). This mode is used for accessing the firmware variables such as TOC data in the System Area. Using Block Address Mode (BAM), the block and offset addresses must be loaded into the *MP Block Address Register* (26h) and *MP Block Offset Low/High Address Registers* (24h, 25h). This mode is used to access data within the CD by the KS9245. This allows the firmware to easily check the contents of the data block, such as Sync Pattern, without converting the block address into a DRAM physical address. The DRAM read or write operation will be initiated when the *SDramRd* and *SDramWrt* bits are set in the *Buffer Access Control Register* (29h, bit 0, 1), respectively. The data for read operations will be available in the *MP Access Data Port Register* (28h) after the *DramBsy* bit of the *Buffer Access Control Register* is cleared (29h, bit 7). The data for write operation must be loaded into the *MP Access Data Port Register* (28h). The write operation will be completed when the *DramBsy* bit of the *Buffer Access Control Register* is cleared (29h, bit 7).

- **Segmented Buffer support**

The buffer DRAM is partitioned into two segments: The Data and System areas. The Data area, is used for storing the CD data block as cache area while the System area is for storing CD system information such as TOC data, Identify device information, Inquiry data, and firmware variables. The System area starts below the last byte of the bottom of the block address which is specified in the *Buffer Bottom Block Address Registers* (2Ch, 2Dh). Therefore, the size of the System Area can be adjustable by setting the *Buffer Bottom Block Address Registers* (2Ch, 2Dh).

- **Up to 64K bytes direct transfer from DRAM**

Host transfers from the System Area is not limited to block boundaries. Up to 64K bytes can be directly transferred from the buffer DRAM to the host. This allows the TOC (Table of Contents) data to be transferred without the limitation of the 2.5K-byte or 3K-byte block boundary. This avoids having to break a transfer into multiple sub-transfers. As a result, the firmware can support the TOC efficiently and code size is reduced. By setting the *Transfer Offset Length Low/High 1/2 Registers* (1Eh, 1Fh, 22h, 23h) with the desired transfer length, the transfer will not complete until the total number of bytes specified in these registers are transferred.

1.1.4 CD Decoder Interface/Manager Functional Descriptions

The KS9245 supports various DSP devices such as Toshiba, Sony, Sanyo, and Matsushita by setting the *DSP Device Type Selection Register* (3Eh). Also, various subcode interface such as Philips V4, EIAJ1 and EIAJ2 can be programmed by setting *Subcode Device Type Selection Register* (42h).

The main DSP data, C2PO error flags, and subcode buffering are supported by setting the *DSP Channel Sel* bit in the *Buffer Configuration Control 1 Register* (2Ah, bit 6, 4, 5). Moreover, the KS9245 uses the C2PO error flags to perform the Erasure Correction up to 2-byte error per Codeword by setting the *EraCorr* bit in the *ECC Control 1 Register* (3Bh, bit 0). The Q-subcode with de-interleaving and CRC check are done by hardware.

Sync pattern protection logic is implemented in the KS9245 to prevent lost sync in the DSP incoming streams. The sync patterns in buffer DRAM are further protected to facilitate the Read Raw operations. This assures that the application is able to retrieve the correct sync pattern when Sync Insertion occurs.

The decoder logic operates in various modes according to the setting of the *Decoder Control Register* (3Ah). The Monitor Mode is used to search the target block and synchronize the Sync Mark in the main data channel before data buffering operation occurs. In this mode, no buffering or ECC operation is active. The decoder interrupt occurs at the relative location of Header or Subheader of the incoming DSP data streams.

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The Audio Buffering Mode is used for CD-DA copy operations. In this mode, the descrambler, ECC, and EDC logic are not active and a decoder interrupt is generated to the microprocessor for every 2352-byte. The buffering operation for data stream is active. The CD-DA data can be accurately synchronized with the subcode data stream if the *AsynWrt* bit in the *ECC Control 2 Register* (3Ch, bit 3) is set.

In the ECC mode, the descrambler, EDC, and ECC are all active with various correction configurations. This mode is normally used for buffering CD data such as Yellow Book, CD-ROM XA, or CD-I data. The correction modes are configured by setting the *ECC Control 1 Register* (3Bh). The decoder interrupts occur at either the completion of *On-The-Fly-EDC™* check when there is no EDC error, or at the end of ECC operations in this mode. The *Decoder Header Min/Sec/Frame/Mode Registers* (30h, 31h, 32h, 33h), *Decoder Subheader 0-3 Registers* (34h, 35h, 36h, 37h), and the *ECC Status Register* (3Dh) contains the information for the block just processed.

The Buffering Only Mode is used for processing Yellow Book Mode 0 and 2 data. In this mode, only the descrambler is active. Neither ECC nor EDC logic will be applied in this mode. The settings of the *ECC Control 1 Register* (3Bh) is ignored by hardware. The decoder interrupt occurs at the end of buffering a block to the buffer DRAM.

If no correction is applied, there is a full sector time for firmware to process the decoder interrupt in most cases. For the KS9245, the maximum time allowed for firmware to process the interrupt is a half sector time. In the Firmware Sector Process Time of the Hardware Application Note section, detailed information is provided for various disk speeds.

- ***On-the-fly-EDC™ correction***

The KS9245 supports On-The-Fly-EDC™ correction. Both Yellow Book Mode 1 and XA Mode 2, Form 1 of incoming DSP data streams are automatically checked by the EDC circuit. If there is no EDC error, the decoder interrupt is immediately generated without further delay and no redundant ECC is applied. As a result, the Buffer Manager can transfer the data to host without ECC latency and lower CPU utilization is achieved. If there is an EDC error, the consecutive ECC correction will be applied. On-The-Fly-EDC™ check can also resolve the buffer DRAM requirements. Therefore, the KS9245 can support the high speed CD application up to 50X with standard DRAMs.

- ***Advanced Erasure Correction up to 2-byte error per Codeword***

The KS9245 supports high performance erasure correction up to 2-byte error per Codeword. The Erasure Correction is enabled by setting the *EraCorr* bit in the *ECC Control 1 Register* (3Bh, bit 0). The erasure correction logic uses the C2PO error flags as correction indication. Therefore, C2PO error flags must be provided in this mode. The standard P and Q Parity Correction are supported for 1-byte error per Codeword. The P and Q Parity are enabled by setting the *EccPen* or *EccQen* bits in the *ECC Control 1 Register* (3Bh, bit 2, 1).

- ***CD-DA COPY support***

The KS9245 also supports CD-DA buffering operations. By setting the *AudiWrt* bit in the *Decoder Control Register* (3Bh, bit 4), the decoder is placed into Audio Buffering Mode. The decoder circuit starts to synchronize with the first left channel. If the *ASynWrt* bit in the *ECC Control 2 Register* (3Ch, bit 3) is set, the CD-DA data stream will be synchronized with the subcode Sync Mark. As a result, the data of CD-DA operations are smoothly connected for different accesses. In Audio Buffering Mode, the internal counter is active and an interrupt is generated to the host for every 2352-bytes.

- ***Audio Playback in CAV mode support***

In CAV (Constant Angular Velocity) applications, the KS9245 allows audio data to be buffered and played at regular CAV speeds without changing the speed to CLV (Constant Linear Velocity) or single speed modes. Along with the CD-DA subcode synchronization techniques in KS9245, Audio frame data

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is guaranteed to be smoothly concatenated without losing audio frames during CAV playback. In the KS9245, up to 50X CAV operation in outer tracks is supported.

The buffered audio data is output to the external audio DAC at 44.1Khz (Word Clock) in either EIAJ or I2S audio formats regardless of the disk speed. Also, the audio data underrun condition is masked by muting both output channels to guard against undesired audio noise. As results, in CAV applications, the audio playback can be achieved by CD-ROM controller in a low cost design.

In order to simplify firmware efforts and efficiently control the audio playback sequences, the Audio Hardware Buffer Manager implemented will automatically keep track of the available audio block(s) in buffer DRAM. When this buffer is full, firmware is able to stop the DSP buffering operation. If the buffer is empty or underrun, the audio mute operation is automatically performed by hardware to avoid any noise from being outputted.

The audio output pins can be selected and configured via the AWCK, ABCK, ADAT and EBUO pins. The clock source is derived directly from the system clock thus eliminating the need for another crystal for the audio clock.

- **Repeated Correction support**

Repeated correction is supported by the KS9245 for intensively non real-time correction environments. By setting the appropriate *Disk Transfer Block Address Registers* (38h, 39h) and writing a one in the *RepCorr* bit in the *ECC Control 2 Register* (3Ch, bit 2), the correction is started. An interrupt will be generated with the *Declnt* bit set in the *Decoder Interrupt Status Register* (11h, bit 0) if the *DeclntE* bit in *Decoder Interrupt Mask Register* (13h, bit 0) is set.

- **Sync Mark Insertion support**

The Sync Mark insertion is supported by the KS9245. When the decoder is in the ECC, Buffering Only Mode, or Monitor Mode, the Sync Insertion logic is active. This allows the DSP Interface logic to recover from lost synchronization errors. If the decoder is in the Monitor Mode, the Sync Insertion logic will always re-synchronize with the most recent Sync Mark to insure that synchronization is never lost.

- **Q-Subcode deinterleave with CRC check support**

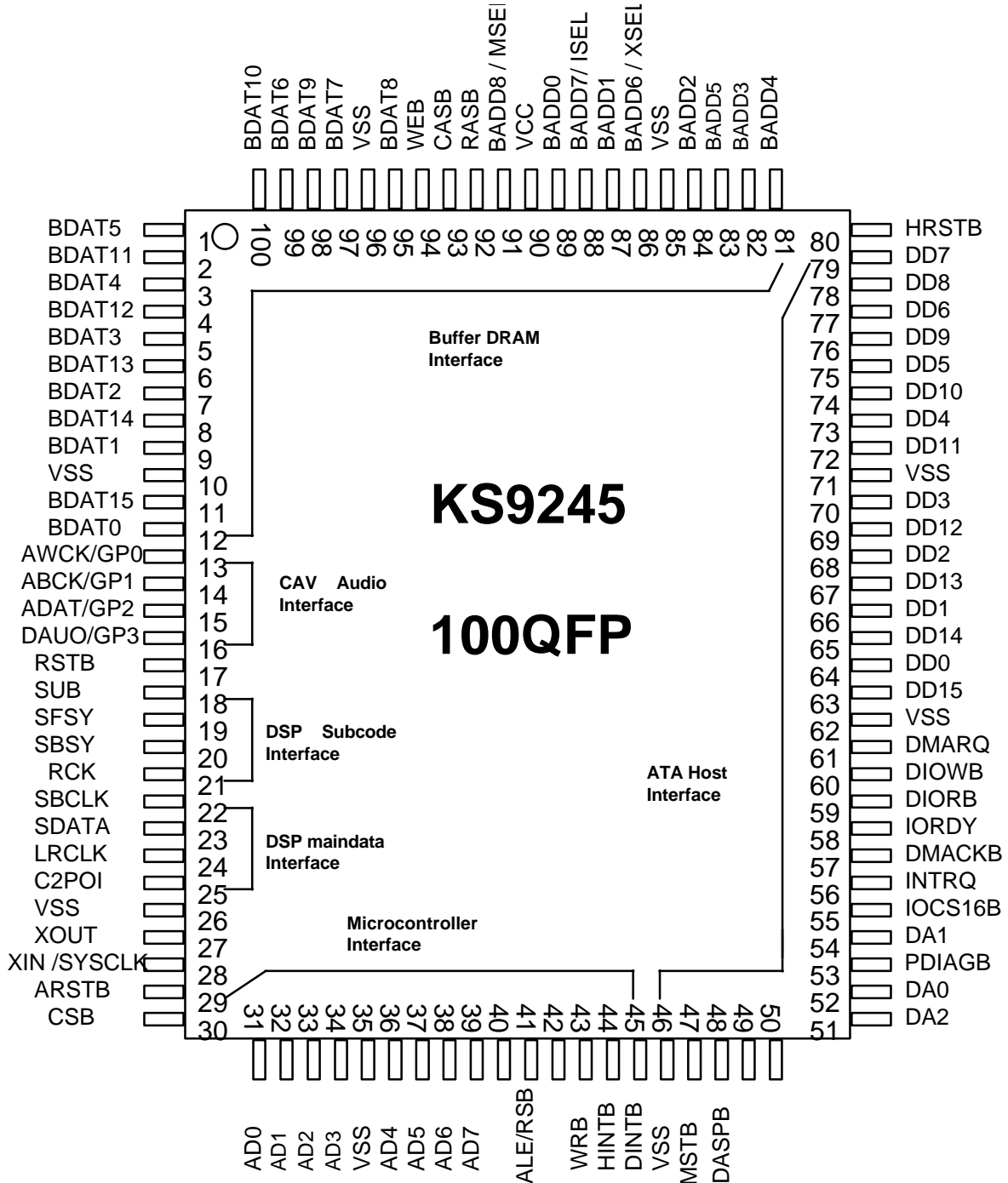
The 12-byte de-interleaved Q subcode is supported by the KS9245. The de-interleaved Q subcode data with four zeros data are written into buffer DRAM without firmware intervention. Also, the CRC check for Q subcode is done by hardware and this CRC result is reported in the *Subcode Status Register* (41h, bit 7, 6) when a subcode interrupt occurs.

- **Real-time ECC and Sector Synchronized method support**

ECC operation starts as soon as the previous block has finished buffering operation with EDC error. The ECC operation is synchronized with the sector sync pattern. As a result, the data block address for ECC operation is always one block behind the DSP buffering operation. Because of the sector synchronized architecture of ECC corrections, blocks are processed in real-time. In other "buffered data correction" or "delayed pipeline ECC correction" methods, the buffer DRAM will quickly fill when some erroneous blocks occur. As a result, a consequent seek may be required. Therefore, the real-time ECC correction of the KS9245 offers a superior correction scheme to other methods.

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1.2 KS9245 QFP Pin Diagram



Note: BADD0 (Pin 89) should be pulled high by a 22K Ohm Resistor for KS9246 compatibility.

1.3 Pin Assignment

The pin assignments are listed in sequential order of pin number with short description in the following table.

Symbol and Convention		
D	Open-Drain	pin used as an open-drain signal
O	Output	pin used as an output signal
I	Input	pin used as an input signal
T	Tristate	pin used as a tristate signal
t	To	pin is an output signal to outside component
f	From	pin is an input signal from outside component
x	don't care	pin may either be used or not used
MP		Microprocessor or Microcontroller
DSP		CD DSP main data channel interface
DSPSUB		CD DSP Subcode interface
DRAM		Dynamic Random Access Memory
Host		IDE Host
Master		IDE Master Drive, drive 0
Slave		IDE Slave Drive, drive 1
DAC		External Audio DAC

Physical Pin Assignment				
<i>Signal</i>	<i>Pin</i>	<i>I/O</i>	<i>Description</i>	<i>Source/ Destination</i>
BDAT5	1	I/O	DRAM data bus 5	t, f, DRAM
BDAT11	2	I/O	DRAM data bus 11	t, f, DRAM
BDAT4	3	I/O	DRAM data bus 4	t, f, DRAM
BDAT12	4	I/O	DRAM data bus 12	t, f, DRAM
BDAT3	5	I/O	DRAM data bus 3	t, f, DRAM
BDAT13	6	I/O	DRAM data bus 13	t, f, DRAM
BDAT2	7	I/O	DRAM data bus 2	t, f, DRAM
BDAT14	8	I/O	DRAM data bus 14	t, f, DRAM
BDAT1	9	I/O	DRAM data bus 1	t, f, DRAM

Physical Pin Assignment				
Signal	Pin	I/O	Description	Source/ Destination
VSS	10	I	Ground	-
BDAT15	11	I/O	DRAM data bus 15	t, f, DRAM
BDAT0	12	I/O	DRAM data bus 0	t, f, DRAM
AWCK/GP0	13	I/O	Audio word clock output or General Purpose I/O Line 0	t,DAC
ABCK/GP1	14	I/O	Audio bit clock output or General Purpose I/O Line 1	t,DAC
ADCK/GP2	15	I/O	Audio data output or General Purpose I/O Line 2	t,DAC
DAUO/GP3	16	I/O	Digital Audio output or General Purpose I/O Line 3	t,DAC
RSTB	17	I	Chip power on reset	-
SUB	18	I	Subcode serial data in	f, DSPSUB
SFSY	19	I	Subcode frame sync	f, DSPSUB
SBSY/CFLG	20	I	EIAJ Subcode block sync / CFLAG	f, DSPSUB
RCK	21	I/O	Subcode bit clock	t, DSPSUB
SBCLK	22	I	DSP Bit Clock	f, DSP
SDATA	23	I	DSP Channel Data	f, DSP
LRCLK	24	I	DSP Left Channel Clock	f, DSP
C2POI	25	I	C2PO Error Flags	f, DSP
VSS	26	I	Ground	-
XOUT	27	O	oscillator output	t,Oscillator
XIN/SYSCLK	28	I	oscillator input/system clock input Normally, 33.868 MHz / 50.8MHz	f,Oscillator
ARSTB	29	O	ATAPI 08 Cmd reset	t, MP
CSB	30	I	Chip select	f, MP
AD0	31	I/O	microprocessor data/address bus 0	t, f, MP
AD1	32	I/O	microprocessor data/address bus 1	t, f, MP
AD2	33	I/O	microprocessor data/address bus 2	t, f, MP
AD3	34	I/O	microprocessor data/address bus 3	t, f, MP
VSS	35	I	Ground	-
AD4	36	I/O	microprocessor data/address bus 4	t, f, MP
AD5	37	I/O	microprocessor data/address bus 5	t, f, MP
AD6	38	I/O	microprocessor data/address bus 6	t, f, MP
AD7	39	I/O	microprocessor data/address bus 7	t, f, MP
VCC	40	I	Power	-

Physical Pin Assignment				
Signal	Pin	I/O	Description	Source/ Destination
ALE RSB	41	I	microprocessor Address Latch Enable Address Register select in indirect access mode.	f, MP
RDB DSB	42	I	microprocessor read strobe (Intel) data strobe signal (Motorola)	f, MP
WRB R/WB	43	I	microprocessor write strobe (Intel) read/write strobe (Motorola)	f, MP
HINTB	44	OD	microprocessor Host interrupt	t, MP
DINTB	45	OD	microprocessor Disk interrupt	t, MP
VSS	46	I	Ground	-
MSTB	47	I	Master/Slave Configuration	Drive SEL
DASPB	48	I/O	IDE drive active-slave present	Mast/Slave
CS3FXB	49	I	IDE host chip select 1	f, Host
CS1FXB	50	I	IDE host chip select 0	f, Host
DA2	51	I	IDE host address 2	f, Host
DA0	52	I	IDE host address 0	f, Host
PDIAGB	53	I/O	IDE Passed Diagnostics	Mast/Slave
DA1	54	I	IDE host address 1	f, Host
IOCS16B	55	OD	IDE 16-bit data transfer	t, Host
INTRQ	56	OT	IDE host interrupt request	t, Host
DMACKB	57	I	IDE host DAM acknowledge	f, Host
IORDY	58	OT	IDE I/O channel ready	t, Host
DIORB	59	I	IDE I/O read strobe	f, Host
DIOWB	60	I	IDE I/O write strobe	f, Host
DMARQ	61	OT	IDE drive DMA request	t, Host
VSS	62	I	Ground	-
DD15	63	I/O	IDE host data bus 15	t, f, Host
DD0	64	I/O	IDE host data bus 0	t, f, Host
DD14	65	I/O	IDE host data bus 14	t, f, Host
DD1	66	I/O	IDE host data bus 1	t, f, Host
DD13	67	I/O	IDE host data bus 13	t, f, Host
DD2	68	I/O	IDE host data bus 2	t, f, Host
DD12	69	I/O	IDE host data bus 12	t, f, Host
DD3	70	I/O	IDE host data bus 3	t, f, Host

Physical Pin Assignment				
Signal	Pin	I/O	Description	Source/ Destination
VSS	71	I	Ground	-
DD11	72	I/O	IDE host data bus 11	t, f, Host
DD4	73	I/O	IDE host data bus 4	t, f, Host
DD10	73	I/O	IDE host data bus 10	t, f, Host
DD5	75	I/O	IDE host data bus 5	t, f, Host
DD9	76	I/O	IDE host data bus 9	t, f, Host
DD6	77	I/O	IDE host data bus 6	t, f, Host
DD8	78	I/O	IDE host data bus 8	t, f, Host
DD7	79	I/O	IDE host data bus 7	t, f, Host
HRSTB	80	I	ATA Host reset	-
BADD4	81	O	DRAM Address line 4	t, DRAM
BADD3	82	O	DRAM Address line 3	t, DRAM
BADD5	83	I/O	DRAM address line 5 Must also be pulled up by 22K Ohm Resistor	t, DRAM
BADD2	84	O	DRAM address line 2	f, DRAM
VSS	85	I	Ground	-
BADD6/XSEL	86	I/O	DRAM address line 6 22K Pull-up for 50.8MHz Sysclk 10K Pull-down for 33.86MHz Sysclk	t, DRAM
BADD1	87	O	DRAM address line 1	t, DRAM
BADD7/ISEL	88	I/O	DRAM Address line 7 Pull-up for MP Register Indirect Select Pull-down for MP Register Direct Select	t, DRAM
BADD0	89	O	DRAM address line 0 Should be pulled up by 22K Resistor	t, DRAM
VCC	90	I	Power	-
BADD8/MSEL	91	I/O	DRAM address line 8 Pull-up for Motorola MP Select Pull-down for Intel MP Select	t, DRAM
RASB	92	O	DRAM RASB line	t, DRAM
CASB	93	O	DRAM, CASB line	t, DRAM
WEB	94	O	DRAM write enable	t, DRAM
BDAT8	95	I/O	DRAM data bus 8	t, f, DRAM
VSS	96	I	Ground	-
BDAT7	97	I/O	DRAM data bus 7	t, f, DRAM
BDAT9	98	I/O	DRAM data bus 9	t, f, DRAM
BDAT6	99	I/O	DRAM data bus 6	t, f, DRAM
BDAT10	100	I/O	DRAM data bus 10	t, f, DRAM

1.4 Pin Description

1.4.1 Pin Description in ATA Host Interface

CS1FXB (Drive chip select 0)

Pin 50

This is the chip select signal decoded from the host address bus used to select the Command Block Registers.

CS3FXB (Drive chip select 1)

Pin 49

This is the chip select signal decoded from the host address bus used to select the Control Block Registers.

DA0,1,2 (Drive address bus)

Pin 52,54,51

This is the chip select signal decoded from the host address bus used to select the Control Block Registers.

DASPB (Drive active slave present)

Pin 48

This is a time-multiplexed signal which indicates that a drive is active or drive 1 is present. This signal is an open collector output with a 10K ohm pull-up resistor.

DD0-DD15 (Drive data bus)

**Pin 64,66,,68,70,73,75,77,79,
78,76,74,72,69,67,65,63**

These signals are used for 16-bit bidirection data bus between the host and the KS9245. The DD0-7 are used for accessing 8-bit ATA Task File Registers.

In ATAPI data transfer mode, it is always 16-bit wide.

DIORB (Drive I/O Read)

Pin 59

This is the Read strobe signal. The rising edge of DIORB enables data from a register or the data port of the KS9245 onto the host data bus, DD0-DD7 or DD0-DD15. The rising edge of DIORB latches data at the host. In Ultra DMA mode, this signal is used by the Host as the DMARDYB signal during host reads, and as the data STROBE signal during Host writes.

DIOWB (Drive I/O Write)

Pin 60

This is the Write strobe signal. The rising edge of DIOWB clocks data from the host data bus, DD0-DD7 or DD0-DD15, into the data port of the KS9245. In Ultra DMA mode, this signal is used by the HOST as the STOP signal.

DMACKB (DMA Acknowledge)

Pin 57

This signal is used by the host in response to DMARQ to either acknowledge that data has been accepted, or that data is available.

DMARQ (DMA Request)

Pin 61

This signal is used for DMA data transfer between host and KS9245. It is asserted by the KS9245 when it is ready to transfer data to or from the host. The direction of transfer is controlled by DIORB and DIOWB. This signal is used in a handshake manner with DMACKB signal.

When a DMA operation is enabled, IOCS16B, CS1FXB and CS3FXB are not asserted and data transfer are 16-bits wide.

IORDY (Host IO Ready)

Pin 58

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This signal is deasserted in order to extend the host access when KS9245 is not ready to response to the request. In Ultra DMA mode, this signal is used by the KS9245 as the drive's DMARDYB signal during Host writes, and as the drive's data STROBE signal during Host reads.

INTRQ (Drive interrupt)**Pin 56**

This signal is used to interrupt the host. INTRQ pin is asserted only when the KS9245 has a pending interrupt while the drive is selected, and the host has cleared nIEN in the ATA Device Control Register. If nIEN=1 or the drive is not selected, this output is in a high impedance state, regardless of the presence or absence of a pending interrupt.

IOCS16B (Device 16-bit I/O)**Pin 55**

Except for DMA transfers, IOC16B indicates to the host that the 16-bit data port has been addressed. This is an open collector output.

In ATAPI PIO data transfer mode, the IOCS16B shall always be asserted.

PDIAGB (Drive passed diagnostics)**Pin 53**

This signal is asserted by drive 1 (slave drive) to indicate to drive 0 (master drive) that it has completed diagnostics. A 10K ohm pull-up resistor is used on this signal by each drive on the same cable.

HRSTB (ATA Host Reset)**Pin 80**

This signal from the host system is asserted for at least 25 usec after voltage levels during power-on and negated thereafter unless some event requires that the drive be reset following power on. When this input signal is asserted, the ATA Task File Registers will be initialized and the BSY bit in ATA Status Register will be set. The *Hrst* bit in *Host Interrupt Status Register* will be set (10h, bit 3) , if *HrstE* bit in *Host Interrupt Mask Register* (12h, bit 3) is set.

1.4.2 Pin Description in Buffer DRAM Interface

BDAT 0-15 (Buffer DRAM data bus)**Pin 12,9,7,5,3,1,99,97,95,98,100,2,4,6,8,11**

These signals are used for buffer DRAM data bus with 16-bit parallel data path to/from the buffer memory.

BADD 0-8 (Buffer DRAM address bus)**Pin 89,87,84,82,81,83,86,88,91**

These signals are used for buffer DRAM address bus. Up to 512K bytes DRAM are supported by KS9245.

IMPORTANT: BADD5 pin 83 must also be pulled high by a 22K Ohm resistor.

CASB (Column address strobe)**Pin 93**

This signal is used as column address strobe for buffer DRAM.

RASB (Row address strobe)**Pin 92**

This signal is used as row address strobe for buffer DRAM.

WEB (DRAM write enable)**Pin 94**

This signal is used as the memory write enable for buffer DRAM.

1.4.3 Pin Description in Microprocessor Interface

AD0-7 (Microprocessor address and data bus) **Pin 31,32,33,34,36,37,38,39**
These signals are bi-directional multiplexed microprocessor address and data lines.

ALE(Address latch enable) **Pin 41**
RSB(Register Select)

The falling edge of this signal is used as address latch for register access in Intel Mode. This signal is used as Address Register Select in indirect register access mode. In this mode, RSB pin is asserted as logic low state for Address Register and RSB pin is negated as logic high state for Data Register.

RDB (microprocessor read strobe) **Pin 42**
DSB (data strobe)

This signal is used as the read strobe signal in Intel multiplexed register addressing mode. When the Motorola microprocessor is selected, this signal is acted as data strobe signal.

WRB (microprocessor write strobe) **Pin 43**
R/WB (R/W Strobe)

This signal is used as the write strobe signal in Intel multiplexed register addressing mode. When the Motorola microprocessor is selected, this signal is acted as read/write strobe signal.

HINTB (Microprocessor host/buffer interrupt) **Pin 44**

This signal is asserted as logic low state when interrupt status is available to microprocessor. This interrupt indicates there is at least one host or buffer event which needs to be serviced by microprocessor.

DINTB (Microprocessor disk interrupt) **Pin 45**

This signal is asserted as logic low state when interrupt status is available to microprocessor. This interrupt indicates there is at least one decoder or disk event which needs to be serviced by microprocessor. The disk interrupt can be combined with host interrupt in HINTB signal by clearing *IntMode* bit in *Interface Configuration Control Register* (0Bh, bit 7). The combined mode is the default mode at power-on.

CSB (Chip Select) **Pin 30**

This signal must be asserted as logic low state for accessing registers of KS9245.

MSEL (Microprocessor select) **Pin 91**

This pin is used to select the Motorola microprocessor when it connects with pull-up resistor 22K. Otherwise, with pull-down resistor 10K, the Intel microprocessor is selected. This pin is sampled only when ISEL pin is negated at the power on stage.

ISEL (microprocessor indirect register access select) **Pin 88**

This pin is used to select the indirect register access mode when it connects with pull-up resistor 22K. Otherwise, with pull-down resistor 10K, the direct register access mode is selected. This pin is sampled only at the power on stage.

In the indirect register access mode, the ALE/RSB pin is used to select register input. When RSB is asserted, the Address Register is selected. When RSB is negated, the internal register addressed by Address Register is accessed by microprocessor.

1.4.4 Pin Description in DSP Interface

SUB (Subcode Serial data in)**Pin 18**

This pin is used to input the subcode channel data.

SFSY (Subcode Frame Sync)**Pin 19**

This pin is used to indicate the subcode Frame Sync Mark. The subcode data is available at the falling edge of this signal. In Philips V4 Subcode mode, this pin should be grounded.

SBSY/ CFLG (Subcode Block Sync/CLAG)**Pin 20**

This pin is used to indicate the subcode Block Sync Mark. In Philips V4 Subcode mode, this pin should connect to CFLAG.

RCK (Subcode Clock)**Pin 21**

This pin is used to input, output and clock the subcode data from DSP. In Philips V4 Subcode mode, this pin should not be connected.

LRCLK (DSP Left Channel Clock)**Pin 24**

This pin is used to indicate the left/right channel data.

SDATA (DSP main channel data)**Pin 23**

This pin is used to input the DSP main channel data.

SBCLK (DSP bit clock)**Pin 22**

This pin is used to input the data clock of DSP main channel.

C2POI (C2 Pointer Input)**Pin 25**

This pin is used to indicate the error flags of DSP main channel data.

1.4.5 Pin Description in Power/Ground/Rest Pins**VSS** (Ground)**Pin 10,26,35, 46,62,71,85,96****VDD** (Power Supply with 5 volt source)**Pin 40,90****1.4.6 Pin Description in System Configuration****MSTB** (Master/Slave Configuration)**Pin 47**

This signal is used to inform the KS9245 that the drive is configured as master or slave. When this signal is asserted as logic low state, it indicates the drive is configured as master. When this signal is negated as logic high state, it indicates the drive is configured as slave.

The DASPb signal will be asserted when the MSTB pin is negated (slave mode) during Power-on/Hardware Reset/ATA SRST.

The PDIAGb signal will be negated when the MSTB pin is asserted (master mode) during Power-on/Hardware Reset/ATA SRST and ATA Diagnostic command.

RSTB (Chip Reset)**Pin 17**

A logic low input will reset the KS9245. All host interface outputs are set to the high-impedance state. The registers of KS9245 will be initialized as their default values.

ARSTB (ATAPI 08 Cmd Reset)**Pin 29**

A logic low pulse with 40 usec will be asserted when host issues the ATAPI Reset Command (08h) to the KS9245. This signal could use as the pulse to reset the micro-controller. The output of 60 usec clock pulse is assumed that the System Clock of 33.8688 MHz is used.

XIN/SYSCLK (Crystal or System clock input)**Pin 28**

This signal is the crystal or CMOS-level clock input as system clock. The KS9245 contains an internal resistor between XIN/XOUT. There is no external resistor required to connect these pins. The standard crystal or CMOS-level clock is either 33.8688 MHz or 50.8MHz.

XOUT (Oscillator output)**Pin 27**

This signals is the oscillator output.

XSEL (System Clock Select)**Pin 86**

The KS9245 supports two frequencies. This pin can use an external jumper select to configure for either 33.86MHz or 50.8MHz. This pin should be pulled-up by a 22K Ohm resistor for 50.8 MHz operation, and strapped-down by a 10K Ohm resistor for 33.86MHz operation.

GPI 0-3 (general purpose Input/Output Lines)**Pin 13,14, 15, 16**

These signals are used as general purpose input pins. The Input or Output can be configured by setting or clearing the *GPC3*, *GPC2*, *GPC1*, *GPC0* bits in *Port Control Register* (44h, bit 7,6,5, 4) and *APCE* bit in *Global Control Register* (2Fh, bit3) is cleared.

1.4.7 Pin Description in Audio DAC Interface

DAUO (Digital Audio Output)**Pin 16**

This pin is used to output the digital audio as IEC-958 format. This bit is enabled when *APCE* bit in *Global Control Register* (2Fh, bit 3) is set.

ADAT (Audio Data output)**Pin 15**

This pin is used to as a audio data output pin when the audio playback in CAV mode is selected to be used. This bit is enabled when *APCE* bit in *Global Control Register* (2Fh, bit 3) is set.

ABCK (Audio bit clock output)**Pin 14**

This pin is used to as a audio bit clock output pin. This bit is enabled when *APCE* bit in *Global Control Register* (2Fh, bit 3) is set.

AWCK (Audio word clock output)**Pin 13**

This pin is used to as a audio word clock output pin. This bit is enabled when *APCE* bit in *Global Control Register* (2Fh, bit 3) is set.

1.4.8 Register Map for KS9245

Page #	Address	Name	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
Host Interface Registers (Chapter 2)											
	00h R	PFIFO	Packet FIFO Register								
	01h R	AFEAT	Reserved						Overlap	DMA	
	01h W	AERR	Sense Key				MCR	ABRT	EOM	ILI	
	02h R	ASECC	ATA Sector Count Register								
	02h W	AINTR	Reserved					Release	IO	CoD	
	03h R/W	ASAM	ATAPI SAM Tag Register/ ATA Sector Number								
	04h R/W	ABCL	ATAPI Byte Count Low Register/ ATA Cylinder Low Register								
	05h R/W	ABCH	ATAPI Byte Count High Register/ ATA Cylinder High Register								
	06h R/W	ADSEL	Rsvd	LBA	Rsvd	DRV	Reserved				
	07h R	ACMD	ATAPI Command Register/ ATA Command Register								
	08h R	ADCV	Reserved				Rsvd	SRST	nIEN	Rsvd	
	09h R	AISTAT	BSY	DRDY	Rsvd	DSC	DRQ	Corr	Rsvd	CHECK	
	09h W	HSC	Rsvd	DRDY	Rsvd	DSC	DRQ	Corr	Rsvd	CHECK	
	0Ah R	HISV	Reserved				MSTB	DASPB	PDIAGB	0	
	0Ah W	HIC	SetBSY	SetDASPB	SetPDIAGB	SetHINT	ClrBSY	ClrDASPB	ClrPDIAGB	ClrHINT	
	0Bh R/W	ICC	IntMode	ATA Transfer Mode		CDRV	SShadow	DisShadR	PcmdInt	DisIORDY	
	0Ch		Reserved								
	0Dh		Reserved								
Hardware Sequence Command Registers (Chapter 3)											
	0Eh W	HSC	Rsvd	SAAabort	Sservice	Srelease	STFInt	SCpl	SCplChk	SDSC	
	0Fh W	TSC	ACacheE	ACpIE	Rsvd	SSxfr	SAbort	SPause	WRDir	SDxfr	
	0Fh R	TSS	ACacheE	ACpIE	Reserved			SPause	WRDir	HxfrBsy	
Microprocessor Interrupt Registers (Chapter 4)											
	10h R/W	HISR/HICR	TxfrDone	Rsvd	Asrst	Srst	Hrst	ScmdRcv	AcmdRcv	PcmdRcv	
	11h R/W	DISR/DICR	Reserved					DACInt	SubInt	Declnt	
	12h R/W	HIM	TxfrDoneE	CxfrDoneE	AsrstE	SrstE	HrstE	ScmdRcvE	AcmdRcvE	PcmdRcvE	
	13h R/W	DIM	Reserved					DACIntE	SubIntE	DeclntE	
Buffer/CD Cache manger Registers (Chapter 5)											
	14h R/W	VCBCL	Valid Cache Block Count Register B7:B0								
	15h		Reserved								
	16h	TTBLL	Total Host Transfer Block Length Register B7:B0								

	R/W		
	17h		Reserved
	18h R/W	CHTBL	Current Host Transfer Block Length Register B7:B0
	19h		Reserved
	1Ah R/W	HTBLA	Host Transfer Block Address Low Register B7:B0
	1Bh R/W		Reserved

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Page	Addresses	Name	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	1Ch R/W	HBOAL1	Host Block Offset Address Low 1 Register B7:B0							
	1Dh R/W	HBOAH1	Reserved				B11	B10	B9	B8
	1Eh R/W	TOLL1	Transfer Offset Length Low 1 Register B7:B0							
	1Fh R/W	TOLH1	Reserved				B11	B10	B9	B8
	20h R/W	HBOAL2	Host Block Offset Address Low 2 Register B7:B0							
	21h R/W	HBOAH2	Reserved				B11	B10	B9	B8
	22h R/W	TOLL2	Transfer Offset Length Low 2 Register B7:B0							
	23h R/W	TOLH2	Reserved				B11	B10	B9	B8
	24h R/W	MPALSB MBOAL	MP Access Physical Address LSB B7:B0 MP Block Offset Address Low Register B7:B0							
	25h R/W	MPAMID MBOAH	MP Access Physical Address MID B15:B8 MP Block Offset Address High Register B11:B8							
	26h R/W	MPAMSB MBA	MP Access Physical Address MSB B18:B16 MP Block Address Register B7:B0							
	27h		Reserved							
	28h R/W	MPDP	MP Access Data Port Register B7:B0							
	29h R	BAC	DramBs y	Reserved				PAMb	Rsvd	Rsvd
	29h W	BAC	IncAudC nt	IncBlkCnt	Reserved			PAMb	SDramWr t	SDramRd
	2Ah R/W	BCC1	C2ErrOR	Dsec	Ssel	Csel	BlkCon f	DramsZ		
	2Bh R/W		Reserved							
	2Ch R/W	BBBA	Buffer Bottom Block Address Register B7:B0							
	2Dh R/W		Reserved							
	2Eh R/W	DRCR	DRAM Resfresh Control Register							
	2Fh R/W	GCR	SSleep	SFReset	BurstNu m	Dspbur st	APCE	Cspeed[2:0]		
CD Block Decoder Registers (Chapter 6)										
	30h R	DHMIN	Decoder Header Min Register							
	31h R	DHSEC	Decoder Header Sec Register							
	32h R	DHFRAME	Decoder Header Frame Register							
	33h R	DHMODE	Decoder Header Mode Register							
	34h R	DSUBH0	Decoder Subheader 0 Register							
	35h R	DSUBH1	Decoder Subheader 1 Register							
	36h R	DSUBH2	Decoder Subheader 2 Register							
	37h R	DSUBH3	Decoder Subheader 3 Register							
	38h R/W	DTBA	Disk Transfer Block Address Register							

	39h		Reserved						
	3Ah R/W	DCR	Reserved	AudMo n	AudiWrt	ECCRQ	DecWrt	Decen	Descen
	3Bh R/W	ECC1	XAMode	Reserved		Edcen	EccPen	EccQen	EraCorr
	3Ch R/W	ECC2	Reserved		PacketW r	ASynWrt	RepCor r	Rsvd	Rsvd

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Page	Addresses	Name	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
	3Dh R/W	DESR	InValid	OVErr	EccFat	EccErr	CBlk	NoSync	IllSync	Rsvd	
	3Eh R/W	DDTS	Rsvd	BCKD1	FPS	BCKLength		LSBF	LCH	BCKF	
	3Fh R	DSER	ESH0	ESH1	ESH2	ESH3	Emin	Esec	Eframe	Emode	
	40h R/W		Reserved								
	41h R	SSR	ScrcErr	SubErr	Reserved						
	42h R/W	SDTS	Sub Format Selection		Reserved						
	43h R	VCR	Version Number								
	44h R/W	PCR	GPC3	GPC2	GPC1	GPC0	GP3	GP2	GP1	GP0	
	45h R/W		Reserved								
	46h R/W		Reserved								
	47h		Reserved								
	48h R/W	VABC	Valid Audio Block Count Register B7:B0								
	49h		Reserved								
	4Ah R/W	DABA	DAC Block Address Register B7:B0								
	4Bh		Reserved								
	4Ch R/W	DOFS	ADAT18	ABCKD1	AFPS	ABCKL		ALSBF	ALCH	ABCKF	
	4Dh R/W	DACR	Reserved					ACC		SPA	
	4Eh R/W	ACCR	Rsvd	ABPS	DAUE	DOVS		DSCD	XINA Div		
	4Fh R/W	AVCR	LCM	RCM	Reserved		VOL				
Diagnostic Miscellaneous Registers (Chapter 7)											
<i>Not Used for Normal Operations</i>											
	50h		Reserved								
	51h		Reserved								
	52h		Reserved								
	53h		Reserved								
	54h		Reserved								
	55h		Reserved								
	56h		Reserved								
	57h		Reserved								
	57h		Reserved								
	58h		Reserved								
Enhancement Control Registers (Chapter 8)											
	60h R/W	UDTR	UDErr	Reserved				UDmaCyc[2:0]			

Chapter 2

ATA/ATAPI Host Interface Registers

2.1 ATA Task File Registers

The ATA Task File Registers can be addressed by CS1FX/CS3FX/DA2/DA1/DA0 pins of ATA Interface Signal. The ATA Task File Registers are specified as follows:

CS1FXB	CS3FXB	DA2	DA1	DA0	DA2-0	Host Read	Host Write
A	N	0	0	0	00h	ATA Data Register ATAPI Data Register	ATA Data Register ATAPI Data Register
A	N	0	0	1	01h	ATA Error Register ATAPI Error Register	ATA Features Register ATAPI Features Register
A	N	0	1	0	02h	ATA Sec Count Register ATAPI Interrupt Reason Register	ATA Sec Count Register ATAPI reserved
A	N	0	1	1	03h	ATA Sec number Register ATAPI Sam Tag Register	ATA Sec number Register ATAPI Sam Tag Register
A	N	1	0	0	04h	ATA Cyl. Low Register ATAPI Byte Count Low Register	ATA Cyl. Low Register ATAPI Byte Count Low Register
A	N	1	0	1	05h	ATA Cyl. High Register ATAPI Byte Count High Register	ATA Cyl. High Register ATAPI Byte Count High Register
A	N	1	1	0	06h	ATA Drive Sel Register ATAPI Drive Sel Register	ATA Drive Sel Register ATAPI Drive Sel Register
A	N	1	1	1	07h	ATA Status Register ATAPI Status Register	ATA Command Register ATAPI Command Register
N	A	1	1	0	06h	ATA Alternate Status Register ATAPI Alternate Status Register	ATA Device Control Register ATAPI Device Control Register

Note: "A" represents signal asserted. "N" represents signal negated.

When the *BSY* or *DRQ* bits are set in the Status Register, the Task File Registers are owned by the KS9245. When this occurs, the host cannot write to the Task File registers. Also, when the *BSY* bit is set, all Task File Registers will contain the same values as the ATA Status Register.

2.2 Host Interface Registers

Register 00h : Packet FIFO Register (Read)

Acronym: PFIFO

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ATAPI Packet FIFO Register							

The Packet FIFO Register contains 12 bytes for receiving the Packet Command. After the host writes the *Packet Command* (A0h) into the *ATAPI Command Register*, the KS9245 will automatically be set to receive 12-bytes of command packet from the host to store into the Packet FIFO register. The firmware should then perform consecutive read operations from this register to obtain the 12-byte packet command.

Register 01h : ATAPI Features Register (Read)

ATA Features Register (Read)**Acronym:** AFEAT

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Rsvd	Reserved (Tag Type)			Reserved		Overlap	DMA

The ATAPI Features Register contains the specific features (such as DMA/PIO mode or Overlap Operation) which the host requests the drive to perform.

Bit 7-2: Reserved

These bits are reserved for future enhancements.

Bit 1: Overlap

When this bit is set during the issuance of an ATAPI Packet Command, the KS9245 may release the ATA bus prior to the completion of that Packet Command. In this case, the KS9245 will use the *Release* bit in its *ATAPI Interrupt Reason Register* (Reg02h, bit2) to inform the host that it has released the ATA bus before completing the command in progress.

Bit 0: DMA

When DMA bit is set, data transfers for the command will use the DMA channel. When the DMA bit is cleared, data transfers for the command will be PIO mode. Firmware uses this bit to configure PIO or DMA mode for host data transfers. The *ATA Transfer Mode* bits in the *Interface Configuration Control Register* (Reg0Bh, bits6,5) are used to select various transfer modes.

Register 01h : ATAPI Error Register (Write)**ATA Error Register (Write)****Acronym:** AERR

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Sense Key				MCR	ABRT	EOM	ILI

The *ATAPI Error Register* contains the errors at the command process or completion stage. The firmware must set the appropriate error bits and Sense Key code when an error occurs in the command processing stage.

Bit 7-4: Sense Key

These bits contain the Sense Key information.

Bit 3: MCR (Media Change Requested)

When this bit is set, it indicates that a media change has occurred.

Bit 2: ABRT (Abort)

When this bit is set, it indicates that the command has been aborted.

Bit 1: EOM (End of Media)

When this bit is set, it indicates that the end of media has been reached.

Bit 0: ILI (Illegal Length Indication)

When this bit is set, it indicates that an illegal length has occurred in the command processing stage.

Register 02: ATA Sector Count Register (Read)

Acronym: ASECC

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ATA Sector Count Register							

The *ATA Sector Count Register* contains the number of sectors to be transferred for the ATA operation. This register is reserved in ATAPI mode.

Register 02: ATAPI Interrupt Reason Register (Write)

Acronym: AINTR

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved					Release	IO	CoD

The *ATAPI Interrupt Reason Register* contains the causes of interrupt when the KS9245 asserts the INTRQ signal to the host. The *ATAPI Interrupt Reason Register* and the *ATAPI Status Register* are interpreted together to indicate the correct ATAPI command phase as follows:

IO	DRQ	CoD	Command Phase
0	1	1	Command From host - command receiving phase
1	1	0	Data To Host - data sending phase
0	1	0	Data From Host - data receiving phase
1	0	1	Completion Status - command completion status

Bit 7-3: Reserved

These bits are reserved for future enhancements

Bit 2: Release

When this bit is set, it indicates to host that the device has released ATA bus prior to completing the current overlapped command.

Bit 1: IO (In/Out)

This bit indicates the direction for the information transfer. When this bit is set, the transfer direction is from the KS9245 to the host. When this bit is reset, the transfer direction is from the host to the KS9245.

Bit 0: CoD (Command/Data)

This bit distinguishes between Command or Data information. When this bit is set, the information being transferred is user data. When this bit is reset, the information transferred is command data.

Register 03: **ATAPI SAM Tag Register (Read/Write)**
 ATA Sector Number (Read/Write)

Acronym: **ASAM**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ATAPI SAM Tag Value (Reserved)							

The *ATAPI SAM Tag Register* contains the SAM Tag number for ATAPI/ATA operations. This register is reserved in ATAPI mode.

Register 04: **ATAPI Byte Count Low Register (Read/Write)**
 ATA Cylinder Low Register (Read/Write)

Acronym: **ABCL**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ATAPI Byte Count Low Register							

The *ATAPI Byte Count Low/High Registers* contain the maximum byte count for each host DRQ packet transfers.

Register 05: **ATAPI Byte Count High Register (Read/Write)**
 ATA Cylinder High Register (Read/Write)

Acronym: **ABCH**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ATAPI Byte Count High Register							

See the *ATAPI Byte Count Low Register* description.

Register 06: **ATAPI Drive Select Register (Read/Write)**
 ATA Drive Select Register (Read/Write)

Acronym: **ADSEL**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Rsvd	LBA	Rsvd	DRV	Reserved for SAM LUN			

Bit 7: Rsvd (Reserved)

This bit is reserved for future enhancements.

Bit 6: LBA (Logic Block Address)

This bit is reserved in ATAPI mode.

Bit 5: Rsvd (Reserved)

This bit is reserved for future enhancements.

Bit 4: DRV (Drive Select)

When this bit is set, it indicates that drive 1 (slave drive) is selected. When this bit is reset, it indicates that drive 0 (master drive) is selected.

Bit 3-0: Reserved for SAM LUN

These bits are reserved for future enhancements.

Register 07: ATAPI Command Register (Read)
ATA Command Register (Read)

Acronym: ACMD

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ATAPI Command Register							

The *ATAPI Command Register* contains the Command Operation Code.

Register 08h: ATAPI Device Control Register (Read)
ATA Device Control Register (Read)

Acronym: ADCV

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved					SRST	nIEN	Rsvd

The *ATAPI Device Control Register* contains the information for ATA soft reset and host interrupt control.

Bit 7-3: Reserved

These bits are reserved for future enhancements.

Bit 2: SRST (ATA Soft Reset)

When the host writes a one to *SRST* bit of the *ATA Device Control Register*, an ATA soft reset is performed.

Bit 1: nIEN (Host Interrupt Enable)

When the host writes a "0" to the *nIEN* bit and the KS9245 selected, the INTRQ signal is enabled. When the host writes a "1" to this bit or the KS9245 is not selected, the INTRQ signal is tri-stated.

Bit 0: Reserved

This bit is reserved for future enhancements.

Register 09h: ATAPI Image Status Register (Read)
ATA Image Status Register (Read)

Acronym: AISTAT

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BSY	DRDY	Rsvd	DSC / SERVICE	DRQ	Corr	Rsvd	CHECK

This register contains an image of the *ATAPI Status Register*. By reading this register, the firmware can obtain the real-time value of the *ATAPI Status Register* in the ATA Task File.

Bit 7: BSY (Busy)

When this bit is set, the KS9245 is busy or in the state of accessing ATA Task File Registers.

Bit 6: DRDY (Drive Ready)

When this bit is set, the drive is capable of responding to a command.

Bit 5: Rsvd (Reserved)

This bit is reserved for future enhancements.

Bit 4: DSC/SERVICE (Disk Seek Complete/Service Request)

This bit is set when a seek operation completes.

Bit 3: DRQ (Data Request)

This bit is set when the KS9245 is ready to transfer data to or receive data from the host.

Bit 2: Corr (Correction Occurred)

This bit is set to indicate that a correctable error occurred during the processing of a command.

Bit 1: Rsvd (Reserved)

This bit is reserved for future enhancements.

Bit 0: CHECK (Check Condition)

This bit is set to indicate that an error occurred during execution of the command.

Register 09h: Host Status Control Register (Write)

Acronym: HSC

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Rsvd	DRDY	Rsvd	DSC / SERVICE	DRQ	Corr	Rsvd	CHECK

The *Host Status Control Register* controls the *ATAPI Status Register* of the ATA Task File.

Bit 7: Rsvd (Reserved)

This bit is reserved for future enhancements.

Bit 6: DRDY (Drive Ready)

When this bit is set, the drive is ready.

Bit 5: Rsvd (Reserved)

This bit is reserved for future enhancement.

Bit 4: DSC/SERVICE (Disk Seek Complete/Service Request)

This bit is set when the seek operation completes.

Bit 3: DRQ (Data Request)

This bit is set when the KS9245 is ready to transfer data to or receive data from the host.

Bit 2: Corr (Correction Occurred)

This bit is set when a correctable error occurs during the processing of the command.

Bit 1: Rsvd (Reserved)

This bit is reserved for future enhancements.

Bit 0: Check (Check Condition)

This bit is set when an error occurs during execution of the command.

Register 0Ah: Host Interface Signal Value Register (Read)

Acronym: HISV

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved				MSTB	DASPB	PDIAGB	0

The *Host Interface Signal Value Register* monitors the ATA interface signals. The microprocessor can read this register to check the state of the MSTB/DASPB/PDIAGB signals. For example, the PDIAGB and DASPB signals are required by firmware to process master/slave handshaking.

Bit 7-4: Reserved

These bits are reserved for future enhancements.

Bit 3: MSTB (MSTB Master/Slave Pin Signal)

This bit reflects the state of the *MSTB* pin. This bit is "1" when the *MSTB* pin is high. This bit is "0" when the *MSTB* pin is low.

Bit 2: DASPB (DASPB Signal of ATA Interface)

This bit reflects the physical state of the *DASPB* pin. When this bit is "1", the *DASPB* pin is high (not asserted). When this bit is "0", the *DASPB* pin is low (asserted).

Bit 1: PDIAGB (PDIAGB Signal of ATA Interface)

This bit reflects the physical state of the *PDIAGB* pin. When this bit is "1", the *PDIAGB* pin is high (not asserted). When this bit is "0", the *PDIAGB* pin is low (asserted).

Bit 0: Reserved

This bit is reserved for future enhancements.

Register 0Ah: Host Interface Control Register (Write)

Acronym: HIC

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SetBSY	SetDASPB	SetPDIAGB	SetHINT	ClrBSY	ClrDASPB	ClrPDIAGB	ClrHINT

The *Host Interface Control Register* controls the *BSY* status of the ATA Status Register and the *PDIAGB*, *DASPB* and *INTRQ* pins of ATA interface signals.

Bit 7: SetBSY (Set BSY Status of ATA Task File Registers)

When this bit is set, the KS9245 sets the *BSY* bit of *ATA Status Register*.

Bit 6: SetDASPB (Set DASPB Signal of ATA Interface)

When this bit is set, the KS9245 asserts its *DASPB* pin low.

Bit 5: SetPDIAGB (Set PDIAGB Signal of ATA Interface)

When this bit is set, the KS9245 asserts its *PDIAGB* pin low.

Bit 4: SetHINT (Set INTRQ Signal of ATA Interface)

When this bit is set, the KS9245 asserts its INTRQ pin high.

Bit 3: ClrBSY (Clear BSY Status of ATA Task File Registers)

When this bit is set, the KS9245 clears the *BSY* bit of *ATA Status Register*.

Bit 2: ClrDASPB (Clear DASPB Signal of ATA Interface)

When this bit is set, the KS9245 drives the DASPB pin high and then releases it.

Bit 1: ClrPDIAGB (Clear PDIAGB Signal of ATA Interface)

When this bit is set, the KS9245 drives the PDIAGB pin high and then releases it.

Bit 0: ClrHINT (Clear INTRQ Signal of ATA Interface)

When this bit is set, the KS9245 negates its INTRQ pin low.

Register 0Bh: Interface Configuration Control Register (Read)
Interface Configuration Control Register (Write)

Acronym: ICC

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IntMode	ATA Transfer Mode		CDRV	SShadow	DisShadR	PcmdInt	DisIORDY

The *Interface Configuration Control Register* is used by firmware to inform the KS9245 with specific drive configuration such as master/slave drive and PIO/DMA etc..

Bit 7: IntMode (Interrupt Signal Mode Control)

When this bit is cleared, all interrupt events (including disk, host, and buffer) are reported via asserting the HINTB pin. When this bit is set, interrupt events from disk/decoder are reported via asserting DINTB pin while host/buffer interrupt events are reported via asserting the HINTB pin.

Bit 6-5: ATA Transfer Mode

These two bits specify the various ATA transfer modes.

ATA PIO/DMA Mode Selection Table		
Bit 6	Bit 5	ATA data transfer mode
0	0	PIO Transfer Mode (Default)
0	1	Single Word DMA Transfer Mode
1	1	Multiword DMA Transfer Mode
1	0	Ultra DMA Transfer Mode

Bit 4: CDRV (Controller Drive Configuration)

When this bit is set, the KS9245 is configured as drive 1 (slave drive). When this bit is cleared, the KS9245 is configured as drive 0 (master drive).

Bit 3: SShadow (Slave Shadow Feature Enabled)

This bit is used together with the *CDRV* bit. The following table summarizes the function of this bit.

Summary for Drive Configuration		
CDRV- Bit 4	Sshadow- Bit 3	Drive Operation Mode
0	0	master only mode with Shadow feature disabled
0	1	master only mode with Shadow feature enabled
1	X	slave drive mode

Bit 2: DisShadR (Disable Shadow Auto Response)

When the *DisShadR* bit is cleared, the *SShadow* bit is set, the *CDRV* bit is cleared, and the host issues a command to the non-existent slave drive, the KS9245 responds to the shadow command sequence automatically. When both *DisShadR* and *SShadow* bits are set, the auto shadow response sequence is disabled

Bit 1: PcmdInt (ATAPI Packet Command host interrupt enable Mode)

When this bit is set and the drive is selected, a HINTRQ is generated when the KS9245 is ready to receive the 12-byte command packet.

Bit 0: DisIORDY (Disable IO Ready Signal)

When this bit is set, the IORDY pin is disabled.

Register 0Ch: Reserved

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved							

This register is reserved.

Register 0Dh: Reserved

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved							

This register is reserved.

Chapter 3

Hardware Sequence Command Registers

Register 0Eh : Host Sequence Command Register (Write)
Acronym: HSC

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Rsvd	SAAabort	Sservice	Srelease	STFInit	SCpl	SCplChk	SDSC

The *Host Sequence Command Register* is used to start the hardware ATAPI interface sequence. By using the features in this register, firmware overhead can be minimized and command operations accelerated. Each of these operations are performed immediately after a "1" is written to the corresponding bit. Therefore, polling is not required to check completion. Writing a "0" to these bits will not cause any operation.

Bit 7: Reserved

This bit is reserved for the future enhancements.

Bit 6: SAAabort (Start ATA Abort Operation)

When this bit is set, the KS9245 automatically aborting ATA illegal commands.

Bit 5: Sservice (Start ATAPI Service Operation)

When this bit is set, the KS9245 automatically performs the ATAPI Service sequence in overlapped command operation.

Bit 4: Srelease (Start ATAPI Release Operation)

When this bit is set, the KS9245 automatically performs the ATAPI Release sequence in overlapped command operation.

Bit 3: STFInit (Task File Registers Initialized)

When this bit is set, the KS9245 initializes the ATA Task File Registers.

Bit 2: SCpl (Start Command Completion with no Error Setting)

When this bit is set, the KS9245 performs the ATAPI command completion without check condition sequence.

Bit 1: SCplChk (Start Command Completion with Error Setting)

When this bit is set, the KS9245 performs the ATAPI command completion with check condition sequence.

Bit 0: SDsc (Set DSC bit for Seek Completion Operation)

When this bit is set, the KS9245 performs the ATAPI seek command completion sequence.

Register 0Fh : Transfer Sequence Command Register (Write)
Acronym: TSC

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ACacheE	ACpIE	Rsvd	SSxfr	Sabort	SPause	WRDir	SDxfr

The *Transfer Sequence Command Register* is used to start or control the ATAPI host transfer operations.

Bit 7: ACacheE (Automated Cache Control)

When the *ACacheE* bit is "1", the Auto Cache Mode is enabled and host transfers are completely automated.

When the *ACacheE* bit is "0", the Auto Cache Feature is disabled.

Bit 6: ACpIE (Automated Command Completion Enabled)

When this bit is set, the ATAPI command completion sequence will automatically start when any of the following events occur:

- The *Total Host Transfer Length Register* is decreased to zero when the host transfer is in the Data Area and initialized by setting the *SDxfr* bit in the *Transfer Sequence Command Register* (0Fh, bit 0).
- The host transfer is in the System Area and initialized by setting the *SSxfr* bit in *Transfer Sequence Command Register* (0Fh, bit 4).

Bit 5: Reserved

This bit is reserved for future enhancements.

Bit 4: SSxfr (Start Host Transfer Operation in System Area)

When this bit is "1", the KS9245 starts host transfer operations to / from the System Area.

Bit 3: SAbort (Start Transfer Abort Operation)

This function is used to abort the host transfer in an emergent occasion such as an abort command or eject disc occurrence. When this bit is set, the KS9245 aborts the current host transfer operation immediately.

Bit 2: SPause (Start Host Transfer Pause Operation)

When this bit is set, the KS9245 pauses the host transfer operation when the transfer in the *Current Host Transfer Length Register* (18h) are complete.

Bit 1: WRDir (Write/Read Direction Control)

When this bit is set, the host is transferring data to KS9245. When this bit is reset, the host is reading data from the KS9245.

Bit 0: SDxfr (Start Host Transfer Operation in Data Area)

When this bit is set, the KS9245 starts host block transfer operations.

Register 0Fh : Transfer Sequence Status Register (Read)**Acronym: TSS**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ACacheE	ACpIE	Reserved			SPause	WRDir	HxfrBsy

The *Transfer Sequence Status Register* indicates the status of the *Transfer Command Register*.

Bit 7: ACacheE (Automated Cache Control)

When this bit is set, Auto Cache is enabled. When this bit is reset, Auto Cache is disabled.

Bit 6: ACpIE (Automated Command Completion Enabled)

When this bit is set, the automated ATAPI Command Completion Sequence is enabled. When this bit is reset, the automated ATAPI Command Completion Sequence is disabled.

Bit 5-3: Reserved

These bits are reserved for future enhancements.

Bit 2: SPause (Start Host Transfer Pause Operation)

When this bit is set, the transfer pause operation is in process. When this bit is reset, no pause operation is performed.

Bit 1: WRDir (Write/Read Direction Control)

When this bit is set, the transfer operation is a write from the host to the KS9245. When this bit is reset, the transfer operation is a read from the KS9245 to the host.

Bit 0: HxfrBsy (Host Transfer Operation Busy)

When this bit set, the host transfer operation is in progress. When this bit is cleared, the host transfer has completed.

Chapter 4

Microprocessor Interface Registers

Register 10h: **Host Interrupt Status Register (Read)**
 Host Interrupt Clear Register (Write)

Acronym: **HISR/HICR**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxfrDone	Reserved	Asrst	Srst	Hrst	ScmdRcv	AcmdRcv	PcmdRcv

This register informs firmware of various interrupts which are reported by the KS9245. Writing a "1" to any bit clears that respective interrupt. Writing a "0" to any bit causes no change for that respective interrupt.

Bit 7: TxfrDone (Total Host Request Transfer Done)

This bit is set when one of the following events occur:

- Data Area Transfer Completed.
- System Area Transfer Completed.
-

Bit 6: Reserved

This bit is reserved for future enhancements.

Bit 5: Asrst (ATAPI Soft Reset Command (08h) received)

This bit is set when the host writes the ATAPI Soft Reset Command (08h) into *ATAPI Command Register (07h)* while the drive is selected.

Bit 4: Srst (ATA SRST Reset)

This bit is set when the *SRST* bit in the *Device Control Register (08h, bit 2)* is set by the host.

Bit 3: Hrst (Host Reset)

This bit is set when the *HRSTB* pin is asserted.

Bit 2: ScmdRcv (Shadow Command received)

This bit is set when the host writes a command byte into the *ATAPI Command Register (07h)* of the non-existent slave drive.

Bit 1: AcmdRcv (ATA Command received)

This bit is set when the host writes a command in the *ATAPI Command Register (07h)* while the drive selected.

Bit 0: PcmdRcv (ATAPI Packet Command received)

This bit is set when the host writes the Packet Command (A0h) into the *ATAPI Command Register (07h)* while the drive selected.

**Register 11h: Decoder Interrupt Status Register (Read)
Decoder Interrupt Clear Register (Write)****Acronym: DISR/DICR**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved					DACInt	SubInt	Declnt

This register informs the firmware of various CD decoder interrupts reported by the KS9245. Writing a "1" to any bit clears that respective interrupt. Writing a "0" to any bit causes no change for that respective interrupt.

Bit 7-3: Reserved

These bits are reserved for future enhancements.

Bit 2: DACInt (Audio DAC Output Interrupt)

This bit is set when one block of audio data (2352 byte) is output to the external audio DAC via the AWCK/ABCK/ADAT pins.

Bit 1: SubInt (CD Subcode Interrupt)

This bit is set when the CD Subcode interrupt occurs.

Bit 0: Declnt (CD Decoder Interrupt)

This bit is set when a CD decoder interrupt occurs.

**Register 12h: Host Interrupt Mask Register (Read)
Host Interrupt Mask Register (Write)****Acronym: HIM**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxfrDoneE	CxfrDoneE	AsrstE	SrstE	HrstE	ScmdRcvE	AcmdRcvE	PcmdRcvE

This register controls the masking for each interrupt source. Writing a "1" to each bit enables the interrupt for that corresponding function. Writing a "0" to each bit, disables the interrupt for that corresponding function.

Bit 7: TxfrDoneE (Total Host Request Transfer Done Enable)

When this bit is set, the *TxfrDone* interrupt (10h, bit 7) is enabled. When this bit is reset, the *TxfrDone* interrupt is disabled.

Bit 6: CxfrDoneE (Host Block Transfer Done Interrupt Enable)

When this bit is set, the *CxfrDone* interrupt (10h, bit 6) is enabled. When this bit is reset, the *CxfrDone* interrupt is disabled.

Bit 5: AsrstE (ATAPI Soft Reset Command Interrupt Enabled)

When this bit is set, the *Asrst* interrupt (10h, bit 5) is enabled. When this bit is reset, the *Asrst* interrupt is disabled.

Bit 4: SrstE (ATA SRST Reset Interrupt Enabled)

When this bit is set, the *Srst* interrupt (10h, bit 4) is enabled. When this bit is reset, the *Srst* interrupt is disabled.

Bit 3: HrstE(ATA Host Rest Interrupt Enabled)

When this bit is set, the *Hrst* interrupt (10h, bit 3) is enabled. When this bit is reset, the *Hrst* interrupt is disabled.

Bit 2: ScmdRcvE (Shadow Command Interrupt Enabled)

When this bit is set, the *ScmdRcv* interrupt (10h, bit 2) is enabled. When this bit is reset, the *ScmdRcv* interrupt is disabled.

Bit 1: AcmdRcvE (ATA Command Interrupt Enabled)

When this bit is set, the *AcmdRcv* (10h, bit 1) interrupt is enabled. When this bit is reset, the *AcmdRcv* interrupt is disabled.

Bit 0: PcmdRcvE (ATAPI Packet Command Interrupt Enabled)

When this bit is set, the *PcmdRcv* interrupt (10h, bit 0) is enabled. When this bit is reset, the *PcmdRcv* interrupt is disabled.

Register 13h: Decoder Interrupt Mask Register (Read)
Decoder Interrupt Mask Register (Write)

Acronym: DIM

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved					DACIntE	SubIntE	DeclntE

This register controls the masking for each interrupt source. Writing a "1" to each bit enables the interrupt for that corresponding function. Writing a "0" to each bit, disables the interrupt for that corresponding function.

Bit 7-3: Reserved

These bits are reserved for future enhancements.

Bit 2: DACIntE (Audio DAC Output Interrupt Enable)

When this bit is set, the *DACInt* interrupt (11h, bit 2) is enabled. When this bit is reset, the *DACInt* interrupt is disabled.

Bit 1: SubIntE (CD Subcode Interrupt Enabled)

When this bit is set, the *SubInt* interrupt (11h, bit 1) is enabled. When this bit is reset, the *SubIntE* interrupt is disabled.

Bit 0: Declnt (CD Decoder Interrupt)

When this bit is set, the *Declnt* interrupt (11h, bit 0) is enabled. When this bit is reset, the *Declnt* interrupt is disabled.

Chapter 5

Buffer/CD Cache Manager Registers

Register 14h : **Valid Cache Block Count Register (Read)**
 Valid Cache Block Count Register (Write)

Acronym: **VCBC**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Valid Cache Block Count Register B7:B0							

The *Valid Cache Block Count Register* indicate the number of valid blocks in the buffer DRAM. These blocks have passed either ECC correction or EDC check and are ready to be transferred to the host.

Register 15h : **Reserved**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved							

This register is reserved for future enhancements.

Register 16h : **Total Host Transfer Block Length Register (Read)**
 Total Host Transfer Block Length Register (Write)

Acronym: **TTBL**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Total Host Transfer Block Length Register B7:B0							

The *Total Host Transfer Length Register* indicate the remaining block length to be transferred between the host and the drive before finishing an ATAPI Read (12h) or Read CD (BEh) Command.

Register 17h : **Reserved**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved							

This register is reserved for future enhancements.

Register 18h : **Current Host Transfer Block Length Register (Read)**
Current Host Transfer Block Length Register (Write)

Acronym: **CHTB**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Current Host Transfer Block Length Register B7:B0							

The *Current Host Transfer Block Length Register* specify the current number of blocks to be transferred between the host and the drive for the current host transfer.

Register 19h : **Reserved**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved							

This register is reserved for future enhancements.

Register 1Ah : **Host Transfer Block Address Low Register (Read)**
Host Transfer Block Address Low Register (Write)

Acronym: **HTBAL**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Host Transfer Block Address Low Register B7:B0							

See *Host Transfer Block Address High Register*.

Register 1Bh : **Reserved**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved							

This register is reserved.

Register 1Ch : **Host Block Offset Address Low 1 Register (Read)**
Host Block Offset Address Low 1 Register (Write)

Acronym: **HBOAL1**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Host Block Offset Address Low 1 Register B7:B0							

See *Host Block Offset Address High 1 Register*.

Register 1Dh : Host Block Offset Address High 1 Register (Read)
Host Block Offset Address High 1 Register (Write)

Acronym: HBOAH1

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved				B11	B10	B9	B8

The *Host Block Offset Address Low/High Registers* specify the starting offset address of the first segment within a block in the buffer DRAM.

Register 1Eh : Transfer Offset Length Low 1 Register (Read)
Transfer Offset Length Low 1 Register (Write)

Acronym: TOLL1

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transfer Offset Length Low 1 Register B7:B0							

See the *Transfer Offset Length High 1 Register*.

Register 1Fh : Transfer Offset Length High 1 Register (Read)
Transfer Offset Length High 1 Register (Write)

Acronym: TOLH1

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved				B11	B10	B9	B8

The *Transfer Offset Length Low/High 1 Registers* (1Eh, 1Fh) specify the number of continuous bytes to be transferred to the first segment.

Register 20h : Host Block Offset Address Low 2 Register (Read)
Host Block Offset Address Low 2 Register (Write)

Acronym: HBOAL2

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Host Block Offset Address Low 2 Register B7:B0							

See *Host Block Offset Address High 2 Register*

Register 21h : Host Block Offset Address High 2 Register (Read)
Host Block Offset Address High 2 Register(Write)

Acronym: HBOAH2

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved				B11	B10	B9	B8

The *Host Block Offset Address Low/High 2 Registers* specify the starting transfer offset address after finishing the transfer for the first segment.

Register 22h : Transfer Offset Length Low 2 Register (Read)
Transfer Offset Length Low 2 Register (Write)

Acronym: TOLL2

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transfer Offset Length Low 2 Register B7:B0							

See *Transfer Offset Length High 2 Register*

Register 23h : Transfer Offset Length High 2 Register (Read)
Transfer Offset Length High 2 Register (Write)

Acronym: TOLH2

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved				B11	B10	B9	B8

The *Transfer Offset Length Low/High 2 Registers* specify the continuous number of bytes to be transferred, after finishing the first segment.

Register 24h : MP Access Physical Address LSB Register(Read)
MP Access Physical Address LSB Register(Write)

or

MP Block Offset Address Low Register (Read)
MP Block Offset Address Low Register (Write)

Acronym: MPALSB
MBOAL

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MP Access Physical Address LSB B7:B0							
MP Block Offset Address Low Register B7:B0							

These registers specify the DRAM physical address or block address when the microprocessor wants to access the DRAM.

Register 25h : **MP Access Physical Address MID (Read)**
 MP Access Physical Address MID (Write)
 or
 MP Block Offset Address High Register (Read)
 MP Block Offset Address High Register (Write)

Acronym: **MPAMID**
 MBOAH

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MP Access Physical Address MID B15:B8							
Reserved				MP Block Offset Address High Register B11:B8			

See *MP Access Physical LSB Register (24h)*.

Register 26h : **MP Access Physical Address MSB (Read)**
 MP Access Physical Address MSB (Write)
 or
 MP Block Address Register (Read)
 MP Block Address Register (Write)

Acronym: **MPAMSB**
 MBA

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved				DRAM Access Physical Address MSB B18:B16			
MP Block Address Register B7:B0							

In Block Addressing mode, the *MP Block Address* register specify the block address in buffer DRAM. Also, refer to the *MP Access Physical LSB Register (24h)* description.

Register 27h : **Reserved**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved							

This register is reserved for future enhancements.

Register 28h : **MP Access Data Port Register (Read)**
 MP Access Data Port Register (Write)

Acronym: **MPDP**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MP Access Data Port B7:B0							

The *MP Access Data Port Register* is used to access the content of the DRAM for both read and write operations.

Register 29h : **Buffer Access Control Register (Read)**

Acronym: **BAC**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DramBsy	Reserved				PAMb	Rsvd	Rsvd

Bit 7: DramBsy (DRAM Busy Status)

This bit set when the DRAM is busy.

Bit 6-3: Reserved

These bits are reserved for future enhancements.

Bit 2: PAMb (Physical Addressing Mode Disabled)

When this bit is reset, Physical Addressing Mode (PAM) is used for DRAM accesses by the microprocessor. When this bit is set, Block Addressing Mode (BAM) is used for DRAM accesses by the microprocessor. Also, refer to the *MP Access Physical Address LSB Register (24h)* description.

Bit 1-0: Reserved

These bits are reserved for future enhancements.

Register 29h : **Buffer Access Control Register (Write)**

Acronym: **BAC**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IncAudCnt	IncBlkCnt	Reserved			PAMb	SDramWrt	SDramRd

Bit 7: IncAudCnt

Writing a "1" to this bit increments the *Valid Audio Block Count Register (48h)* by one. Writing a "0" to this bit causes no operation.

Bit 6: IncBlkCnt

Writing a "1" to this bit increments the *Valid Cache Block Count Register (14h)* by one.

Bit 5-3: Reserved

These bits are reserved for future enhancements.

Bit 2: PAMb (Physical Addressing Mode Disabled)

Writing a “0” to this bit places the KS9245 into Physical Addressing Mode (PAM) for DRAM accesses. Writing a “1” to this bit places the KS9245 into Block Addressing Mode (BAM) for DRAM accesses.

Bit 1: SDramWrt (Start DRAM Write)

Writing a “1” to this bit causes the KS9245 to start the DRAM write operation.

Bit 0: SDramRd (Start DRAM Read)

Writing a “1” to this bit causes the hardware to start the DRAM read operation.

Register 2Ah : Buffer Configuration Control 1 Register (Read)
Buffer Configuration Control 1 Register (Write)

Acronym: BCC1

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
C2ErrOR	Dsel	Ssel	Csel	BlkConf	Dramsz		
C2ErrOR	DSP Channel Sel			BlkConf	Dramsz		

The *Buffer Configuration Control 1 Register* specifies the DRAM size and configuration.

Bit 7: C2ErrOR(C2 Error Block OR Format)

When this bit is set, the first byte of C2 Block Error is the result of logically ORing all of the C2 Error Flag bytes. When this bit is cleared, the first byte of the C2 Block Error is the longitudinal parity (XOR) of all the C2 Error Flag bytes.

Bit 6-4 : DSP Channel Sel (DSP Channel Select for Buffering)

The *DSP Channel Sel* bits select various DSP data channels to be buffered when the decoder is in Buffer Only / ECC / Audio Buffering / Test Modes.

Bit 6: Dsel (Data Channel Select DSP for Buffering)

Writing a “1” to this bit selects the DSP main data channel for buffering. Writing a “0” to this bit disables the DSP main data channel and prevents it from being buffered.

Bit 5: Ssel (Subcode Channel Select DSP for Buffering)

Writing a “1” to this bit selects the DSP subcode channel for buffering. Writing a zero to this bit disables the DSP subcode channel and prevents it from being buffered.

Bit 4: Csel (C2PO Channel Select DSP for Buffering)

Writing a “1” to this bit, selects the DSP C2PO error flags for buffering. Writing a “0” to this bit prevents the DSP C2PO error flags from being buffered.

Bit 3: BlkConf (DRAM Block Configuration)

This bit configures the CD Block size in DRAM. When this bit is set, each CD Block size is partitioned as 2.5K (2560 bytes). When this bit is cleared, each CD Block size is partitioned as 3K (3072 bytes).

Bit 2-0: Dramsz (DRAM Size Selection)

These bits specify the DRAM size.

Register 2Bh : Reserved

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DRCD1							

The register is reserved.

**Register 2Ch : Buffer Bottom Block Address Register(Read)
Buffer Bottom Block Address Register(Write)**
Acronym: BBBA

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Buffer Bottom Block Address Register							

The *Buffer Bottom Block Address Register* configures the end or the last CD block address in DRAM.

Register 2Dh : Reserved

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved							

This register is reserved for future enhancements.

**Register 2Eh : DRAM Refresh Control Register (Read)
DRAM Refresh Control Register (Write)**
Acronym: DRCR

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DRAM Refresh Control Register							

The DRAM Refresh Control Register is used to program the DRAM refresh period.

**Register 2Fh : Global Control Register (Write)
Global Control Register (Read)**
Acronym: GCR

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SSleep	SFReset	BurstNum	Dspbust	APCE	Cspeed[2:0]		

The *Global Control Register* controls power management, DRAM arbitration mode, and soft reset operation.

Bit 7: SSleep (Start Sleep Mode)

When this bit is set to "1", the KS9245 enters sleep mode immediately. Writing a "0" to this bit causes the KS9245 to wake to normal operation.

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Bit 6: SFReset (Start Firmware Reset)

Writing a "1" to this bit causes a firmware reset for the KS9245.

Bit 5: BurstNum - Host DRAM page access burst (Byte) Size

Refer to KS9245 Performance Table below.

Bit 4: DspBurst - CD Buffer to DRAM burst size

Refer to KS9245 Performance Table below.

Bit 3: APCE (Audio Port Configuration Enable)

When this bit is set, the GP0, GP1, GP2, and GP3 pins are configured as the AWCK, ABCK, ADAT, and DAUO pins for the audio word clock, bit clock, data, and digital audio output to an external DAC, respectively.

Bit 2-0: Cspeed[2:0] - Adjust Arbiter's Priority Scheme

Refer to KS9245 Performance Table below.

KS9245 Performance Table

System Clock	Dram Type	Max Disk Speed	BurstNum,DspBurst Cspeed[2:0] Programming Value	Sustain Mode	Max Host Mode
33.8 MHz	60ns Fast Page	34 X	[0, 0, 0, 0, 0]	PIO4 / DMA2	Ultra DMA2
33.8 MHz	45ns Fast Page 50ns EDO	37 X	[0, 0, 0, 0, 0]	PIO4 / DMA2	Ultra DMA2
50.8 MHz	40ns EDO	50 X	[0, 0, 0, 0, 0]	Ultra DMA1	Ultra DMA2
50.8 MHz	45ns Fast Page 50ns EDO	45 X	[0, 0, 0, 0, 0]	Ultra DMA1	Ultra DMA2
50.8 MHz	40ns EDO	35 X	[0, 1, 1, 0, 0]	Ultra DMA2	Ultra DMA2
50.8 MHz	45ns Fast Page 50ns EDO	32 X	[0, 1, 1, 0, 0]	Ultra DMA2	Ultra DMA2

Chapter 6

CD Block Decoder Registers

Register 30h : Decoder Header Min Register (Read)

Acronym: DHMIN

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Decoder Header Min Register							

The *Decoder Header Min Register* contains the Minute byte of the CD Header information. This register is valid only after a CD decoder interrupt occurs.

Register 31h : Decoder Header Sec Register (Read)

Acronym: DHSEC

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Decoder Header Second Register							

The *Decoder Header Sec Register* contains the Second byte of the CD Header information.

Register 32h : Decoder Header Frame Register (Read)

Acronym: DHFRAME

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Decoder Header Frame Register							

The *Decoder Header Frame Register* contains the Frame byte of the CD Header information.

Register 33h : Decoder Header Mode Register (Read)

Acronym: DHMODE

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Decoder Header Mode Register							

The *Decoder Header Mode Register* contains the Mode byte of the CD Header information.

Register 34h : Decoder Subheader 0 Register (Read)**Acronym: DSUBH0**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Decoder Subheader 0 Register							

The *Decoder Subheader 0 Register* contains the first byte of the subheader, which is the File Number byte. This register is valid only after a CD decoder interrupt occurs.

Register 35h : Decoder Subheader 1 Register (Read)**Acronym: DSUBH1**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Decoder Subheader 1 Register							

The *Decoder Subheader 1 Register* contains the second byte of the subheader, which is the Channel Number byte.

Register 36h : Decoder Subheader 2 Register (Read)**Acronym: DSUBH2**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Decoder Subheader 2 Register							

The *Decoder Subheader 2 Register* contains the third byte of the subheader, which is the Submode byte.

Register 37h : Decoder Subheader 3 Register (Read)**Acronym: DSUBH3**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Decoder Subheader 3 Register							

The *Decoder Subheader 3 Register* contains the fourth byte of the subheader, which is Coding Information byte.

Register 38h : Disk Transfer Block Address Register (Read)**Disk Transfer Block Address Register (Write)****Acronym: DTBA**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Disk Transfer Block Address Register							

The *Disk Transfer Block Address Register* indicate the block address of the incoming DSP data currently being buffered.

Register 39h : Reserved

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved							

This register is reserved for future enhancements.

Register 3Ah : **Decoder Control Register (Read)**
 Decoder Control Register (Write)

Acronym: **DCR**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved		SubMon	AudWrt	ECCRQ	DecWrt	Decen	Decsen

This register is used to control the CD decoder operation. The CD decoder stays in one of the following modes:

Stop Mode :

In Stop Mode, the decoder completely stopped. Refer to Decoder Operation State Table below.

Data Monitor Mode:

In Monitor Mode, the decoder and descrambler operations are active. Refer to Decoder Operation State Table below.

Buffering Only Mode:

In Buffering Only Mode, the decoder and descrambler operations are active. Refer to Decoder Operation State Table below.

Audio Buffering Mode:

In Audio Buffering Mode, the *Dsel* bit in the *Buffer Configuration Control 1 Register* (2Ah, bit 6) must be set. Refer to Decoder Operation State Table below.

Subcode Monitor Mode:

If the *SubMon* bit is set and the *AudWrt* bit is cleared, the decoder is in the Subcode Monitor Mode. Refer to Decoder Operation State Table below.

ECC Mode:

In ECC Mode, the decoder and descrambler operations are active. Refer to Decoder Operation State Table below.

Test Mode:

In Test Mode, the decoder operation is active while the descrambler logic is disabled. Refer to Decoder Operation State Table below.

Decoder Operation State						
SubMon	AudWrt	ECCRQ	DecWrt	Decen	Decscen	Operation Status
0	0	0	0	0	0	Decoder Stop Mode
0	0	0	0	1	1	Monitor Mode
0	0	0	1	1	1	Buffering Only Mode
0	1	x	x	x	x	Audio Buffering Mode
1	0	x	x	x	x	Subcode Monitor Mode
0	0	1	1	1	1	ECC Mode
0	0	0	1	1	0	Test Mode
Other Values						Invalid Mode

Bit 7-6: Reserved

These bits are reserved for future enhancement.

Bit 5: SubMon (Subcode Monitor Mode Enable)

When this bit is set and the AudWrt bit is cleared, the decoder is placed into the Subcode Monitor Mode.

Bit 4: AudiWrt (Audio Buffer Mode Enable)

When this bit is set, the KS9245 will buffer the CD-DA data.

Bit 3: ECCRQ (Error Correction Request)

Writing a "1" to this bit when both the *Decen* and *DecWrt* bits are set causes the decoder logic to switch into ECC Mode.

Bit 2: DecWrt (Decoder Writing/Buffering Enable)

Writing a "1" to this bit when the *Decen* bit is set causes the buffering for the main data streams, DSP subcode, C2PO Error Flags to become active.

Bit 1: Decen (Decoder Operation Enable)

When this bit set, the CD decoder operation is active for processing the incoming DSP data.

Bit 0: Descen (Descrambler Enabled)

When this bit set, the descrambler logic is active.

Register 3Bh : **ECC Control 1 Register (Read)**
 ECC Control 1 Register (Write)

Acronym: **ECC1**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
XAMode	Reserved			Edcen	EccPen	EccQen	EraCorr

The *ECC Control 1 Register* controls the ECC, EDC, and decoder operations.

Bit 7: XAMode (CD XA Data Mode Enable)

When this bit cleared, the ECC/EDC logic assumes the data block is Yellow Book Mode 0,1,2. When this bit is set, the ECC/EDC logic assumes the data block is either XA Mode 2 Form 1 or Mode 2 Form 2.

Bit 6-4: Reserved

These bits are reserved for future enhancements.

Bit 3: Edcen (EDC Check Enable)

When this bit is set, the EDC Checker is enabled and the KS9245 performs an EDC check after the ECC operation completes.

Bit 2: EccPen (ECC P Parity Check)

When this bit set, the ECC P Parity Checker is enabled and the ECC logic will correct the data using the P Codewords.

Bit 1: EccQen (ECC Q Parity Check)

When this bit set, the ECC Q Parity Checker is enabled and the ECC logic will correct the data using the Q Codewords.

Bit 0: EraCorr (C2PO Erasure Correction Enable)

When this bit is cleared, the C2PO error flags are not used for correction reference.

Register 3Ch : ECC Control 2 Register (Read)
ECC Control 2 Register (Write)

Acronym: ECC2

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved			PacketWr	ASynWrt	RepCorr	Rsvd	DisCowr

The *ECC Control 2 Register* controls special decoder operations.

Bit 7-5: Reserved

These bits are reserved for future enhancements.

Bit 4: PacketWr (Packet Writing Blocks Start/Stop)

When this bit is set, KS9245 will start reading CD-WO disc with packet writing.

Bit 3: ASynWrt (Audio Synchronized Buffering)

When this bit is set, the writing or buffering of CD-DA data is delayed until the first subcode in the incoming DSP subcode stream is detected.

Bit 2: RepCorr (Repeat Correction Start)

The *RepCorr* bit triggers the repeat correction feature.

Bit 1: Reserved

This bit is reserved for future enhancements.

Bit 0: Reserved

This bit is reserved for future enhancements.

Register 3Dh : ECC Status Register (Read)**Acronym: ECCS**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
InValid	OVErr	EccFat	EccErr	CBlk	NoSync	IllSync	Rsvd

The *ECC Status Register* is used to provide the results of ECC and EDC operations.

Bit 7: InValid (ECC Status information Invalid)

This bit is set when the succeeding ECC or DSP status has overwritten the *ECC Status Register* before firmware has read the status.

Bit 6: OVerErr (DSP FIFO Overflow Error)

This bit is set when a FIFO overflow error occurs in the DSP interface.

Bit 5: EccFat (Fatal Error in ECC logic)

This bit is set when the ECC logic detected a fatal error.

Bit 4: EccErr (Uncorrectable Error block)

When this bit is set, there is an uncorrectable error in the data block.

Bit 3: CBlk (Corrected Block)

This bit is set when one or more error bytes have been corrected by the last ECC operation.

Bit 2: NoSync (No Sync Error)

This bit is set when the sync pattern was not detected in its expected location.

Bit 1: IllSync (Illegal Sync Error)

This bit is set when the sync pattern is not detected as expected.

Bit 0: Reserved

This bit is reserved for future enhancements.

Register 3Eh : DSP Device Type Selection Register (Read)
DSP Device Type Selection Register (Write)

Acronym: DOTS

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Rsvd	BCKD1	FPS	BCKLength		LSBF	LCH	BCKF

The *DSP Device Type Selection Register* selects various CD DSP and Subcode Interface formats.

Bit 7: Reserved

This bit is reserved for future enhancements.

Bit 6: BCKD1 (BCK data sampling delay one clock)

When this bit is set, the data is delayed by one BCK clock in sampling.

Bit 5: FPS (Forward Packet Stream)

When this bit is set, the main data stream is a forward packet stream.

Bit 4-3: BCKLength (Clock Length)

These bits specify the DSP main channel Clock Length.

Bit 2: LSBF (Main Channel Data LSB byte comes first)

When this bit is set, the KS9245 takes the first byte of the DSP channel data as the LSB and the second byte as the MSB on the SDATA Pin. When this bit is cleared, the KS9245 takes the first byte of the DSP channel data as the MSB and the second byte as the LSB on the SDATA Pin.

Bit 1: LCH (Left Channel High)

When this bit is set, a high level on the LRCK pin indicates the left channel. When this bit is cleared, a high level on the LRCK pin indicates the right channel.

Bit 0: BCKF (Data Latched on Falling Edge)

When this bit is set, the data is valid on the falling edge of the BCK signal. When this bit is cleared, the data is valid on the rising edge of the BCK signal.

Register 3Fh : Decoder Header Erasure Register (Read)

Acronym: DHER

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ESH0	ESH1	ESH2	ESH3	Emin	Esec	Eframe	Emode

The Decoder Header Erasure Register contains the error flags for the header or subheader of the data block.

Bit 7: ESH0 (Error flag for Subheader 0 - File Number)

When this bit is set, the error flag of the File Number Byte in both subheaders is set. When this bit is cleared, the error flag of the File Number Byte in either of the subheaders is cleared

Bit 6: ESH1 (Error flag for Subheader 1 - Channel Number)

When this bit is set, the error flag of the Channel Number Byte in both subheaders is set. When this bit is cleared, the error flag of the Channel Byte in either of the subheaders is cleared.

Bit 5: ESH2 (Error flag for Subheader 2 - Submode)

When this bit is set, the error flag of the Submode Byte in both subheaders is set. When this bit is cleared, the error flag of the Submode Byte in either of the subheaders is cleared.

Bit 4: ESH3 (Error flag for Subheader 3 - Coding Information)

When this bit is set, the error flag of the Coding Information Byte in both subheaders is set. When this bit is cleared, the error flag of the Coding Information Byte in either of the subheaders is cleared.

Bit 3: Emin (Error flag for Header Min Byte)

When this bit is set, the error flag of the Header Min Byte is set. When this bit is cleared, the error flag of the Header Min Byte is cleared.

Bit 2: Esec (Error flag for Header Sec Byte)

When this bit is set, the error flag of the Header Sec Byte is set. When this bit is cleared, the error flag of the Header Sec Byte is cleared.

Bit 1: Eframe (Error flag for Header Frame Byte)

When this bit is set, the error flag of the Header Frame Byte is set. When this bit is cleared, the error flag of the Header Frame Byte cleared.

Bit 0: Emode (Error flag for Header Mode Byte)

When this bit is set, the error flag of the Header Mode Byte is set. When this bit is cleared, the error flag of the Header Mode Byte is cleared.

Register 40h : Reserved

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved							

This register is reserved.

Register 41h : Subcode Status Register (Read)

Acronym: SSR

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SCrcErr	SubErr	Reserved					

The *Subcode Status Register* provides the results of subcode operations.

Bit 7: SCrcErr (Subcode CRC Error)

When this bit is set, a CRC error exists in the Q channel subcode. When this bit is cleared, no CRC error exists in the Q channel subcode.

Bit 6: SubErr (Subcode Buffer Error)

When this bit is set, one of the following errors occurred:

- A subcode sync word is not found.

- A subcode sync indication comes either earlier or later than the 96 byte subcode data.

Bit 5-0: Reserved

These bits are reserved for future enhancements.

Register 42h : Subcode Device Type Selection Register (Read)
Subcode Device Type Selection Register (Write)

Acronym: SDTS

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Sub Format Selection		Reserved					

These bits specify the Subcode Interface format and Subcode Interface pin connection. The Philips' V4-Subcode Interface, EIAJ-1 (4-wired) and EIAJ-2 (3-wired) are supported as follows:

Subcode Format Selection			
Bits value	Description	Pin Connection	Clock Source
00	V4-Subcode for Philips DSP	SUB: connected to V4 as input SFSY: Ground SBSY: Ground RCK: Not Connected	Internal clock for 1X-50X
01	EIAJ-1 (4-wired) DSP	SUB: Input, as channel data SFSY: Input, as byte clock SBSY: Input, as sync clock RCK: Output as bit clock	RCK output as bit clock
10	EIAJ-2 (3-wired) DSP	SUB: Input, as channel data SFSY: Input, as byte/sync clock SBSY: Ground RCK: Output as bit clock	RCK output as bit clock
11	Invalid		

Bit 7-6: Sub Format Selection

These bits specify the Subcode Interface format and Subcode Interface pin connection. The Philips' V4-Subcode Interface, EIAJ-1 (4-wired) and EIAJ-2 (3-wired) are supported.

Bit 5-0: Reserved

These bits are reserved for future enhancements.

Register 43h : Version Control Register (Read)

Acronym: VCR

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Version Control Number							

The Version Control Register indicates the version number of the KS9245. The version number for the KS9245 is 20h. This register is hard-wired and read-only.

**Register 44h : Port Control Register (Write)
Port Control Register (Read)****Acronym: PCR**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
GPC3	GPC2	GPC1	GPC0	GP3	GP2	GP1	GP0

The *Port Control Register* controls the GP0, GP1, GP2 and GP3 pins as either Input/Output ports.

Bit 7 GPC3 (General Port Configuration for GP3)

When this bit is set, the GP3 pin is configured as an Output pin. When this bit is cleared, the GP3 pin is configured as an Input pin.

Bit 6 GPC2 (General Port Configuration for GP2)

When this bit is set, the GP2 pin is configured as an Output pin. When this bit is cleared, the GP2 pin is configured as an Input pin.

Bit 5 GPC1 (General Port Configuration for GP1)

When this bit is set, the GP1 pin is configured as an Output pin. When this bit is cleared, the GP1 pin is configured as an Input pin.

Bit 4 GPC0 (General Port Configuration for GP0)

When this bit is set, the GP0 pin is configured as an Output pin. When this bit is cleared, the GP0 pin is configured as an Input pin.

Bit 3: GP3 (General Port value for GP3)

When the GP3 pin is configured as an output pin, writing a "1" to this bit sets the GP3 Pin high. Writing a "0" resets the GP3 pin low. When the GP3 pin is configured as an input pin, reading this bit obtains the state of the GP3 pin.

Bit 2: GP2 (General Port value for GP2)

When the GP2 pin is configured as an output pin, writing a "1" to this bit sets the GP2 Pin high. Writing a "0" resets the GP2 pin low. When the GP2 pin is configured as an input pin, reading this bit obtains the state of the GP2 pin.

Bit 1: GP1 (General Port value for GP1)

When the GP1 pin is configured as an output pin, writing a "1" to this bit sets the GP1 Pin high. Writing a "0" resets the GP1 pin low. When the GP1 pin is configured as an input pin, reading this bit obtains the state of the GP1 pin.

Bit 0: GP0 (General Port value for GP0)

When the GP0 pin is configured as an output pin, writing a "1" to this bit sets the GP0 Pin high. Writing a "0" resets the GP0 pin low. When the GP0 pin is configured as an input pin, reading this bit obtains the state of the GP0 pin.

Register 45h : Reserved

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved							

This register is reserved.

Register 46h : Reserved

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved							

This register is reserved.

Register 47h : Reserved

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved							

This register is reserved for future enhancements.

Bit 7-0: Reserved

These bits are reserved for future enhancements.

**Register 48h : Valid Audio Block Count Register (Read)
Valid Audio Block Count Register (Write)**

Acronym: VABC

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Valid Audio Block Count Register B7:B0							

The *Valid Audio Block Count Register* indicate the number of valid audio blocks in the buffer DRAM which are available for audio playback in CAV mode.

Register 49h : Reserved

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved							

This register is reserved for future enhancements.

**Register 4Ah : DAC Block Address Register (Read)
DAC Block Address Register (Write)**

Acronym: DABA

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DAC Block Address Register							

The *DAC Block Address Register* point to the address of the data block currently being output to the external DAC during audio playback.

Register 4Bh : Reserved

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved							

This register is reserved for future enhancements.

Register 4Ch : DAC Output Format Selection Register (Read)
DAC Output Format Selection Register (Write)
Acronym: DOFS

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ADAT18	ABCKD1	AFPS	ABCKL		ALSBF	ALCH	ABCKF

The *DAC Output Format Selection Register* selects various audio output Interface formats in CAV playback mode only.

Bit 7: ADAT18 (Audio data output as 18 bit format)

When this bit is set, the audio data format is 18-bits. When this bit is cleared, audio data format is 16-bits.

Bit 6: ABCKD1 (ABCK data sampling delay one clock)

When this bit is set, the data is delayed by one ABCK clock in sampling.

Bit 5: AFPS (Audio Forward Packet Stream)

When this bit is set, the main data stream is a forward packet stream.

Bit 4-3: ABCKL (Audio Bit Clock Length)

These two bits specify the audio data bit clock length.

Bit 2: ALSBF (Audio Channel Data LSB byte comes first)

When this bit is set, the KS9245 takes the first byte of audio data as the LSB and the second byte as the MSB in the ADAT Pin. When this is cleared, the KS9245 takes the first byte of audio data as the MSB and the second byte as the LSB in the ADAT Pin.

Bit 1: ALCH (Audio Left Channel High)

When this bit is set, a high level on AWCK pin indicates the left channel. When this is cleared, a high level on the AWCK indicates the right channel.

Bit 0: ABCKF (Audio Data Latched on Falling Edge)

When this bit is set, the data is valid on the falling edge of the ABCK signal. When this bit is cleared, the data is valid on rising edge of the ABCK signal.

**Register 4Dh : DAC Control Register (Read)
DAC Control Register(Write)****Acronym: DACR**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved				ACC		SPA	

The *DAC Control Register* controls various DAC output operations such as mono, stereo, and swap left / right channel modes.

Bit 7-3: Reserved

These bits are reserved for future enhancements.

Bit 2-1: ACC (Audio Channel Control)

These bits control various audio channel outputs.

Bit 0: SPA (Start Play Audio)

When this bit is set and the ABPS bit is 0, the KS9245 starts outputting the audio data pointed to by the *DAC Block Address Register* (4Ah).

**Register 4Eh : Audio Clock Control Register (Read)
Audio Clock Control Register(Write)****Acronym: ACCR**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Rsvd	ABPS	DAUE	DOVS		DSCD	XINA Div	

The *Audio Clock Control Register* selects the audio clock source and various audio enables for Bypass mode and Digital Audio as well as the DSP input oversampling rate.

Bit 7 Reserved

This bit is reserved for future enhancements.

Bit 6: ABPS (Audio Bypass Mode Start)

When this bit is set regardless of what mode the CD decoder is in, the audio data is directly selected from the DSP input and then output to AWCK / ABCK / ADAT / DAUO pins. When this bit is cleared, the audio Bypass Mode is disabled.

Bit 5: DAUE (Digital Audio Output Enable)

Writing an "1" to this bit enables the Digital Audio output, IEC 958, on Pin 4.

Bit 4-3: DOVS (DSP Input Over Sampling Rate)

These bits select the over-sampling rate for the DSP input.

Bit 2: DSCD (Disable Subcode Clock Detect)

When this bit is set, the subcode clock auto-detection is disabled and the Subcode Clock Control and Adjustments Registers (40h, 45h, and 46h) are valid. When this bit is cleared, the subcode clock auto-detection is enabled and the Subcode Clock Control Register is invalid.

Bit 1-0: XINA Select (Audio Clock Select)

These bits select the Audio Clock word length for CAV mode only.

Register 4Fh : Audio Volume Control Register (Read)
Audio Volume Control Register (Write)

Acronym: AVCR

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LCM	RCM	Reserved		VOL			

Bit 7: LCM (Left Audio Channel Mute)

When this bit is set, the KS9245 mutes the left audio channel. When this bit is cleared, the KS9245 enables the left audio channel.

Bit 6: RCM (Right Audio Channel Mute)

When this bit is set, the KS9245 mutes the right audio channel. When this bit is cleared, the KS9245 enables the right audio channel.

Bit 5-4: Reserved

These bits are reserved for future enhancements.

Bit 3-0: VOL (Volume Control)

The bits control the volume level.

Chapter 7

Diagnostic and Miscellaneous Registers

The following registers are reserved for diagnostic purposes only. In normal operation, these registers need not be programmed.

Register 50h : Reserved

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved							

Bit 7-0: Reserved

These bits are reserved for internal diagnostic purposes.

Register 51h : Reserved

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved							

Bit 7-0: Reserved

These bits are reserved for internal diagnostic purposes.

Register 52h : Reserved

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved							

Bit 7-0: Reserved

These bits are reserved for internal diagnostic purposes.

Register 53h : Reserved

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved							

Bit 7-0: Reserved

These bits are reserved for internal diagnostic purposes.

Register 54h : Reserved

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved							

Bit 7-0: Reserved

These bits are reserved for internal diagnostic purposes.

Register 55h : Reserved

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved							

Bit 7-0: Reserved

These bits are reserved for internal diagnostic purposes.

Register 56h : Reserved

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved							

Bit 7-0: Reserved

These bits are reserved for internal diagnostic purposes.

Register 57h : Reserved

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved							

Bit 7-0: Reserved

These bits are reserved for internal diagnostic purposes.

Register 58h : Reserved

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved							

Bit 7-0: Reserved

These bits are reserved for internal diagnostic purposes.

Chapter 8

Enhancement Control Registers

Register 60h : **Ultra DMA Timing Register (Read)**
 Ultra DMA Timing Register (Write)

Acronym: **UDTR**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UDErr	Reserved				Udmacyc		

Bit 7 : UDErr (Ultra DMA Error)

This status bit will be set when the CRC logic of the Ultra DMA engine detects an error while transferring data.

Bit 6-3 : Reserved

These bits are reserved for the future enhancements.

Bit 2-0 : Udmacyc (Ultra DMA Programming Cycle Time)

These bits defined the cycle timing for the Ultra DMA engine.

Chapter 9

Electrical Specifications

9.1 Absolute Maximum Ratings

Item	Symbol	Rating	Unit
DC Supply voltage	VCC	-0.3 to 7	V
Storage Temperature	Tstg	-40 To 125	C
Power Dissipation	Pd	0.5	W
DC Input Voltage	Vin	-0.3 to VCC+0.3	V
DC Input Current	Iin	-10 to 10	mA

9.2 Recommended Operating Conditions

Item	Symbol	Rating	Unit
DC Supply voltage	VCC	4.5 to 5.5	V
Commercial Temperature	Ta	0 to 70	C

9.3 DC Characteristic

(VCC=5V-5% to 5V+5%, Ta=0 to 70 C, VSS=0)

Item	Symbol	Min.	Type.	Max.	Unit
Input High Voltage	Vih	2.0	-	-	V
Input Low Voltage	Vil	-	-	0.8	V
Output High Voltage	Voh	2.4	-	-	V
Output Low Voltage	Vol	-	-	0.4	V
Input High Current Vin=VCC	Iih	-10	-	10	uA
Input Low Current Vin=VSS	Iil	-10	-	10	uA
Input with pull-up		-200		-10	
Output Leakage Current	Ioz	-10	-	10	uA

9.4 Input/Output DC Characteristic

DC Characteristics of Pins					
Signal	Pin	I/O	Input Level	Output Current	Remark
BDAT5	1	I/O	TTL	4 mA	Internal Pull Up Resistor
BDAT11	2	I/O	TTL	4 mA	Internal Pull Up Resistor
BDAT4	3	I/O	TTL	4 mA	Internal Pull Up Resistor
BDAT12	4	I/O	TTL	4 mA	Internal Pull Up Resistor
BDAT3	5	I/O	TTL	4 mA	Internal Pull Up Resistor
BDAT13	6	I/O	TTL	4 mA	Internal Pull Up Resistor
BDAT2	7	I/O	TTL	4 mA	Internal Pull Up Resistor
BDAT14	8	I/O	TTL	4 mA	Internal Pull Up Resistor
BDAT1	9	I/O	TTL	4 mA	Internal Pull Up Resistor
VSS	10	I			
BDAT15	11	I/O	TTL	4 mA	Internal Pull Up Resistor
BDAT0	12	I/O	TTL	4 mA	Internal Pull Up Resistor
AWCK/GP0	13	I/O	TTL	4 mA	O: Audio Word Clock
ABCK/GP1	14	I/O	TTL	4 mA	O: Audio Bit Clock
ADAT/GP2	15	I/O	TTL	4 mA	O: Audio Data
DAUO/GP3	16	I/O	TTL	4 mA	O: Digital Audio
RSTB	17	I			Schmitt Trigger
SUB	18	I	TTL		
SFSY	19	I	TTL		
SBSY	20	I	TTL		
RCK	21	I/O		4 mA	
SBCLK	22	I	TTL		
SDATA	23	I	TTL		
LRCLK	24	I	TTL		
C2POI	25	I	TTL		

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VSS	26	I			
XOUT	27	O			
XIN/SYSCLK	28	I			33.8688 MHz
ARSTB	29	O		4 mA	
CSB	30	I	TTL		
AD0	31	I/O	TTL	4 mA	
AD1	32	I/O	TTL	4 mA	
AD2	33	I/O	TTL	4 mA	

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Signal	Pin	I/O	Input Level	Output Current	Remark
AD3	34	I/O	TTL	4 mA	
VSS	35	I			
AD4	36	I/O	TTL	4 mA	
AD5	37	I/O	TTL	4 mA	
AD6	38	I/O	TTL	4 mA	
AD7	39	I/O	TTL	4 mA	
VCC	40	I			
ALE/RSB	41	I	TTL		
RDB/DSB	42	I	TTL		
WRB R/WB	43	I	TTL		
HINTB	44	OD		4 mA	
DINTB	45	OD		4 mA	
VSS	46	I			
MSTB	47	I	TTL		
DASPB	48	I/O	TTL	12 mA	Internal Pull Up Resistor
CS3FXB	49	I	TTL		
CS1FXB	50	I	TTL		
DA2	51	I	TTL		
DA0	52	I	TTL		
PDIAGB	53	I/O	TTL	12 mA	Internal Pull Up Resistor
DA1	54	I	TTL		
IOCS16B	55	OD		12 mA	
INTRQ	56	OT		12 mA	
DMACKB	57	I	TTL		
IORDY	58	OT		12 mA	
DIORB	59	I	TTL		
DIOWB	60	I	TTL		
DMARQ	61	OT		12 mA	
VSS	62	I			
DD15	63	I/O	TTL	12 mA	
DD0	64	I/O	TTL	12 mA	
DD14	65	I/O	TTL	12 mA	
DD1	66	I/O	TTL	12 mA	
DD13	67	I/O	TTL	12 mA	
DD2	68	I/O	TTL	12 mA	

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Signal	Pin	I/O	Input Level	Output Current	Remark
DD12	69	I/O	TTL	12 mA	
DD3	70	I/O	TTL	12 mA	
VSS	71	I			
DD11	72	I/O	TTL	12 mA	
DD4	73	I/O	TTL	12 mA	
DD10	74	I/O	TTL	12 mA	
DD5	75	I/O	TTL	12 mA	
DD9	76	I/O	TTL	12 mA	
DD6	77	I/O	TTL	12 mA	
DD8	79	I/O	TTL	12 mA	
DD7	79	I/O	TTL	12 mA	
HRSTB	80	I	TTL		Schmitt Trigger
BADD4	81	O		4 mA	
BADD3	82	O		4 mA	
BADD5	83	I/O		4 mA	
BADD2	84	O		4 mA	
VSS	85	I			
BADD6/XSEL	86	I/O		4 mA	External Jumper
BADD1	87	O		4 mA	
BADD7/ISEL	88	I/O		4 mA	External Jumper
BADD0	89	O		4 mA	
VCC	90	I			
BADD8/MSEL	91	I/O		8 mA	External Jumper
RASB	92	O		8 mA	
CASB	93	O		4 mA	
WEB	94	O		4 mA	
BDAT8	95	I/O	TTL	4 mA	Internal Pull Up Resistor
VSS	96	I			
BDAT7	97	I/O	TTL	4 mA	Internal Pull Up Resistor
BDAT9	98	I/O	TTL	4 mA	Internal Pull Up Resistor
BDAT6	99	I/O	TTL	4 mA	Internal Pull Up Resistor
BDAT10	100	I/O	TTL	4 mA	Internal Pull Up Resistor

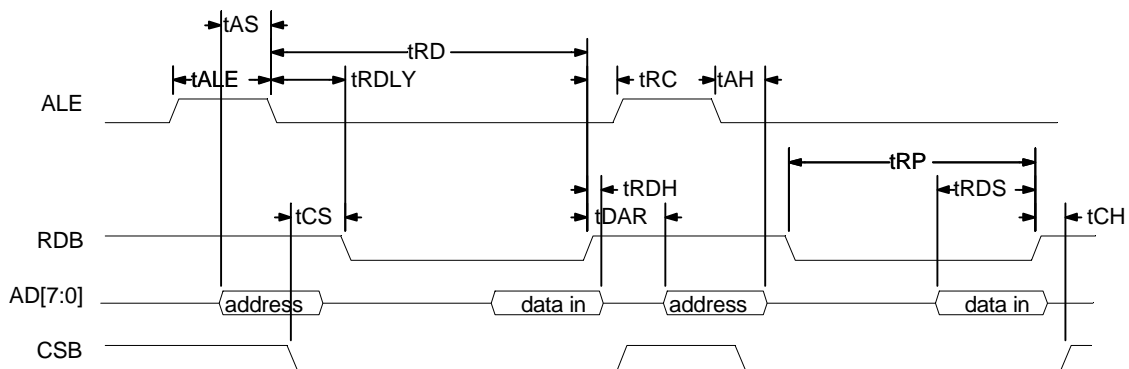
Chapter 10

General Timing

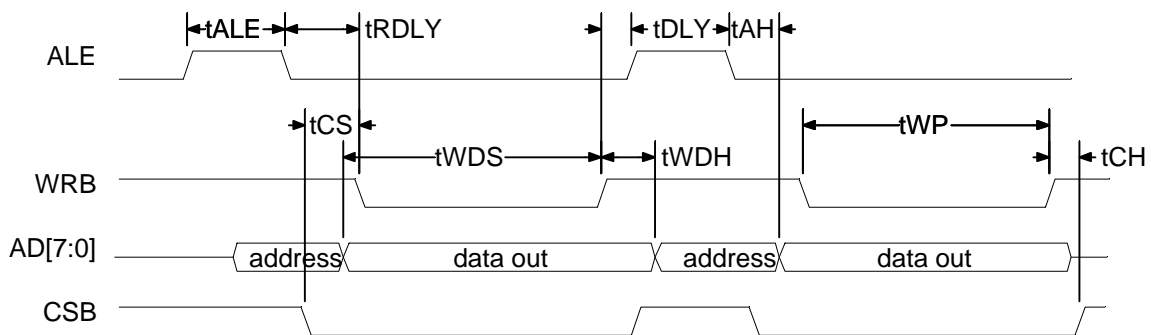
10.1 Microprocessor Interface

10.1.1 Multiplexed Intel Mode Register Read/Write Timing

Microcontroller Read Cycle



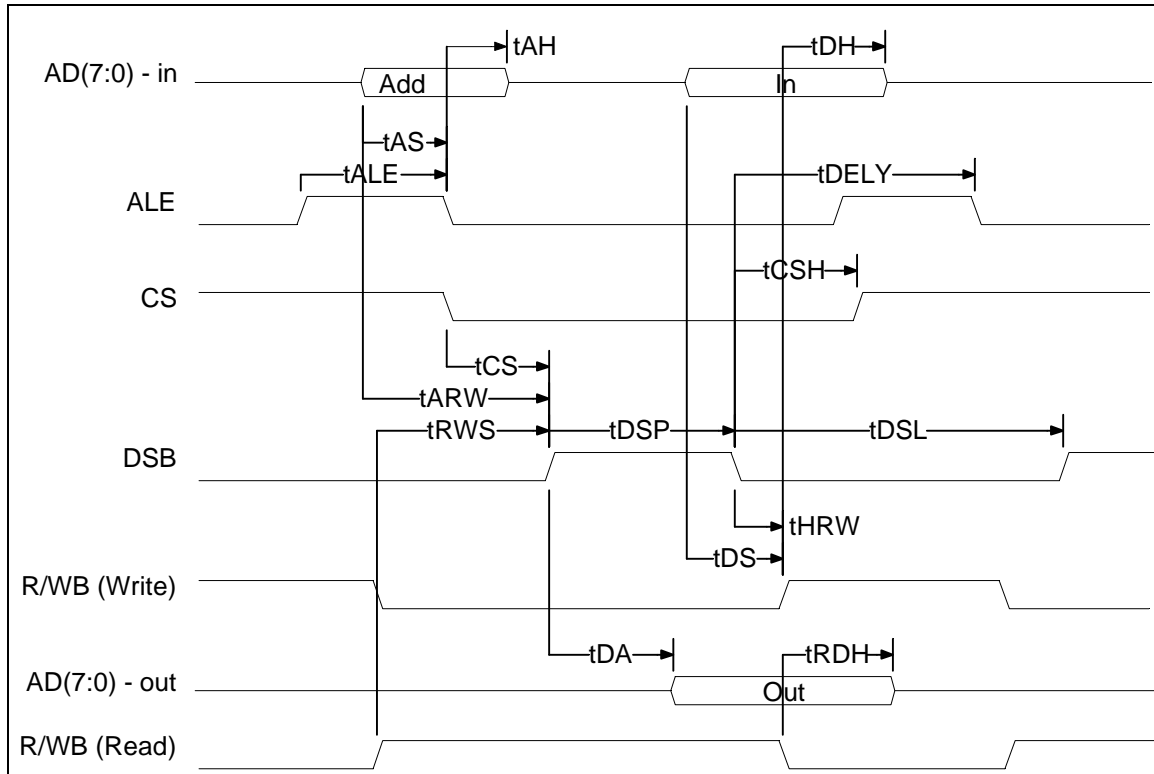
Microcontroller Write Cycle



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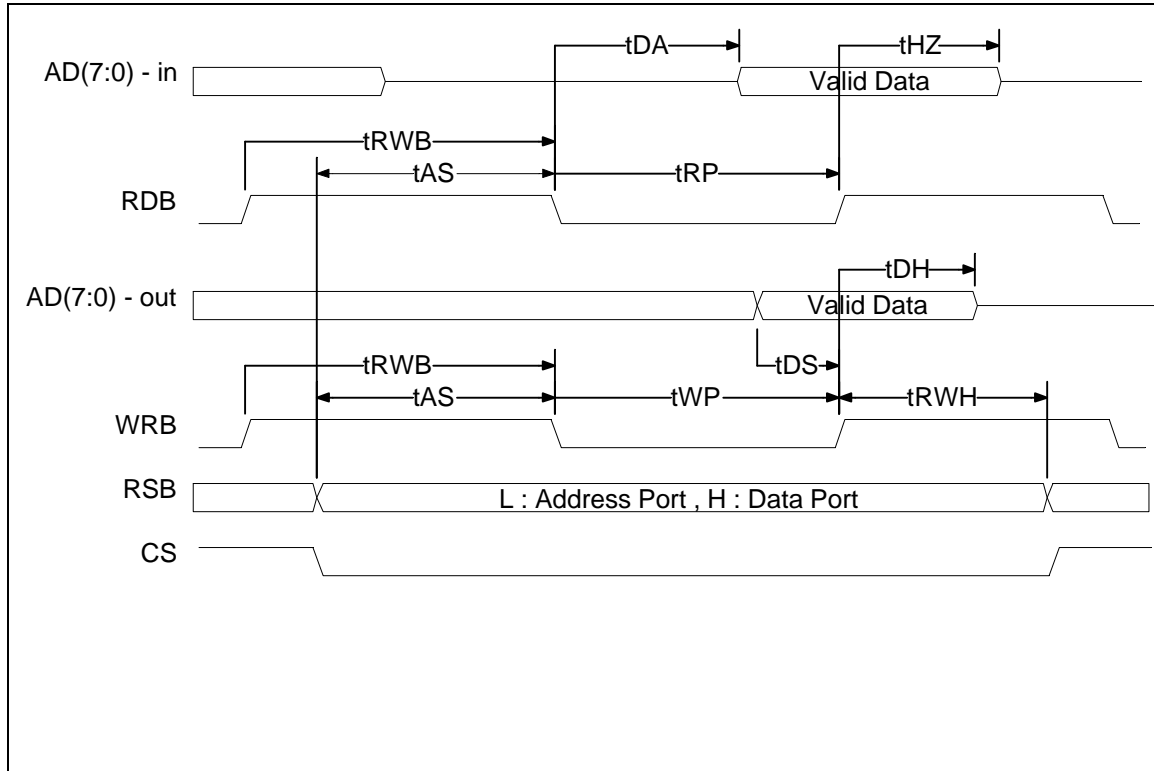
Parameter	Symbol	Min.	Max.	Unit
ALE Pulse Width	tALE	1 Sysclk		ns
Address Setup Time	tAS	10		
Address Hold Time	tAH	5		ns
Chip Select Setup for Read / Write Command	tCS	10		ns
Chip Select Hold for Read / Write Command	tCH	0		ns
ALE Active from Read / Write Rising Edge Delay	tDLY	0		ns
Write Pulse Width	tWP	2 Sysclk		ns
Read Pulse Width	tRP	3 Sysclk		ns
Read Pulse to Next Address Valid	tDAR	10		ns
Data Setup Time For Write	tWDS	10		ns
Data Hold Time for Write	tWDH	10		ns
ALE falling to RDB/ WRB falling	tRDLY	15		ns
Read Data Setup Time	tRDS	1 Sysclk		ns
Read Data Hold Time	tRDH	0		ns

10.1.2 Multiplexed Motorola Mode Register Read/Write Timing



Parameter	Symbol	Min.	Max.	Unit
ALE Pulse Width	tALE	1 Sysclk		ns
Address Setup Time	tAS	10		ns
Address Hold Time	tAH	10		ns
Address Valid Before Read/Write Command	tARW	15		ns
Chip Select Setup for Read/Write	tCS	10		ns
Chip Select Hold for Read/Write	tCH	0		ns
R/WB- Setup Before DS	tRWS	5		ns
R/WB- Hold After DS	tHRW	5		ns
DSB Pulse Width	tDSP	3 Sysclk		ns
DSB Recover Time	tDSL	1 Sysclk		ns
Data Setup Time For Write	tDS	10		ns
Data Hold Time for Write	tDH	10		ns
Read Access Time	tDA	1 Sysclk	2 Sysclk	ns
DSB to ALE Falling Edge Delay	tDELY	1.5 Sysclk		ns
Read Data Hold Time	tRDH	0		ns

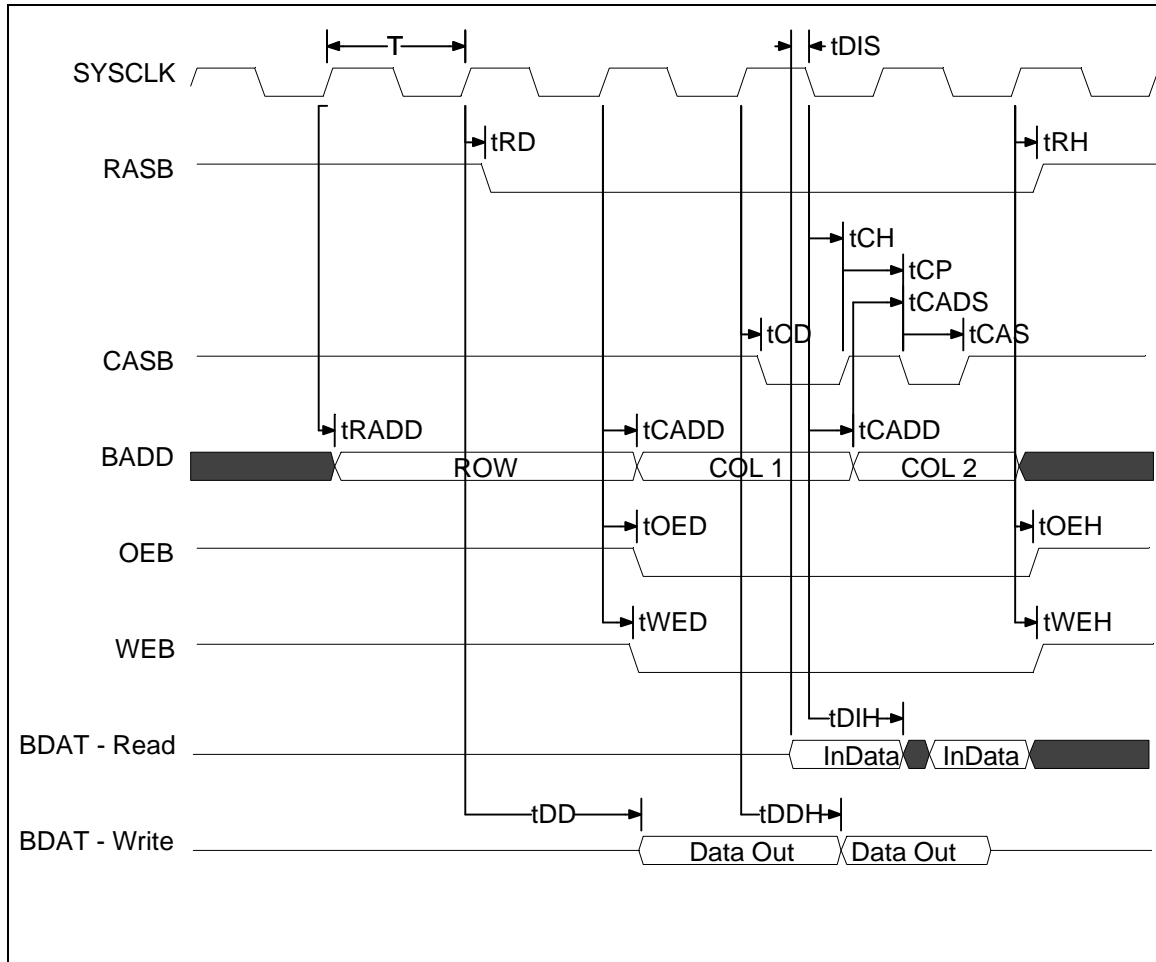
10.1.3 Indirect Access Register Mode Read/Write Timing



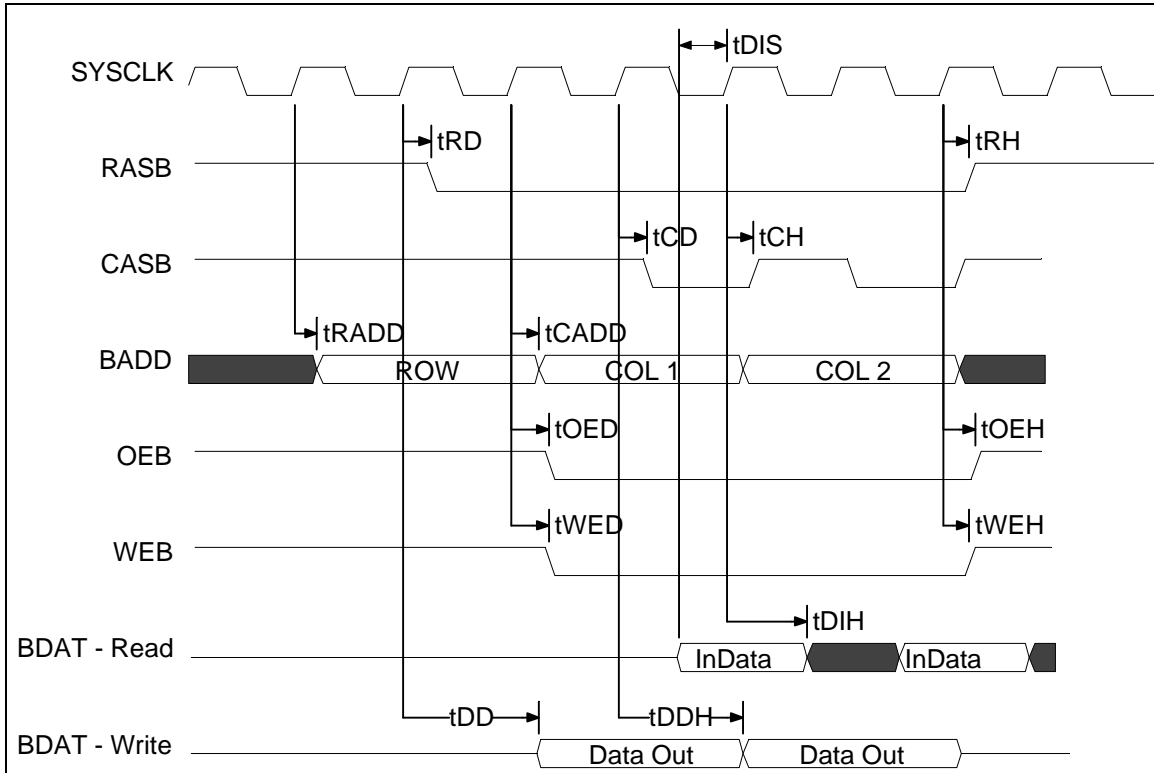
Parameter	Symbol	Min.	Max.	Unit
WRB Recover Time to next RDB or WRB	t_{RWB}	2 Sysclk		ns
CS or RSB Setup for Read/Write	t_{AS}	10		ns
WRB Pulse Width	t_{WP}	40		ns
RDB Pulse Width	t_{RP}	40		ns
CS or RSB Hold Time	t_{RWH}	5		ns
Data Setup Time For Write	t_{DS}	10		ns
Data Hold Time for Write	t_{DH}	10		ns
Read Access Time	t_{DA}	10	20	ns
Read Data Hold Time	t_{HZ}	0		ns

10.2 DRAM Interface

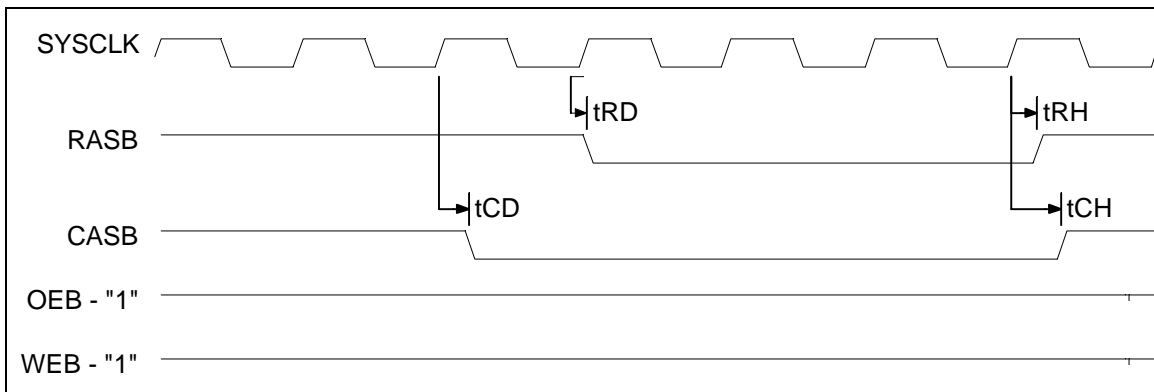
10.2.1 DRAM Single Clock Cycle Read/Write Timing



10.2.2 DRAM Non-Single Clock Cycle Read/Write Timing



10.2.3 DRAM Refresh Timing

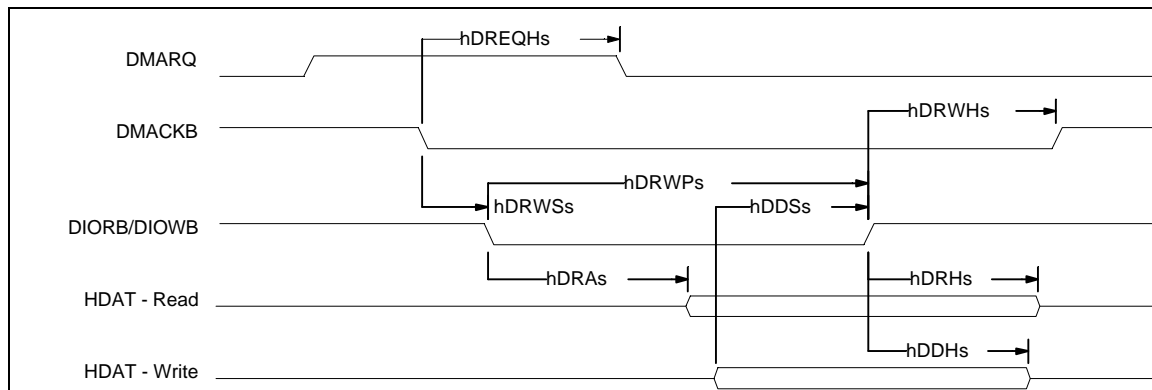


10.2.4 DRAM AC Timing

<i>Parameter</i>	<i>Symbol</i>	<i>Min.</i>	<i>Max.</i>	<i>Unit</i>
SYSCLK Cycle Time	T	20.8		ns
SYSCLK to RASB Low Delay	tRD		15	ns
SYSCLK to RASB High Delay	tRH		15	ns
SYSCLK to CASB Low Delay	tCD		15	ns
SYSCLK to CASB High Delay	tCH		15	ns
SYSCLK to Row Add Valid Delay	tRADD		15	ns
SYSCLK to Column Add Valid Delay	tCADD		15	ns
SYSCLK to OEB Low Delay	tOED		15	ns
SYSCLK to OEB High Delay	tOEH		15	ns
SYSCLK to WEB Low Delay	tWED		15	ns
SYSCLK to WEB High Delay	tWEH		15	ns
CASB High To Data In Setup Time	tDIS	0		ns
CASB High To Data In Hold Time	tDIH	6		ns
SYSCLK to Valid Data Delay for Write	tDD	20		ns
SYSCLK to Invalid Delay for Write	tDDH	20		ns
CAS High Pulse Width	tCP	5		ns
CAS Low Pulse Width	tCAS	T/2 + 1.5		ns
Column Address Set Up	tCADS	4		ns

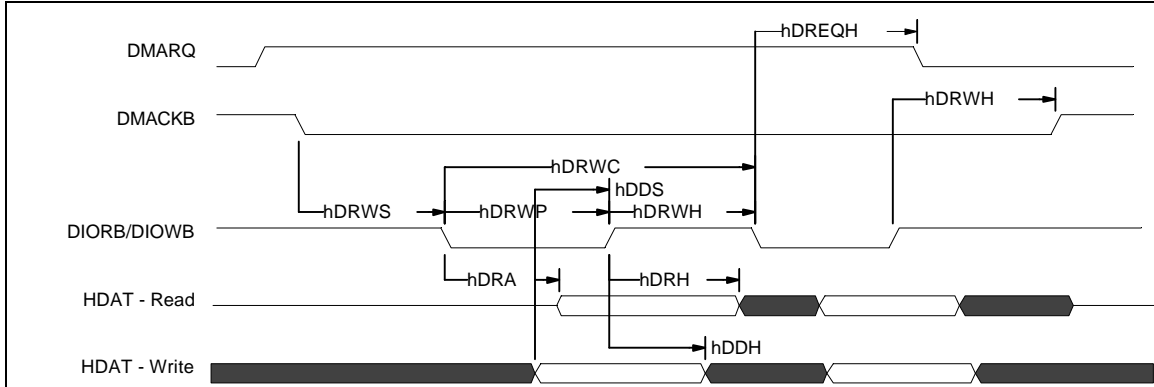
10.3 ATA Interface

10.3.1 Single Word DMA Data Transfer



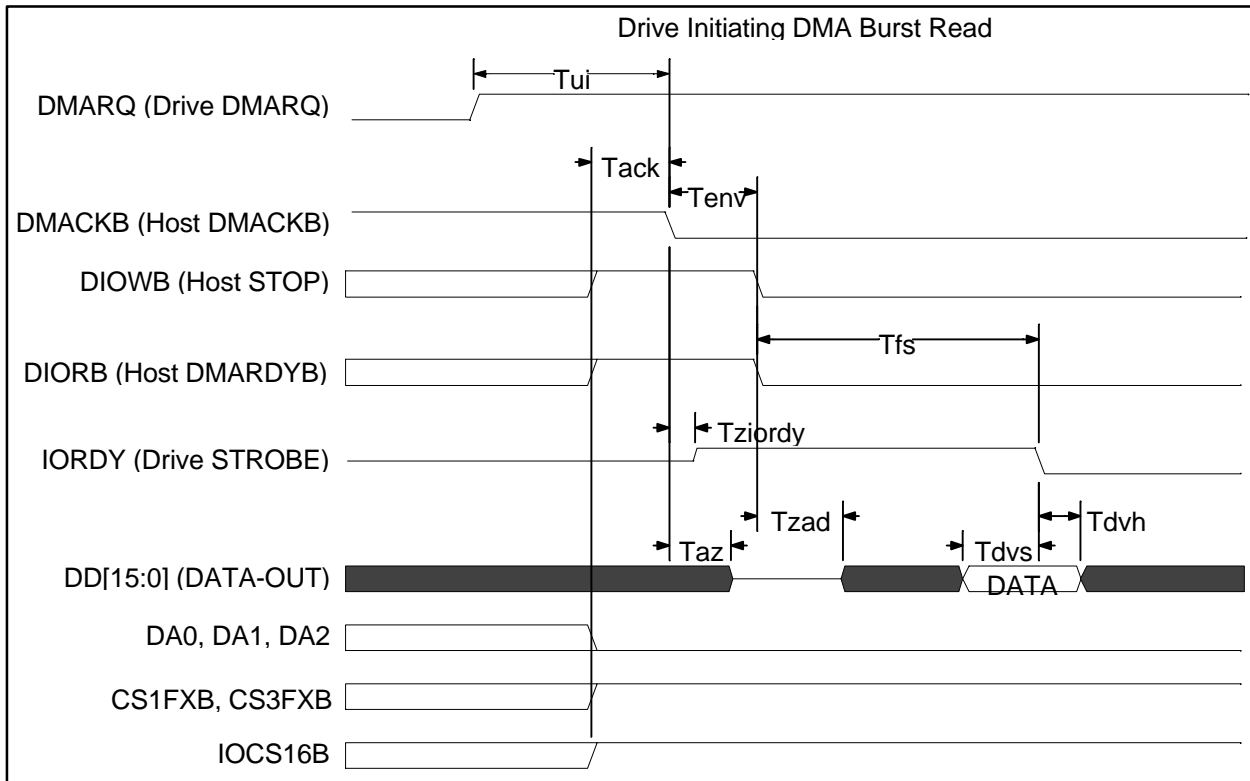
Parameter	Symbol	Min.	Max.	Unit
DMACKB to DMARQ Delay	hDREQHs	80		ns
DMACKB to DIOR(W)B Setup	hDRWSs	0		ns
DIORB/DIOWB Pulse Width	hDRWPs	120		ns
DIOR(W)B to DMACKB Hold	hDRWHs	0		ns
DIORB Read Access Time	hDRAs	60		ns
DIORB Data Hold	hDRHs	5		ns
DIOWB Data Setup	hDDSs	35		ns
DIOWB Data Hold	hDDHs	20		ns

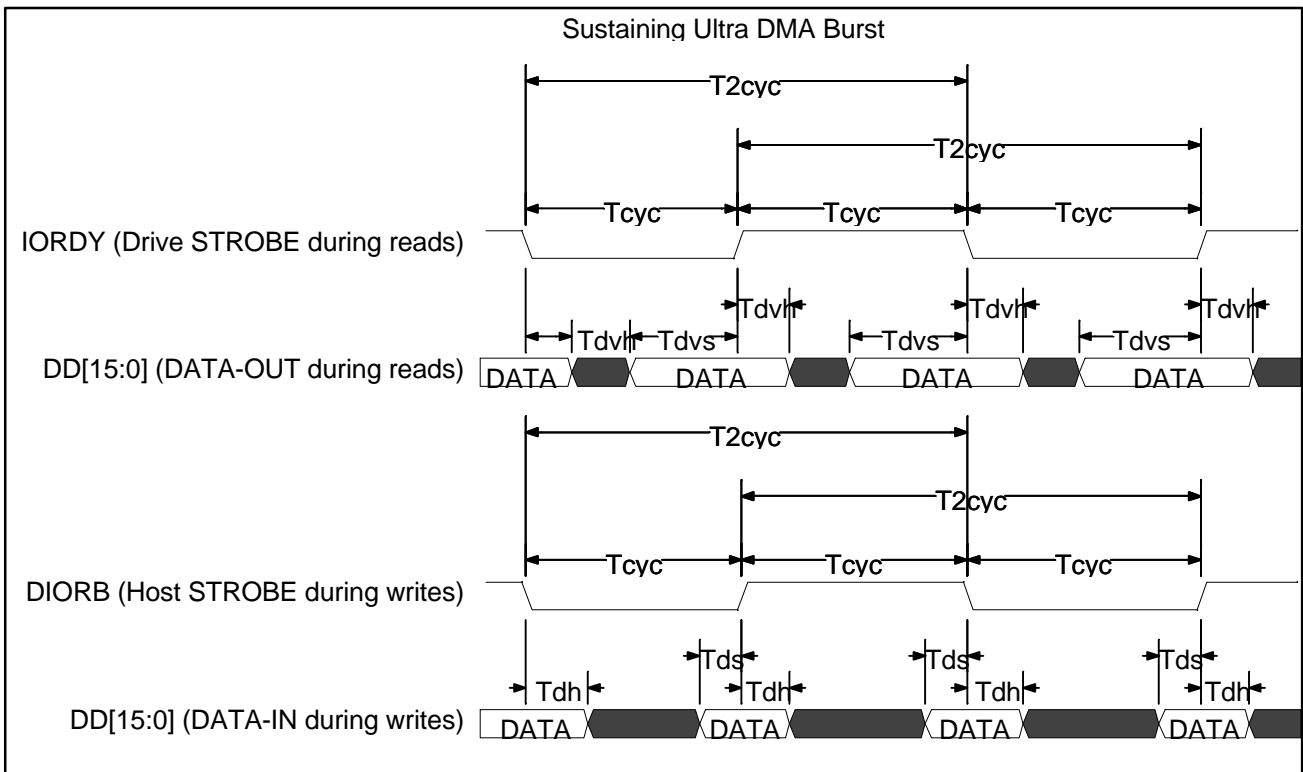
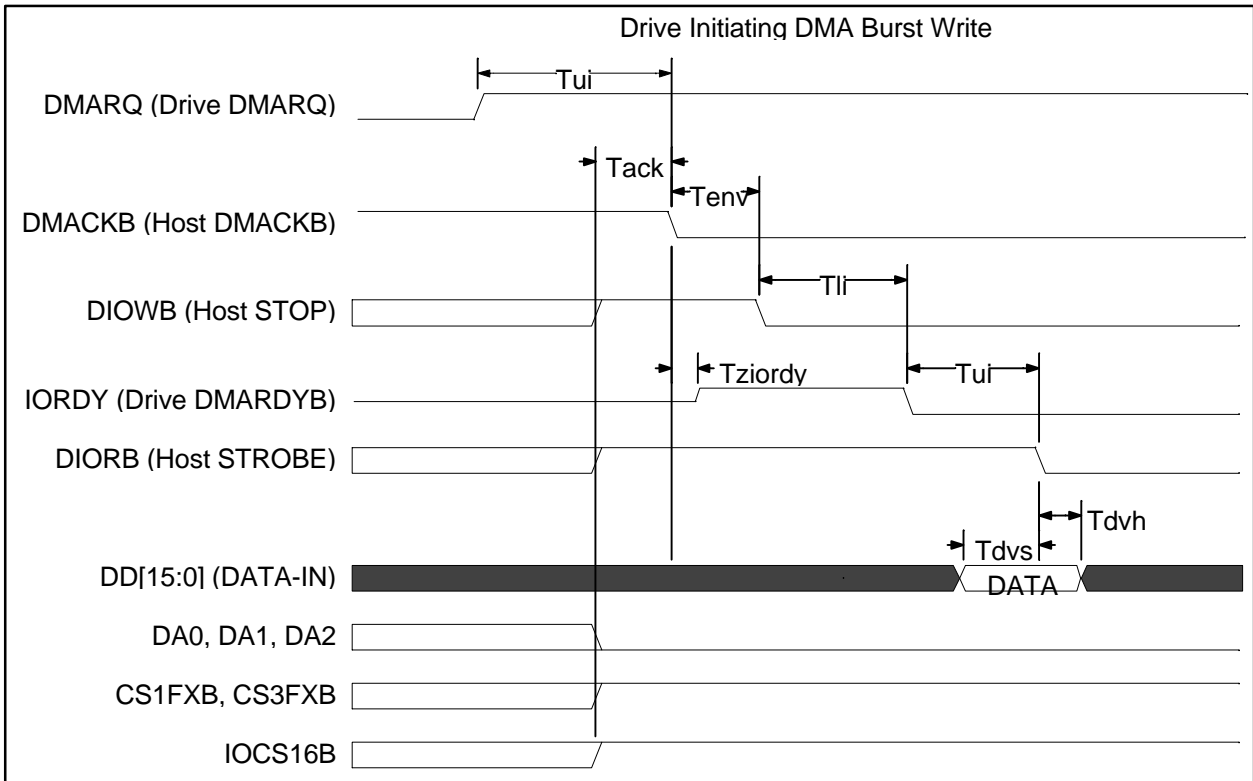
10.3.2 Multiword Word DMA Data Transfer

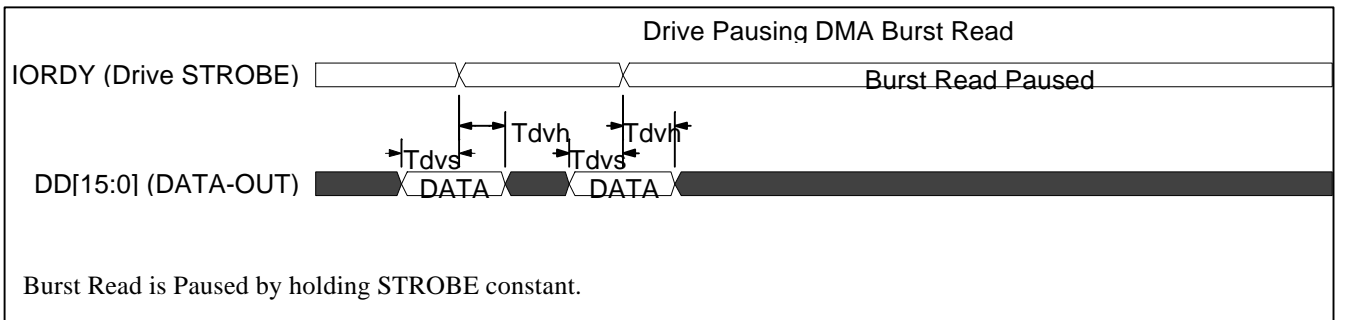
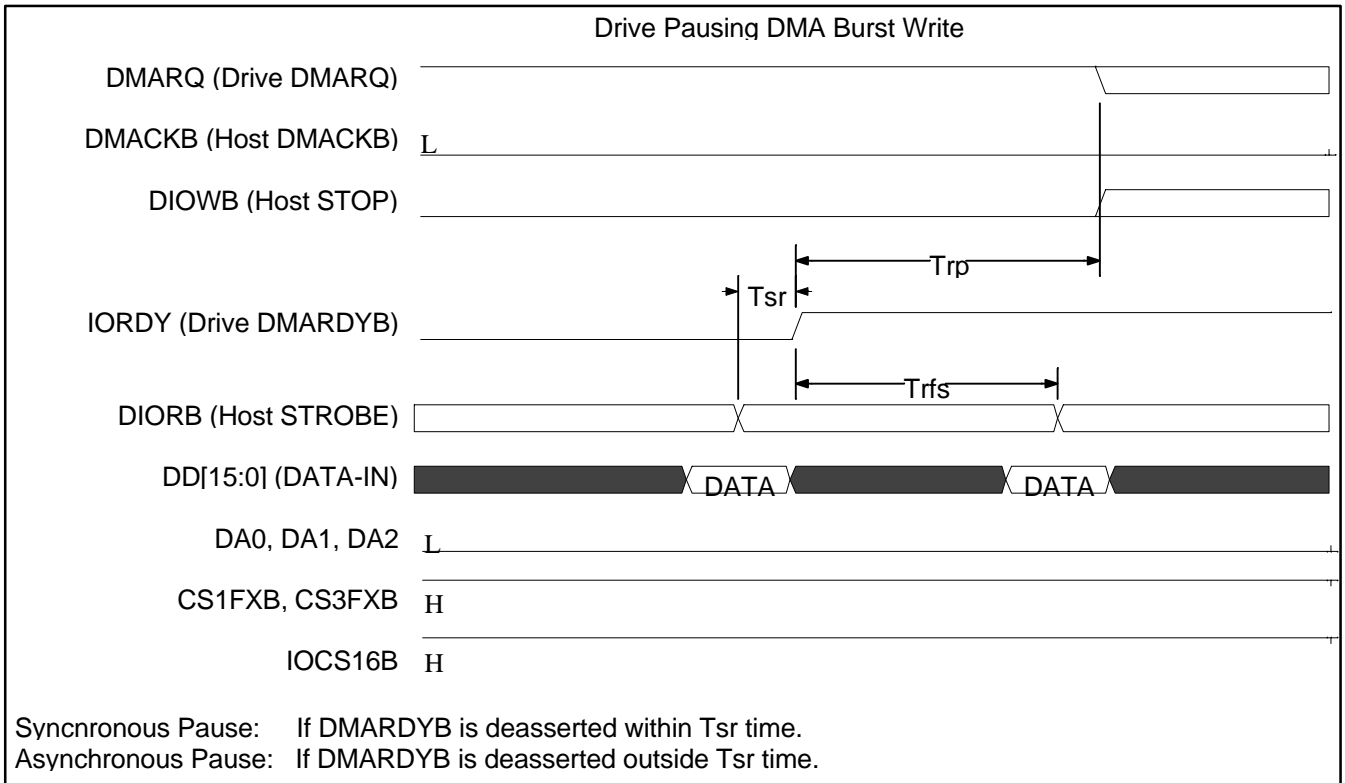


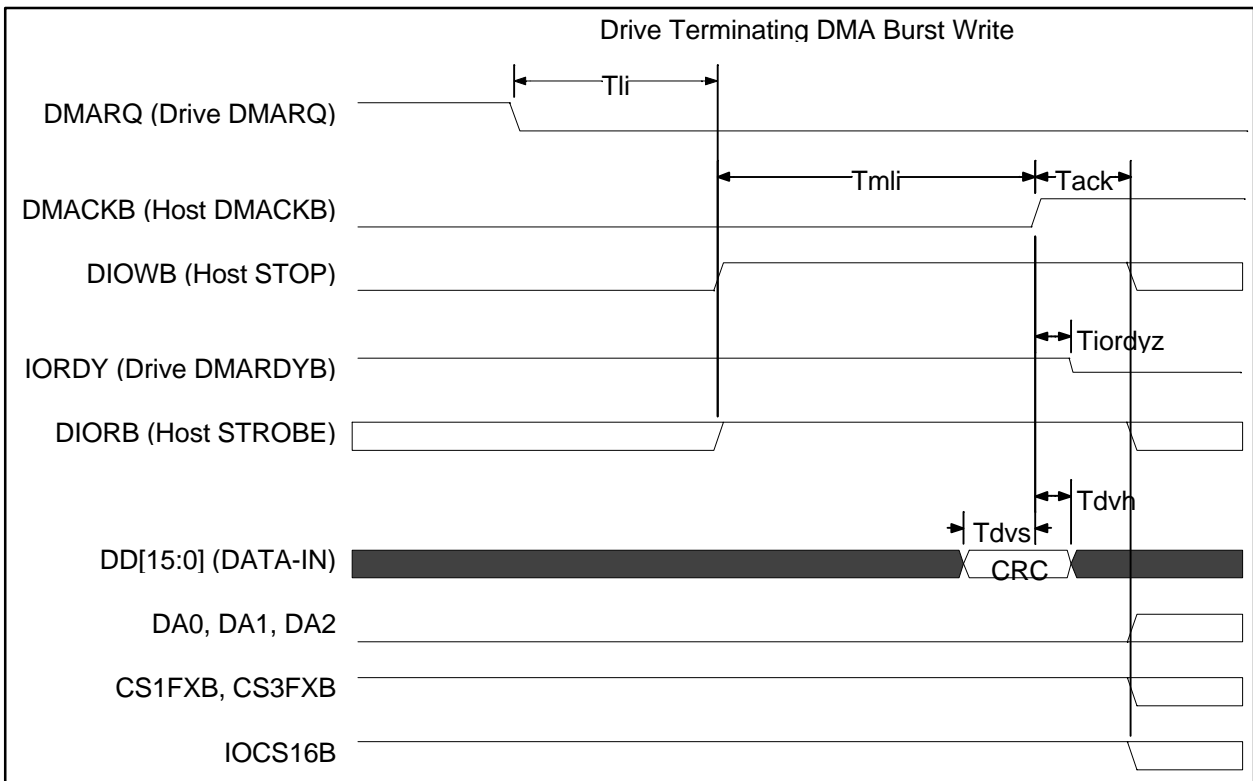
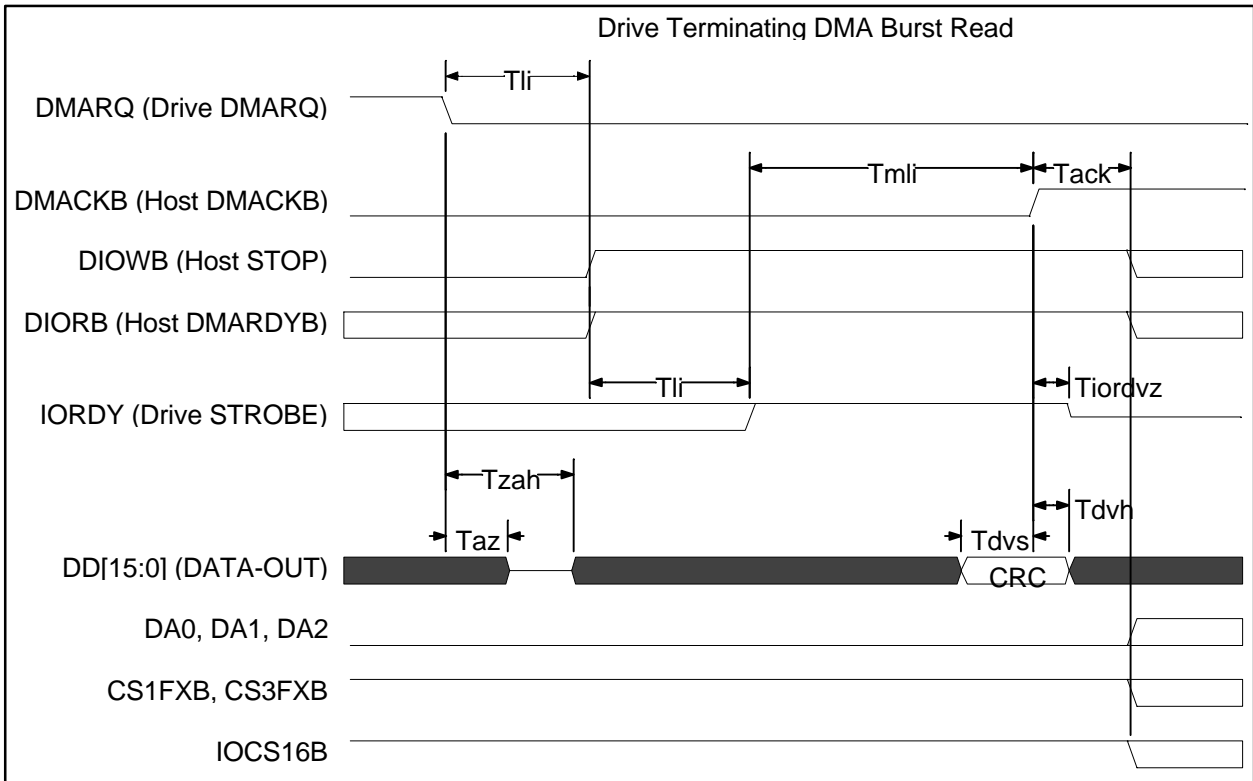
Parameter	Symbol	Min.	Max.	Unit
DIOR(W)B to DMACKB Delay	hDREQH	35		ns
DIOR(W)B to DMACKB Hold	hDRWH	5		ns
DMACKB to DIOR(W) Setup	hDRWS	0		ns
DIORB/DIOWB Pulse Width	hDRWP	70		ns
DIORB/DIOWB Negated Pulse Width	hDRWH	25		ns
DIORB/DIOWB Cycle Time	hDRWC	120		ns
DIORB Read Access Time	hDRA	60		ns
DIORB Data Hold	hDRHs	5		ns
DIOWB Data Setup	hDDS	20		ns
DIOWB Data Hold	hDDH	10		ns

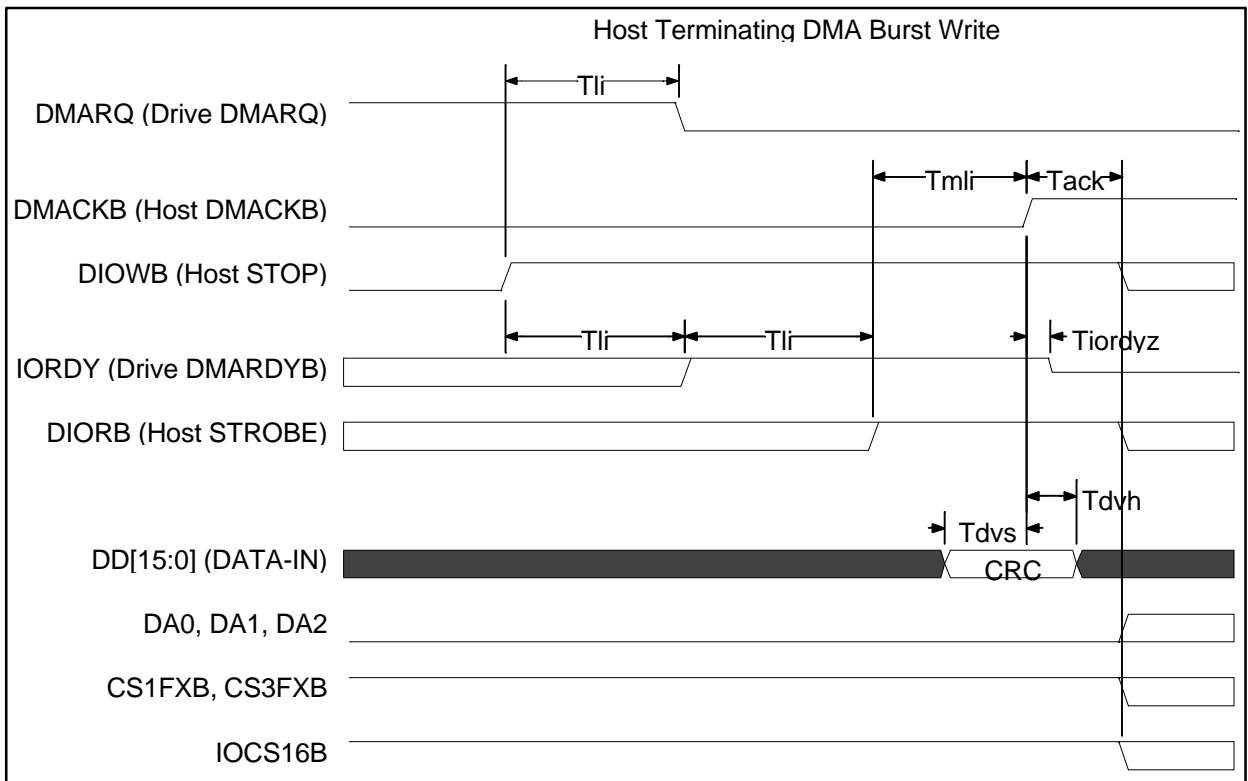
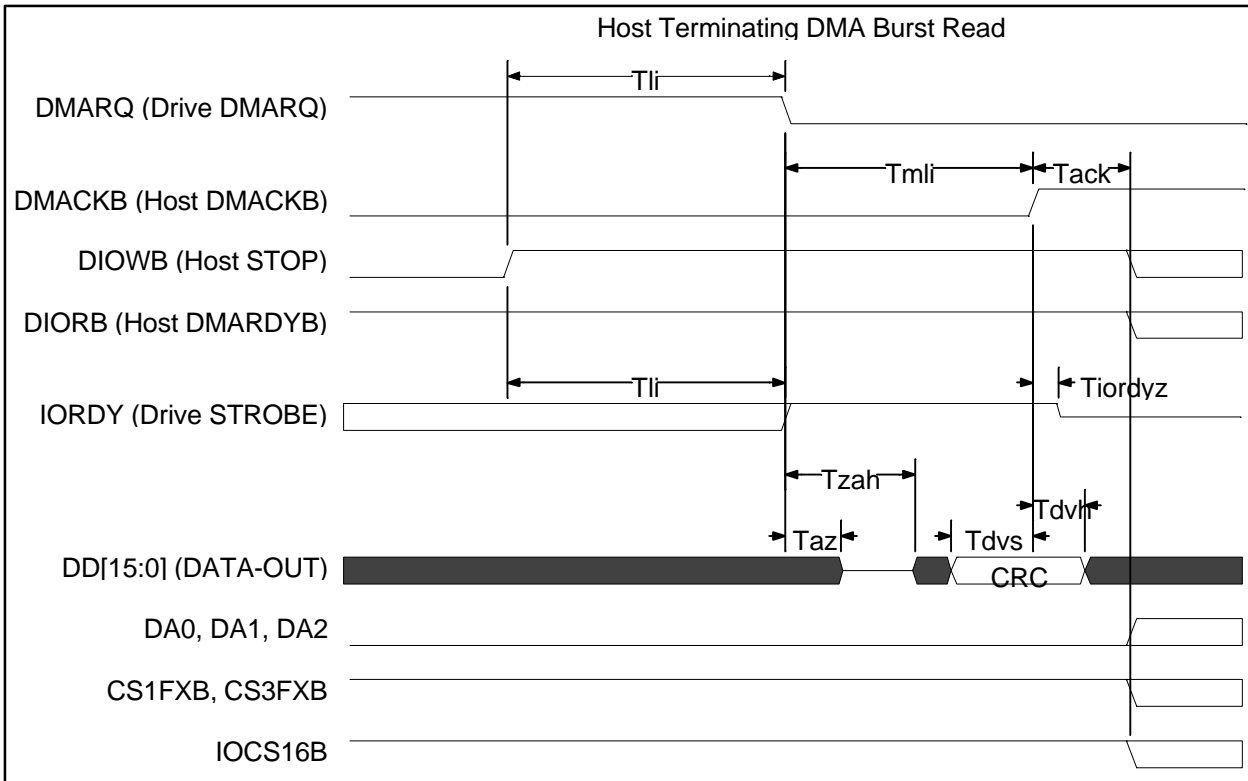
10.3.3 Ultra DMA Data Transfer

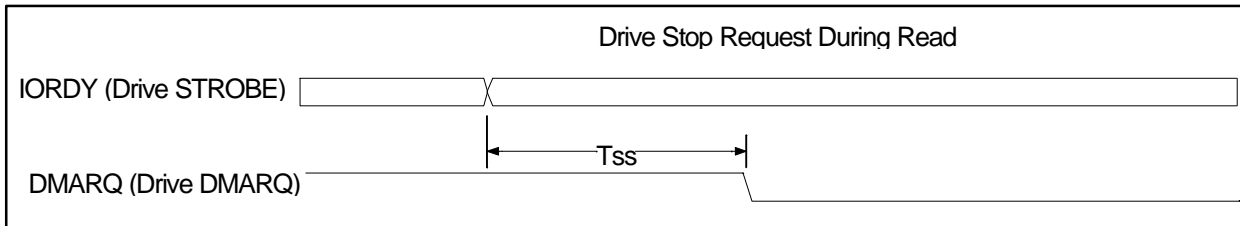








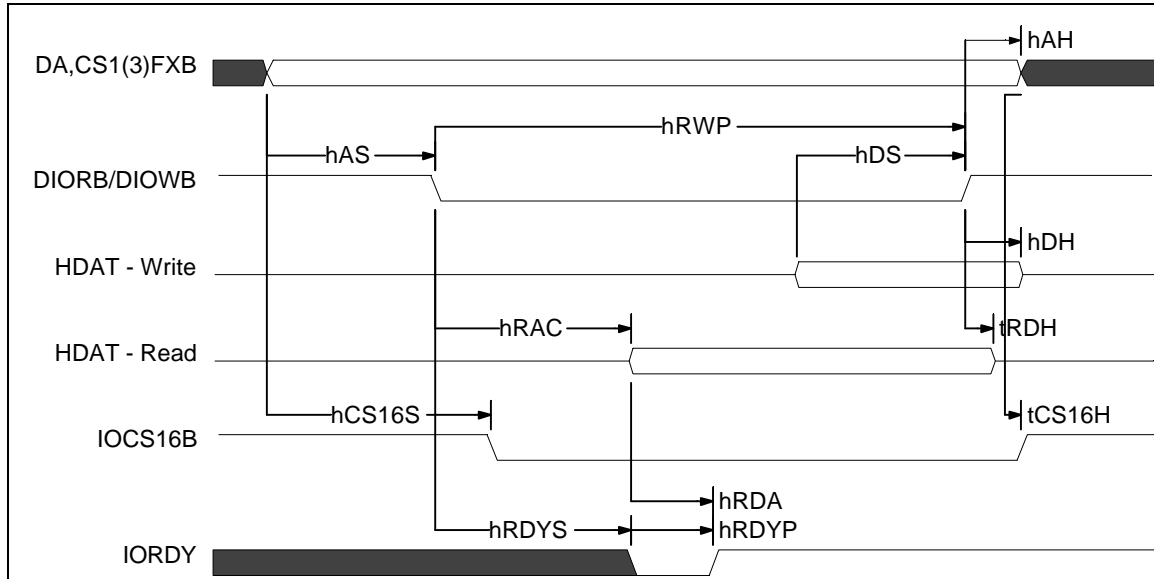




Ultra DMA Timing Parameters (Mode-2)

Parameter	Symbol	Min.	Max.	Unit
Cycle Time	Tcyc	55		ns
Two Cycle Time	T2cyc	117		ns
Data Setup Time at Receiver	Tds	7		ns
Data Hold Time at Receiver	Tdh	3		ns
Data Valid Setup Time at Sender	Tdvs	34		ns
Data Valid Hold Time at Sender	Tdvh	6		ns
First Strobe Time - time allowed for drive to send first STROBE	Tfs	0	170	ns
Limited Interlock Time	Tli	0	150	ns
Limited Interlock Time with Minimum	Tmli	20		ns
Unlimited Interlock Time	Tui	0		ns
Maximum time allowed for outputs to tristate	Taz		10	ns
Minimum delay required for output drivers to turn on from High Z	Tzah	20		ns
	Tzad	0		ns
Envelope Time	Tenv	20	70	ns
STROBE-to-DMARDY response time to ensure Synchronous Pause	Tsr		20	ns
READY-to-Final-STROBE Time	Trfs		50	ns
READY-to-Pause Time	Trp	100		ns
Pull-Up Time before allowing IORDY to go High Z	Tiordyz		20	ns
Minimum time Drive must wait before driving IORDY	Tziordy	0		ns
Setup and Hold times before assertion and deassertion of /DMACK	Tack	20		ns
Time from STROBE edge to STOP assertion when sender is stopping	Tss	50		ns

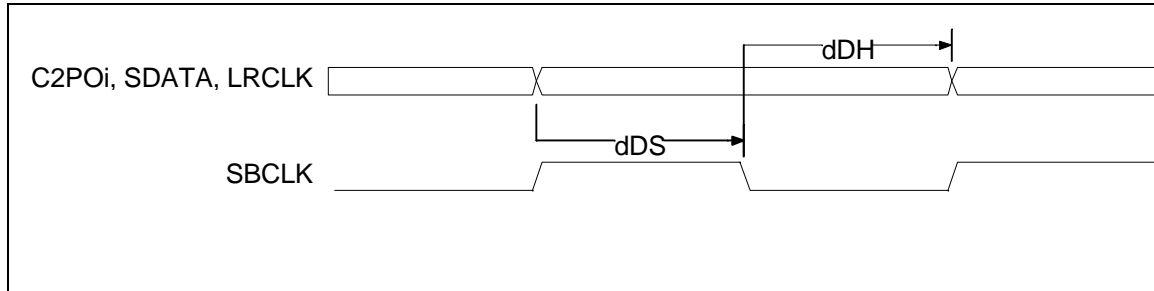
10.3.4 Programmed I/O Read/Write Timing



Parameter	Symbol	Min.	Max.	Units
Address Setup Time	hAS	25		ns
Address Hold Time	hAH	10		ns
DIOR-/DIOW- Pulse Width : 16 Bits	hRWP	70		ns
DIOW- Data Setup Time	hDS	20		ns
DIOW- Data Hold Time	hDH	10		ns
DIOR- Read Access Time	hRAC	25		ns
DIOR- Read Data Hold Time	hRDH	5		ns
Address Valid To IOCS16B Delay	hCS16S	40		ns
Address Valid To IOCS16B Hold	hCS16H	25		ns
IORDY Setup Time	hRDYS	35		ns
Read Data Valid To IORDY selected	hRDA	0		ns
IORDY Pulse Width	hRDYP		1250	ns

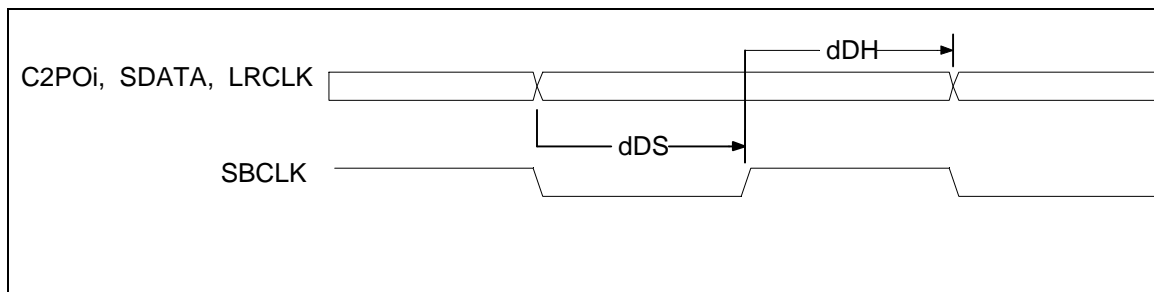
10.4 CD DSP Interface

10.4.1 SBCLK Falling Edge Strobe



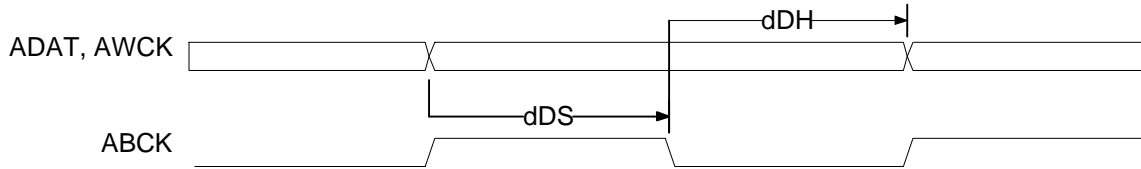
Parameter	Symbol	Min.	Max.	Unit
C2POi, SDATA, LRCLK Setup Before SBCLK	dDS	5		ns
C2POi, SDATA, LRCLK Hold After SBCLK	dDH	5		ns

10.4.2 SBCLK Raising Edge Strobe



Parameter	Symbol	Min.	Max.	Unit
C2Poi, SDATA, LRCLK Setup Before SBCLK	dDS	5		ns
C2Poi, SDATA, LRCLK Hold After SBCLK	dDH	5		ns

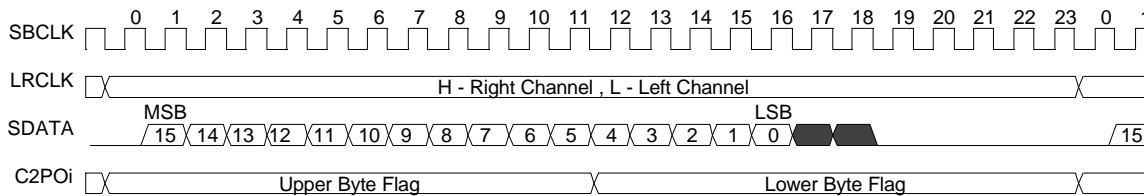
10.4.3 Audio Output Edge Strobe



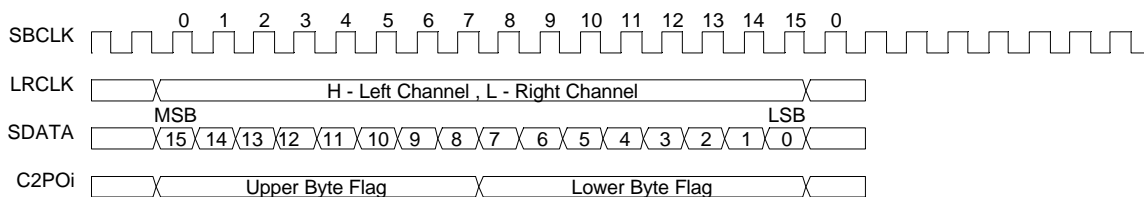
Parameter	Symbol	Min.	Max.	Unit
ADAT, AWCK Setup Before ABCK	dDS	5		ns
ADAT, AWCK Hold After ABCK	dDH	5		ns

10.4.4 DSP Interface Format

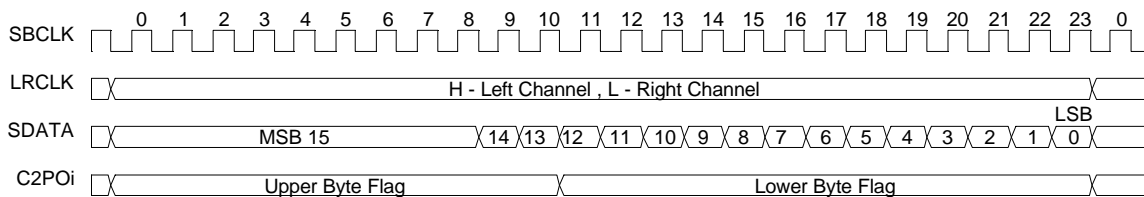
Philips IIS DSP Interface Format



Toshiba DSP Interface Format

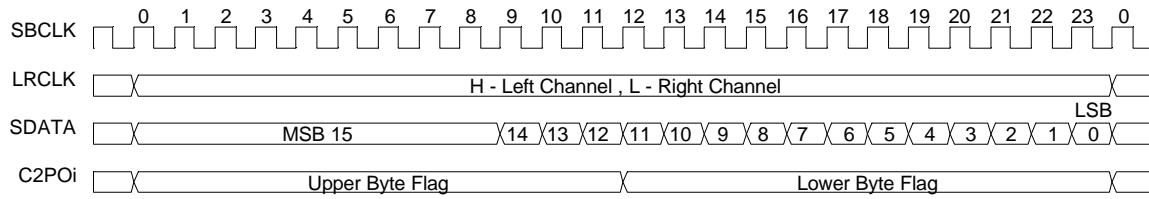


Sony 24-Clock DSP Interface Format-1

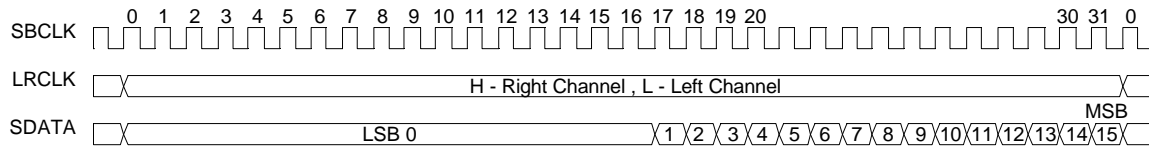


Sony 24-Clock DSP Interface Format-2

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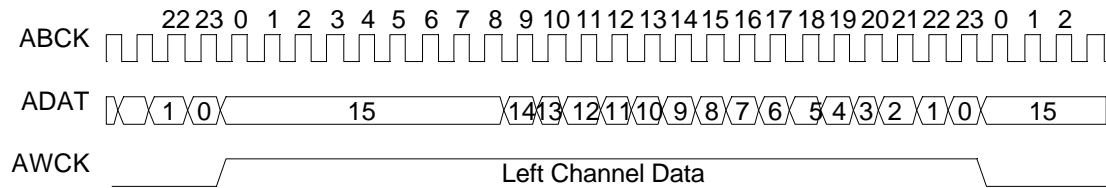


Sony 32-Clock DSP Interface Format-3

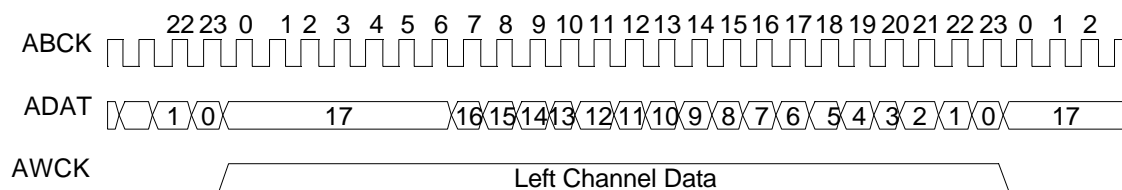


10.4.5 Audio Output Interface Format

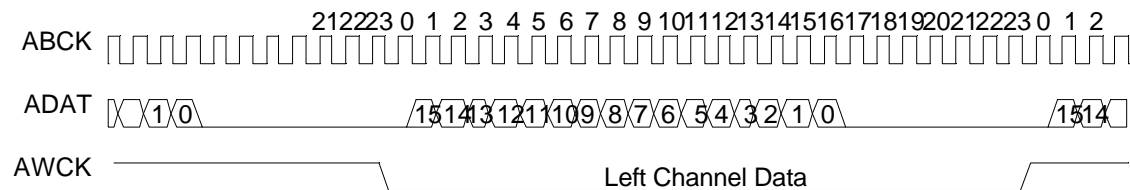
EIAJ (16-bit) Audio Data Interface Format



EIAJ (18-bit) Audio Data Interface Format

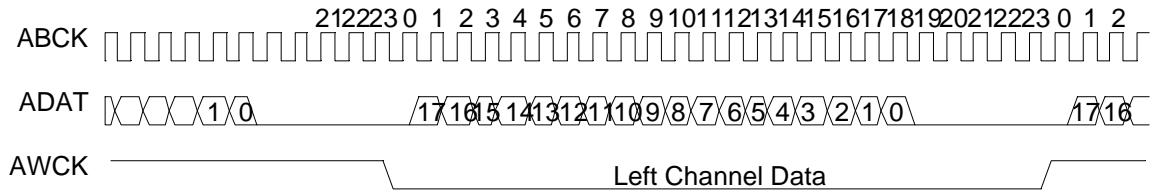


Philips I2S (16-bit) Audio Data Interface Format

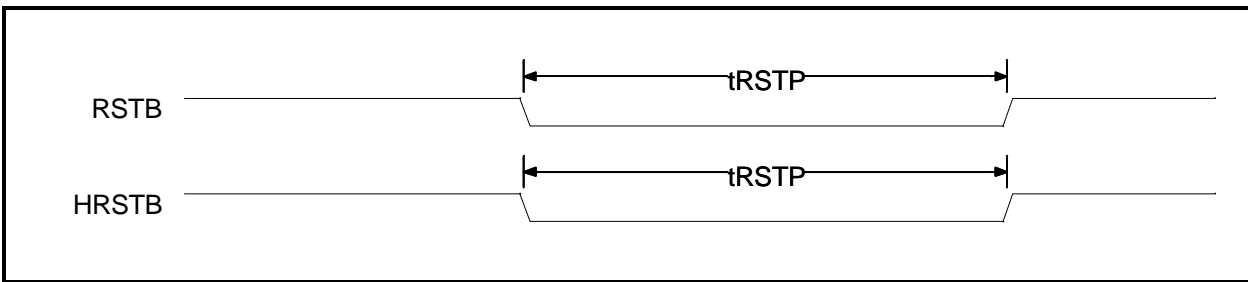


Philips I2S (18-bit) Audio Data Interface Format

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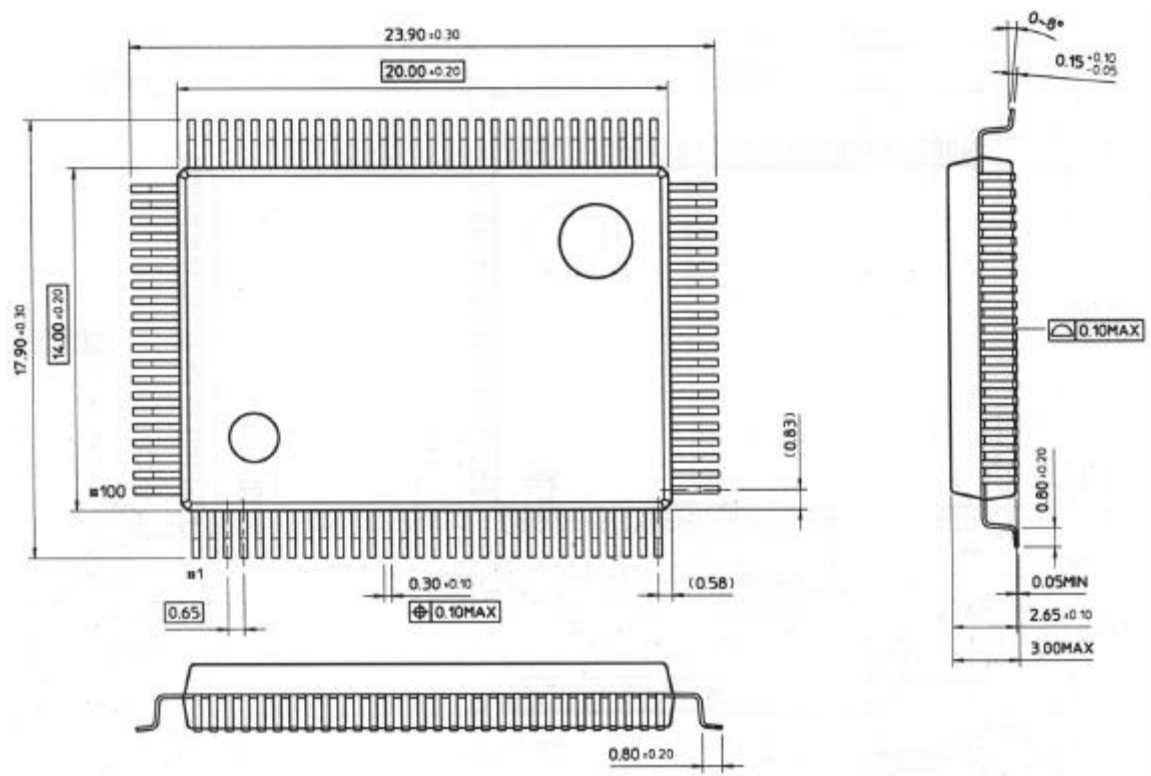
10.5 Power On Reset Interface Timing



<i>Parameter</i>	<i>Symbol</i>	<i>Min.</i>	<i>Max.</i>	<i>Units</i>
Reset Pulse Width	t_{RSTP}	10		us

Chapter 11

Package and Dimensions



Chapter 12

Hardware Application Notes

12.1 PIO/DMA Support Modes

The following tables list the various disk speed and PIO/DMA mode which are supported in our specification.

<i>PIO Mode Summary/Disk Speed</i>				
PIO Mode	Burst Speed	Cycle Time	Support	Remark
Mode 0	3.33 MB/Sec	600 nsec	yes	without flow control
Mode 1	5.33 MB/Sec	383 nsec	yes	without flow control
Mode 2	8.33 MB/Sec	240 nsec	yes	without flow control
Mode 3	11.1 MB/Sec	180 nsec	yes	without flow control
Mode 4	16.7 MB/Sec	120 nsec	yes	without flow control

<i>DMA Mode Summary/Disk Speed</i>				
Single/Multi Word	Burst Speed	Cycle Time	Support	Remark
Single Word Mode 0	2.08 MB/Sec	960 nsec	yes	
Single Word Mode 1	4.17 MB/Sec	480 nsec	yes	
Single Word Mode 2	8.33 MB/Sec	240 nsec	yes	
MultiWord Mode 0	4.17 MB/Sec	480 nsec	yes	
MultiWord Mode 1	13.3 MB/Sec	150 nsec	yes	
MultiWord Mode 2	16.7 MB/Sec	120 nsec	yes	

12.2 Firmware Sector Process Time

The following tables list the various disk rate against the worst case time left for firmware to process a sector after decoder interrupt is generated by hardware.

<i>Firmware sector process time</i>			
Disk Speed	Sector Period	DSP Rate	Worst F/W Sector Time
1X	13.333 ms	150KB/Sec	6.666 msec
2X	6.666 ms	300KB/Sec	3.333 msec
4X	3.333 ms	600KB/Sec	1.666 msec
6X	2.222 ms	900KB/Sec	1.111 msec
8X	1.666 ms	1.2MB/Sec	.833 msec
10X	1.333 ms	1.5MB/Sec	.666 msec
12X	1.111 ms	1.8MB/Sec	.555 msec
14X	.952 ms	2.1MB/Sec	.476 msec
16X	.833 ms	2.4MB/Sec	.416 msec
24X	.555 ms	3.6MB/Sec	.277 msec

12.3 Sleep Mode

How To Enter Sleep Mode

KS9245 can be programmed into sleep mode for saving power and most of hardware will be cut off by Clock. The only way into sleep mode is the register 2F Bit 7 Must be set to High.

How To Quit Sleep Mode

There are two ways to quit from sleep mode. One done by firmware is clear Bit 7 of register 2F directly and The other is New ATA Command received or ATA Software reset Command received in this case KS9245 Hardware will automatically wake up.

Something Important Before Enter Sleep Mode

In the sleep mode, DSP interface will be shut off automatically, so make sure KS9245 is in DSP STOP mode. ECC engine and Buffer Manager are totally turned off. In DRAM Control logic, the refresh time will still work to keep the buffer data is valid. Following Table is for each Block Function affected by sleep mode.

	Dram Refresh	DSP	Subcode	MicroP	ECC EDC	Buffer Manager	IDE
Sleep On	On	Off	Off	On	Off	Off	On

How Much Power is saved in Sleep Mode

In the Sleep Mode, it is about 75%-80% less than the normal operation mode.

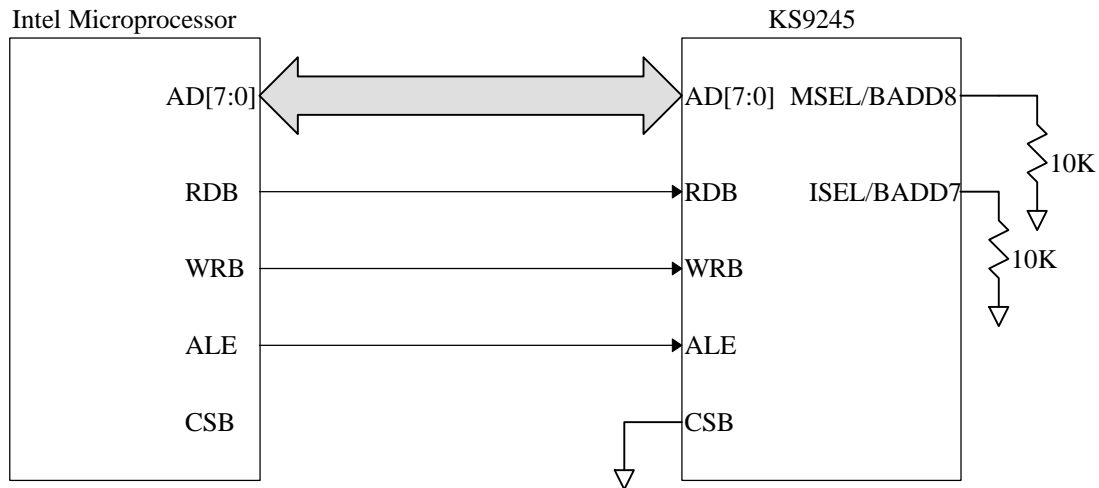
12.4 Automatic Power-savings Mode

Besides sleep mode, the KS9245 has an automatic power-savings feature for the CD-DSP/Subcode interface, ECC, and CAV audio playback modules. In this mode, the clocks driving these modules are stopped when the modules are not active. The following describes the automatic power-savings feature:

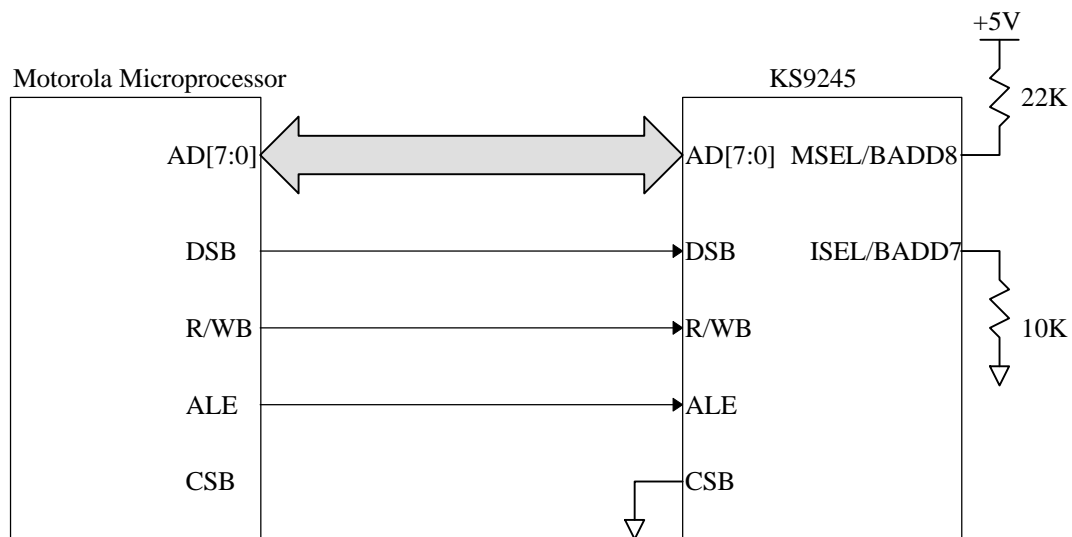
- 1) The clock to the CD-DSP/Subcode interface is automatically shut off while the CD-decoder is in Stop mode.
- 2) The clock to the ECC module is normally stopped until there is a header, a correction or repeat correction request occurs. After the request is serviced, the ECC clock will again be automatically shut off.
- 3) The clock to the CAV audio playback module is shut off until the SPA (Start Play Audio) bit 0 in register 4Dh is set.

12.5 Intel & Motorola Microprocessor Direct Access

The KS9245 is designed to be directly interfaced with Intel and Motorola type microprocessors without any external glue logic (refer to the Microprocessor Interface timing in section 9.1.1 and 9.1.2). The following diagrams show the connections for an Intel-type and Motorola-type microprocessor connected to the KS9245 in a direct access configuration. *Note: ISEL and MSEL can still be used as BADD7 and BADD8 to connect to DRAM addresses.*



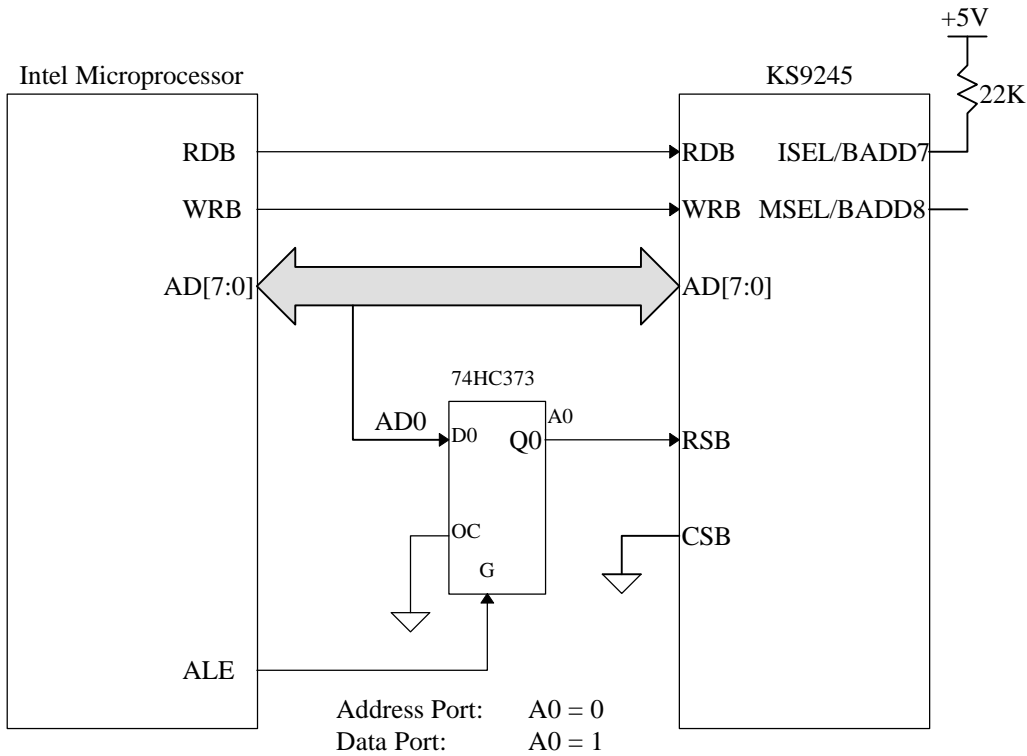
Intel Direct Access Interface Diagram



Motorola Direct Access Interface

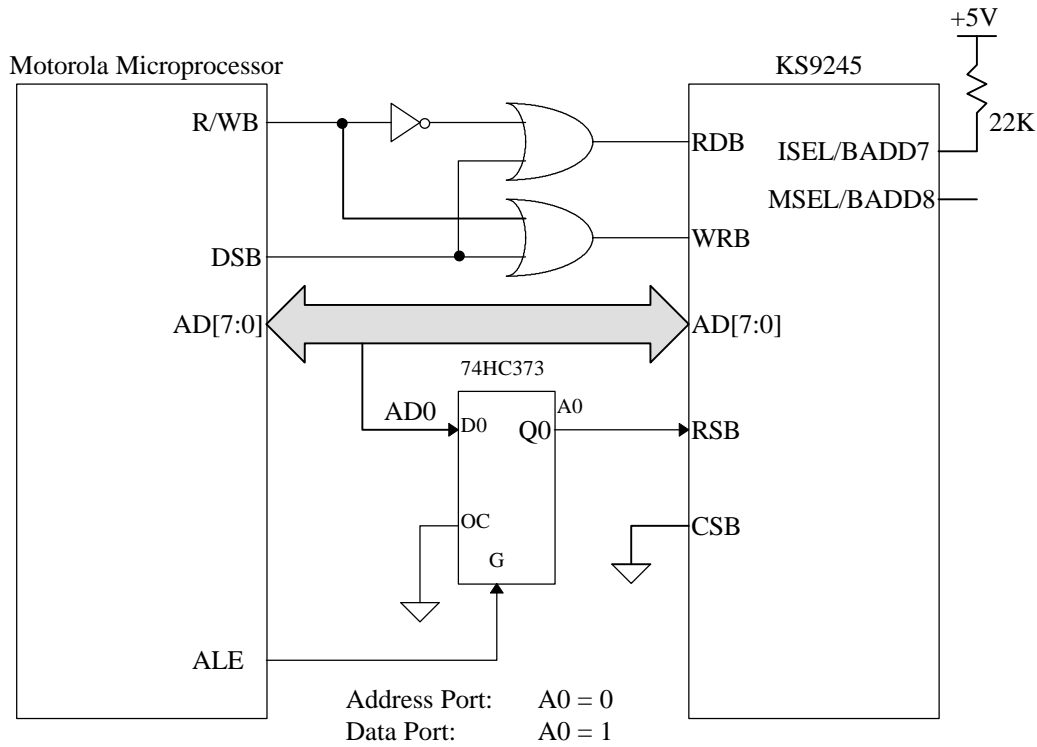
12.6 Intel & Motorola Microprocessor Indirect Access

The KS9245 is designed to be directly interfaced with Intel and Motorola type microprocessors without any external glue logic (refer to the Microprocessor Interface timing in section 9.1.1 and 9.1.2). However, if the timing specifications 9.1.1 and 9.1.2 cannot be satisfied, then an indirect access method must be used. For this case, the timing of section 9.1.3 is used. The following shows an interface scheme for using indirect access on the KS9245 with Intel and Motorola type microprocessors. *Note: For Indirect Access mode, ISEL needs to be sampled high by the KS9245 immediately after power-on. After this, both ISEL and MSEL can be used as BADD7 and BADD8 to interface with the DRAM, respectively.*



Intel Indirect Access Interface Diagram

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Motorola Indirect Access Interface Diagram

In this scheme, two access are required if the previous access is to a different location. The first access writes the address port to select a register in the KS9245 while the second access reads/writes the selected KS9245 register. For example, to read from register 10h of the KS9245, the first access should write 10h to any even address (A0=0) to program the address port with 10h. The next access must then be a read to any odd address (A0=1) to obtain the data from register location 10h.

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12.7 CAV Audio Playback and Digital Audio Support

Introduction

In traditional CLV (Constant Linear Velocity) applications, the CD disc speed must constantly be changed in order to maintain a constant linear velocity as the pickup head moves from inner track to outer track or vice versa. As a result, CD-ROM access times are severely impacted, especially when audio tracks must be played at single speed rates. To overcome this limitation, the KS9245 Automated ATAPI CD-ROM Controller integrates an Audio Buffer Manager and dedicated pins for support of CAV (Constant Angular Velocity) mode playback. In this mode, the KS9245 allows audio data to be buffered at up to 50X and played back at a constant 1X speed. Thus, CD-ROM access times are not impacted as a result of speed changes. Additionally, since the audio data is buffered, the KS9245 easily provides support for IEC-958 Digital Audio output at no extra cost. This applications note describes the Audio Buffer Manager, the CAV pins and register sets along with its Digital Audio support, and shows how to configure those pins and registers for CAV and Digital Audio mode playback.

Audio Buffer Manager

The KS9245 integrates an Audio Buffer Manager in order to simplify firmware efforts and efficiently control the CAV audio playback sequence. This hardware automatically keeps track of the available audio block(s) in the buffer DRAM and monitors buffer full and empty conditions. Audio blocks that are stored in DRAM are tracked by the **Valid Audio Block Count Register** (Reg48h). In the event of buffer full conditions, the firmware must stop the DSP buffering operation. In the event of buffer under-run conditions, the hardware automatically mutes the audio channels to mask any undesired noise. *Note that buffer full is determined by firmware keeping track of available DRAM space. Thus, firmware should stop the Audio Buffering before the DRAM actually becomes full to account for any response delays.*

CAV Pin Description

Table 1 lists the pins used for CAV mode playback. In CAV mode, these pins are dedicated outputs from the KS9245 to the audio DAC and carry audio data that have been buffered to DRAM by the KS9245. *Note: When not in CAV mode, these pins are General Purpose I/O pins.*

Physical Pin Assignment				
Signal	Pin	I/O	Description	Source / Destination
AWCK	13	O	Audio word clock output	KS9245 / DAC
ABCK	14	O	Audio bit clock output	KS9245 / DAC
ADAT	15	O	Audio data output	KS9245 / DAC

Table 1: CAV Pins

CAV Register Summary

Address	Name	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
48h R/W	VABC	Valid Audio Block Count Register B7:B0							
4Ah R/W	DABA	DAC Block Address Low Register B7:B0							
4Ch R/W	DOFS	ADAT18	ABCK D1	AFPS	ABCKL	ALSB F	ALCH	ABCKF	
4Dh R/W	DACR	LCM	RCM	Rsvd	Reserved	ACC	SPA		
4Eh R/W	ACCR	Rsvd	ABPS	DAUE	Rsvd		XINA Div		

Table 2: KS9245 Audio Mode Register Set

KS9245 ATAPI Automated CD-ROM Controller
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Table 2 lists a subset of the KS9245's registers used for configuring CAV mode playback. Detailed descriptions of these registers can be referenced in the *KS9245 ATAPI Automated CD-ROM Controller Engineering Specification*, available from IML.

Valid Audio Block Count Registers (VABC at 48h): This register specifies the number of valid audio blocks buffered into DRAM which are available for audio playback. Firmware must increment this register by one (to keep track of the audio block count) by writing a "1" to the **IncAudCnt** bit in the **Buffer Access Control Register** (Reg29h, bit7) after a decoder interrupt occurs in Audio Buffering Mode. This register is automatically decremented by one after one audio block has been output to the AWCK/ABCK/ADAT pins during CAV playback. *Note that a DAC interrupt is generated after one audio block is output to the AWCK/ABCK/ADAT pins. Also, when this occurs, the DACInt bit in the Decoder Interrupt Status Register (Reg11h, bit2) is set if the DACIntE bit in the Decoder Interrupt Mask Register (Reg13h, bit2) is set.*

DAC Block Address Register (DABA at 4Ah): This register points to the audio block in DRAM to be output or currently being output to the audio DAC. This register is automatically incremented to point to the next audio block to be played once the current block is completely outputted. *Note that this pointer will wrap around after the bottom of the buffer is reached.*

DAC Output Format Selection Register (DOFS at 4Ch): This register is used to select various audio output interface formats for CAV mode playback only. Table 3 lists the available formats using this register.

Audio Output Format Selection Summary								
Audio Format	ADAT18	ABCKD1	AFPS	ABCKL	ALSBF	ALCH	ABCKF	hex
EIAJ 16 bit	0	0	0	10	0	1	0	12h
EIAJ 18 bit	1	0	0	10	0	1	0	92h
I2S 16 bit	0	1	1	10	0	0	0	70h
I2S 18 bit	1	1	1	10	0	0	0	F0h

Table 3: Audio Output Format Selection

In addition, the KS9245 also supports an Audio Bypass mode where it allows inputs from DSP devices (such as Toshiba, Sanyo, and Sony) to be directly output to the AWCK / ABCK / ADAT pins without any conversions. This mode is set when the **ABPS** (Audio Bypass Mode) bit is set to "1" in the **Audio Clock Control Register** (Reg4Eh, bit 6).

DAC Control Register (DACR at 4Dh): This register is used to control various DAC output operations such as muting, mono / stereo / swap modes, and start play audio. Bit 7 and Bit 6 control the Left and Right Audio Channel muting for CAV and Audio Bypass modes, except for DAU Audio Bypass. When any of these bits are set to "1" in CAV or Audio Bypass modes, the corresponding audio channel is muted. When any of these bits are reset to "0", the corresponding audio channel is enabled. Following power-on, software reset, or ATAPI reset conditions, the state of these bits are set to "1" and both audio channels are muted. Table 4 summarizes the mono / stereo / swapped modes selected by bits 2 and 1.

Audio Channel Mode Selection			
Bit 2, Bit 1	Channel Mode	Description	Valid
00	Stereo	Output both left and right channels	CAV & Audio Bypass
01	Mono Right	Output right channel data to both channels	CAV Only
10	Mono Left	Output left channel data to both channels	CAV Only
11	Channel Swap	Left and Right channels data swap	CAV & Audio Bypass

Table 4: Audio Channel Mode Selection

SPA (bit 0) is used to start playing (outputting) the buffered audio blocks to the AWCK / ABCK / ADAT / DAUO pins. When **SPA** is set to “1” and the **ABPS** is reset to “0”, buffered audio data will be output to the AWCK / ABCK / ADAT pins. *Note: If the **DAUE** is also set to “1” in the **Audio Clock Control Register** (Reg4Eh, bit5), the buffered audio data will also be output to the **DAUO** (Digital Audio Output pin 4) simultaneously*

Audio Clock Control Register (ACCR at 4Eh): This register is used to select the audio clock source and audio bypass mode. Table 6 summarizes the audio clock selection for CAV mode only. *Note: the audio clock source is derived directly from the KS9245 system clock and is not internally configurable. Thus, the system clock should be driven from either a 33.8688MHz / 50.8 MHz source in order to match the Audio Clock requirements.*

Audio Clock Select					
Bit [1, 0]	System Clock Inputs	Audio Word Clock Length			Digital output
		16-BCK	24-BCK	32-BCK	DAUO
01	33.8688 MHz	valid	valid	valid	valid
11	50.8032 MHz	valid	valid	valid	valid
X0	Reserved				

Table 5: Audio Clock Selection

Additionally, bits 6 and 5 of this register control the enabling / disabling of Audio Bypass mode and Digital Audio mode (described above) respectively. Table 6 shows the Audio Mode Configuration Truth Table.

ABPS	SPA	DAUE	Audio Mode Selected	Channel Controls Allowed
1	X	X	DSP Inputs Bypass to DAC	Swap, Mute L/R
			DAUO Outputs	None
0	0	X	None	None
0	1	0	DAC Outputs	Swap, Mute L/R, Mono, Stereo
0	1	1	DAC and DAU Outputs Simultaneously	Swap, Mute L/R, Mono, Stereo

Table 6: Audio Mode Selection Table

CAV Mode Configuration

The following sequence shows how to configure the KS9245 for CAV mode playback:

1. Set the **APCE** (Audio Port Configuration Enable) bit to “1” in the **Global Control Register** (Reg2F, Bit3) to configure the **AWCK**, **ABCK**, and **ADAT** pins as output for CAV mode.
2. Select the KS9245’s DSP interface format in the **DSP Device Type Selection Register** (Reg3Eh). *Note that this selection must match the requirements of the DSP format for correction operation of audio playback.*
3. Select the audio output format (either EIAJ 16/18 bits or I2S 16/18 bits) in the **DAC Output Format Selection Register** (Reg4C). *Note that this selection must match the requirements of the Audio DAC to be interfaced with for correction operation of audio playback.*
4. Configure the audio sample rate and channel mode for stereo, mono, or swapped in the **DAC Control Register** (Reg4D).

-
5. Select the appropriate Audio Word Clock Length in the **Audio Clock Control Register** (Reg4E).
 6. Set the Address Pointer in the **DAC Block Address Registers** (Reg4A) to point to the start of Audio Data in DRAM to be played.
 7. Set the **SPA** (Start Play Audio) bit to "1" in the **DAC Control Register** (Reg4D) to start outputting the audio data pointed to by the **DAC Block Address Register**.

IEC-958 Digital Audio Support

Digital Audio support has traditionally been provided by the CD-DSP controllers and not the CD-Decoders. However, since Decoders such as the KS9245 now provide support for CAV mode playback by buffering the Audio data, Digital Audio on the DSP controllers cannot be used while the Decoders are in CAV mode. Thus, to take advantage of both CAV and Digital Audio, the KS9245 implements on-board Digital Audio support (EIAJ IEC-958 standard) using the Sony/Phillips Digital Signal format. This implementation comprises an DAUO pin (output pin 4) and an DAUIN pin (input pin 16), as well as an DAUE (enable) bit in the **Audio Clock Control Register** (Reg4Eh, bit5).

IEC-958 Digital Audio Configuration

To configure the Digital Audio channel for outputting audio data, CAV mode and the DAC interface must first be properly configured (refer to CAV Mode Configuration described above and note that a 33.8MHz system clock must be used). Once CAV mode and the DAC interface are configured, setting both the **DAUE** bit (Reg4Eh) and the **SPA** bit (Reg4Dh) to "1" will allow IEC-958 Sony/Phillips Digital Audio formatted data to be output on the DAUO pin. *Note that the **ABPS** bit (Reg4Eh) must be reset to "0".* Additionally, when the Audio Bypass mode is selected, the KS9245 allows the Digital Audio data to come from an outside source such as the CD-DSP. In this case, the CD-DSP's DAUO pin would be connected to the KS9245's DAUIN pin, and the audio data would be directly bypassed to the DAUO pin of the KS9245. The benefit of the feature is that it allows for the same board design to support both CAV and CLV mode playback. *Note that in the Digital Audio (DAU) Bypass mode, all audio channel mode controls such as channel muting, channel swapping, and mono left and right channels have no affect on the Digital Audio data being output on the DAUO. Thus, this data is always played back in stereo on the DAUO pin in DAU Bypass mode.*