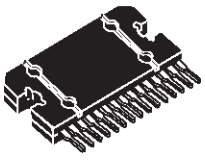
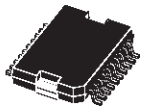
L3000S

HIGH VOLTAGE INTERFACE

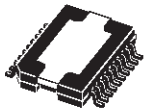
- TELEPHONE LINE FEEDING WITH DIRECT OR REVERSAL POLARITY
- EXTRA FEEDING FOR LONG TELEPHONE LINE
- LINE SENSING ON BOTH WIRES
- BALANCED RINGING SIGNAL INJECTION
- HIGH OUTPUT CURRENT CAPABILITY
- THERMAL OVERLOAD PROTECTION



Flexiwatt15



PowerSO20 (slug-down)



PowerSO20 (slug-up)

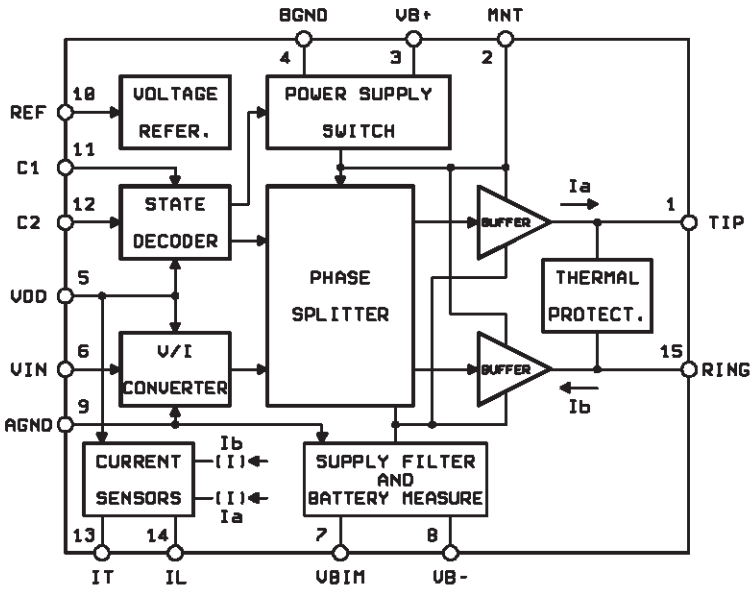
ORDERING NUMBERS:

L3000SX-VC	L3000SX-77	L3000SX

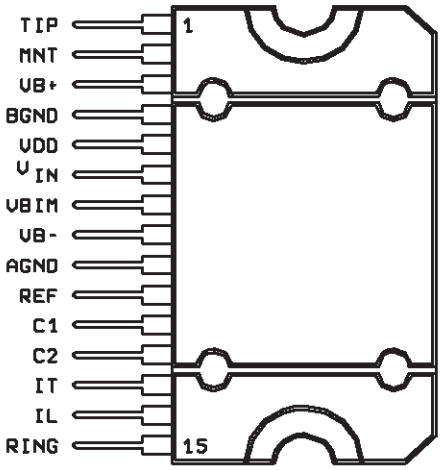
DESCRIPTION

The L3000S line interface provides a battery feeding for telephone lines and ringing injection. It contains a state decoder that under external control forces three operational modes (with their options): standby, conversation and ringing. Two pins give information about the line status detected by sensing the line current into the output stage. The IC amplifies the signal entering at pin 6(V_{IN}). Separate ground pins are also provided for the output stages that are referred to battery ground, and for analog signal processing circuits that are referred to analog ground. The L3000S needs only two external components; a resistor to provide internal bias current and a capacitor to filter battery AC components.

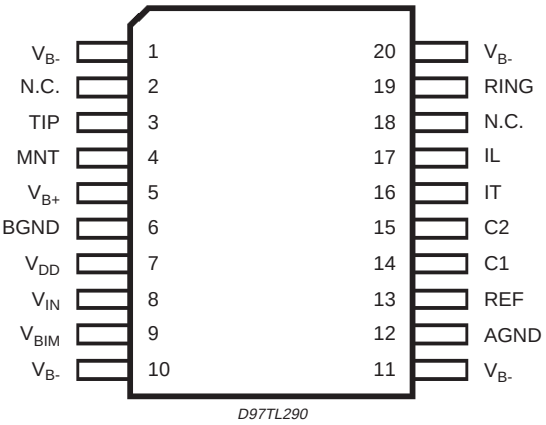
BLOCK DIAGRAM



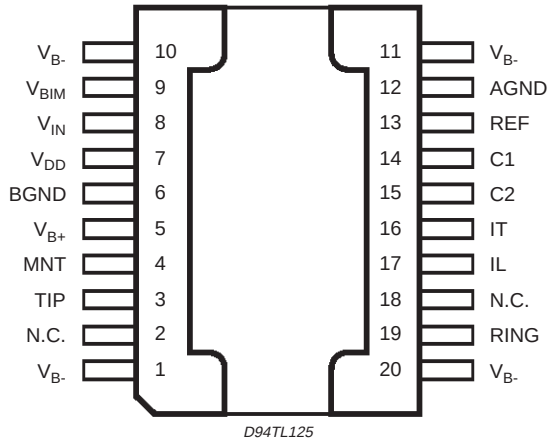
PIN CONNECTIONS (Top view)



FLEXIWATT15



PowerSO20 (Slug-down)



PowerSO20 (Slug-up)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_b–	Negative Battery Voltage	– 80	V
V_b+	Positive Battery Voltage	80	V
$\|V_b–\|+\|V_b+\|$	Total Battery Voltage	140	V
V_{dd}	Positive Supply Voltage	+ 6	V
$\|V_{agnd}–V_{bgnd}\|$	Max Voltage between Analog Ground and Battery Ground	5	V
T_j	Max Junction Temperature	+ 150	°C
T_{stg}	Storage Temperature	– 55 to + 150	°C

OPERATING RANGE

Symbol	Parameter	Min.	Typ.	Max.	Unit
$T_{j\ oper}$	Operating Temperature Range	–40		120	°C
V_b–	Negative Battery Voltage	– 70	– 48	– 24	V
V_b+	Positive Battery Voltage	0	+ 72	+ 75	V
$\|V_b– \|+\|V_b+\|$	Total Battery Voltage		120	130	V
V_{dd}	Positive Supply Voltage	+ 4.5		+ 5.5	V
I_{max}	Total Line Current ($I_L + I_T$)			85	mA

PIN DESCRIPTION

FLEX. N°	SO-P. N°	Name	Description
1	3	TIP	A line termination output with current capability up to 100mA (I_s is the current sourced from this pin).
2	4	MNT	Positive Supply Voltage Monitor.
3	5	V_{B+}	Positive Battery Supply Voltage.
4	6	BGND	Battery ground relative to the V_{B+} and the V_{B-} supply voltages. It is also the reference ground for TIP and RING signals.
5	7	V_{DD}	Positive Power Supply +5V.
6	8	V_{IN}	2 wire unbalanced voltage input.
7	9	VBIM	Output voltage without current capability, with the following functions: - give an image of the total battery voltage scaled by 40 to the low voltage part. - filter by an external capacitor the noise on V_{B+} and the V_{B-}.
8	1,10,11, 20	V_{B-}	Negative Battery Supply Voltage.
9	12	AGND	Analog Ground. All input signals and the V_{DD} supply voltage must be referred to this pin.
10	13	REF	Voltage reference output with very low temperature coefficient. The connected resistor sets Internal circuit bias current.
11	14	C1 (NB/BB/RG)	Digital signal input (3 levels) that defines device status with pin 12. In thermal overload condition a 240µA typ. current is sunk by this pin (*).
12	15	C2 (PD/DP/RP)	Digital signal input (3 levels) that defines device status with pin 11. (*)
13	16	I_T	High precision scaled transversal line current signal. $I_T = \frac{I_a + I_b}{100}$
14	17	I_L	Scaled longitudinal line current signal. $I_L = \frac{I_a - I_b}{100}$
15	19	RING	B line termination output with current capability up to 100mA (I_b is the current sunk into this pin).
–	2, 18	N.C.	Not connected.

Note: 1) Unless otherwise specified all the diagrams in this datasheet refers to the FLEXIWATT15 pin connection.

(*) Truth table for the State Control Inputs C1 and C2.

		C1		
		+3V	**0V**	**–3V**
C2	**+3V**	STBY	A OPEN	B OPEN RP
	0V	CONV.NP	BB. NP	RING NP
	–3V	CONV.RP	BB. RP	RING RP

1)Recommended sequence for power on during automatic testing is: **1)** GND; **2)** VB–; **3)** VDD; **4)** VB+. During power off the opposite sequence should be used: **1)** VB+; **2)** VDD; **3)** VB–; **4)** GND.

2)In case power on sequence cannot be guaranteed (i.e. not insertion in real application and so on). a shottky diode should be connected between BGND and VB–. The shottky diode characteristics should be: $V_F < 450mV$ @ $I_F = n \cdot 15mA$, $T_{amb} = 25°C$
$V_F < 350mV$ @ $I_F = n \cdot 15mA$, $T_{amb} = 50°C$ ($T_{jL3000} = 90°C$)
$V_F < 245mV$ @ $I_F = n \cdot 15mA$, $T_{amb} = 85°C$ ($T_{jL3000} = 120°C$)
Where n is the number of line sharing the same diode

DC ELECTRICAL CHARACTERISTICS (Refer to the test circuits, Tamb +25°C, $V_{B+} = 72V$, $V_{BT} = –48V$, $V_{DD} = +5V$)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_{dds}	Stand-by V_{DD} Supply Current			1.4	1.9	mA	1
I_{ddo}	Operation V_{DD} Supply Current	Pin 11 to +5V		2	2.8	mA	2
$I_{dd\ DE}$	Power Denial V_{DD} Supply Current	Pin 10 Not Connected			150	µA	1, 2
$I_{b–s}$	Stand–by $V_{B–}$ Supply Current			2	2.5	mA	1
$I_{b–o}$	Operation $V_{B–}$ supply current	Pin 11 to +5V		5	6.5	mA	2
$I_{b\ –DE}$	Power Denial $V_{B–}$ Supply Current	Pin 10 Not Connected			50	µA	1, 2
I_{b+s} I_{b+o}	Stand–by and Operation V_{B+} Supply Current	Pin 11 to +5V		10	15	µA	1, 2
$I_{b\ +DE}$	Power Denial VB+ Supply Current	Pin 10 Not Connected			15	µA	1, 2
I_{b+b}	V_{B+} Supply Current in Boost Battery	Pin 11 to AGND		4.5	5.5	mA	2
$I_{b–b}$	$V_{B–}$ Supply Current in Boost Battery			6.6	8	mA	2
$I_{b–r}$	$V_{B–}$ Supply Current	Pin 11 to –5V		14	17	mA	2
I_{b+r}	V_{B+} Supply Current			12	13.5	mA	2
V_{ref}	Voltage Reference	(Note 1)	1.20	1.30	1.40	V	2
V_{hl}	Input High Level	inputs on pins 11, 12	2			V	–
V_{zl}	Input Zero Level		–0.8	0	+0.8	V	–
V_{ll}	Input Low Level				–2	V	–
$\|I_{lc}\|$	Input Bias Current				4	µA	–
Leak 1,15	Leakage on Pin1 and Pin15	Pin10 = Not Connected Pin1 + Pin15 to V_{B+} $V_{B+} = +60V, V_{B-} = -60V$			30	µA	–
Leak 2	Leakage on Pin 2	Pin10 = Not Connected $V_{B+} = +60V, V_{B-} = -60V$ $V_{P2} = 60V$			30	µA	–
V_{mnt}	Monitor VB+ Voltage (Note 2)	Pin 11 to +5V	–1.1	–0.8		V	2
		Pin 11 to 0V	70	71		V	2
V_{bim}	Battery Image Voltage (Notes 2,4)	Pin 11 to +5V	–1.163	–1.09	–1.013	V	2
		Pin 11 to AGND	–3.08	–2.93	–2.78	V	2
R_{2W}	Input Resistance	Pin 6	100			KΩ	–
$C_{L\ ref}$	Max. Capacitor for pin 10				5	pF	–
$\|I_{tm}\|$	Output Current on pin 13	$I_a = I_b = 0mA$ $I_a = I_b = 20mA$ $V_{in} = –180mV$ Pin12 = +5V or 0V or –5V Pin11 = +5V	–15 380		+15 420	µA µA	3
		$I_a = I_b = 50mA$ $V_{in} = –0.5V$ Pin12 = 0Vor –5V Pin11 = +5V	950		1050	µA	3

DC ELECTRICAL CHARACTERISTICS (Refer to the test circuits, Tamb +25°C, V_{B+} = 72V, V_{BT} = –48V, V_{DD} = +5V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
$\|I_{tm}\|$	Output Current on pin 13	$I_a = I_b$ = 0mA V_{in} = 0V Pin12 = 0V Pin11 = –5V	–10		10	µA	3
$\|I_{lm}\|$	Output Current on pin 14	$I_a = I_b$ = 0mA $I_a = I_b$ = 20mA V_{in} = –180mV Pin12 = +5V or 0V or –5V Pin11 = +5V	–30 –30		30 30	µA µA	3
		I_a = 15mA I_b = 25mA V_{in} = –180mV Pin12 = +5V or 0V or –5V Pin11 = +5V	65		135	µA	3
		I_a = 37.5mA I_b = 62.5mA V_{in} = –0.5V Pin12 = 0Vor –5V Pin11 = +5V	182		318	µA	3
V_{ldc}	Voltage Between Pins1 and 15 (Notes 3,5)	V_{bt} = -70V, Pin12 = 5V Pin11 = 5V V_{IN} = –0.5V V_{IN} = –2V Pin12 = 0 or -5V Pin11 = 5V V_{IN} = 0V V_{IN} = –0.5V V_{IN} = -1V V_{IN} = –2V	 42 63 46 25.5		 58.5 0 67.5 48 28.5 0	 V V V V V V	3
V_{lrg}	Voltage Between pins 1 and 15		20.4	23	25.6	V	4
$\|I_{om}\|$	Maximum Output Current at Pins 1, 15	Pin 12 = 0 or –5V Pin 12 = +5V; Pin 10 = N.C.	90 38		130 70 30	mA mA µA	4A
$\|I_{oma}\|$	Maximum Output Current at Pin 1 (A open)	Pin 12 = +5V Pin 11 = 0V			30	µA	4A
$\|I_{omb}\|$	Maximum Output Current at Pin 15 (B open R_P)	Pin 12 = +5V Pin 11 = 0V			30	µA	4A
I_{thv}	Thermal Overload Current from Pin11	T_{case} = 150°C	400			µA	–

Note 1: Use a voltmeter in series with 10KΩ connected to pins 10 and 9. **Note 2:** With high impedance voltmeter (>100KΩ).
Note 3: 0V max means inversion of pin1 and 15. **Note 4:** $|V_{BIM}| = (|V_{BTot}| – 2.8V – 2 \cdot V_{BE}) / 40$ Where: $V_{BTot} = |V_{B–}|$ for pin11 to +5V; pin 12 to GND or –5V $V_{BTot} = |V_{B+}| + |V_{B–}|$ for pin 11 to 0V; Pin 12 to GND or –5V. $2 \cdot V_{BE}$ = 1.5V @ T_{amb} = 25°C. **Note 5:** $V_{ldc} = |V_{BT}| – |V_{in}| \cdot 40 – 2.8$.

AC ELECTRICAL CHARACTERISTICS(Refer to the test circuits, Tamb +25°C, V_{B+} = 72V, V_{BT} = –48V, V_{DD} = +5V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
| G_R |	Receiving Gain (note 6)	nor.bat I_L = 20mA I_L = 50mA	31.92 31.88	32.04 32.04	32.16 32.20	dB dB	5
		boo.bat I_L = 20mA	31.74	32.04	32.34	dB	5
d | G_R |	Gain Flatness Rx	300 < f < 3400Hz (note 7, 9)	–0.05		+0.05	dB	5
d | G_T |	Gain Flatness Tx (note 8)	300 < f < 3400Hz (note 7, 9)	–0.05		+0.05	dB	5A
THD	Total Harmonic Distortion of Receiving Signal	f = 1KHz $V_{ab\ AC}$			0.3	%	5A
K_{ITAC}	AC Transversal Current Ratio	Normal and Reverse @ I_L = 20mA, I_L = 50mA boo.bat @ I_L = 20mA	49.5 49.4	50	50.5 50.6		6
G_T	Gain Tracking Rx, Tx (Note 10)	VLine = +3 to –20dBm0	–0.2		+0.2	dB	5
THD_{TTX}	Metering Distortion	f = 16KHz I_{LDC} = 0 I_{LDC} = 50mA V_{abAC} = 2Vrms V_{abAC} = 5Vrms			 5 3 3	 % % %	13
|Cmlt|	CMRR Longitud. to Transv.	US Market 1020Hz World Market (300 to 3400Hz)	81 75			dB dB	7
|Cmtl|	CMRR Transv. to Longitud.		48			dB	8
SVRR	Supply Voltage Rejection Rat. on Vb–	300 < f < 3400Hz	30			dB	9
SVRR	Supply Voltage Rejection Rat. on V_{DD}	f = 3.4KHz on V_{ab} NP, RP f = 3.4KHz on V_{tAC} NP f = 3.4KHz on V_{tAC} RP	30 40 40			dB dB dB	10
V_{ring}	Output Ringing Voltage	V_{IN} = 1.550Vrms (16-66Hz)	61			Vrms	11
THD	Ringing Signal Distortion	V_{IN} = 1.550Vrms (16-66Hz)			4	%	11
Np	Psophometric Noise	Between Pin1 and 15 on Pin13		 -102	–75	dBmp	12

Note 6: $|G_R| = 20\log(|VabAC|/V_{IN}\ AC|)$; **Note 7:** Guaranteed by design; **Note 8:** d | G_T | defines K_{ITAC} accuracy vs. frequency.
Note 9: Measured respect the value @ f = 1020Hz; **Note 10:** Gain Tracking Tx defines K_{ITAC} accuracy vs. level.

DC ELECTRICAL CHARACTERISTICS (Refer to the test circuits, T_j = 90°C, V_{B+} = 72V, V_{BT} = –48V, V_{DD} = +5V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_{dds}	Stand-by V_{DD} Supply Current				1.95	mA	1
I_{ddo}	Operation V_{DD} Supply Current	Pin 11 to +5V			2.9	mA	2
$I_{dd\ DE}$	Power Denial V_{DD} Supply Current	Pin 10 Not Connected			240	µA	1, 2
I_{b-s}	Stand–by V_{B-} Supply Current				2.6	mA	1
I_{b-o}	Operation V_{B-} supply current	Pin 11 to +5V			6.7	mA	2
$I_{b\ -DE}$	Power Denial V_{B-} Supply Current	Pin 10 Not Connected			150	µA	1, 2
I_{b+s} I_{b+o}	Stand–by and Operation V_{B+} Supply Current	Pin 11 to +5V			30	µA	1, 2
$I_{b\ +DE}$	Power Denial VB+ Supply Current	Pin 10 Not Connected			30	µA	1, 2
I_{b+b}	V_{B+} Supply Current in Boost Battery	Pin 11 to AGND			5.8	mA	2
I_{b-b}	V_{B-} Supply Current in Boost Battery				8.4	mA	2
I_{b-r}	V_{B-} Supply Current	Pin 11 to –5V			17.8	mA	2
I_{b+r}	V_{B+} Supply Current				14	mA	2
V_{ref}	Voltage Reference	(Note 1)	1.175		1.425	V	2
V_{hl}	Input High Level	inputs on pins 11, 12	2			V	–
V_{zl}	Input Zero Level		–0.8	0	+0.8	V	–
V_{ll}	Input Low Level				–2	V	–
$\|I_{lc}\|$	Input Bias Current	Pin 12			10	µA	–
		(Note 11) Pin 11			60	µA	–
Leak 1,15	Leakage on Pin1 and Pin15	Pin10 = Not Connected Pin1 + Pin15 to V_{B+} V_{B+} = +60V,V_{B-} = -60V			200	µA	–
Leak 2	Leakage on Pin 2	Pin10 = Not Connected V_{B+} = +60V,V_{B-} = -60V V_{P2} = 60V			200	µA	–
V_{mnt}	Monitor VB+ Voltage (Note 2)	Pin 11 to +5V	–1.15			V	2
		Pin 11 to 0V	69.8			V	2
V_{bim}	Battery Image Voltage (Notes 2,4)	Pin 11 to +5V	–1.178		–0.998	V	2
		Pin 11 to AGND	–3.12		–2.73	V	2
R_{2W}	Input Resistance	Pin 6	100			KΩ	–
$C_{L\ ref}$	Max. Capacitor for pin 10				5	pF	–
$\|I_{tm}\|$	Output Current on pin 13	I_a = I_b = 0mA I_a = I_b = 20mA V_{in} = –180mV Pin12 = +5V or 0V or –5V Pin11 = +5V	–20 374		+20 426	µA µA	3
		I_a = I_b = 50mA V_{in} = –0.5V Pin12 = 0Vor –5V Pin11 = +5V	935		1065	µA	3
		I_a = I_b = 0mA V_{in} = 0V Pin12 = 0V Pin11 = –5V	–13		+13	µA	3

DC ELECTRICAL CHARACTERISTICS (Refer to the test circuits, T_j = 90°C, V_{B+} = 72V, V_{BT} = –48V, V_{DD} = +5V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
$\|I_{Im}\|$	Output Current on pin 14	I_a = I_b = 0mA I_a = I_b = 20mA V_{in} = –180mV Pin12 = +5V or 0V or –5V Pin11 = +5V	–35 –45		+35 +45	µA µA	3
		I_a = 15mA I_b = 25mA V_{in} = –180mV Pin12 = +5V or 0V or–5V Pin11 = +5V	62		138	µA	3
		I_a = 37.5mA I_b = 62.5mA V_{in} = –0.5V Pin12 = 0Vor –5V Pin11 = +5V	176		324	µA	3
V_{Idc}	Voltage Between Pins1 and 15 (Notes 3,5)	V_{bt} = -70V,Pin12 = 5V Pin11 = 5V V_{IN} = –0.5V V_{IN} = –2V Pin12 = 0 or -5V Pin11 = 5V V_{IN} = 0V V_{IN}= –0.5V V_{IN} = -1V V_{IN}= –2V	41.5 62.5 45.5 25		59 0 68 48.5 29 0	V V V V V V	3
V_{Irg}	Voltage Between pins 1 and 15		19.9		26.2	V	4
$\|I_{Iom}\|$	Maximum Output Current at Pins 1, 15	Pin 12 = 0 or –5V Pin 12 = +5V; Pin 10 = N.C.	86 30		134 70 50	mA mA µA	4A
$\|I_{Ioma}\|$	Maximum Output Current at Pin 1 (A open)	Pin 12 = +5V Pin 11 = 0V			50	µA	4A
$\|I_{Iomb}\|$	Maximum Output Current at Pin 15 (B open R_P)	Pin 12 = +5V Pin 11 = 0V			50	µA	4A

Note 1: Use a voltmeter in series with 10KΩ connected to pins 10 and 9.
Note 2: With high impedance voltmeter (>100KΩ).
Note 3: 0V max means inversion of pin1 and 15.
Note 4: $|V_{BIM}| = (|V_{BTot}| – 2.8V – 2 \cdot V_{BE}) / 40$ Where: $V_{BTot} = |V_{B–}|$ for pin11 to +5V; pin 12 to GND or –5V $V_{BTot} = |V_{B+}|+|V_{B–}|$ for pin 11 to 0V; Pin 12 to GND or –5V. $2 \cdot V_{BE}$ = 1.5V @ T_{amb} = 25°C.
Note 5: $V_{Idc} = |V_{BT}| – |V_{in}| \cdot 40 – 2.8$.
Note 11: Due to the analog structure of the thermal sensor connected to pin 11 the input bias current at this pin is not a step function but depends on junction temperature (compare with I_{thv} parameter at page 5).

AC ELECTRICAL CHARACTERISTICS(Refer to the test circuits, T_j = 90°C, V_{B+} = 72V, V_{BT} = –48V, V_{DD} = +5V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
$\|G_R\|$	Receiving Gain (note 6)	nor.bat I_L = 20mA I_L = 50mA	31.82 31.78		32.26 32.30	dB dB	5
		boo.bat I_L = 20mA	31.64		32.44	dB	5
$d\|G_R\|$	Gain Flatness Rx	300 < f < 3400Hz (note 7, 9)	–0.08		+0.08	dB	5
$d\|G_T\|$	Gain Flatness Tx (note 8)	300 < f < 3400Hz (note 7, 9)	–0.08		+0.08	dB	5A
THD	Total Harmonic Distortion of Receiving Signal	f = 1KHz $V_{ab\ AC}$			0.35	%	5A
K_{ITAC}	AC Transversal Current Ratio	Normal and Reverse @ I_L = 20mA, I_L = 50mA boo.bat @ I_L = 20mA	49.2 49.1	50	50.8 50.9		6
G_T	Gain Tracking Rx, Tx (Note 10)	VLine = +3 to –20dBm0	–0.25		+0.25	dB	5
THD_{TTX}	Metering Distortion	f = 16KHz I_{LDC} = 0 I_{LDC} = 50mA V_{abAC} = 2Vrms V_{abAC} = 5Vrms			 6 3.5 3.5	 % % %	13
|Cmlt|	CMRR Longitud. to Transv.	World Market (300 to 3400Hz)	72			dB	7
|Cmtl|	CMRR Transv. to Longitud.		46			dB	8
SVRR	Supply Voltage Rejection Rat. on Vb–	300 < f < 3400Hz	27			dB	9
SVRR	Supply Voltage Rejection Rat. on V_{DD}	f = 3.4KHz on V_{ab} NP, RP f = 3.4KHz on V_{tAC} NP f = 3.4KHz on V_{tAC} RP	28 40 40			dB dB dB	10
V_{ring}	Output Ringing Voltage	V_{IN} = 1.550Vrms (16-66Hz)	60			Vrms	11
THD	Ringing Signal Distortion	V_{IN} = 1.550Vrms (16-66Hz)			5	%	11
Np	Psophometric Noise	Between Pin1 and 15 on Pin13		 -101	–74	dBmp	12

Note 6: $|G_R| = 20\log(|VabAC|/V_{IN}\ AC|)$;
Note 7: Guaranteed by design;
Note 8: $d|G_T|$ defines K_{ITAC} accuracy vs. frequency.
Note 9: Measured respect the value @ f = 1020Hz;
Note 10: Gain Tracking Tx defines K_{ITAC} accuracy vs. level.

DC ELECTRICAL CHARACTERISTICS (Refer to the test circuits, –40°C < T_j < 0°C and 90°C < T_j < 120°C, V_{B+} = 72V, V_{BT} = –48V, V_{DD} = +5V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_{dds}	Stand-by V_{DD} Supply Current				2.0	mA	1
I_{ddo}	Operation V_{DD} Supply Current	Pin 11 to +5V			3.0	mA	2
$I_{dd\ DE}$	Power Denial V_{DD} Supply Current	Pin 10 Not Connected			300	µA	1, 2
I_{b-s}	Stand–by V_{B-} Supply Current				2.7	mA	1
I_{b-o}	Operation V_{B-} supply current	Pin 11 to +5V			6.9	mA	2
$I_{b\ -DE}$	Power Denial V_{B-} Supply Current	Pin 10 Not Connected			350	µA	1, 2
I_{b+s} I_{b+o}	Stand–by and Operation V_{B+} Supply Current	Pin 11 to +5V			50	µA	1, 2
$I_{b\ +DE}$	Power Denial VB+ Supply Current	Pin 10 Not Connected			50	µA	1, 2
I_{b+b}	V_{B+} Supply Current in Boost Battery	Pin 11 to AGND			6.2	mA	2
I_{b-b}	V_{B-} Supply Current in Boost Battery				8.8	mA	2
I_{b-r}	V_{B-} Supply Current	Pin 11 to –5V			18.5	mA	2
I_{b+r}	V_{B+} Supply Current				14.5	mA	2
V_{ref}	Voltage Reference	(Note 1)	1.150		1.450	V	2
V_{hl}	Input High Level	inputs on pins 11, 12	2			V	–
V_{zl}	Input Zero Level		–0.8		+0.8	V	–
V_{ll}	Input Low Level				–2	V	–
$\|I_{lc}\|$	Input Bias Current	Pin 12			30	µA	–
		(Note 11) Pin 11			300	µA	–
V_{mnt}	Monitor VB+ Voltage (Note 2)	Pin 11 to +5V	–1.2			V	2
		Pin 11 to 0V V_{B+} = +45V	42.6			V	2
V_{bim}	Battery Image Voltage (Notes 2,4)	Pin 11 to +5V	–1.193		–0.983	V	2
		Pin 11 to AGND V_{B+} = +45V, V_{B-} = –56V	–2.58		–2.2	V	2
R_{2W}	Input Resistance	Pin 6	100			KΩ	–
$C_{L\ ref}$	Max. Capacitor for pin 10				5	pF	–
$\|I_{tm}\|$	Output Current on pin 13	I_a = I_b = 0mA I_a = I_b = 20mA V_{in} = –180mV Pin12 = +5V or 0V or –5V Pin11 = +5V	–25 370		+25 430	µA µA	3
		I_a = I_b = 0mA V_{in} = 0V Pin12 = 0V Pin11 = –5V	–15		+15	µA	3

DC ELECTRICAL CHARACTERISTICS (Refer to the test circuits, –40°C < T_j < 0°C and 90°C < T_j < 120°C, V_{B+} = 72V, V_{BT} = –48V, V_{DD} = +5V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
$\|I_{lm}\|$	Output Current on pin 14	I_a = I_b = 0mA I_a = I_b = 20mA V_{in} = –180mV Pin12 = +5V or 0V or –5V Pin11 = +5V	–40 –50		+40 +50	µA µA	3
		I_a = 15mA I_b = 25mA V_{in} = –180mV Pin12 = +5V or 0V or –5V Pin11 = +5V	60		140	µA	3
V_{ldc}	Voltage Between Pins1 and 15 (Notes 3,5)	V_{bt} = -70V, Pin12 = 5V Pin11 = 5V V_{IN} = –0.5V V_{IN} = –2V Pin12 = 0 or -5V Pin11 = 5V V_{IN} = 0V V_{IN} = –0.5V V_{IN} = -1V V_{IN} = –2V	 41 62 45 24.6		 59.5 0 68.5 49 29.4 0	 V V V V V V	3
V_{lrg}	Voltage Between pins 1 and 15	V_{B+} = +45V, V_{B-} = -56V	17		25	V	4
$\|I_{om}\|$	Maximum Output Current at Pins 1, 15	Pin 12 = 0 or –5V Pin12 = +5V P1 or P15 to GND Pin12 = +5V P1 or P15 to V_{B-}	70 30 20		140 70 70	mA mA mA	4A

Note 1: Use a voltmeter in series with 10KΩ connected to pins 10 and 9.
Note 2: With high impedance voltmeter (>100KΩ).
Note 3: 0V max means inversion of pin1 and 15.
Note 4: $|V_{BIM}| = (|V_{BTot}| – 2.8V – 2 \cdot V_{BE}) / 40$ Where: $V_{BTot} = |V_{B–}|$ for pin11 to +5V; pin 12 to GND or –5V $V_{BTot} = |V_{B+}|+|V_{B–}|$ for pin 11 to 0V; Pin 12 to GND or –5V. $2 \cdot V_{BE}$ = 1.5V @ T_{amb} = 25°C.
Note 5: $V_{ldc} = |V_{BT}| – |V_{in}| \cdot 40 – 2.8$.
Note 11: Due to the analog structure of the thermal sensor connected to pin 11 the input bias current at this pin is not a step function but depends on junction temperature (compare with I_{thv} parameter at page 5).

AC ELECTRICAL CHARACTERISTICS (Refer to the test circuits, –40°C < T_j < 0°C and 90°C < T_j < 120°C, V_{B+} = 72V, V_{BT} = –48V, V_{DD} = +5V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
$\| G_R \|$	Receiving Gain (note 6)	nor.bat I_L = 25mA	31.82		32.26	dB	5
d $\| G_R \|$	Gain Flatness Rx	300 < f < 3400Hz (note 7, 9)	–0.1		+0.1	dB	5
d $\| G_T \|$	Gain Flatness Tx (note 8)	300 < f < 3400Hz (note 7, 9)	–0.1		+0.1	dB	5A
THD	Total Harmonic Distortion of Receiving Signal	f = 1KHz $V_{ab\ AC}$			0.4	%	5A
K_{ITAC}	AC Transversal Current Ratio	Normal and Reverse @ I_L = 20mA,	49		51		6
G_T	Gain Tracking Rx, Tx (Note 5)	VLine = +3 to –20dBm0	–0.3		+0.3	dB	5
THD_{TTX}	Metering Distortion	f = 16KHz I_{LDC} = 50mA V_{abAC} = 2Vrms			 4	 %	13
|Cmlt|	CMRR Longitud. to Transv.	World Market (300 to 3400Hz)	70			dB	7
|Cmtl|	CMRR Transv. to Longitud.		45			dB	8
SVRR	Supply Voltage Rejection Rat. on Vb–	300 < f < 3400Hz	22			dB	9
SVRR	Supply Voltage Rejection Rat. on V_{DD}	f = 3.4KHz on V_{ab} NP, RP f = 3.4KHz on V_{tAC} NP f = 3.4KHz on V_{tAC} RP	27 40 40			dB dB dB	10
V_{ring}	Output Ringing Voltage	V_{B+} = +45V, V_{B-} = -56V V_{IN} = (16-66Hz)1Vrms	38.5	40.0		Vrms	11
THD	Ringing Signal Distortion	V_{B+} = +45V, V_{B-} = -56V V_{IN} = (16-66Hz)1Vrms Rloop = 450Ω + 3.4µF			4.5	%	11
Np	Psophometric Noise	Between Pin1 and 15 on Pin13		 -94	–65	dBmp	12

Note 6: $|G_R| = 20\log(|VabAC|/V_{IN}\ AC|)$;
Note 7: Guaranteed by design;
Note 8: d $| G_T |$ defines K_{ITAC} accuracy vs. frequency.
Note 9: Measured respect the value @ f = 1020Hz;
Note 10: Gain Tracking Tx defines K_{ITAC} accuracy vs. level.

TEST CIRCUITS

Figure 1: Stand-by Supply Current

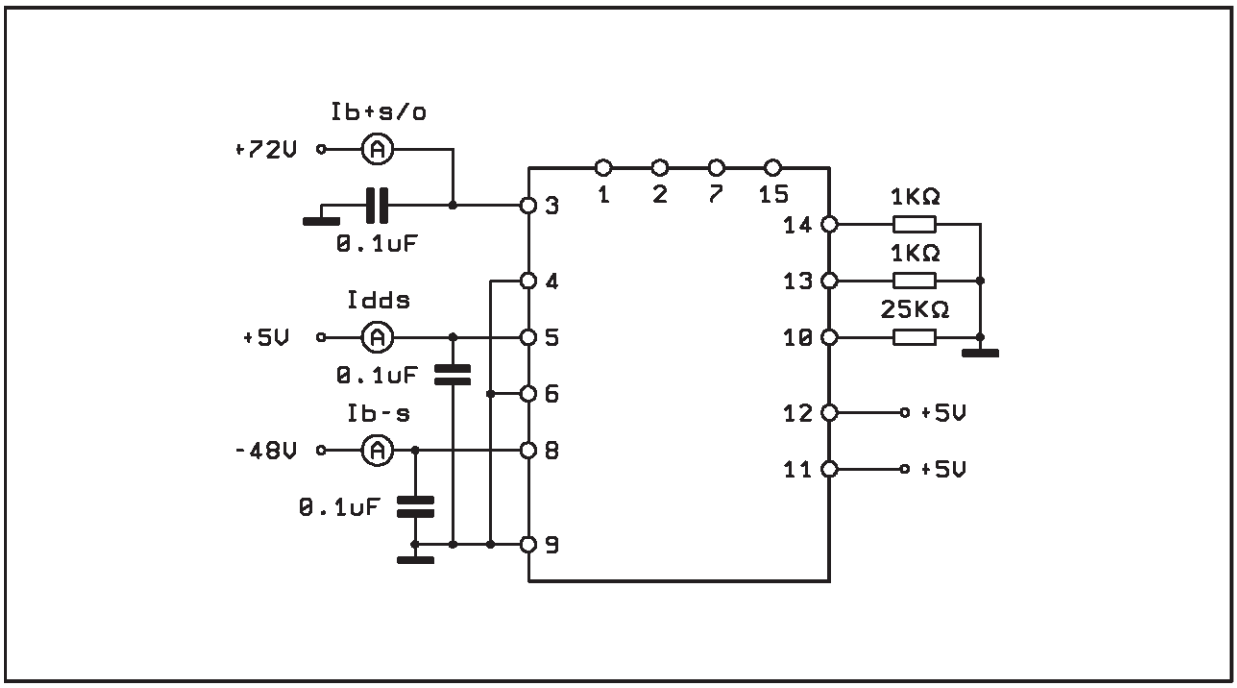


Figure 2: Conversation Supply Voltage

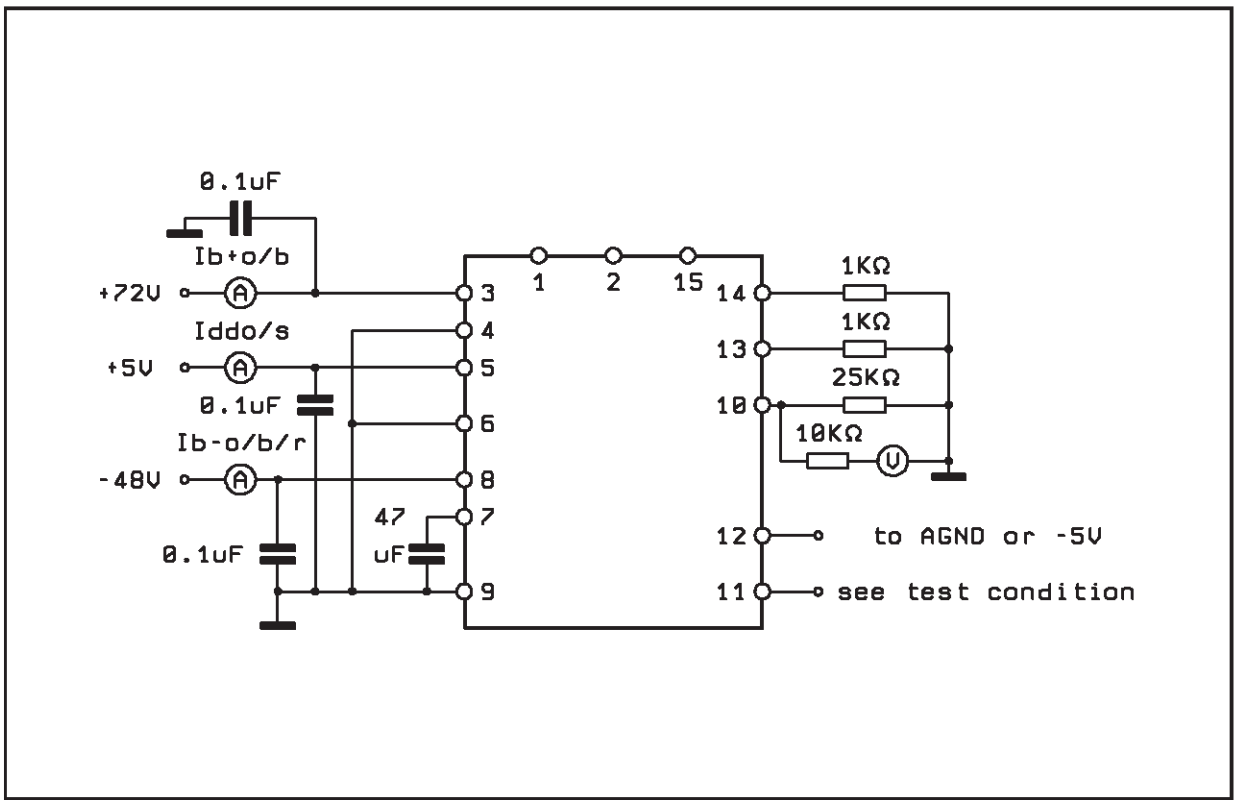


Figure 3: DC Transversal and Longitudinal Current

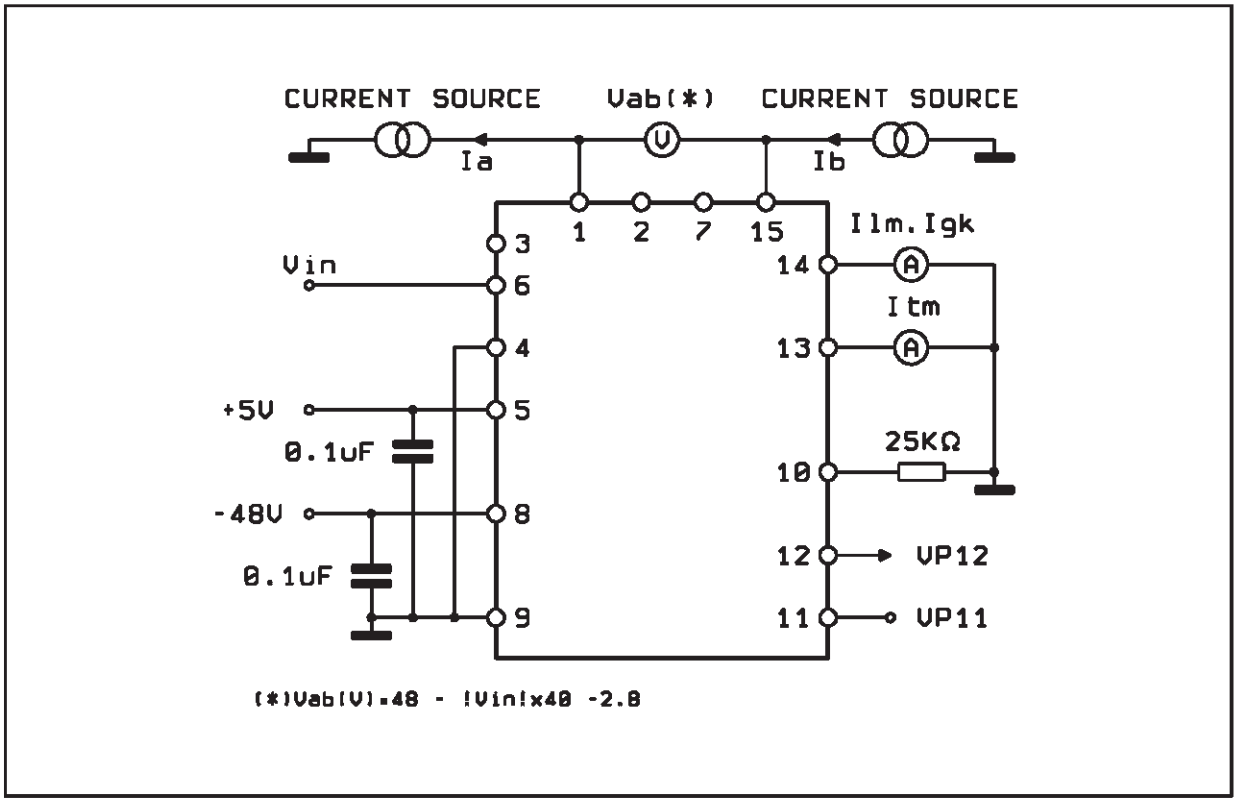


Figure 4: DC Voltage Between Pins 1 and 15 in Ringing Operation Mode

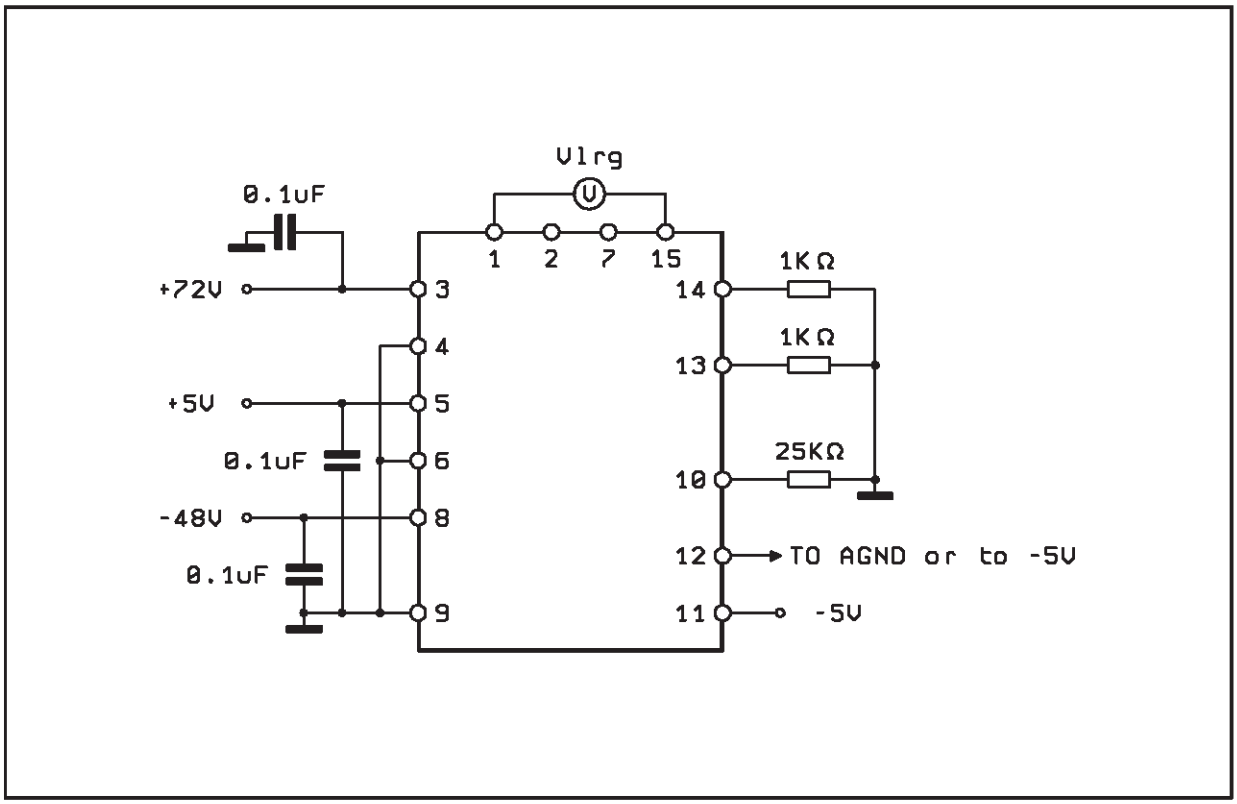
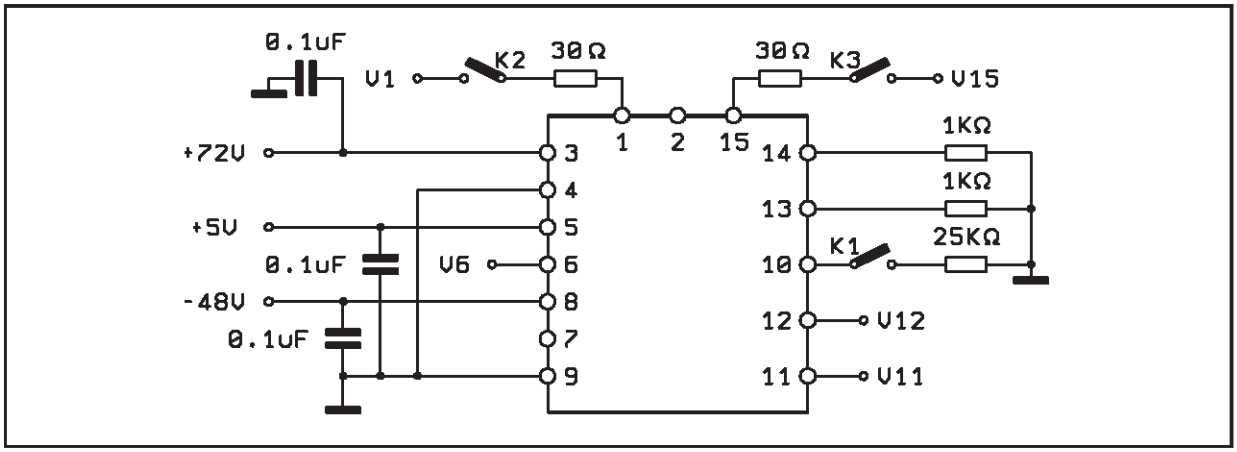


Figure 4A: Maximum Output Current at Pin 1 and 15



TEST	K1	K2	K3	V6	V1	V15	V11	V12
TIP to GND NBNP	OFF	ON	OFF	–0.3V	0V	–	5V	0V
TIP to GND POWER D.	OFF	ON	OFF	–0.3V	0V	–	5V	5V
TIP to GND LOOP OP.	ON	ON	OFF	–0.3V	–1V	–	5V	5V
A OPEN	OFF	ON	OFF	–0.3V	–1V	–	0V	5V
TIP to V_{B-} NBNP	OFF	ON	OFF	–0.3V	–48V	–	5V	0V
TIP to V_{B-} POWER D.	OFF	ON	OFF	–0.3V	–48V	–	5V	5V
TIP to V_{B-} LOOP OP.	ON	ON	OFF	–0.3V	–48V	–	5V	5V
A OPEN	OFF	ON	OFF	–0.3V	–48V	–	0V	5V

Example of test condition for I_{om} and I_{oma} on Pin 1. For Pin 15 must be changed K2 with K3 and V1 with V15. For B open V11 must be –5V instead of 0V.

Figure 5: Receving Gain

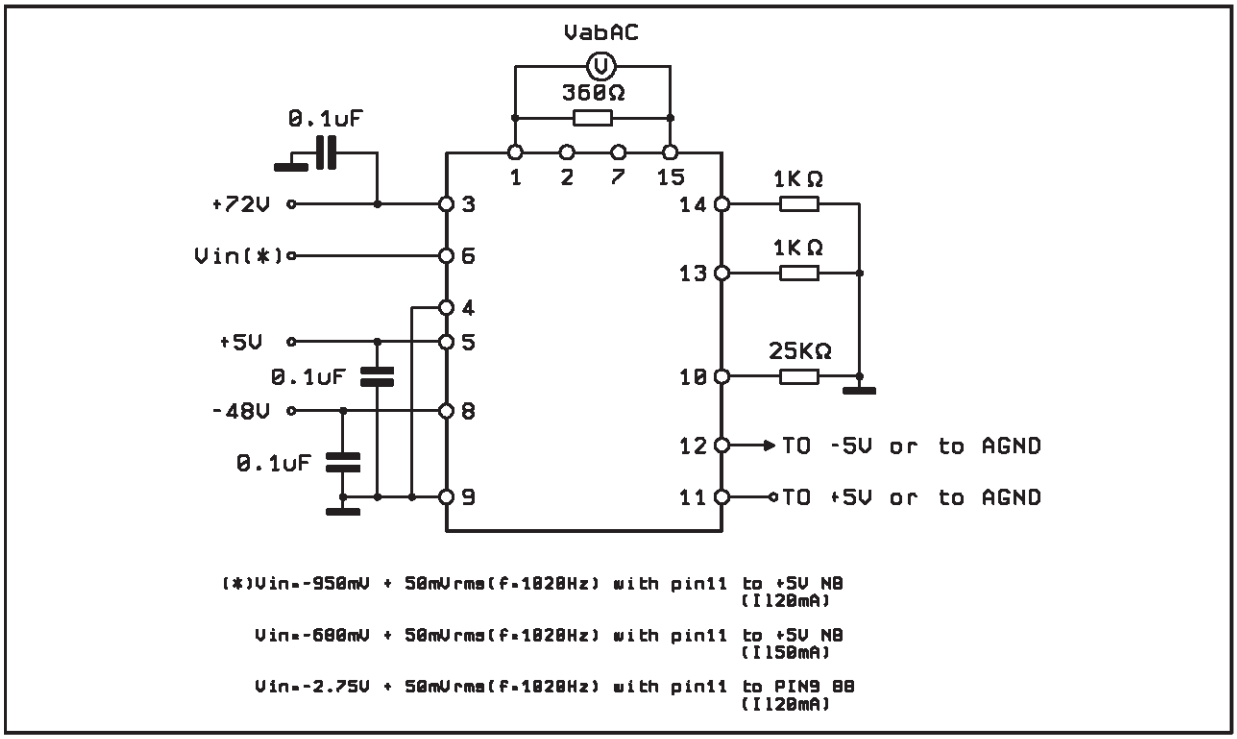


Figure 5A: THD and Tx Gain Flatness (and linearity)

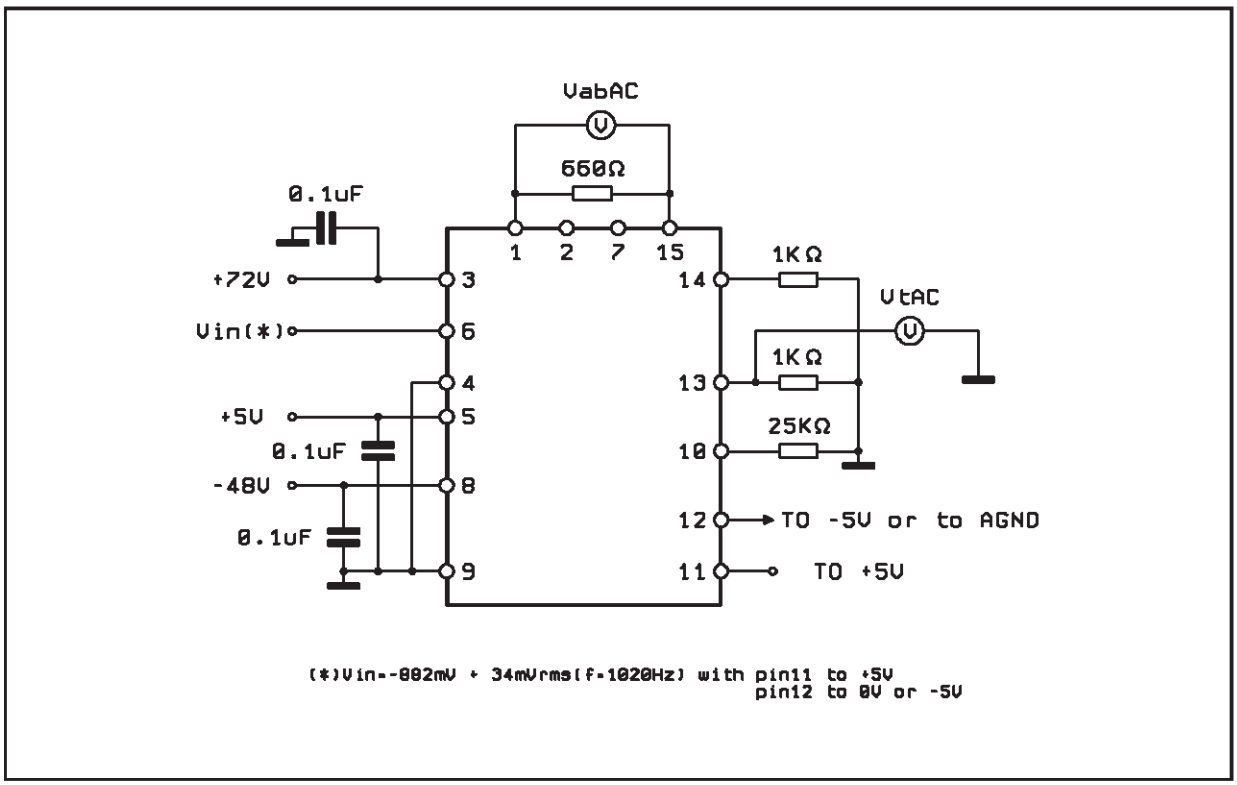


Figure 6: AC Transversal Current

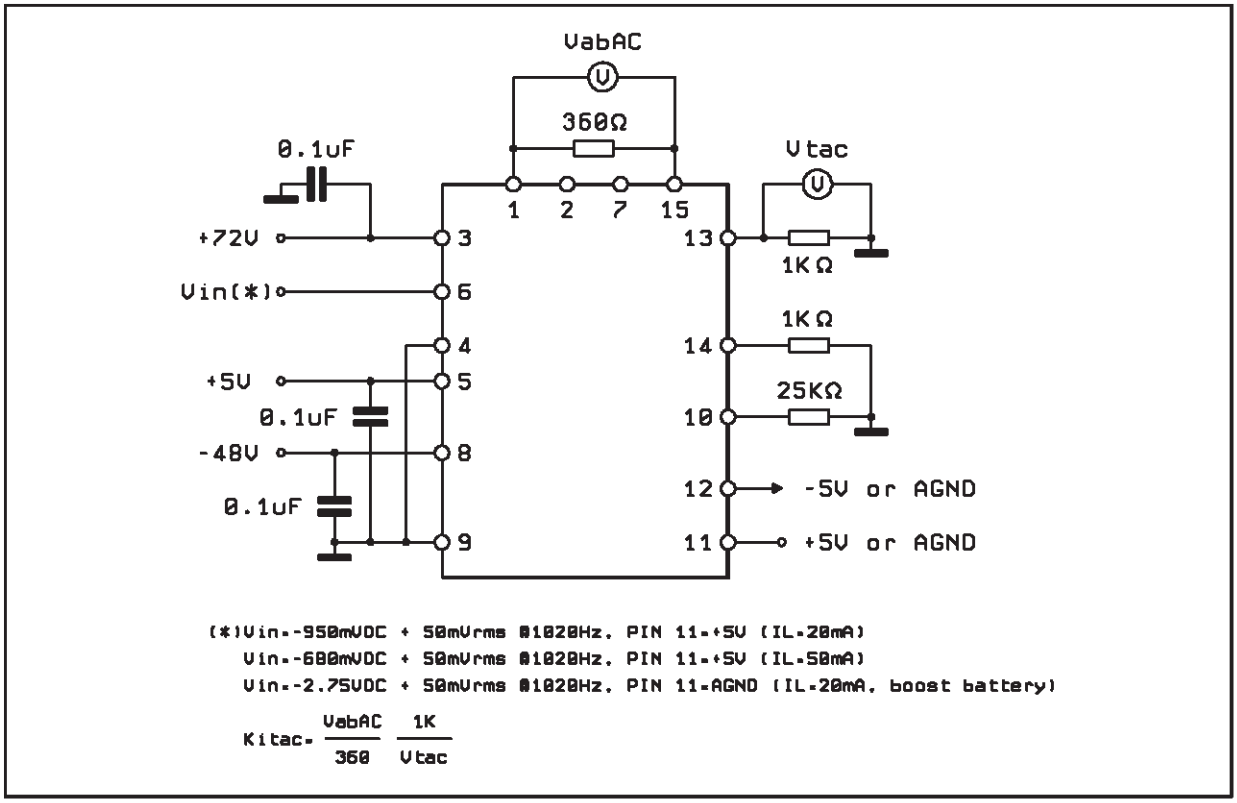


Figure 7: Common Mode Rejection Longitudinal to Transversal

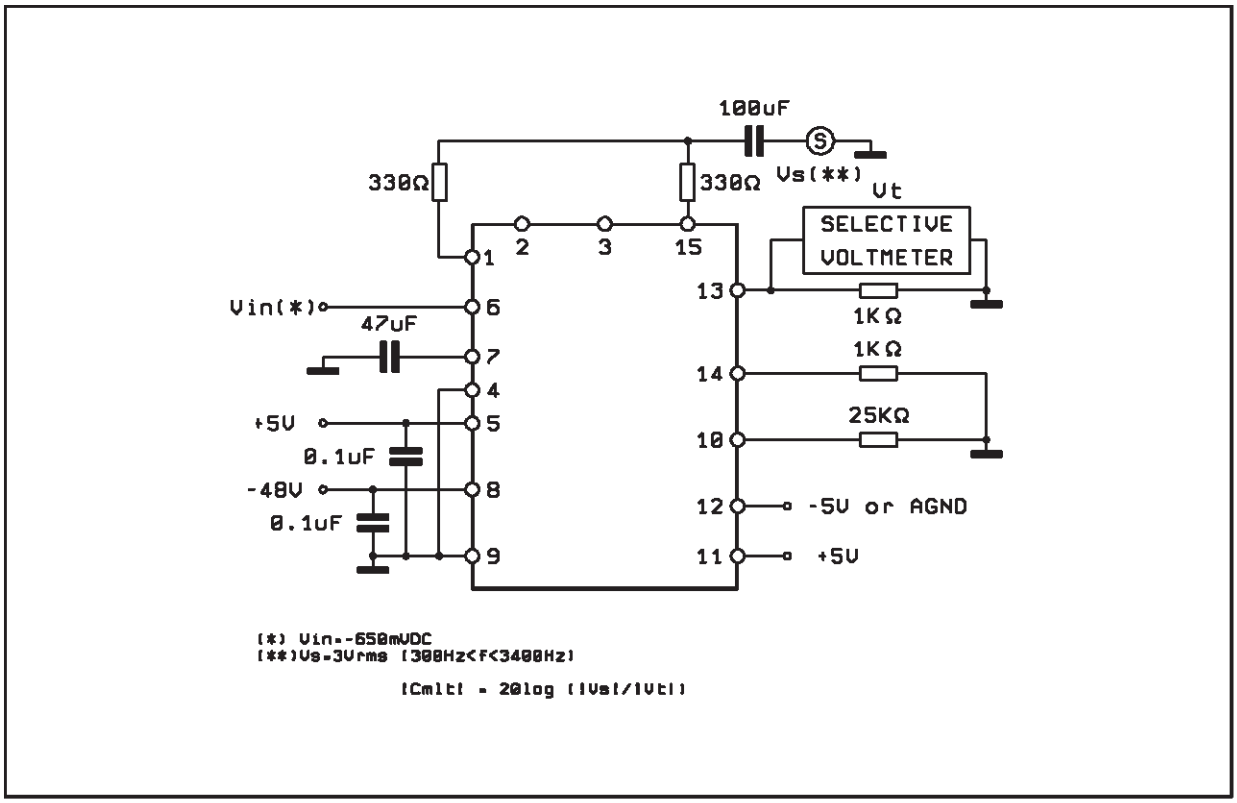


Figure 8: Common Mode Rejection Transversal to Longitudinal

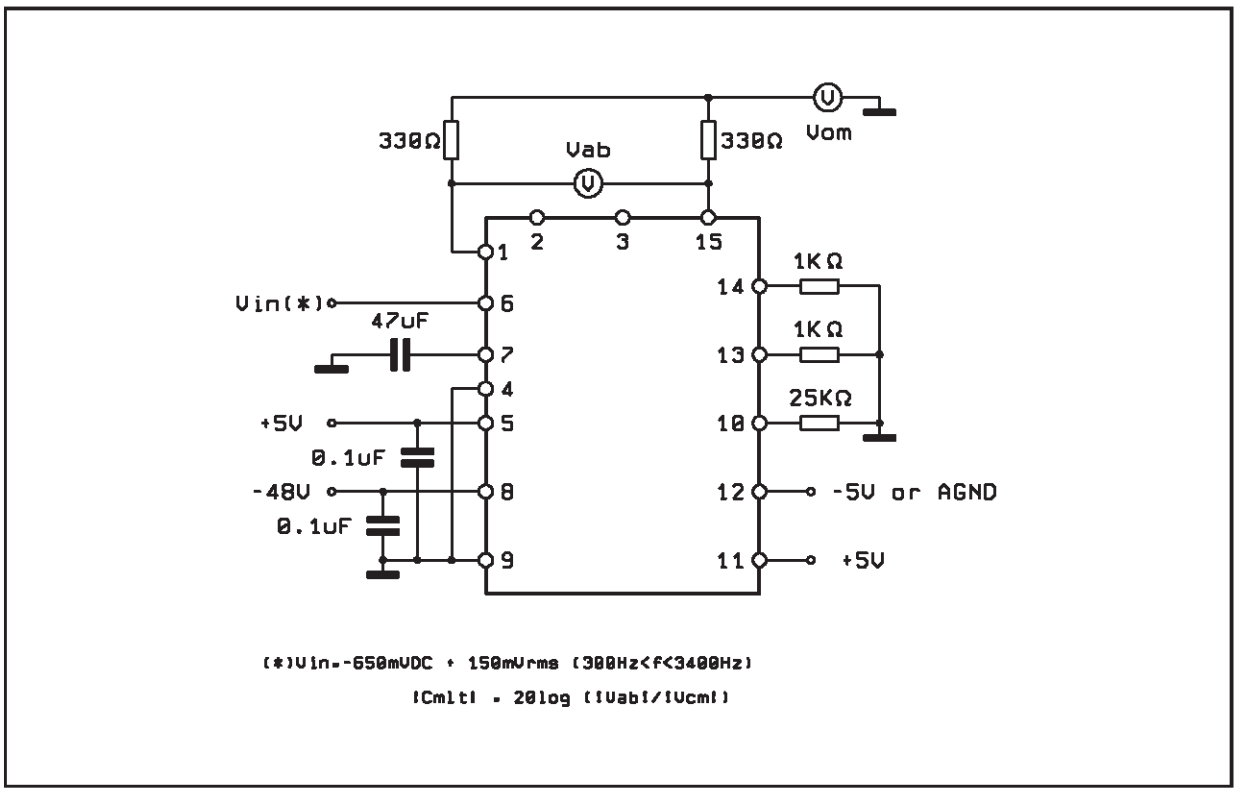


Figure 9: Supply Voltage Rejection Ratio

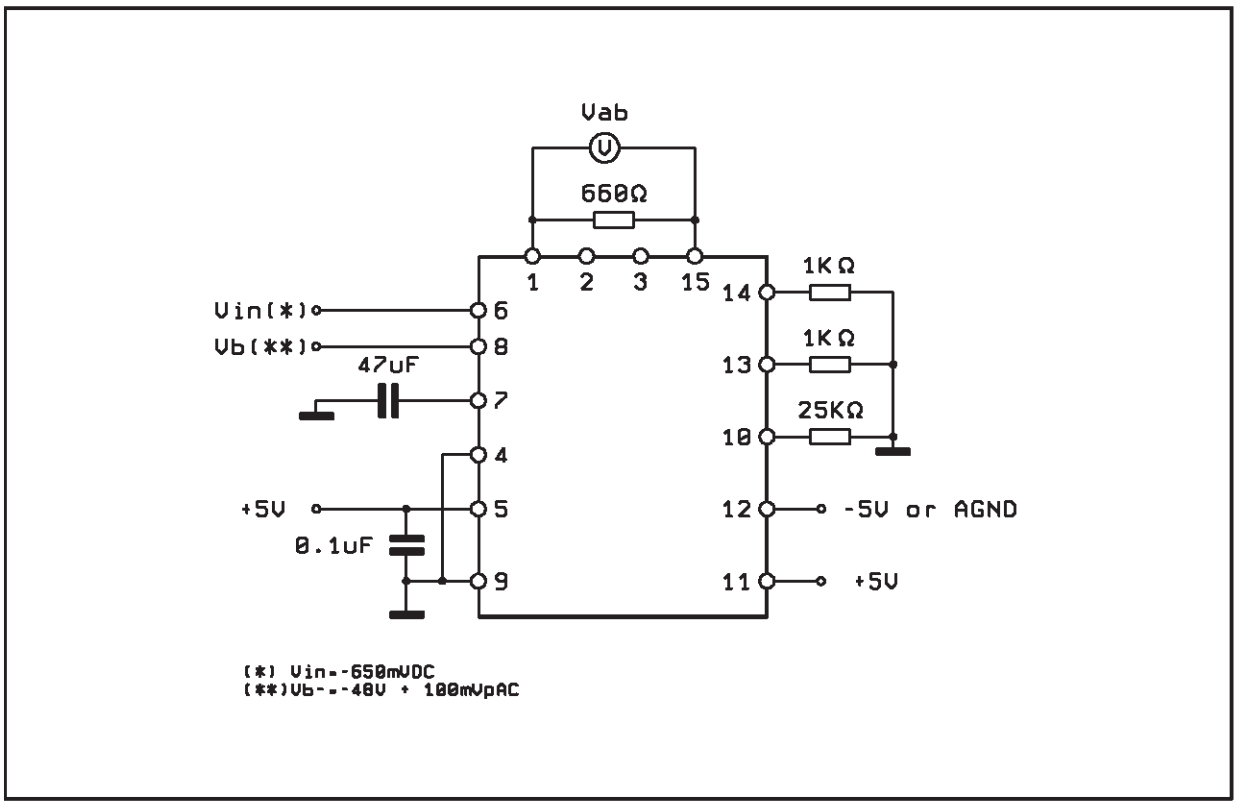


Figure 10: Supply Voltage Rejection Ratio

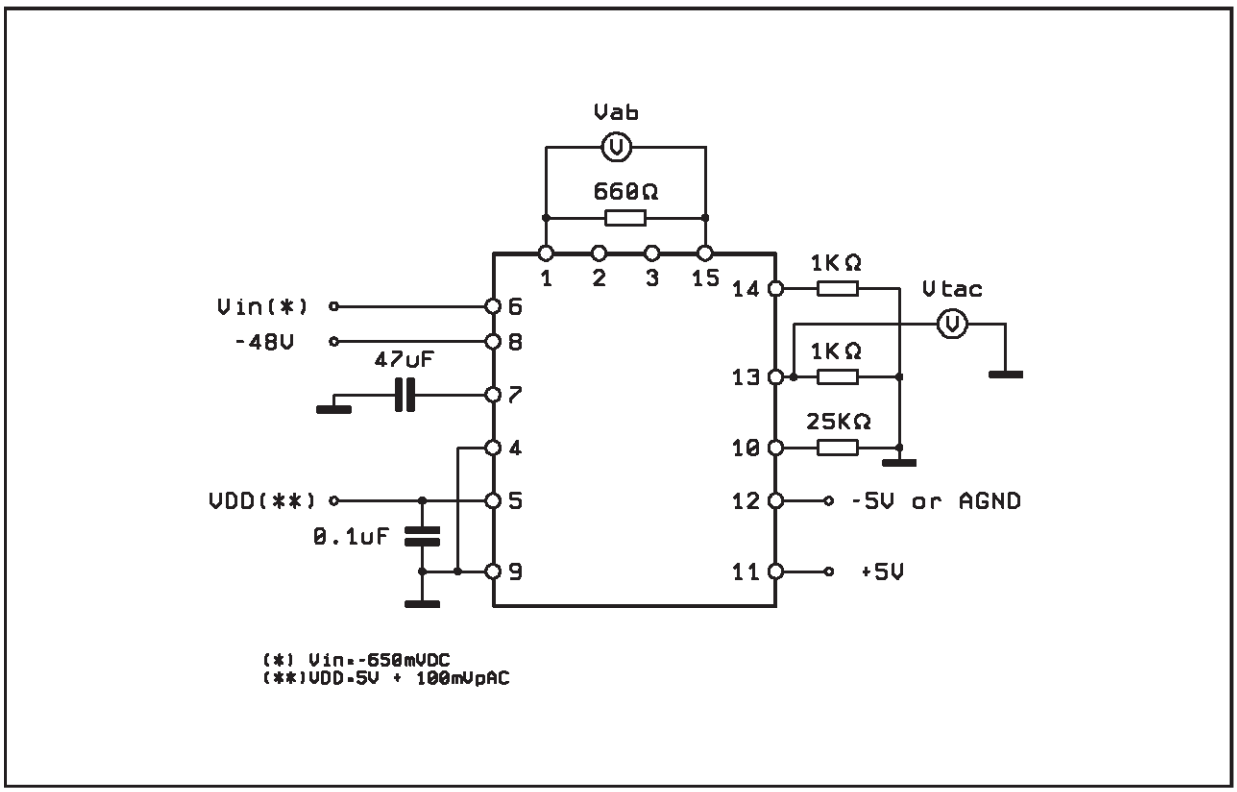


Figure 11: Output Ringing Voltage

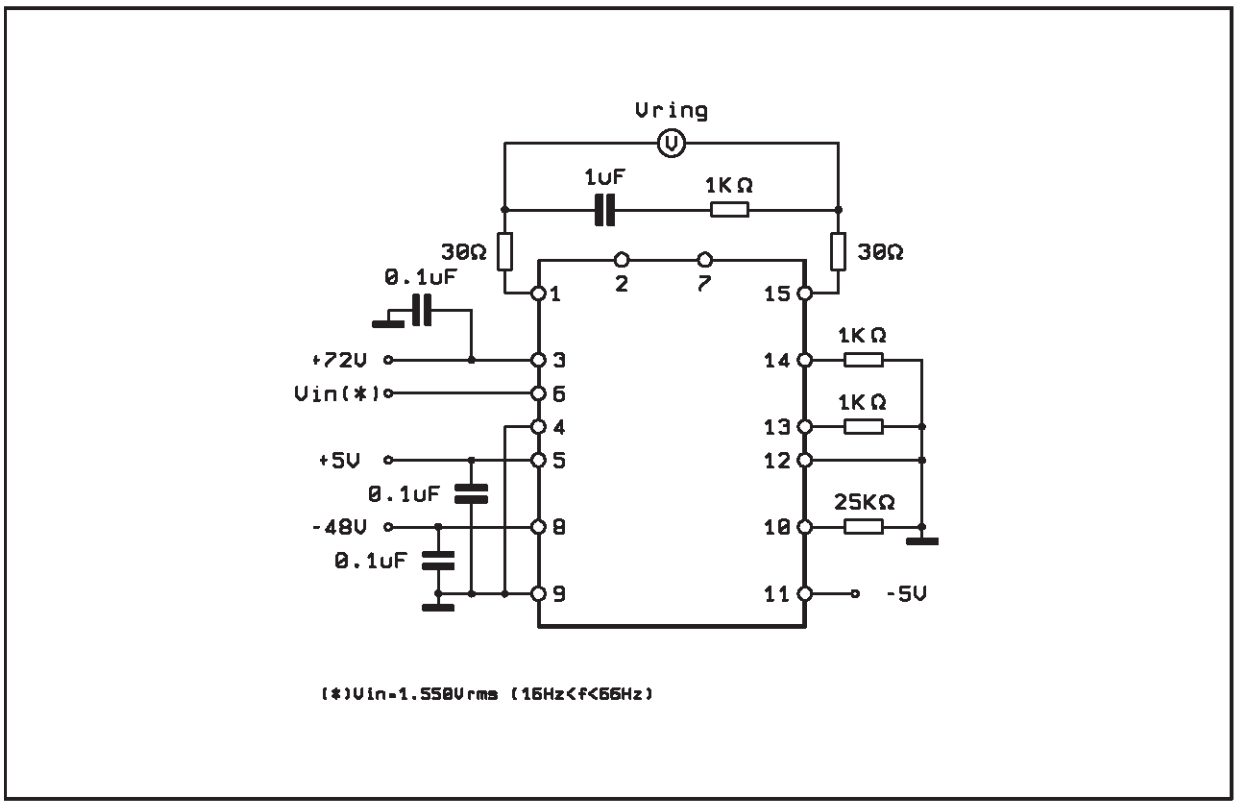


Figure 12: Psophometric Noise

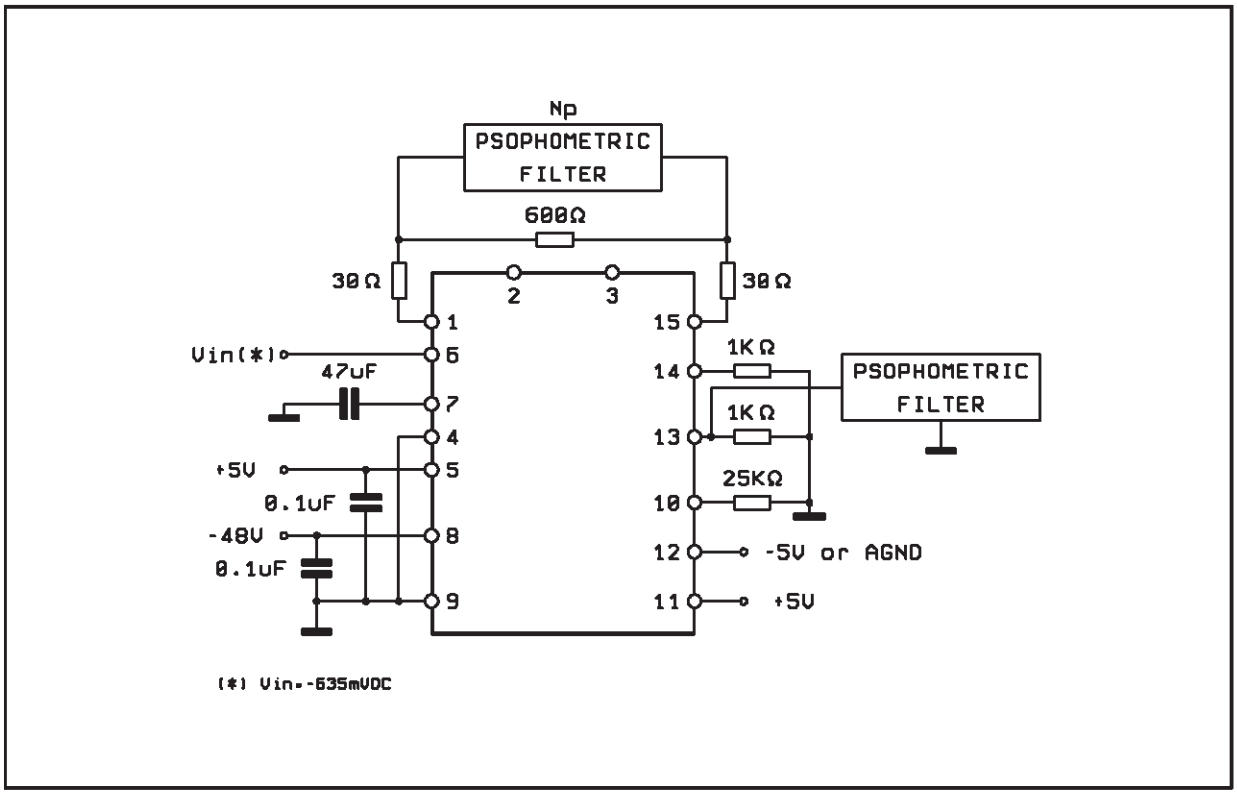
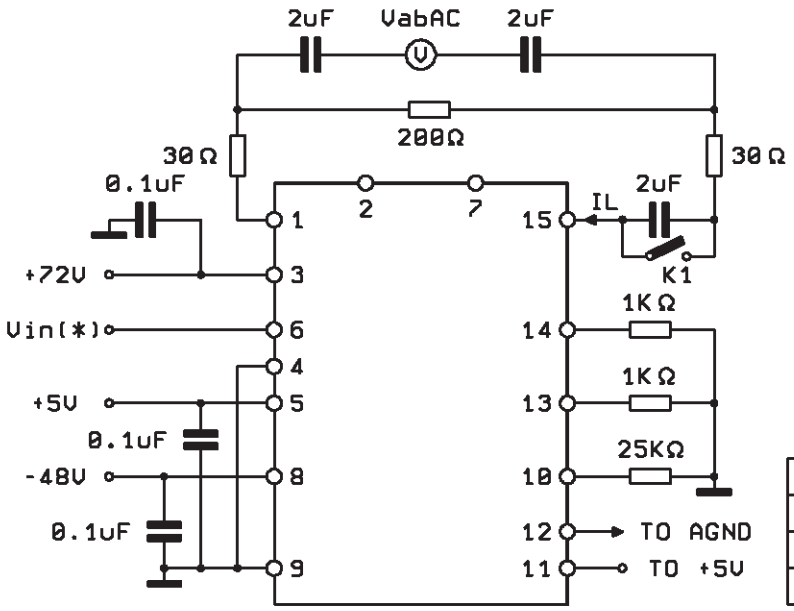


Figure 13: THD_{TTX} Metering

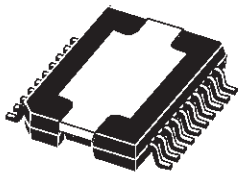


	M1	M2	M3
VIN=mV	-180	-800	-800
VAC=mVrms	50	50	125
K1 =	OFF	ON	ON

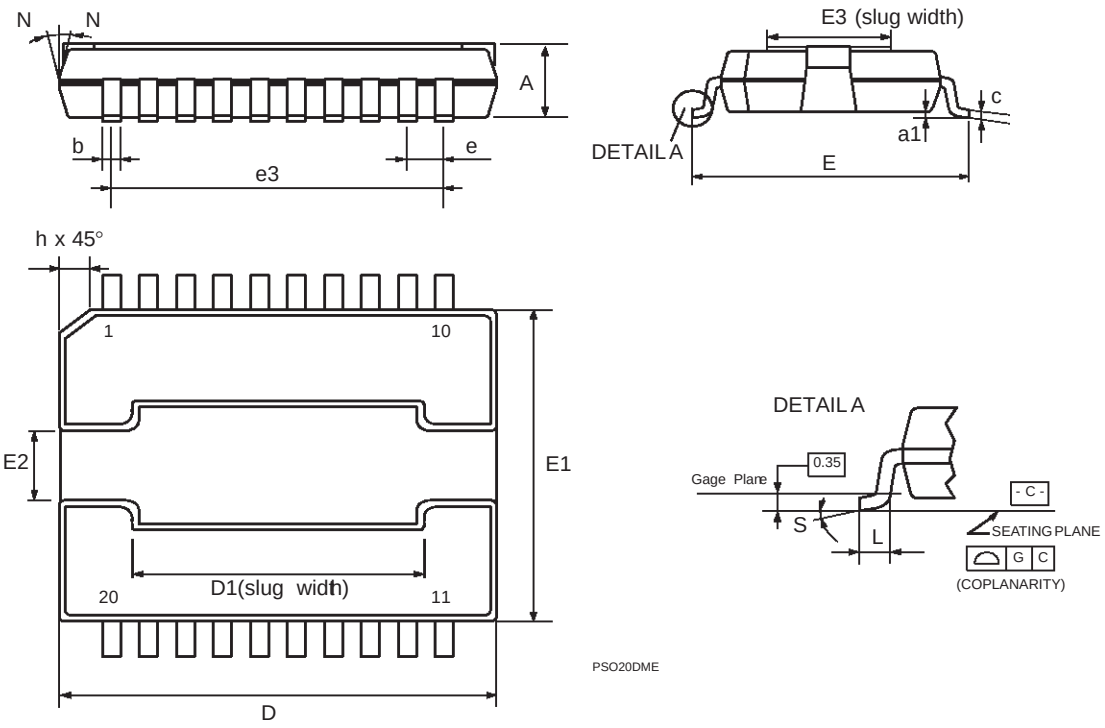
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.7			0.145
A2	3	3.15	3.3	0.118	0.124	0.130
a1	0.1		0.25	0.004		0.010
A4	0.8		1	0.031		0.039
A5	0.15	0.2	0.25	0.006	0.008	0.010
b	0.4		0.53	0.016		0.021
c	0.23		0.32	0.009		0.012
D (1)	15.8		16	0.622		0.630
D1	9.4		9.8	0.370		0.385
D2	0.9		1.1	0.035		0.043
E	13.9		14.5	0.547		0.570
e	1.12	1.27	1.42	0.044	0.050	0.056
e3		11.43			0.450	
E1 (1)	10.9		11.1	0.429		0.437
E2	2.7		2.9	0.106		0.114
E3	5.8		6.2	0.228		0.244
G	0		0.1	0.000		0.004
h			1.1			0.043
L	0.8		1.1	0.031		0.043
L1		1.6			0.063	
N	10° (max)					
R		0.6			0.024	
R1		0.5			0.020	
S	0° (min.)8° (max.)					
V	5° (min.)7° (max.)					

(1) "D and E1" do not include mold flash or protrusions.
- Mold flash or protrusions shall not exceed 0.15 mm (0.006").
- Critical dimensions: "E", "a1", "e", and "G"

OUTLINE AND MECHANICAL DATA



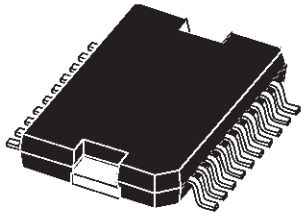
PowerSO-20 (Slug-up)



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.6			0.142
a1	0.1		0.3	0.004		0.012
a2			3.3			0.130
a3	0		0.1	0.000		0.004
b	0.4		0.53	0.016		0.021
c	0.23		0.32	0.009		0.013
D (1)	15.8		16	0.622		0.630
D1	9.4		9.8	0.370		0.386
E	13.9		14.5	0.547		0.570
e		1.27			0.050	
e3		11.43			0.450	
E1 (1)	10.9		11.1	0.429		0.437
E2			2.9			0.114
E3	5.8		6.2	0.228		0.244
G	0		0.1	0.000		0.004
H	15.5		15.9	0.610		0.626
h			1.1			0.043
L	0.8		1.1	0.031		0.043
N	10° (max.)					
S	8° (max.)					
T		10			0.394	

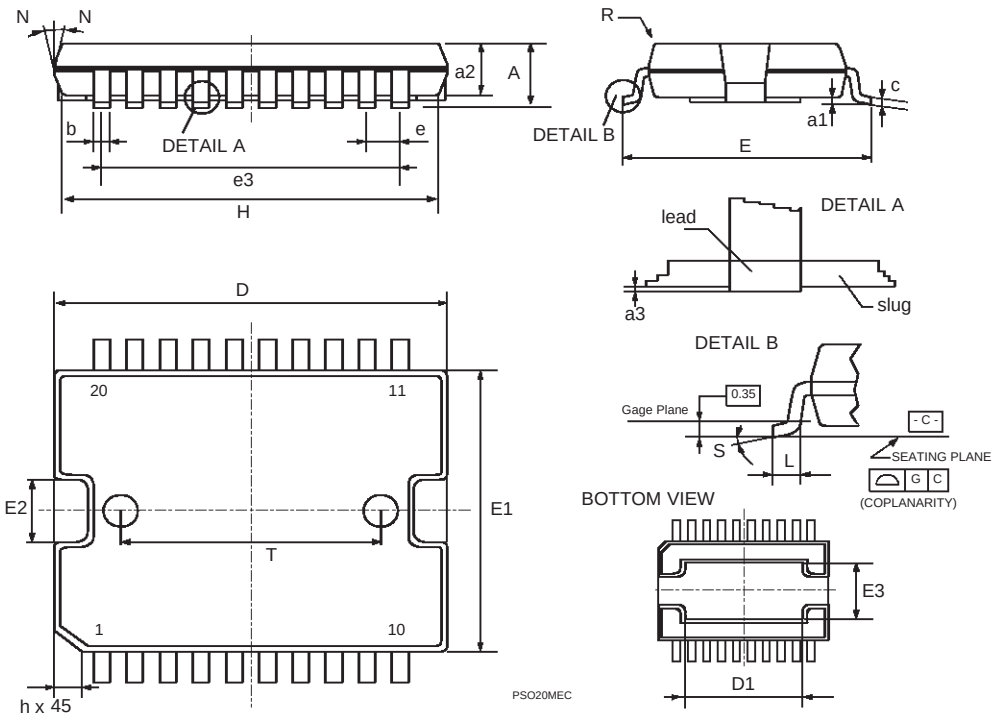
(1) "D and F" do not include mold flash or protrusions.
- Mold flash or protrusions shall not exceed 0.15 mm (0.006").
- Critical dimensions: "E", "G" and "a3"

OUTLINE AND MECHANICAL DATA



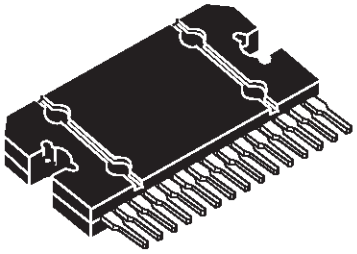
JEDEC MO-166

PowerSO20
(Slug-down)

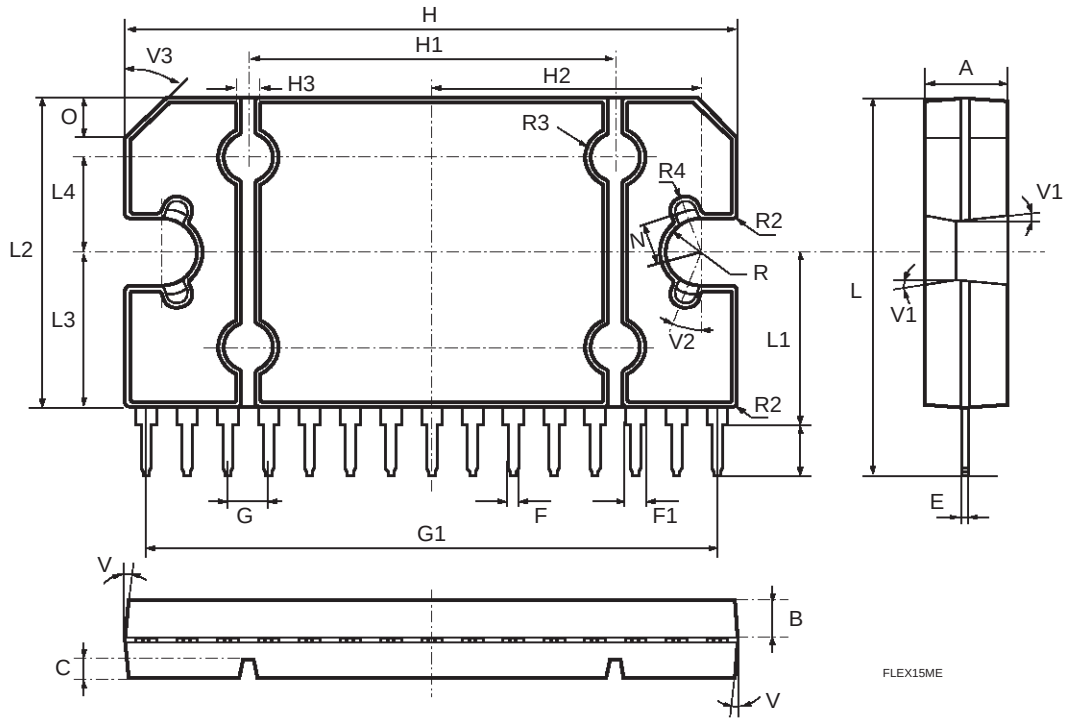


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.45	4.5	4.65	0.175	0.177	0.183
B	1.8	1.9	2	0.071	0.075	0.079
C		1.4			0.055	
E	0.37	0.39	0.42	0.014	0.015	0.016
F			0.57			0.022
F1			0.97			0.038
G	1.7	1.9	2.1	0.067	0.075	0.083
G1	26.35	26.6	26.85	1.037	1.048	1.057
H	28.9	29.23	29.3	1.138	1.151	1.153
H1		17			0.670	
H2		12.8			0.504	
H3		0.8			0.031	
L	19.25	19.65	20.05	0.758	0.774	0.789
L1	8.7	9.1	9.5	0.342	0.358	
L2	15.5	15.7	15.9	0.610	0.618	0.626
L3	7.7	7.85	7.95	0.303	0.309	0.313
L4		5			0.197	
L5		2.7			0.106	
N		2.2			0.096	
O		2			0.078	
R		1.7			0.067	
R2		0.3			0.012	
R3		1.25			0.049	
R4		0.5			0.02	
V	5° (Typ.)					
V1	3° (Typ.)					
V2	20° (Typ.)					
V3	45° (Typ.)					

OUTLINE AND MECHANICAL DATA



Flexiwatt15



ESD - The STMicroelectronics Internal Quality Standards set a target of 2 KV that each pin of the device should withstand in a series of tests based on the Human Body Model (MIL-STD 883 Method 3015): with C = 100pF; R = 1500Ω and performing 3 pulses for each pin versus V_{CC} and GND.

Device characterization showed that, in front of the STMicrolectronics Internaly Quality Standards, all pins of L3000S withstand at least 1kV.

The above points are not expected to represent a pratical limit for the correct device utilization nor for its reliability in the field. Nevertheless they must be mentioned in connection with the applicability of the different SURE 6 requirements to L3000S.