L 65756

32 K × 8 High Speed CMOS SRAM 3.3 Volt

Description

The L 65756 is a high speed CMOS static RAM organised as 32,768 × 8 bits. It is manufactured using MHS's high performance CMOS technology.

The L 65756 provides fast access time of 25 ns for a 3 volts power supply.

The L 65756 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 80 % when the circuit is deselected.

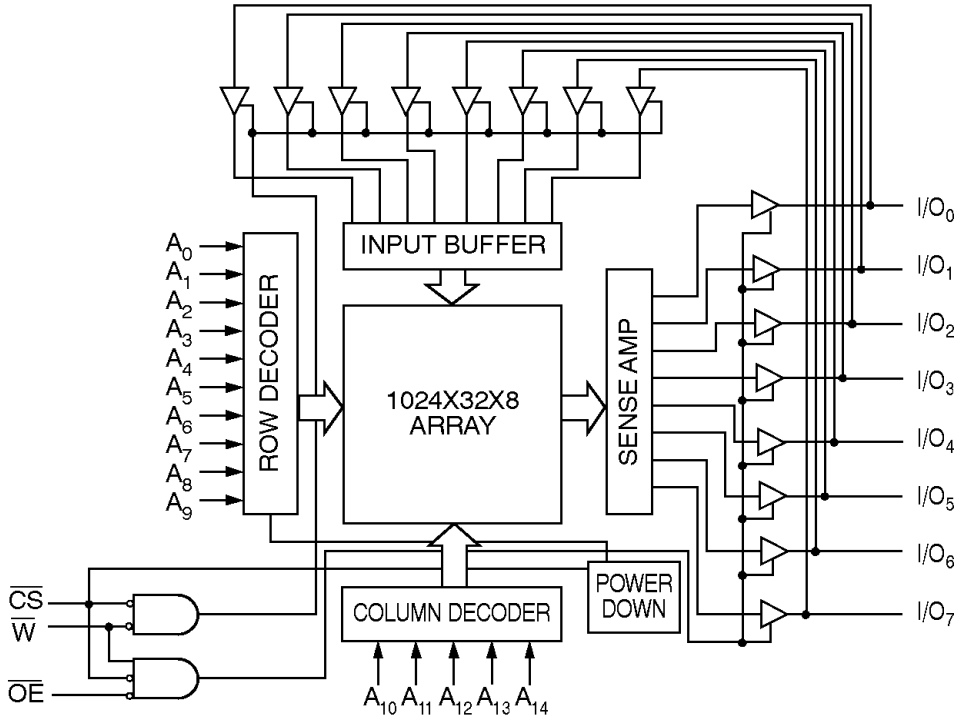
Easy memory expansion is provided by an active low chip select ($\overline{CS}$) an active low output enable ($\overline{OE}$), and three state drivers.

Features

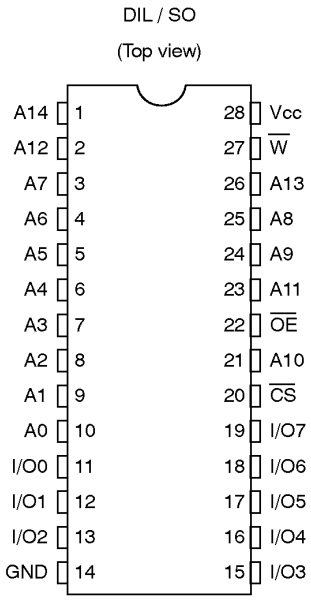
- Single supply 3.3 ± 0.3 Volts
- Fast access time
- Commercial : 25/35/45/55 ns (max)
- Low power consumption
  Active : 290 mW
  Standby : 72 mW
- Asynchronous

Interface

Block Diagram



Pin Configuration



Pin Description

A0–A14	: Address inputs	$\overline{CS}$	: Chip-select
I/00–I/07	: Inputs/Outputs	$\overline{OE}$	: Output enable
VCC	: Power	$\overline{W}$	: Write Enable
GND	: Ground		

Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{W}$	INPUT/OUTPUT	MODE
H	X	X	Z	Deselect/ Power down
L	L	H	Output	Read
L	X	L	Input	Write
L	H	H	Z	Output Disable

L = low, H = high, X = H or L, Z = High impedance.

Electrical Characteristics

Absolute Maximum Ratings

Supply voltage to GND potential . . . . . –0.5 V to + 7.0 V
DC input voltage . . . . . –3.0 V to + 7.0 V
DC output voltage in high Z state . . . . . –0.5 V to + 7.0 V

Storage temperature . . . . . –65 °C to + 150 °C
Output current into outputs (low) . . . . . 20 mA
Electro static discharge voltage . . . . . 4 000 V
(MIL STD 883C method 3015.5)

Operating Range

	OPERATING VOLTAGE	OPERATING TEMPERATURE
Commercial	3.3 V ± 0.3 V	0 °C to + 70 °C

DC Operating Conditions

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
V_{CC}	Supply voltage	3.0	3.3	3.6	V
Gnd	Ground	0.0	0.0	0.0	V
VIL	Input low voltage	– 0.3	0.0	0.7	V
VIH	Input high voltage	1.5	–	VCC	V

DC Parameter

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX	(2)	Input leakage current	– 10.0	–	10.0	µA
IOZ	(2)	Output leakage current	– 10.0	–	10.0	µA
IOS	(3)	Output short circuit current	–	–	– 300.0	mA
VOL	(4)	Output low voltage	–	–	0.4	V
VOH	(5)	Output high voltage	1.8	–	–	V

Notes :
2. Gnd < Vin < Vcc, Gnd < Vout < V_{CC} Output disabled.
3. V_{CC} = max, V_{out} = Gnd, duration of the short circuit should not exceed 30 seconds. Not more than 1 output should be shorted at one time.
4. V_{CC} min, IOL = 4.0 mA
5. V_{CC} min, IOH = -250 µA.

Consumption

SYMBOL		PARAMETER	L 65756 – 25	L 65756 – 35	L 65756 – 45	L 65756 – 55	UNIT	VALUE
ICCSB	(6)	Standby supply current	20	20	20	20	mA	max
ICCSB1	(7)	Standby supply current	15	15	15	15	mA	max
ICCOP	(8)	Dynamic operating current	80	80	80	80	mA	max

Notes :
6. $\overline{CS} \geq$ VIH, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, a pull-up resistor to V_{CC} on the $\overline{CS}$ is required to keep the device unselected during the V_{CC} power-up. Otherwise ICCSB will exceed the above value. Min duty cycle = 100 %.
7. $\overline{CS} \geq V_{CC} - 0.3$ V, $V_{IN} \geq V_{CC} - 0.3$ V or $V_{IN} \leq 0.3$ V.
8. V_{CC} max, Output current = 0 mA, f = max, Vin = V_{CC} or Gnd.

Capacitance

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin	(1)	Input capacitance	–	–	5	pF
Cout	(1)	Output capacitance	–	–	7	pF

Note : 1. TA = 25°C, f = 1 MHz, Vcc = 5.0 V, these parameters are not tested.

AC Parameters

AC Conditions

Input pulse levels . . . . . Gnd to 3.0 V
Input rise . . . . . ≤ 5 ns
Input timing reference levels . . . . . 1.5 V
Output loading IOL/IOH (see figure 1a) . . . . . + 30 pF

AC Test Loads and Waveforms

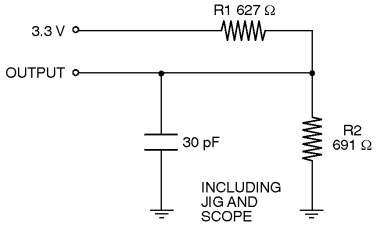


Figure 1a

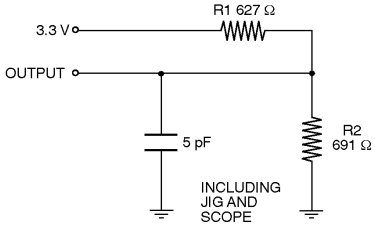


Figure 1b

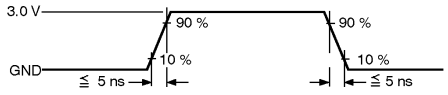
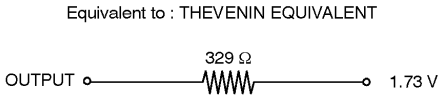


Figure 2

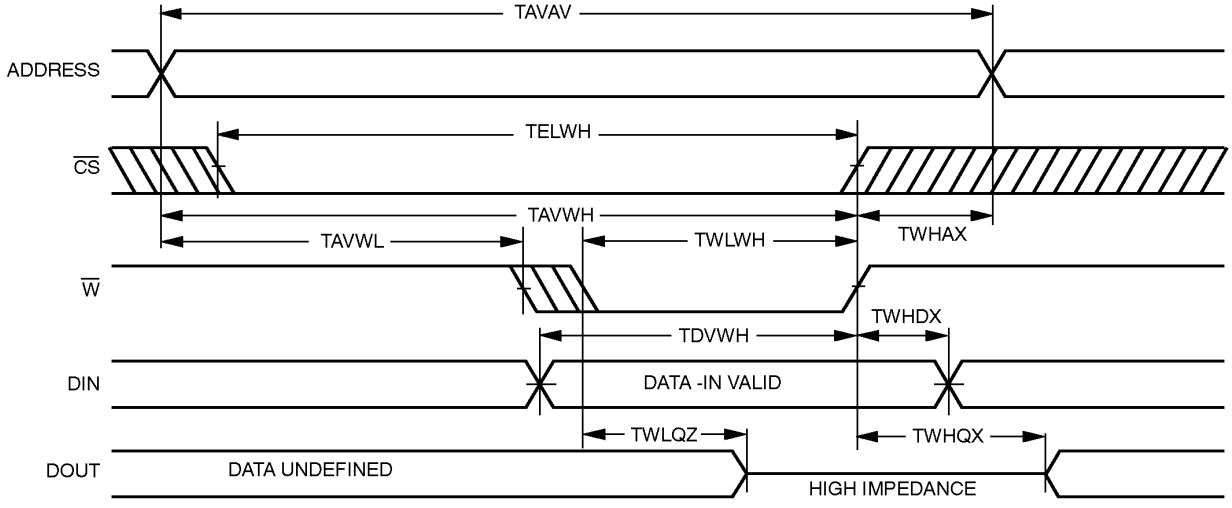


Write Cycle Specification (note 9)

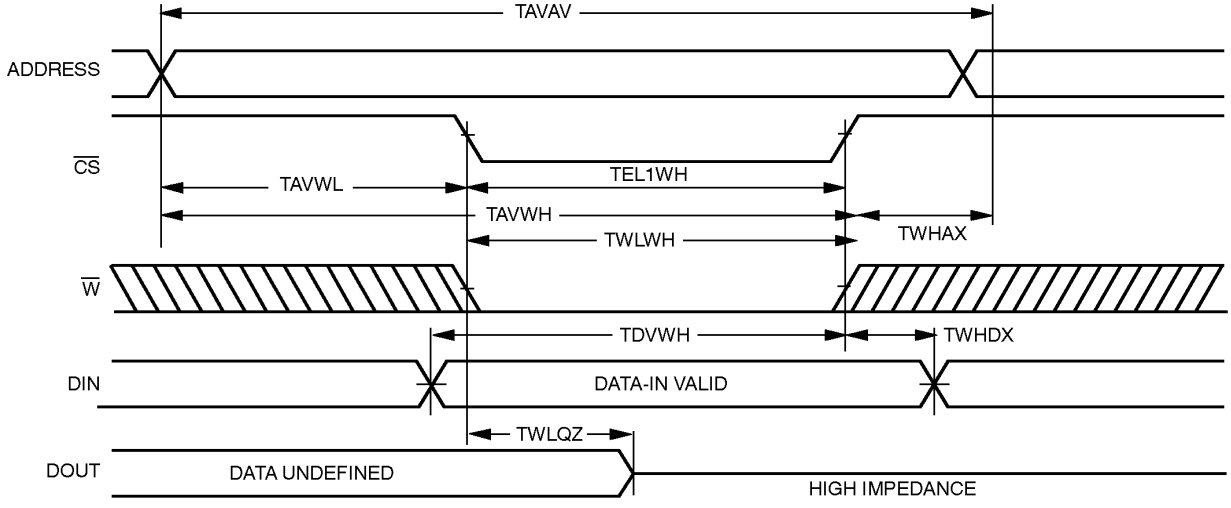
SYMBOL	PARAMETER	L 65756 – 25	L 65756 – 35	L 65756 – 45	L 65756 – 55	UNIT	VALUE
TAVAV	Write cycle time	25	35	45	50	ns	min
TAVWL	Address set-up time	0	0	0	0	ns	min
TAVWH	Address Valid to write end	20	30	40	50	ns	min
TDVWH	Data set-up time	15	17	20	25	ns	min
TELWH	$\overline{CS}$ low to write end	20	30	40	50	ns	min
TWLQZ (8)	Write low to high Z	13	15	20	25	ns	max
TWLWH	Write pulse width	20	25	30	40	ns	min
TWHAX	Address hold from write end	0	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	0	ns	min
TWHQX (8)	Write high to low Z	3	3	3	3	ns	min

Note : 8. Specified with CL = 5 pF (see figure 1b).

Write Cycle 1 : $\overline{W}$ Controlled (note 9)



Write Cycle 2 : $\overline{CS}$ controlled (note 9)



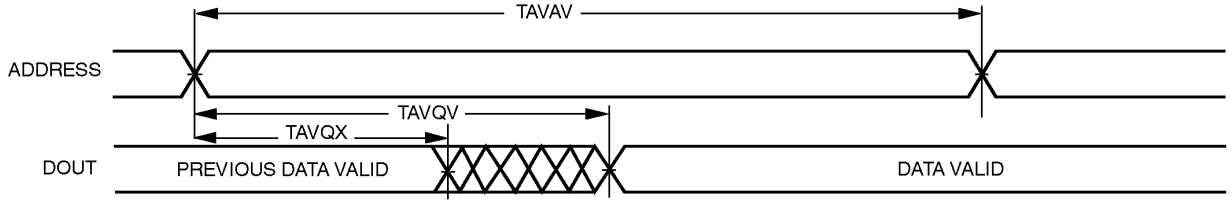
Note : 9. The internal write of the memory is defined ty the overlap of $\overline{CS}$ LOW and $\overline{W}$ LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to rising edge of the signal that terminates the write.
Data out will be high impedance if $\overline{OE}$ = VIH.

Read Cycle Specification

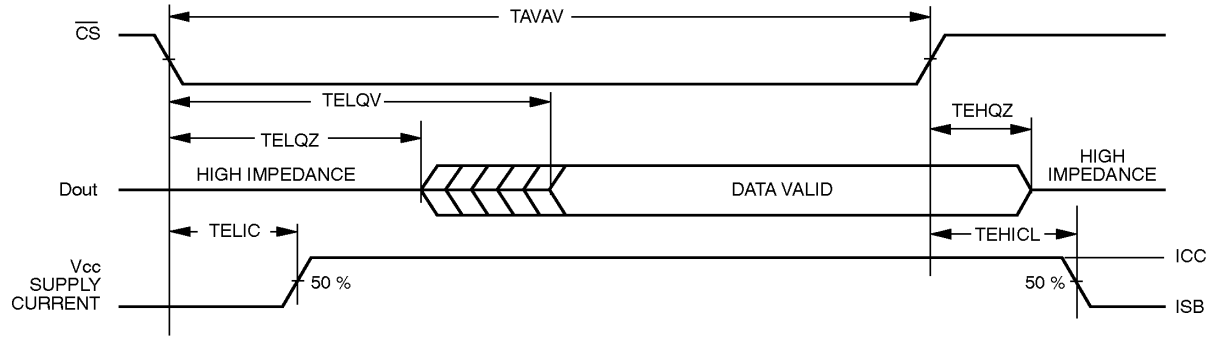
SYMBOL	PARAMETER	L 65756 – 25	L 65756 – 35	L 65756 – 45	L 65756 – 55	UNIT	VALUE
TAVAV	Read cycle time	25	35	45	55	ns	min
TAVQV	Address access time	25	35	45	55	ns	max
TAVQX (10)	Address valid to low Z	3	3	3	3	ns	min
TELQV	Chip-select access time	25	35	45	55	ns	max
TELQX (10)	$\overline{CS}$ low to low Z	3	3	3	3	ns	min
TEHQZ (10)	$\overline{CS}$ high to high Z	13	15	20	20	ns	max
TELIC	$\overline{CS}$ low to power up	0	0	0	0	ns	min
TEHICL	$\overline{CS}$ high to power down	20	20	25	25	ns	max
TGLQV	Output Enable access time	15	20	20	20	ns	max
TGLQX (10)	$\overline{OE}$ low to low Z	3	3	3	3	ns	min
TGHQZ (10)	$\overline{OE}$ high to high Z	13	15	20	25	ns	max

Note : 10. Specified with CL = 5 pF (see figure 1b).

Read Cycle 1 (note 11, 12, 13)



Read Cycle 2 (note 11, 13)



Notes : 11. $\overline{W}$ is high for read cycle.
12. Device is continuously selected, $\overline{CS}$ = VIL, $\overline{OE}$ = VIL.
13. Address valid prior or coincident with $\overline{CS}$ transition low.

Ordering Information