Ordering number: EN 1595B

Monolithic Linear IC

SANYO No.1595B

LA5655

VOLTAGE REGULATOR FOR FLT DISPLAY DESK-TOP CALCULATOR

The LA5655 is an IC containing all the voltage regulators required for an FLT display desk-top calculator with a printer.

Features and Functions

a. On-chip voltage regulators required for desk-top calculator (FLT display) with a printer.
   1. Printer voltage regulator.
   2. LSI voltage regulator.
   3. FLT anode, grid voltage regulator.
   4. FLT heater grid voltage regulator.
   5. FLT bias grid voltage regulator.

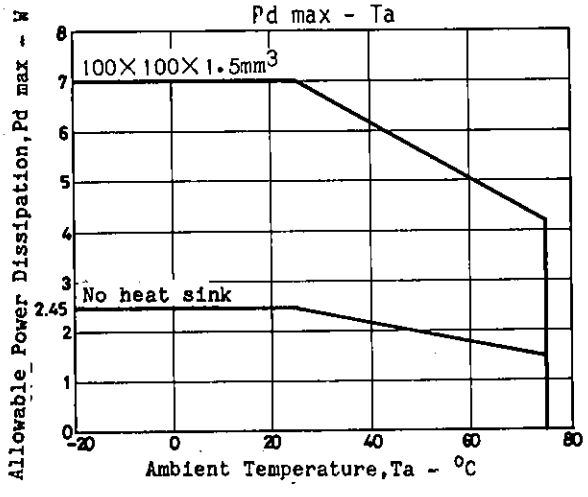
b. On-chip printer motor brake circuit

Maximum Ratings at Ta=25°C

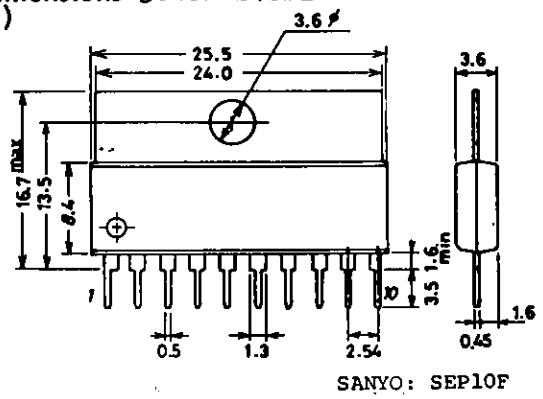
				unit
Voltage Regulator Input Voltage 1	V_{IN1}		50	V
Voltage Regulator Input Voltage 2	V_{IN2}		25	V
Output Current 1	I_{OUT1}		40	mA
Output Current 2	I_{OUT2}		2.0	A
Output Current 3	I_{OUTX}	(X=3,4,5) other regulator	40	mA
Allowable Power Dissipation	Pdmax	IC alone	2.45	W
Operating Temperature	Topr		-20 to +75	°C
Storage Temperature	Tstg		-40 to +125	°C

Operating Conditions at Ta=25°C

			unit
Voltage Regulator Input Voltage Range	V_{IN1}	+20 to +50	V
MT Pin H Voltage	V_{ENAH}	2.0 to 7.0	V
MT Pin L Voltage	V_{ENAL}	-0.3 to +0.3	V



Package Dimensions 3046A-S10FIC
(unit: mm)



SANYO: SEP10F

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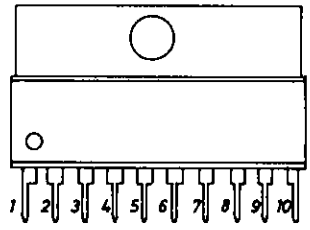
Operating Characteristics at Ta=25°C V_{IN1}=35V, V_{IN2}=10V, I_{OUT2}=200mA

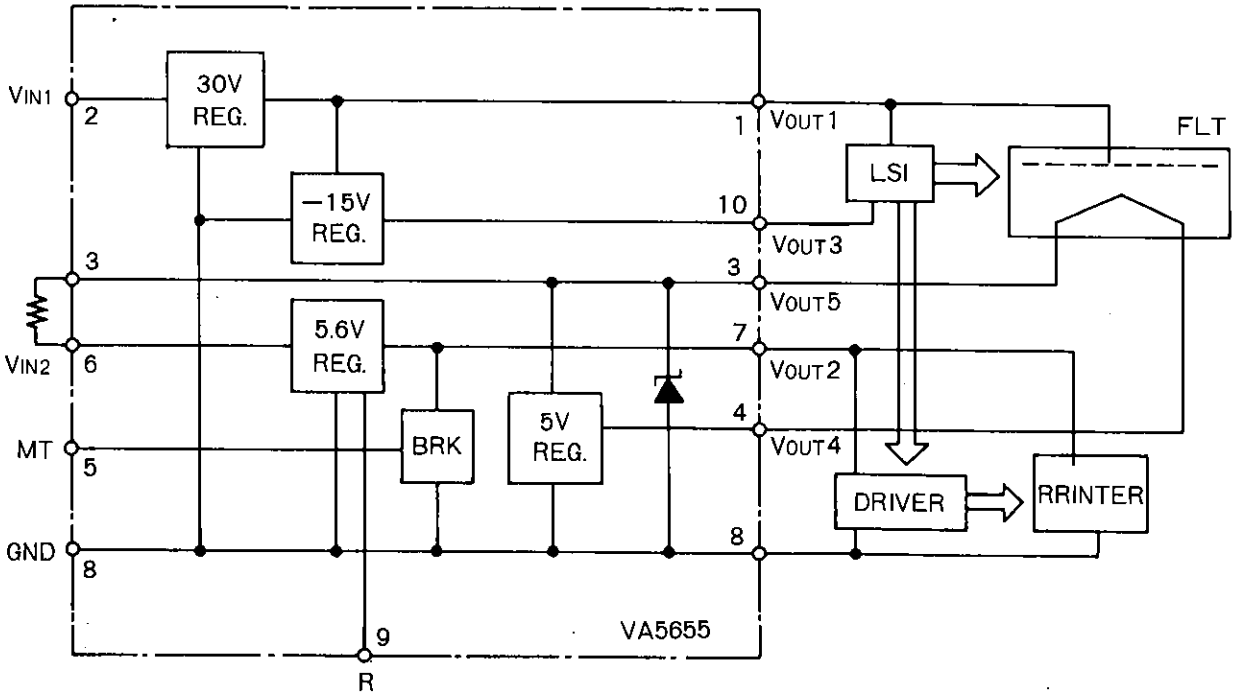
			min	typ	max	unit
Output Voltage 1	V_{OUT1}	①→⑧ I_{OUT1}=30mA	28.5	30	32.5	V
Output Votlage 2	V_{OUT2}	⑦→⑧	5.3	5.6	6.0	V
Output Voltage 3	V_{OUT3}	①→⑩ I_{OUT3}=-12mA	13.8	15	16.2	V
Output Votlage 4	V_{OUT4}	③→④ I_{OUT4}=-30mA	4.6	5	5.4	V
Output Votlage 5	V_{OUT5}	③→⑧ I_{IN5}=30mA	7.3	8	8.7	V
Load Regulation 1	ΔV_{01LOAD}	10mA<I_{OUT1}<30mA			250	mA
Load Regulation 2	ΔV_{02LOAD}	100mA<I_{OUT2}<2A			250	mA
Load Regulation 3	ΔV_{03LOAD}	-20mA<I_{OUT3}<-5mA			100	mA
Load Regulation 4	ΔV_{04LOAD}	-40mA<I_{OUT4}<-10mA			100	mA
Load Regulation 5	ΔV_{05LOAD}	20mA<I_{IN5}<40mA			200	mA
Line Regulation 1	ΔV_{01LINE}	33V<V_{IN1}<45V			250	mA
Line Regulation 2	ΔV_{02LINE}	7.5V<V_{IN2}<20V			100	mA
Line Regulation 3	ΔV_{03LINE}	33V<V_{IN1}<45V			100	mA
Line Regulation 4	ΔV_{04LINE}	6.5V<V_{IN5}<8V			100	mA
Quiescent Current 1	I_{CC1}			6.5	9.0	mA
Quiescent Current 2	I_{CC2}			8.5	12.0	mA
Input-Output Voltage Drop	V_{D1}	$V_{OUT1}\Delta V_{01}$=10%, I_{OUT1}=35mA			1.3	V
	V_{D2-1}	$V_{OUT2}\Delta V_{02}$=10%, I_{OUT2}=1A			1.4	V
	V_{D2-2}	$V_{OUT2}\Delta V_{02}$=10%, I_{OUT2}=2A			1.9	V
Saturation Voltage at V_{OUT2} OFF Mode	$V_{02\ OFF(sat)}$	I_{OUT2}=-1A			1.4	V

Pin Assignment



Pin No.	Pin Name	Pin No.	Pin Name
1	V_{OUT1}	6	V_{IN2}
2	V_{IN1}	7	V_{OUT2}
3	V_{OUT5}	8	GND
4	V_{OUT4}	9	R
5	MT	10	V_{OUT3}

Block Diagram and Sample Application Circuit



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