

SANYO**LA6542M****4-Channel Bridge (BTL) Driver for CD-ROM****Overview**

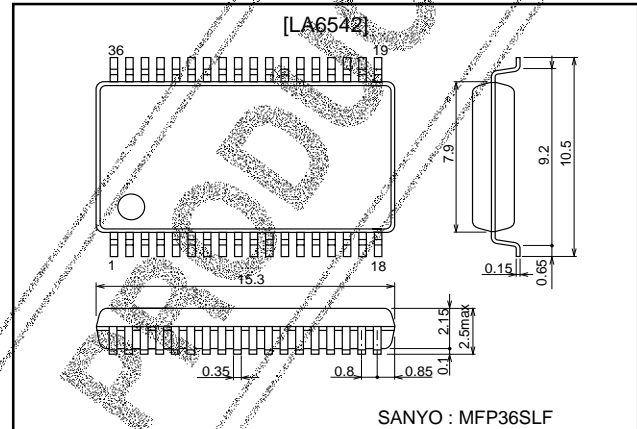
The LA6542M is a 4-channel bridge (BTL) driver developed for CD-ROM applications.

Functions

- 4-channel power amplifier with bridge circuit (BTL)
- I_{Omax} : 1A
- Integrated muting circuit
(MUTE: Output OFF at Low, output ON at High.
MUTE1 is for channels 1 and 2, and MUTE2 for channels 3 and 4.)
- Slew rate 0.5 V/ μ s
- Integrated thermal shutdown circuit

Package Dimensions

unit: mm

3204-MFP36SLF**Specifications****Maximum Ratings at $T_a = 25^\circ\text{C}$**

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage 1	V_{CCmax}		14	V
Maximum supply voltage 2	V_{Smax}	$V_{S1, 2}$	14	V
Maximum input voltage	V_{INmax}	Input pins V_{IN1} to 4	13	V
Mute pin voltage	$V_{MUTEmax}$		13	V
Allowable power dissipation	$Pd max$	IC only	0.9	W
Operating temperature	T_{opr}		-20 to +75	$^\circ\text{C}$
Storage temperature	T_{stg}		-55 to +150	$^\circ\text{C}$

Operating Conditions at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Recommended operation voltage 1	V_{CC}		4 to 13	V
Recommended operation voltage 2-1	V_{S1}		4 to 13	V
Recommended operation voltage 2-2	V_{S2}		4 to 13	V

* $V_{CC} \geq V_{S1, 2}$

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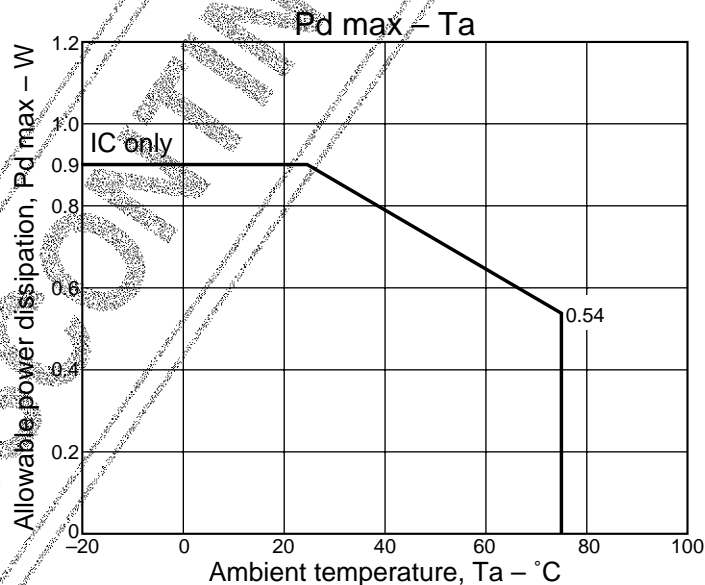
LA6542M

Electrical Characteristics at $V_{CC} = 12V$, $V_S = 5V$, $T_a = 25^\circ C$

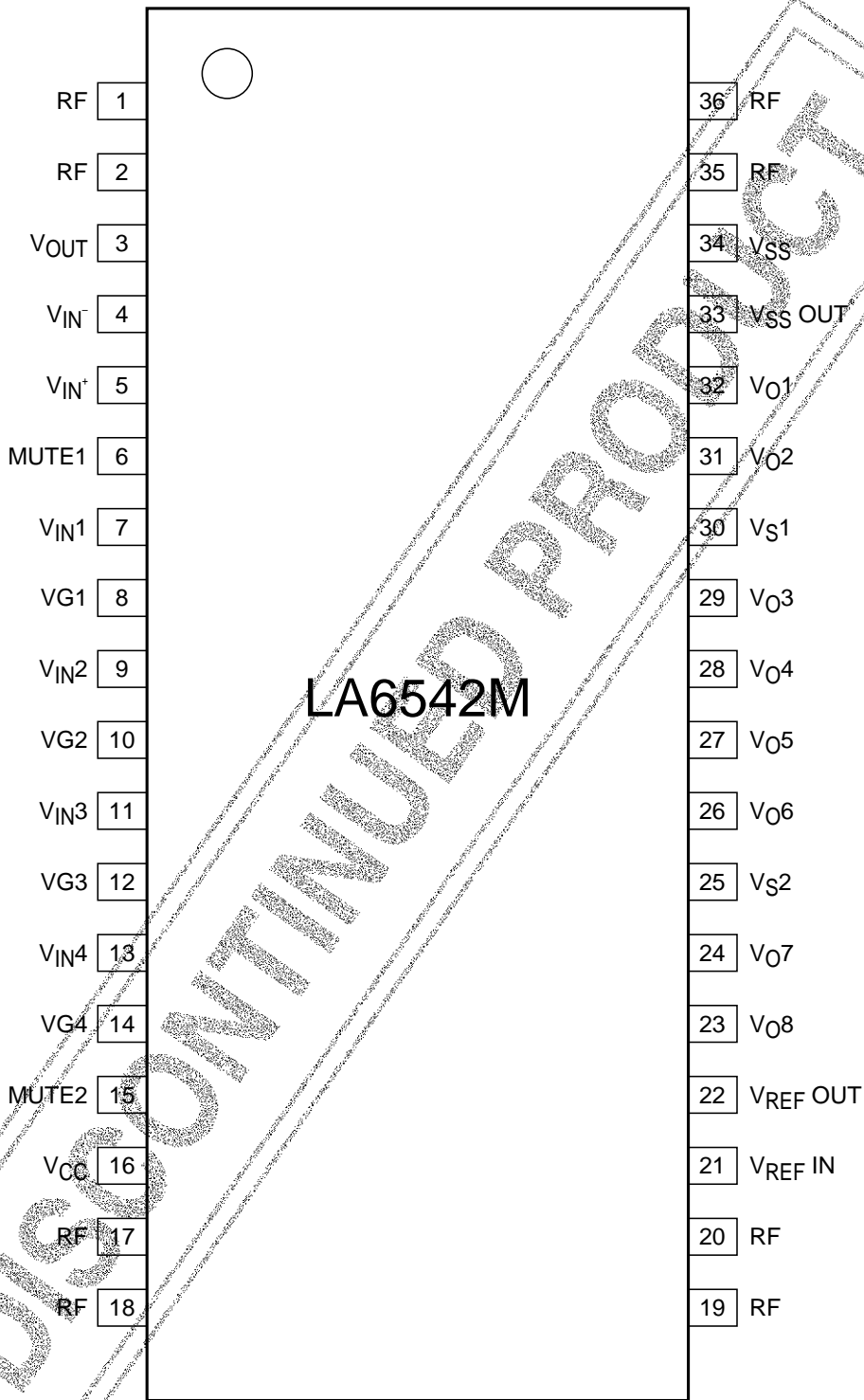
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
V_{CC} no-load current drain	I_{CC1}	All outputs ON (MUTE1, MUTE2: High)	5	10	20	mA
	I_{CC2}	All outputs OFF (MUTE1, MUTE2: Low)		5	10	mA
V_S1 no-load current drain	I_{S1-1}	CH1, 2 ON (MUTE1, MUTE2: High)		10	30	mA
	I_{S1-2}	CH1, 2 OFF (MUTE1, MUTE2: Low)			4	mA
V_S2 no-load current drain	I_{S2-1}	CH3, 4 ON (MUTE1, MUTE2: High)		10	30	mA
	I_{S2-2}	CH3, 4 OFF (MUTE1, MUTE2: Low)			4	mA
Output offset voltage	V_{OF1} to 4	Potential difference between plus and minus outputs for CH1 to CH4	-50		50	mV
Input voltage range	V_{IN}	Input voltage range for V_{IN1} to V_{IN4}	0.5		5	V
Output voltage (source) (sink)	V_{source}	Plus and minus outputs at high level	4.4	4.7		V
		$I_O = 700$ mA				
	V_{sink}	Plus and minus outputs at low level		0.3	0.6	V
		$I_O = 700$ mA				
Closed circuit voltage gain	V_G	Voltage gain between BTL amplifiers		6		dB
Slew rate	SR	(Note 1)		0.5		V/ μ s
Mute ON voltage	V_{MUTE}	MUTE1, MUTE2 voltage when output is ON (Note 2)		1.5	2	V
Mute ON current	I_{MUTE}	MUTE1, MUTE2 current when output is ON (Note 2)		6	10	μ A

Note 1: Guaranteed design value

Note 2: MUTE works on all channels. At High, amplifier output is ON and at Low amplifier output is OFF (output impedance becomes HI).



Pin Assignment



Top view

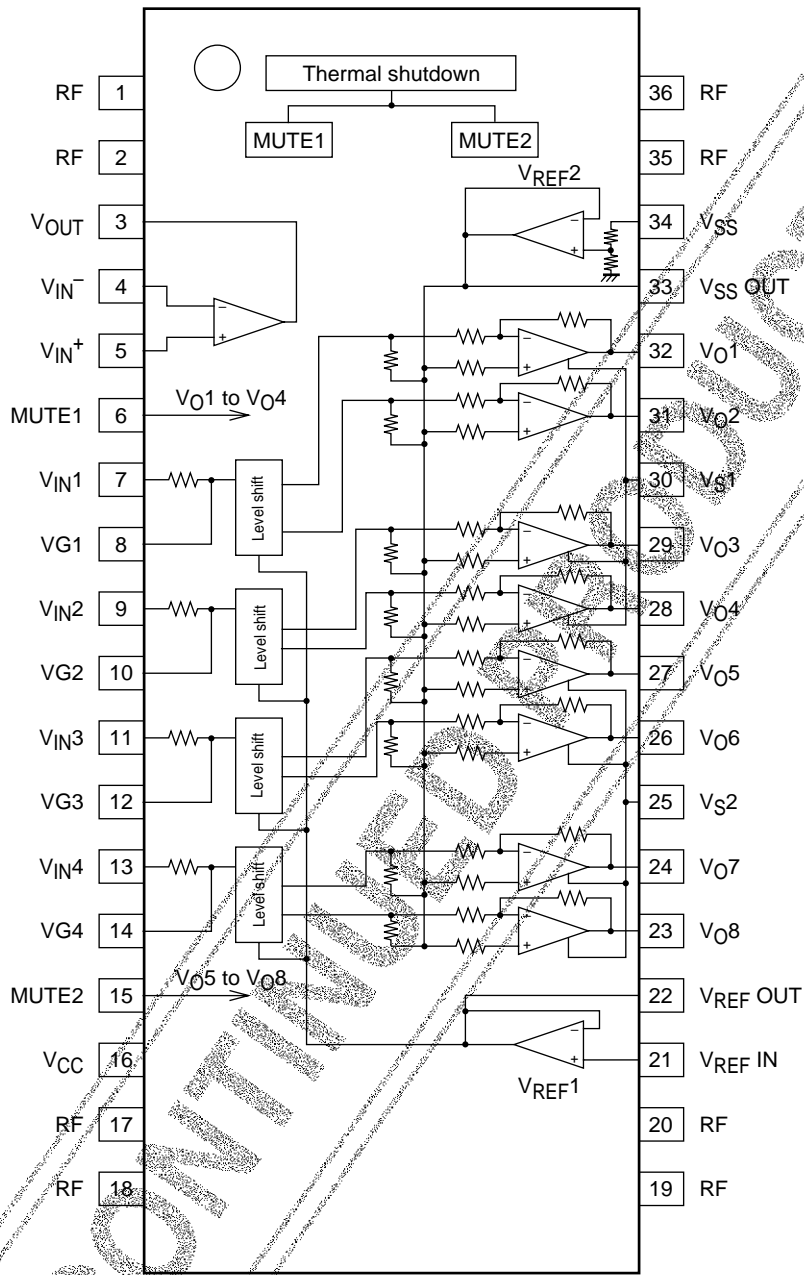
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Pin Function

Pin number	Pin name	Equivalent circuit	Pin function
1, 2 17, 18 19, 20 35, 36	RF		Substrate (minimum potential)
7, 9	V_{IN1}, V_{IN2}		Input pins for CH1 and CH2
11, 13	V_{IN3}, V_{IN4}		Input pins for CH3 and CH4
8, 10	VG1, VG2		Input pins for CH1 and CH2 (for gain adjustment)
12, 14	VG3, VG4		Input pins for CH3 and CH4 (for gain adjustment)
16	V_{CC}		Power supply
22	V_{REFOUT}		Level shift circuit reference voltage (V_{REF1} buffer amplifier output*)
3	V_{OUT}		OP amp output
4	V_{IN-}		OP amp inverted input
5	V_{IN+}		OP amp non-inverted input
6 15	MUTE1 MUTE2		CH1, CH2 output ON/OFF CH3, CH4 output ON/OFF
21	V_{REFIN}		Level shift circuit reference voltage input (V_{REF} buffer amplifier input*)
23 24 26 27 28 29 31 32	V_{O8} V_{O7} V_{O6} V_{O5} V_{O4} V_{O3} V_{O2} V_{O1}		CH4 inverted output (AMP8 output) CH4 non-inverted output (AMP7 output) CH3 inverted output (AMP6 output) CH3 non-inverted output (AMP5 output) CH2 inverted output (AMP4 output) CH2 non-inverted output (AMP3 output) CH1 inverted output (AMP2 output) CH1 non-inverted output (AMP1 output)
25	V_{S2}		CH3 (AMP5, AMP6), CH4 (AMP7, AMP8) output stage power supply
30	V_{S1}		CH1 (AMP1, AMP2), CH2 (AMP3, AMP4) output stage power supply
33	V_{SS-OUT}		Output stage reference voltage ($V_{SS1/2}$: typ) (V_{REF2} buffer amplifier output*)
34	V_{SS}		Connect to VS1, VS2 (resistance split) to generate V_{SSOUT}

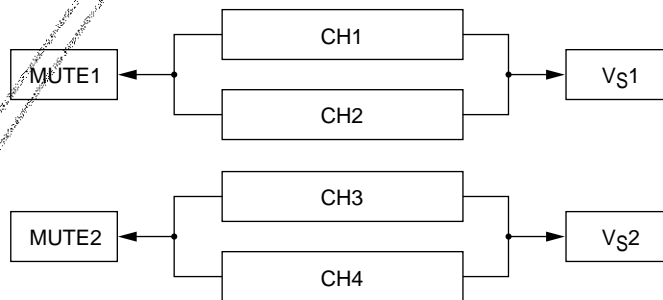
*See block diagram on next page.

Block Diagram



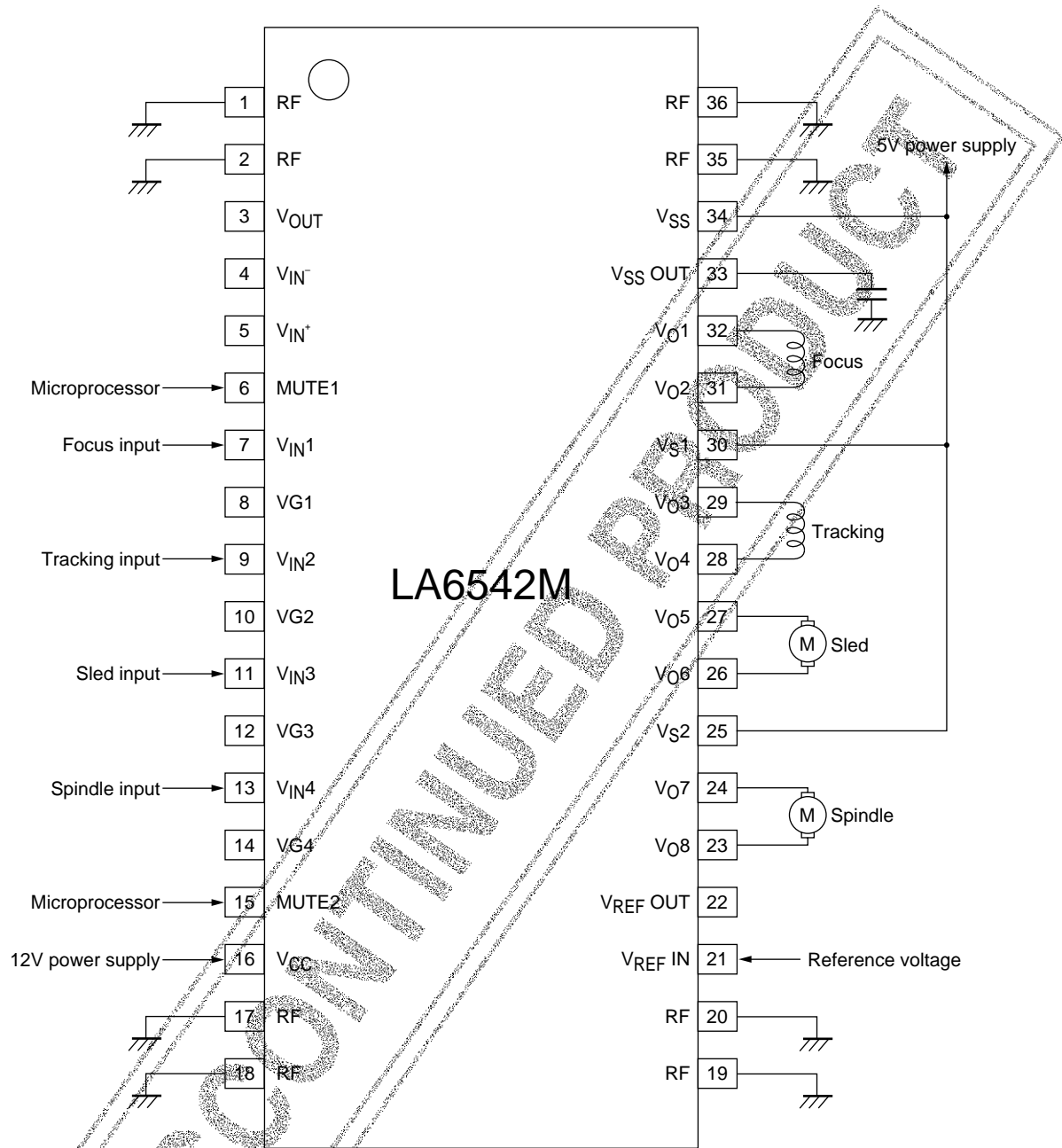
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System Diagram (relationship between power supply and MUTE)



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Sample Application Circuit



A11141

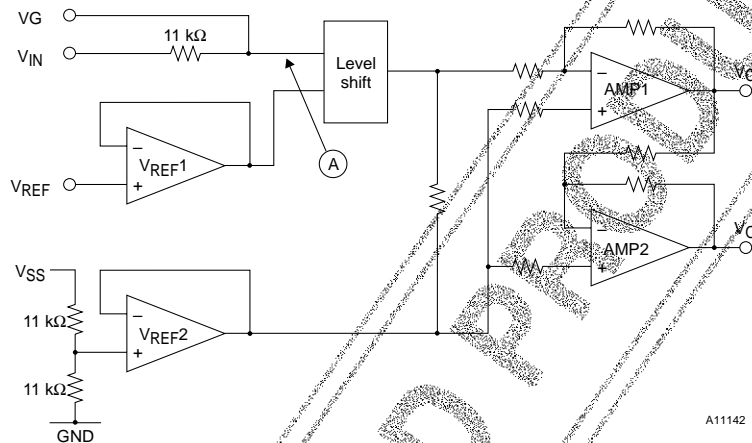
Gain Setting (input pins and adjustment pins)

A simplified diagram of V_{IN} and V_G is shown below.

- 1) Consider an 11 k Ω (typ.) resistor inserted between V_{IN} and V_G .
- 2) When not the pin V_G but the pin V_{IN} is used alone, the BTL gain (between V_{O+} and V_{O-}) is set to 6 dB (0 dB for AMP only). This also applies for the case when V_{IN} is not used and an 11 k Ω external resistor is connected to V_G for input.
- 3) Gain is set by the input impedance as seen from point A.

When V_G only is used and the external resistor is R , the BTL gain (between V_{O+} and V_{O-}) is $20 \log (11 \text{ k}\Omega/R) + 6 \text{ dB}$.

When an 11 k Ω resistor is inserted between V_{IN} and V_G , and input is via V_{IN} , the combined resistance R_z as seen from point A is $R_z = 5.5 \text{ k}\Omega$. Gain is $20 \log (11 \text{ k}\Omega / 5.5 \text{ k}\Omega) + 6 \text{ dB} = 12 \text{ dB}$.



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Offset Voltage

This IC incorporates a level shifter circuit. The input references the V_{REF} to be applied, and references the voltage $(V_{SS} - V_{BE} (0.7))/2V$ to be output.

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