## Functions

- Three-phase current linear drive with switching between full-wave and half-wave operations
- Torque ripple correction circuit
- Current limiter circuit
- Upper and lower sides output stage saturation prevention circuits
- Short brake circuit
- FG amplifier
- Thermal shutdown circuit


## Specifications

## Absolute Maximum Ratings at $\mathbf{T a}=25^{\circ} \mathrm{C}$

## Package Dimensions

unit: mm
3233-HSOP28H


| Parameter | Symbol | Conditions | Ratings | Unit |
| :---: | :---: | :---: | :---: | :---: |
| Maximum supply voltage | $\mathrm{V}_{\text {CCImax }}$ |  | 6 | V |
|  | $\mathrm{V}_{\text {S }}$ max |  | 15.5 | V |
| Maximum output current | lomax |  | 1.5 | A |
| Maximum output voltage | $\mathrm{V}_{\mathrm{O}}$ max |  | 30 | V |
| Allowable power dissipation | Pdmax | Independent IC | 0.8 | W |
|  |  | $76.1 \times 114.3 \times 1.6 \mathrm{~mm}^{3}$ : With glass epoxy | 2.0 | W |
| Operating temperature | Topr |  | -20 to +75 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature | Tstg |  | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |

## Allowable Operating Ranges at $\mathbf{T a}=\mathbf{2 5}^{\circ} \mathbf{C}$

| Parameter | Symbol | Conditions | Ratings | Unit |
| :---: | :---: | :---: | :---: | :---: |
| Supply voltage | $\mathrm{V}_{\mathrm{S}}$ |  | 8 to 15 | V |
|  | $\mathrm{V}_{\mathrm{CC}}$ |  | 4.5 to 5.5 |  |
| Hall input amplitude | $\mathrm{V}_{\text {HALL }}$ | Between Hall inputs | $\pm 20$ to $\pm 100$ | mV 0-P |
| GSENSE input range | VGSENSE | With respect to the control system ground | -0.20 to +0.20 | V |

Note : Forward/reverse switching is not possible in half-wave operation mode.
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## LB11985H

Electrical Characteristics at $\mathbf{T a}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~V}_{\mathrm{S}}=\mathbf{1 5} \mathrm{V}$

| Parameter | Symbol | Conditions | Ratings |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | min | typ | max |  |
| $\mathrm{V}_{\text {CC }}$ current drain | ICC | $\mathrm{RL}=\infty, \mathrm{VCTL}=0 \mathrm{~V}$ (quiescent mode) |  | 10 | 15 | mA |
| [Output] |  |  |  |  |  |  |
| Output saturation voltage | $\mathrm{V}_{\text {Osat }} 1$ | $\begin{aligned} & \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA}, \mathrm{Rf}=0.5 \Omega \text {, Sink }+ \text { Source } \\ & \mathrm{VCTL}=\mathrm{VLIM}=5 \mathrm{~V} \text { (with saturation prevention) } \end{aligned}$ |  | 2.2 | 2.7 | V |
|  | $\mathrm{V}_{\text {Osat }}{ }^{2}$ | $\begin{aligned} & \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}, \mathrm{Rf}=0.5 \Omega, \text { Sink }+ \text { Source } \\ & \mathrm{VCTL}=\mathrm{VLIM}=5 \mathrm{~V} \text { (with saturation prevention) } \end{aligned}$ |  | 2.8 | 3.7 | V |
| Output leakage current | Ioleak |  |  |  | 1.0 | mA |
| [FR] |  |  |  |  |  |  |
| FR pin input Threshold voltage | $V_{\text {FR }}$ |  | 1 |  | 4 | V |
| FR pin input Input bias current | lb (FR) | $\mathrm{VFR}=5 \mathrm{~V}$ |  | 100 | 150 | $\mu \mathrm{A}$ |
| [BR] |  |  |  |  |  |  |
| BR pin input Threshold voltage | $\mathrm{V}_{\text {BRTH }}$ |  | 1 |  | 4 | V |
| BR pin input Input bias current | lb (BR) | $\mathrm{VBR}=5 \mathrm{~V}$ |  | 100 | 150 | $\mu \mathrm{A}$ |
| [Control] |  |  |  |  |  |  |
| CTLREF pin voltage | $\mathrm{V}_{\text {CREF }}$ |  | 2.0 | 2.15 | 2.3 | V |
| CTLREF pin input range | $\mathrm{V}_{\text {CREF }} \mathrm{IN}$ |  | 1 |  | 4 | V |
| CTL pin input bias current | lb (CTL) | VCTL $=5 \mathrm{~V}$, with CTLREF open |  |  | 5 | $\mu \mathrm{A}$ |
| CTL pin control start voltage | $\mathrm{V}_{\text {CTL }}(\mathrm{ST})$ | $\mathrm{Rf}=0.5 \Omega, \mathrm{VLIM}=5 \mathrm{~V}, \mathrm{Io} \geq 40 \mathrm{~mA}$ <br> With the Hall input logic states fixed ( $\mathrm{U}, \mathrm{V}, \mathrm{W}=$ high, high, low) | 2.0 | 2.2 | 2.4 | V |
| CTL pin control Gm | $\mathrm{G}_{\mathrm{m}}(\mathrm{CTL})$ | $\mathrm{Rf}=0.5 \Omega, \Delta \mathrm{lo}=200 \mathrm{~mA}$ <br> With the Hall input logic states fixed (U, V, W = high, high, low) | 1.8 | 2.25 | 2.7 | V |
| [Current Limiter] |  |  |  |  |  |  |
| LIM current limit offset voltage | $\mathrm{V}_{\text {off }}($ LIM $)$ | $\begin{aligned} & \hline \mathrm{Rf}=0.5 \Omega \text {, VCTL }=5 \mathrm{~V} \text {, lo } \geq 40 \mathrm{~mA} \\ & \text { With the Hall input logic states fixed ( } \mathrm{U}, \mathrm{~V}, \mathrm{~W}=\text { high, high, low) } \\ & \hline \end{aligned}$ | 80 | 200 | 320 | mV |
| LIM pin input bias current | lb (LIM) | VCTL $=5 \mathrm{~V}, \mathrm{VREF}$ : OPEN, VLIM $=0 \mathrm{~V}$ | -2 | -1 |  | $\mu \mathrm{A}$ |
| LIM pin current limit level | Gm (LIM) | $\mathrm{Rf}=0.5 \Omega, \mathrm{VCTL}=5 \mathrm{~V}$ <br> With the Hall input logic states fixed ( $\mathrm{U}, \mathrm{V}, \mathrm{W}=$ high, high, low) | 0.37 | 0.47 | 0.57 | mA |
| [Hall Amplifier] |  |  |  |  |  |  |
| Input offset voltage | $\mathrm{V}_{\text {off }}$ (HALL) |  | -6 |  | +6 | mV |
| Input bias current | $\mathrm{Ib}_{\mathrm{b}}$ (HALL) |  |  | 1.0 | 3.0 | $\mu \mathrm{A}$ |
| Common-mode input voltage | $\mathrm{V}_{\mathrm{cm}}$ (HALL) |  | 1.3 |  | 3.3 | V |
| Torque ripple correction ratio | TRC | At the bottom and peak that occur in the Rf waveform at $200 \mathrm{~mA}(\mathrm{Rf}=0.5 \Omega)$ |  | 14.5 |  | \% |
| [FG Amplifier] |  |  |  |  |  |  |
| FG amplifier input offset voltage | $\mathrm{V}_{\text {off }}(\mathrm{FG})$ |  | -8 |  | +8 | mV |
| FG amplifier input bias current | $\mathrm{l}_{\mathrm{b}}(\mathrm{FG})$ |  | -100 |  |  | nA |
| FG amplifier output saturation voltage | $\mathrm{V}_{\text {Osat }}(\mathrm{FG})$ | For the sink side, at the internal pull-up resistor |  | 0.4 | 0.55 | V |
| FG amplifier common-mode input voltage | $\mathrm{V}_{\mathrm{CM}}$ (FG) |  | 1.0 |  | 4.0 | V |
| [Saturation] |  |  |  |  |  |  |
| Saturation prevention circuit lower side set voltage | $\mathrm{V}_{\text {Osat }}(\mathrm{DET})$ | $\mathrm{Io}=10 \mathrm{~mA}, \mathrm{Rf}=0.5 \Omega, \mathrm{VCTL}=\mathrm{VLIM}=5 \mathrm{~V}$ <br> The voltages between the OUT-Rf pairs at full wave. | 0.13 | 0.25 | 0.42 | V |
| [Schmitt Amplifier] |  |  |  |  |  |  |
| Duty | DUTY | $60 \mathrm{mVp}-\mathrm{p}, 1 \mathrm{kHz}$ input *1 | 49 | 50 | 51 | \% |
| Upper side output saturation voltage | $\mathrm{V}_{\text {satu }}(\mathrm{SH})$ |  | 4.8 |  |  | V |
| Lower side output saturation voltage | $\mathrm{V}_{\text {satd }}(\mathrm{SH})$ |  |  |  | 0.2 | V |
| Hysteresis | Vhys | Design target values *2 |  | 45 |  | mV |
| TSD operating temperature | T-TSD | Design target values *2 |  | 180 |  | ${ }^{\circ} \mathrm{C}$ |
| TSD hysteresis | $\Delta \mathrm{T}$-TSD | Design target values *2 |  | 15 |  | ${ }^{\circ} \mathrm{C}$ |

Note *1 : The ratings are just the measured value with no margin afforded.
*2 : Items shown to be design target values in the conditions column are not measured.

## Truth Table and Control Functions

|  | Source $\rightarrow$ Sink | Hall input |  |  | FR |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | U | V | W |  |
| 1 | $\mathrm{V} \rightarrow \mathrm{W}$ | H | H | L | H |
|  | $\mathrm{W} \rightarrow \mathrm{V}$ |  |  |  | L |
| 2 | $\mathrm{U} \rightarrow \mathrm{W}$ | H | L | L | H |
|  | $\mathrm{W} \rightarrow \mathrm{U}$ |  |  |  | L |
| 3 | $\mathrm{U} \rightarrow \mathrm{V}$ | H | L | H | H |
|  | $V \rightarrow U$ |  |  |  | L |
| 4 | $\mathrm{W} \rightarrow \mathrm{V}$ | L | L | H | H |
|  | $\mathrm{V} \rightarrow \mathrm{W}$ |  |  |  | L |
| 5 | $\mathrm{W} \rightarrow \mathrm{U}$ | L | H | H | H |
|  | $\mathrm{U} \rightarrow \mathrm{W}$ |  |  |  | L |
| 6 | $V \rightarrow U$ | L | H | L | H |
|  | $U \rightarrow V$ |  |  |  | L |

Note: 1. In the FR column, "H" indicates a voltage of 2.75 V or higher, and " L " indicates a voltage of 2.25 V or lower. (When $\mathrm{V}_{\mathrm{CC}}$ is 5 V .)
2. For the Hall inputs, the input high state is defined to be the state where the (+) input is higher than the corresponding (-) input by at least 0.02 V , and the input low state is defined to be the state where the (+) input is lower than the corresponding ( - ) input by at least 0.02 V .

## Allowable Power Dissipation



## Pin Assignment



## Sample Application Circuit



A12221

Block Diagram


Pin Functions
Unit (resistance : $\Omega$ )

\begin{tabular}{|c|c|c|c|c|}
\hline Pin No. \& Symbol \& Pin Voltage \& Description \& Equivalent circuit \\
\hline \& FRAME GND \& \& Ground for circuits other than the output transistors. The lowest potential of the output transistors will be the that of the RF pin. \& \\
\hline 1 \& VS1 \& 8 V to 15 V \& Output block power supply \& \\
\hline 2 \& VS2 \& \& A diode is internally connected between VS1 and this pin to prevent reverse current flow in half-wave operating mode. \& \\
\hline 3 \& GSENSE \& \& \begin{tabular}{l}
Ground sensing. \\
The influence of the common ground impedance on Rf can be excluded by connecting this pin to the ground near the Rf resistor in the motor ground lines that include RF. (This pin must not be left open.)
\end{tabular} \& \\
\hline \[
\begin{aligned}
\& 4 \\
\& 5
\end{aligned}
\] \& RF(SENSE) RF(POWER) \& \& \begin{tabular}{l}
Output current detection. \\
Current feedback is applied to the control block by inserting the resistor Rf between these pins and ground. Also, both the lower side saturation prevention circuit and the torque ripple correction circuit operate according to the voltage on this pin. In particular, since this voltage sets the oversaturation prevention level, the lower side oversaturation prevention operation can be degraded if the value of this resistor is set too low. \\
Note that the POWER pin and the SENSE pin must be connected together.
\end{tabular} \& \\
\hline 6 \& U OUT \& \& \&  \\
\hline 7

8 \& $\mathrm{V}_{\text {OUT }}$

W OUT \& \& Coil output \& A13015 <br>
\hline 9 \& MCOM \& \& Motor midpoint connection. Half-wave drive is implemented by connecting the motor midpoint to this pin. \& A13016 <br>
\hline
\end{tabular}

Continued on next page

Continued from preceding page.
Unit (resistance : $\Omega$, current : A )


Continued from preceding page.
Unit (resistance : $\Omega$, current : A )

\begin{tabular}{|c|c|c|c|c|}
\hline Pin No. \& Symbol \& Pin Voltage \& Description \& Equivalent circuit <br>
\hline 22 \& FC \& \& Frequency characteristics correction. Oscillation in the current control system closed loop can be prevented by inserting a capacitor between this pin and ground. \& A13022 <br>
\hline 23

25 \& CTLREF

CTL \& \begin{tabular}{l}
$$
\begin{gathered}
1 \mathrm{~V} \text { to } 4 \mathrm{~V} \\
\left(\mathrm{~V}_{\mathrm{CC}}=5 \mathrm{~V}\right)
\end{gathered}
$$ <br>
0 V to $\mathrm{V}_{\mathrm{CC}}$

 \& 

Control reference voltage. <br>
Although this voltage is set to $\mathrm{V}_{C C} \times(15 / 35)$ internally, it can be modified by applying a voltage from a low-impedance circuit. <br>
Speed control. <br>
Control consists of a constant current drive scheme implemented by applying current feedback from RF.
\end{tabular} \& A13023 <br>

\hline 24 \& LIM \& 0 V to $\mathrm{V}_{\mathrm{Cc}}$ \& | Current limiter function control. |
| :--- |
| The voltage applied to this pin modifies the output current linearly. | \&  <br>


\hline 26 \& FR \& 0 V to $\mathrm{V}_{\mathrm{Cc}}$ \& | Forward/reverse control. |
| :--- |
| The voltage applied to this pin selects forward or reverse operation. | \& A13025 <br>


\hline 27 \& ADJ \& \& | External torque ripple correction ratio adjustment. To adjust the correction ratio, apply the stipulated voltage to the ADJ pin from a low-impedance external circuit. |
| :--- |
| If the applied voltage is increased, the correction ratio rises, and if the applied voltage is lowered, the correction ratio falls. | \&  <br>


\hline 28 \& $\mathrm{V}_{\mathrm{CC}}$ \& 4.5 V to 5.5 V \& | Power supply for all circuits other than the IC internal output block. |
| :--- |
| This voltage must be stabilized so that ripple and noise do not enter the IC. | \& <br>

\hline
\end{tabular}

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