Monolithic Digital IC



# LB1817M

# **FDD Spindle Motor Driver**

### **Overview**

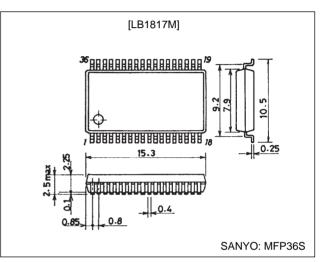
The LB1817M is the ideal IC for applications requiring a 5 V, low-profile FDD spindle motor driver.

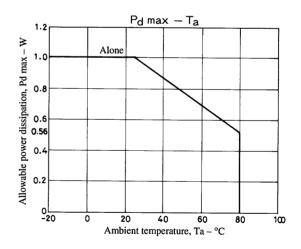
## **Functions and Features**

- Three phase total wave linear driver (external PNP)
- Low saturation voltage
- On-chip digital speed control
- Start/stop circuit ("L" level active)
- Rotation speed switching
- Current limiter circuit
- On-chip index processing circuit
- Index timing supports adjustments using VR
- AGC circuit
- Temperature protection circuit

# **Package Dimensions**

unit: mm **3129-MFP36S** 





# Specifications

#### Absolute Maximum Ratings at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V <sub>CC</sub> max		7.0	V
Maximum output current	I <sub>CC</sub> max1	t≤0.5	1.5	A
Steady maximum output current	I <sub>O</sub> max2		1.0	А
Allowable power dissipation	Pd max	Independent IC	1	W
Operating temperature	Topr		-20 to +80	°C
Storage temperature range	Tstg		-40 to +150	°C

#### Allowable Operating Conditions at $Ta=25^{\circ}C$

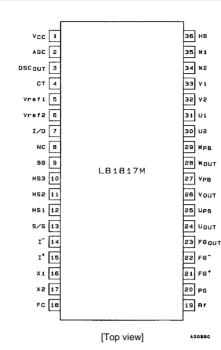
Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V <sub>CC</sub>		4.2 to 6.5	V

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# Electrical Characteristics at Ta = 25°C, $V_{CC}$ = 5V

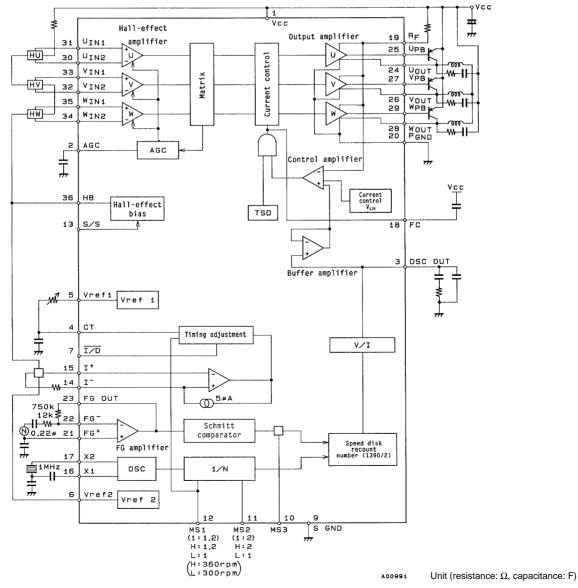
Parameter	Symbol	Conditions		Ratings	1	Unit	Note
			min typ		max		
Current drain	Icco	S/S = 5V (Standby)		70	100	μA	
	Icc	S/S = 0V (Steady)		25	35	mA	
MS1 bias current	I <sub>MS1</sub>	V <sub>MS1</sub> = 5V		180	270	μA	
MS1 "L" level input voltage	V <sub>MS1L</sub>		0		0.8	V	
MS1 "H" level input voltage	V <sub>MS1H</sub>		2.0		V <sub>CC</sub>	V	
MS2 bias current	I <sub>MS2</sub>	$V_{MS2} = 5V$		90	135	μA	
MS2 "L" level input voltage	V <sub>MS2L</sub>		0		0.8	V	
MS2 "H" level input voltage	V <sub>MS2H</sub>		2.0		V <sub>CC</sub>	V	
MS3 bias current	I <sub>MS3</sub>	V <sub>MS3</sub> = 5V		90	135	μA	
MS3 "L" level input voltage	V <sub>MS3L</sub>		0		0.8	V	
MS3 "H" level input voltage	V <sub>MS3H</sub>		2.0		V <sub>CC</sub>	V	
S/S bias current	I <sub>S/S</sub>				20	μA	
S/S "L" level voltage	V <sub>S/SL</sub>		0		0.8	v.	
S/S "H" level voltage	V <sub>S/SH</sub>		2.0		V <sub>CC</sub>	V	
Hall-effect bias amplifier input current	I <sub>HB</sub>				15	μA	
In-phase input voltage range	Vh		2.0		V <sub>CC</sub> - 0.7	V	
Differential input voltage range	Vdif		50		200	w mVp-p	
· · · ·	Vuil		50		±10	mV	*
Input offset voltage		L 5m0	0.5	0.0		V	
Hall-effect output voltage	V <sub>H</sub>	$I_{\rm H} = 5 {\rm mA}$	0.5	0.8	1.1		
Leak current	I <sub>HL</sub>	S/S = 5V			±10	μΑ	
Output saturation voltage	Vsat	I <sub>O</sub> = 0.8A		0.45	0.64	V	
Output leak current	I <sub>OL</sub>				1.0	mA	
Current limiter	I <sub>lim</sub>	$R_F = 3k\Omega$ , ROUT = 100 $\Omega$	6.3	7.5	8.7	mA	
Control amplifier voltage gain	G <sub>C</sub>		-7.5	-5.5	-3.5	dB	
Voltage gain phase differential	∆G <sub>C</sub>				±1	dB	
V/I conversion source current	I+		19	28	37	μA	
V/I conversion sink current	I-		-19	-28	-37	μA	
V/I conversion current ratio	I+/I-		0.8	1.0	1.2		
DSC buffer input current	IDSC				1.0	μA	
FG amplifier input voltage	V <sub>FG</sub>	f <sub>FG</sub> = 300Hz	2		20	mVp-p	
FG amplifier voltage gain	G <sub>FG</sub>	Open loop		60		dB	*
FG amplifier input offset	V <sub>FGO</sub>				±10	mV	*
FG amplifier internal reference voltage	V <sub>FGB</sub>		2.2	2.5	2.8	V	
	∆Vsh1	"H" → "L"		25		mV	*
FG schmitt hysteresis width	∆Vsh2	"L" → "H"		25		mV	*
Speed disk recount number	N			1390/2			
Disk operation frequency	FD				1.1	MHz	*
Oscillation range	Fosc				1.1	MHz	*
Oscillation frequency error	△F <sub>OSC</sub>				±0.2	%	
Index output "L" level voltage		I <sub>O</sub> = 2mA			0.4	70 V	
Index output Leak current	V <sub>IDL</sub>				±10		
Index output leak current Index amplifier in-phase input voltage range	I <sub>IDL</sub>		0.0			μA V	
	VI		0.2		V <sub>CC</sub> -0.7		
Index amplifier differential input voltage range	V <sub>DIF</sub>	Hysteresis width<25mA	25	10	100	mV	
Index amplifier hysteresis setting current	I <sub>HYS</sub>	MOL	2.9	4.2	5.5	μΑ	
Timing adjustment "H" level	V <sub>TH</sub>	MS1 = L	1.15	1.26	1.35	V	
Timing adjustment "L" level	V <sub>TL</sub>	MS1 = L	0.4	0.52	0.6	V	
Timing adjustment ratio	T <sub>HL</sub>	$V_{TH}$ (MS1 = L)/ $V_{TH}$ (MS1 = H)		1.148			
Reference voltage	V <sub>REF1</sub>		2.20	2.50	2.80	V	
	V <sub>REF2</sub>		1.85	2.15	2.45	V	
Excessive heat protected operating temperature	TSD		150	180		°C	*
Hysteresis width	∆TSD			10		°C	*

Note: Marked values (\*) are guaranteed by the design itself and therefore do not require measurement.



### **Block Diagram**

**Pin Assignment** 



## **Pin Description**

			Unit (resistance: Ω)							
Pin No.	Symbol	Pin voltage	Equivalent circuit	Pin description						
1	V <sub>CC</sub>			Power supply voltage pin.     Voltage must be stable and free of ripple     noise interference.						
2	AGC		00 V CC	AGC pin.     Controls hall-effect amplifier gain in     response to hall-effect input frequency.     External capacitor installation.						
3	DSC out		300 V CC 3 3 3 4 3 4 4 4 4 0 5 0 0 4 4 0 0 5 3 4 4 0 0 5 5 3 4 4 5 6 5 7 5 7 5 7 5 7 7 7 7 7 7 7 7 7 7 7	Speed discriminator pin.						
4	СТ		• V <sub>CC</sub> 4 4 4 4 4 4 4 4 4 4 4 4 4	Timing adjustment pin. External CR for delay time constant connected.						
5	Vref1	2.5V typ	0 V CC 100 € 5 8 8 7 7 7 7 7 7 7 7 7 7 7 8 8 7 7 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8	Vref1 pin. Used as external CR power supply for index timing adjustment applications.						
6	Vref2	2.15V typ	Sover Sover	<ul> <li>Vref2 pin. Used for sensor bias for external index applications.</li> </ul>						

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	d from precedin		Unit (resistance: Ω	)
Pin No.	Symbol	Pin voltage	Equivalent circuit	Pin description
7	I/D		~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~	Index pulse output pin.
8	NC			No connection.
9	GND			<ul> <li>Ground pin for signal system.</li> <li>Grounded as with pin 20.</li> </ul>
10	MS3	H: 2.0V min L: 0.8V max	0 V CC 10 ↓ 50 K ↓ 50 K ↓ 005588	<ul> <li>FG changeover pin. When operating at an "H" level, FG sets to a through state. An "L" level results in 1- step division of FG.</li> </ul>
11	MS2	H: 2.0V min L: 0.8V max	0VCC	<ul> <li>CLK changeover pin. When operating at an "H" level, CLK sets to a through state. An "L" level results in 1-step division of CLK.</li> </ul>
12	MS1	H: 2.0V min L: 0.8V max	0VCC 12 50K 50K 50K 50K 401000	<ul> <li>Rotation speed changeover pin. An "H" level sets rotation speed to 360 rpm. An "L" level sets rotation speed to 300 rpm. For more details, refer to the rotation speed changeover table.</li> </ul>
13	S/S	H: 2.0V min L: 0.8V max	200 200 13 401001	Start/stop changeover pin.     "L" level active.

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Unit (resistance:  $\Omega$ )

	Unit (resistance: Ω)						
Pin No.	Symbol	Pin voltage	Equivalent circuit	Pin description			
14	-  +		I A01002	<ul> <li>External index negative input pin.</li> <li>External index positive input pin. When the I- pin is at an "H" level, I1 operates with the fixed current; at an "L" level, I1 does not flow. Hysteresis width is determined by the resistor attached externally to the I- pin.</li> </ul>			
16	X1		400 400 15 200 400 400 400 400 400 400 400	Reference clock generating pin.			
17	X2		17 W A01004				
18	FC			• Frequency characteristics revision pin By installing a capacitor between this pin and $V_{CC}$ , close-loop oscillation for the current control system halts.			
19	RF			• Output current detection pin. By installing an $R_f$ resistor between this pin and $V_{CC}$ , output current is detected as voltage. Voltage detection at this pin activates the current limiter. Detection level is approximately 1/50 of output current.			
20	PGND			Output transistor grounding pin. Grounded as with pin 9.			

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Unit (resistance:  $\Omega$ )

			Unit (resistance: Ω)						
Pin No.	Symbol	Pin voltage	Equivalent circuit	Pin description					
21 22	FG+ FG-	2.5V typ	200 100 200 12k 12k 200 12k 200 12k 200 12k 200 12k 200 12k 200 12k 200 12k 200 10k 10k 10k 10k 10k 10k 10k 1	<ul><li>FG amplifier positive pin.</li><li>FG amplifier negative pin.</li></ul>					
23	FG out		× × × × × × × × × × × × × × × × × × ×	• FG amplifier output pin.					
24 25 26 27 28 29	U <sub>OUT</sub> U <sub>PB</sub> Vout V <sub>PB</sub> W <sub>OUT</sub> W <sub>PB</sub>		V <sub>CC</sub> ~ (24) (25) (29) (29) (29) (28) (28) (20) (20) (20) (20) (20) (20) (20) (20	<ul> <li>U-phase output pin.</li> <li>Base connection pin for U-phase external PNP.</li> <li>V-phase output pin.</li> <li>Base connection pin for V-phase external PNP.</li> <li>W-phase output pin.</li> <li>Base connection pin for W-phase external PNP.</li> </ul>					
30 31 32 33 34 35	$\begin{array}{c} U_{IN}^{}2\\ U_{IN}^{}1\\ V_{IN}^{}2\\ V_{IN}^{}1\\ W_{IN}^{}2\\ W_{IN}^{}1\end{array}$		31 200 33 200 34 35 77 401009	<ul> <li>U-phase hall-effect input pin. U<sub>IN1</sub> &gt; U<sub>IN2</sub> is established when logic is at an "H" level.</li> <li>V-phase hall-effect input pin. V<sub>IN1</sub> &gt; V<sub>IN2</sub> is established when logic is at an "H" level.</li> <li>W-phase hall-effect input pin. W<sub>IN1</sub> &gt; W<sub>IN2</sub> is established when logic is at an "H" level.</li> </ul>					
36	НВ		V <sub>CC</sub> ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~	<ul> <li>Hall-effect bias applied to minus-side pin. When stopped, switches open and hall- effect bias severs.</li> </ul>					

### **Truth Table**

$\square$	Source $\rightarrow$ Sink	Hall-Effect Input				
		U	V	W		
1	V-phase $\rightarrow$ W-phase	н	Н	L		
2	V-phase $\rightarrow$ U-phase	L	н	L		
3	W-phase $\rightarrow$ U-phase	L	Н	Н		
4	W-phase $\rightarrow$ V-phase	L	L	н		
5	U-phase $\rightarrow$ V-phase	Н	L	Н		
6	U-phase $\rightarrow$ W-phase	н	L	L		

When an "H" level exists for hall-effect input,

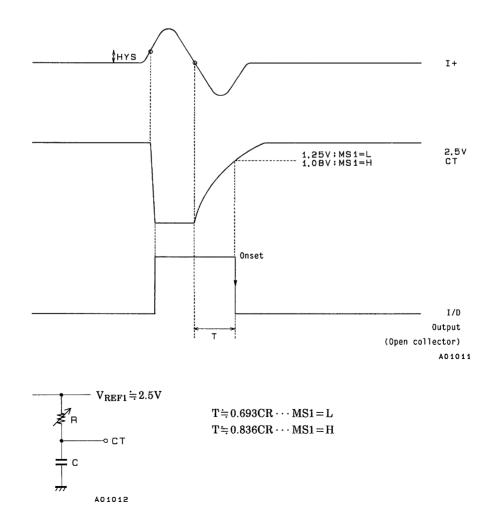
 $U_{IN1} > U_{IN2}$  $V_{IN1} > V_{IN2}$ 

$$W_{IN1} > W_{IN2}$$

# **Rotation Speed Changeover Table**

$f_{OSC} = 1M$	Hz							
MS1	Н	L	Н	L	Н	L	Н	L
MS2	Н		L		Н		L	
MS3	Н		L		L		ŀ	4
f <sub>FG</sub> [Hz]	720	600	720	600	1440	1200	360	300

# Index and Timing Chart



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