Ordering number : EN4947A

Monolithic Digital IC

SANYO No. 4947A

# LB1886V

## Three-Phase Brushless Motor Driver

## Overview

The LB1886V is a three-phase brushless motor driver IC that is optimal for capstan and drum motor drive in camcorders and other VCR products and for motor drive in digital audio products.

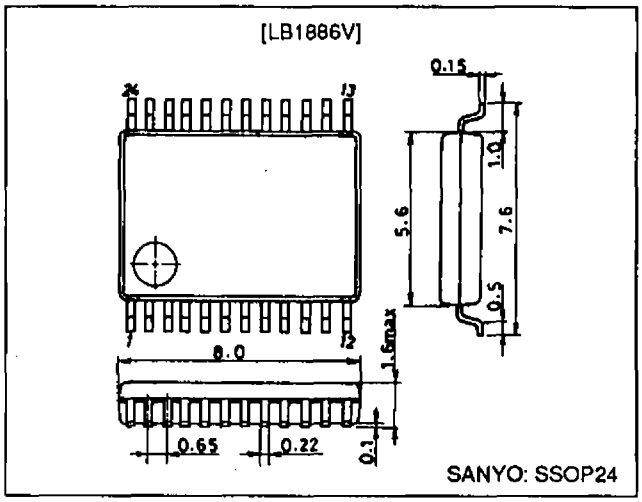
## Features

- 120° voltage linear drive scheme
- Motor voltage control based speed control provides reduced power (and thus is optimal for use in portable equipment)
- Built-in torque ripple compensation filter
- Soft switching scheme requires a smaller external capacitance (thus chip capacitors can be used)
- Built-in thermal shutdown circuit
- Built-in FG amplifier

## Package Dimensions

unit: mm

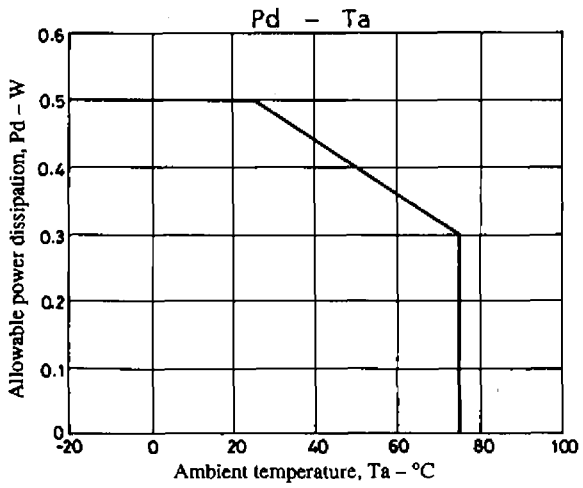
**3175A-SSOP24**




## Specifications

**Absolute Maximum Ratings at Ta = 25°C**

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Maximum supply voltage 1 | $V_{CC}1$ max | | 7 | V |
| Maximum supply voltage 2 | $V_{CC}2$ max | | 12 | V |
| Maximum supply voltage 3 | $V_S$ max | | $V_{CC}2$ | V |
| Applied output voltage | $V_O$ max | | $V_S$ + 2 | V |
| Applied input voltage | $V_I$ max | All input pins | $V_{CC}1$ | V |
| Output current | $I_O$ max | | 1.0 | A |
| Allowable power dissipation | Pd max | | 0.5 | W |
| Operating temperature | Topr | | −20 to +75 | °C |
| Storage temperature | Tstg | | −55 to +150 | °C |





SANYO Electric Co., Ltd. Semiconductor Business Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

## Allowable Operating Ranges at Ta = 25°C

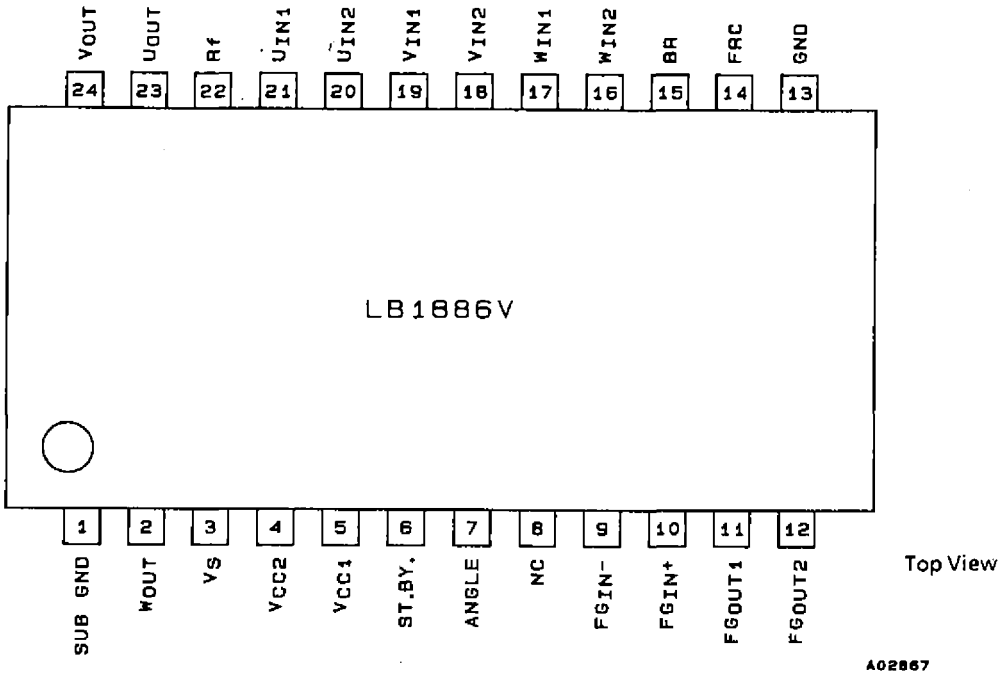
| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage 1 | $V_{CC}1$ | $V_{CC}1 \leq V_{CC}2$ | 4.0 to 6.0 | V |
| Supply voltage 2 | $V_{CC}2$ | | 4 to 10 | V |
| Supply voltage 3 | $V_S$ | | up to $V_{CC}2$ | V |

## Electrical Characteristics at Ta = 25°C, $V_{CC}1$ = 5 V, $V_{CC}2$ = 7 V, $V_S$ = 3 V

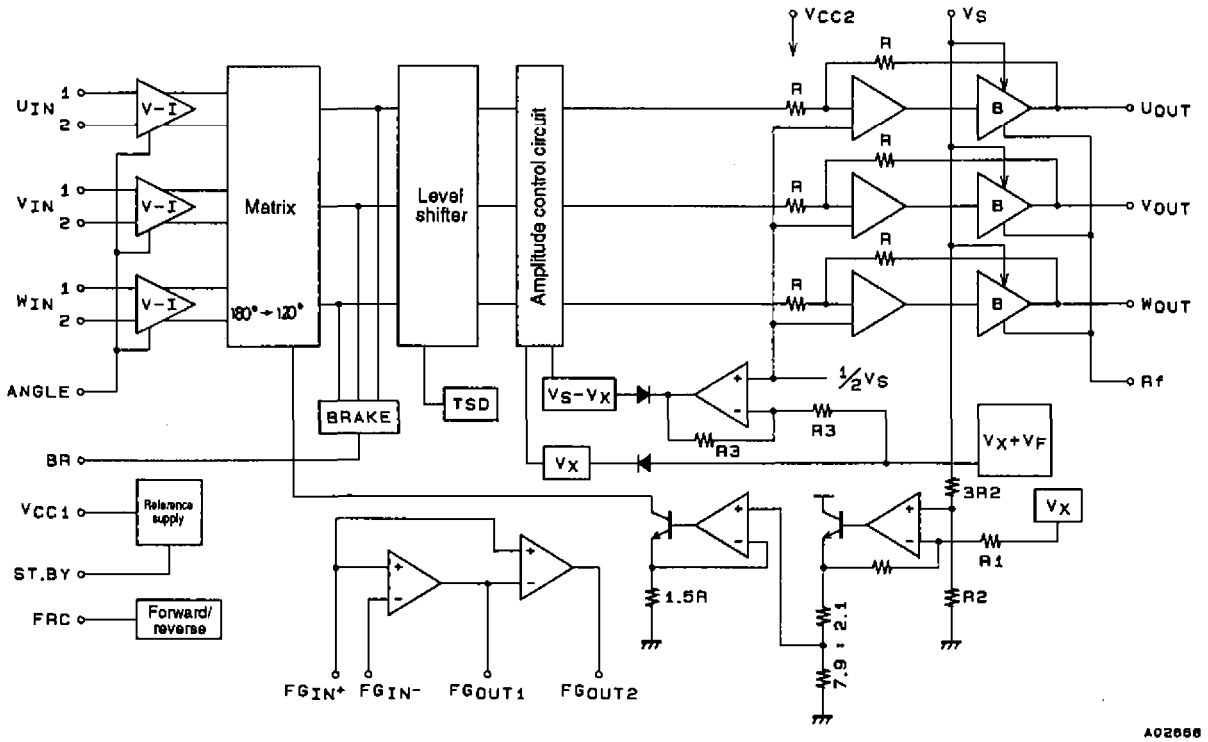
| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Current drain 1 | $I_{CC}1$ | $V_{BR}$ = 5 V | | 3.0 | 5.0 | mA |
| Current drain 2 | $I_{CC}2$ | $V_{BR}$ = 5 V | | 6.5 | 10.0 | mA |
| Current drain 3 | $I_S$ | $V_{BR}$ = 5 V, $R_L$ = ∞ | | | 5.0 | mA |
| Quiescent current 1 | $I_{CCOQ}$ | $V_{STBY}$ = 0 V | | | 100 | µA |
| Quiescent current 2 | $I_{SOQ}$ | $V_{STBY}$ = 0 V, $R_L$ = ∞ | | | 150 | µA |
| Output saturation voltage | $V_{O\,(sat)}$ | $I_{OUT}$ = 0.6 A, sink + source | | | 1.7 | V |
| Output transistor breakdown voltage | $V_{O\,(sus)}$ | $I_{OUT}$ = 20 mA, *2 | 12 | | | V |
| Quiescent voltage | $V_{OQ}$ | $V_{BR}$ = 5 V | 1.45 | 1.55 | 1.65 | V |
| Hall amplifier input offset voltage | $V_{H\,offset}$ | *2 | –5 | | +5 | mV |
| Hall amplifier common mode input voltage range | $V_{HCOM}$ | | 1.4 | | 2.8 | V |
| Hall I/O voltage gain | $G_{VHO}$ | Rangle = 8.2 kΩ | 34.5 | 37.5 | 40.5 | dB |
| Brake pin high level voltage | $V_{BRH}$ | | 2.0 | | | V |
| Brake pin low level voltage | $V_{BRL}$ | | | | 0.8 | V |
| Brake pin input current | $I_{BRIN}$ | | | | 120 | µA |
| Brake pin leakage current | $I_{BR\,leak}$ | | | | –30 | µA |
| FRC pin high level voltage | $V_{FRCH}$ | | 2.8 | | | µA |
| FRC pin low level voltage | $V_{FRCL}$ | | | | 1.2 | µA |
| FRC pin input current | $I_{FRCIN}$ | | | | 100 | µA |
| FRC pin leakage current | $I_{FRC\,leak}$ | | | | –30 | µA |
| Upper side residual voltage | $V_{XH}$ | $I_{OUT}$ = 100 mA, $V_{CC}2$ = 6 V, $V_S$ = 2 V | 0.285 | | 0.455 | V |
| Lower side residual voltage | $V_{XL}$ | $I_{OUT}$ = 100 mA, $V_{CC}2$ = 6 V, $V_S$ = 2 V | 0.350 | | 0.440 | V |
| Residual voltage inflection point | $V_S\Delta V_X$ | $I_{OUT}$ = 100 mA, $V_{CC}2$ = 6 V, *2 | | 0.9 | | V |
| Overlap | OL | $V_{CC}2$ = 6 V, $V_S$ = 3 V, $R_L$ = 100 Ω (Y) | 69 | 79 | 89 | % |
| Overlap vertical delta | ΔOL | $V_{CC}2$ = 6 V, $V_S$ = 3 V, $R_L$ = 100 Ω (Y) | –10 | 0 | +10 | % |
| Standby on voltage | $V_{STBYL}$ | *1 | –0.2 | | +0.8 | V |
| Standby off voltage | $V_{STBYH}$ | | 2 | | 5 | V |
| Standby pin bias current | $I_{STBYIN}$ | | | | 100 | µA |
| Thermal protection circuit operating temperature | $T_{TSD}$ | *2 | 150 | 180 | 210 | °C |
| Thermal protection circuit hysteresis | $\Delta T_{TSD}$ | *2 | | 15 | | °C |
| [FG Amplifier] | | | | | | |
| FG amplifier input offset voltage | $V_{FG\,offset}$ | | –8 | | +8 | mV |
| Open loop voltage gain | $G_{VFG}$ | f = 10 kHz | | 43 | | dB |
| Source output saturation voltage | $V_{FG\,OU}$ | $I_O$ = –2 mA | 3.7 | | | V |
| Sink output saturation voltage | $V_{FG\,OD}$ | $I_O$ = 2 mA | | | 1.3 | V |
| Common mode signal rejection ratio | GHR | *2 | | 80 | | dB |
| FG amplifier common mode input voltage range | $V_{FG\,CH}$ | | 0 | | +3.5 | V |
| Phase margin | øM | *2 | | 20 | | deg |
| Schmitt amplifier threshold voltage | $V_{FGS\,SH}$ | VFGin+ = 2.5 V, when VFGout2 goes from high to low | 2.45 | 2.50 | 2.55 | V |
| Schmitt amplifier hysteresis | $V_{FGS\,HIS}$ | VFGin+ = 2.5 V | 20 | 40 | 60 | mV |

Note: 1. The IC goes to the standby state when the standby pin is open.
2. These are design target values and are not measured.
The overlap standard is taken as the test standard without change.

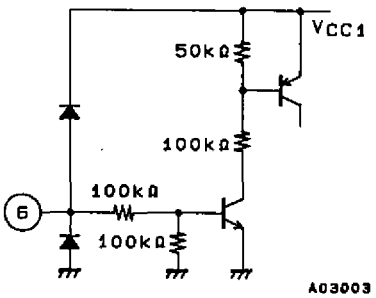
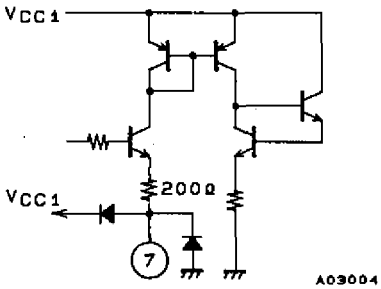
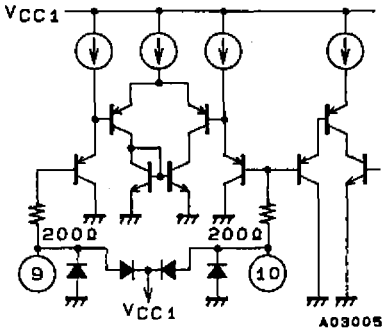
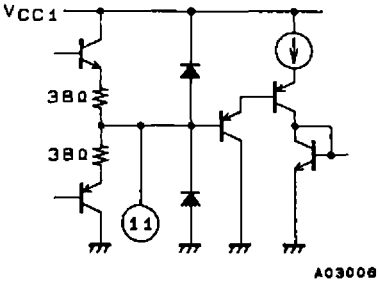
## Pin Assignment




## Internal Equivalent Circuit Block Diagram



## Pin Functions

| Pin No. | Symbol | Pin voltage | Equivalent circuit | Function |
|---|---|---|---|---|
| 3 | $V_S$ | < $V_{CC}2$ | | Supply pin that determines the output amplitude. This pin must be set lower than the $V_{CC}2$ voltage. |
| 4 | $V_{CC}2$ | 4 to 10 V | | Power amplifier system power supply for transistors other than those that drive the motor. Power supply voltage for control blocks other than those provided by $V_{CC}1$. |
| 5 | $V_{CC}1$ | 4 to 6 V | | Power supply voltage for the Hall amplifier, forward/reverse, FG amplifier, and thermal shutdown circuits |
| 6 | ST. BY | H: 2.0 V min<br>L: 0.8 V max<br>(when $V_{CC}1$ is 5 V.) |  | All circuits are turned off by connecting this pin to ground or leaving it open. The current drain is about 0 μA in this mode. Apply 2.0 V or higher for motor drive operation. |
| 7 | ANGLE | |  | Connect a resistor between this pin and ground. The Hall input/output gain can be changed by changing the value of this resistor. |
| 9<br>10 | FGin⁻<br>FGin⁺ | min 0 V<br>max 3.5 V<br>(when $V_{CC}1$ is 5 V.) |  | FG signal input |
| 11 | FGout1 | |  | FG amplifier output |

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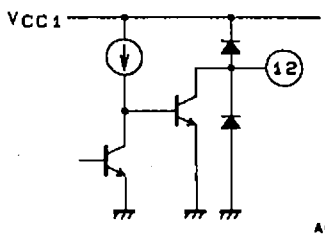
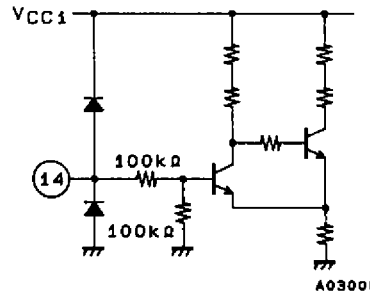
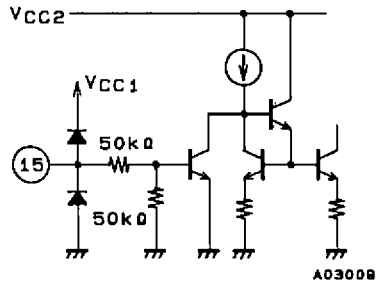
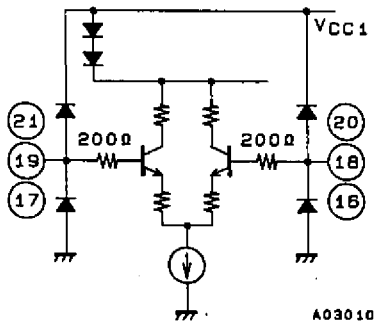
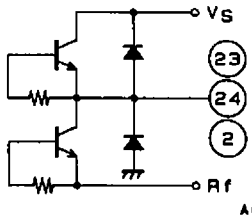
| Pin No. | Symbol | Pin voltage | Equivalent circuit | Function |
|---|---|---|---|---|
| 12 | FGout2 | |  | FG Schmitt amplifier output |
| 14 | FRC | H: 2.8 V min<br>L: 1.2 V max<br>(when $V_{CC}1$ is 5 V.) |  | Motor forward/reverse control<br>Low level: forward<br>(1.2 V or lower: when $V_{CC}1$ = 5 V)<br>High level: reverse<br>(2.8 V or higher: when $V_{CC}1$ = 5 V) |
| 15 | BR | H: 2.0 V min<br>L: 0.8 V max |  | Motor stop control<br>Low level: motor drive (0.8 V or lower)<br>High level: Motor stop (2.0 V or higher) |
| 16<br>17<br>18<br>19<br>20<br>21 | Win2<br>Win1<br>Vin2<br>Vin1<br>Uin2<br>Uin1 | min 1.4 V<br>max 2.8 V<br>(when $V_{CC}1$ is 5 V.) |  | W phase Hall element input pin logic<br>High refers to the state where $W_{IN}1 > W_{IN}2$<br>V phase Hall element input pin logic<br>High refers to the state where $V_{IN}1 > V_{IN}2$<br>U phase Hall element input pin logic<br>High refers to the state where $U_{IN}1 > U_{IN}2$ |
| 22 | Rf | | | Ground for the output transistors |
| 23<br>24<br>2 | Uout<br>Vout<br>Wout | |  | Outputs |
| 1<br>13 | SUB GND<br>GND | | | Ground for all circuits other than the output transistor |

## Truth Table

| | Source → sink | Input | | | Forward/reverse control F/RC |
|---|---|---|---|---|---|
| | | U | V | W | |
| 1 | W phase → V phase<br>V phase → W phase | H | H | L | L<br>H |
| 2 | W phase → U phase<br>U phase → W phase | H | L | L | L<br>H |
| 3 | V phase → W phase<br>W phase → V phase | L | L | H | L<br>H |
| 4 | U phase → V phase<br>V phase → U phase | L | H | L | L<br>H |
| 5 | V phase → U phase<br>U phase → V phase | H | L | H | L<br>H |
| 6 | U phase → W phase<br>W phase → U phase | L | H | H | L<br>H |

Input high: Indicates that the phase 1 input is at least 0.2 V higher than the phase 2 input for each phase.
Input low: Indicates that the phase 1 input is at least 0.2 V lower than the phase 2 input for each phase.
Forward/reverse control: High: 2.8 V to $V_{CC}1$
Low: 0 V to 1.2 V

## Sample Application Circuit