Ordering number : EN4354

Monolithic Digital IC

LB1890M

FDD Spindle Motor Driver

Overview

The LB1890M is a 3-phase DD motor driver IC and is an ideal FDD spindle motor driver for 3.5 inch applications.

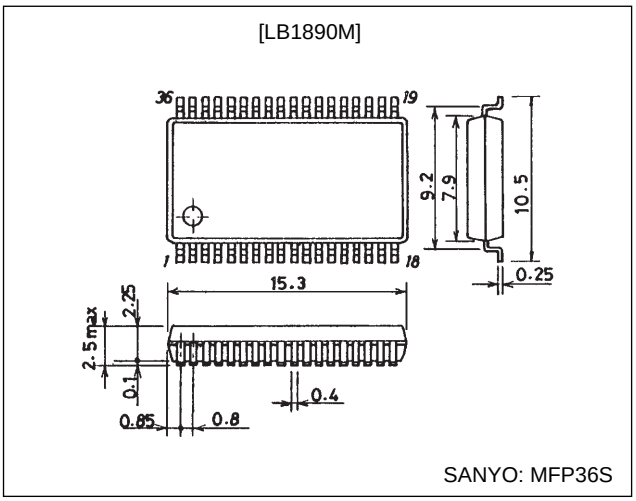
Functions and Features

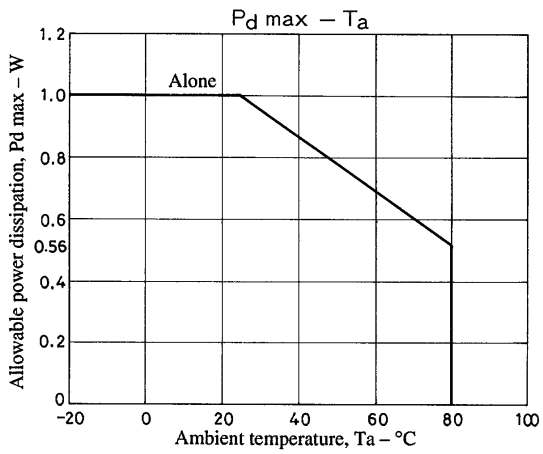
- Three phase total wave linear driver
- Eliminates need for output electrolytic capacitor (however, depending on the motor, this may not apply)
- On-chip digital speed control
- Start/stop circuit
- Current limiter circuit
- On-chip index comparator (single HYS)
- On-chip index delay circuit
- AGC circuit
- Temperature protection circuit

Package Dimensions

unit: mm

3129-MFP36S





Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		7.0	V
Maximum output current	I_O max1	t≤0.5	1.0	A
Steady Maximum output current	I_O max2		0.7	A
Allowable power dissipation	Pd max	Independent IC	1	W
Operating temperature	Topr		–20 to +80	°C
Storage temperature range	Tstg		–40 to +150	°C

Allowable Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range	V_{CC}		4.2 to 6.5	V

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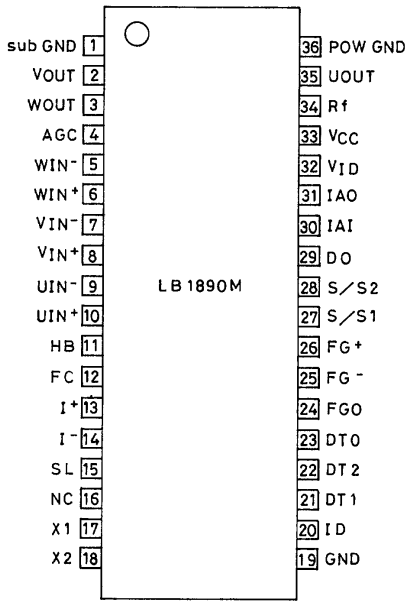
Electrical Characteristics at Ta = 25°C, V_{CC} = 5V

Parameter	Symbol	Conditions	Ratings			Unit	Note
			min	typ	max		
Current drain	$I_{CCO}1$	V_{CC} = 5.0V (Stop)			0.2	mA	
	$I_{CC}1$	V_{CC} = 5.0V (Steady)		20	30	mA	
Time changeover bias current	I_{SL}				0.4	mA	
Time changeover input voltage 1	V_{SLL}		0		0.8	V	
Time changeover input voltage 2	V_{SLH}		2.0		V_{CC}	V	
S/S1 bias current	$I_{S/S1}$				0.4	mA	
S/S1 start voltage	$V_{S/S1}$		2.0		V_{CC}	V	
S/S1 stop voltage	$V_{S/S1}$		0		0.8	V	
S/S2 bias current	$I_{S/S2}$				0.1	mA	
S/S2 start voltage	$V_{S/S2}$		0		0.8	V	
S/S2 stop voltage	$V_{S/S2}$		2.0		V_{CC}	V	
Hall-effect bias amplifier input current	I_{HB}				20	µA	
In-phase input voltage range	Vh		2.2		V_{CC} – 0.7	V	
Differential input voltage range	Vdif		70		250	mVp-p	*2
Input offset voltage	Vho				±1.0	mV	*1
Hall-Effect output voltage	V_H	I_H = 5mA		1.5	1.8	V	
Leak current	I_{HL}	Stop			±10	µA	
Output saturation voltage (Sink plus source)	Vsat1	I_O = 0.35A, V_{CC} = 4.2V		1.2	1.4	V	
	Vsat2	I_O = 0.70A, V_{CC} = 4.2V		1.5	2.0	V	
Output leak current	I_{OL}				±1.0	mA	
Current limiter	Vref1		0.27	0.30	0.33	V	
Control amplifier voltage gain	G_C			–6		dB	
Voltage gain phase differential	$\triangle G_C$				±1	dB	
Integrated amplifier internal reference voltage	Vref2			$V_{CC}/2$		V	
Integrated amplifier bias current	Iib				±1	µA	
Integrated output voltage amplitude	Vi^+	Ii = –0.5 mA with reference of Vref2		0.75		V	
	Vi^-	Ii = 0.5 mA with reference of Vref2		–1.4		V	
Gain band width				1000		kHz	*1
FG amplifier input voltage	V_{FG}		5		100	mVp-p	
FG amplifier voltage gain	G_{FG}	Open loop		60		dB	*1
FG amplifier input offset	$V_{FG}0$				±10	mV	
FG amplifier internal reference voltage	V_{FGB}		2.20	2.50	2.80	V	
Schmitt hysteresis width	△Vsh1	"H" → "L"		25		mV	*1
	△Vsh2	"L" → "H"		25		mV	*1
Schmitt input operation level	Vsh		1		V_{CC} –1	V	
Speed disk recount number	N			992			
Disk recount out "L" level voltage	V_{DL}	I_D = –0.5mA			0.3	V	
Disk recount out "H" level voltage	V_{DH}	I_D = 0.5mA	V_{CC} –0.4			V	
Disk recount out leak current	I_{DI}				±1.0	µA	
Disk recount operation frequency	F_D				1.0	MHz	*1
Oscillation range	F_{OSC}				1.0	MHz	*1
Index bias current	I_{IDB}				±10	µA	
In-phase input voltage range	V_{ID}		1.5		V_{CC} –0.5	V	
Hysteresis setting current range	I_{IDO}		5	10	15	µA	
Index output "L" level voltage	V_{IDL}	V_{ID} = 5V			0.4	V	
Index output "H" level voltage	V_{IDH}	V_{ID} = 5V	4.5			V	
Break-down voltage	V_{DLDC}	V_{ID} = 5V		2.50		V	
Delay output "L" level voltage	V_{DLL}	V_{ID} = 5V			0.4	V	
Delay output "H" level voltage	V_{DLH}	V_{ID} = 5V	4.5			V	
Excessive heat protected operating temperature	TSD		150	180		°C	*1
Hysteresis width	△TSD			40		°C	*1

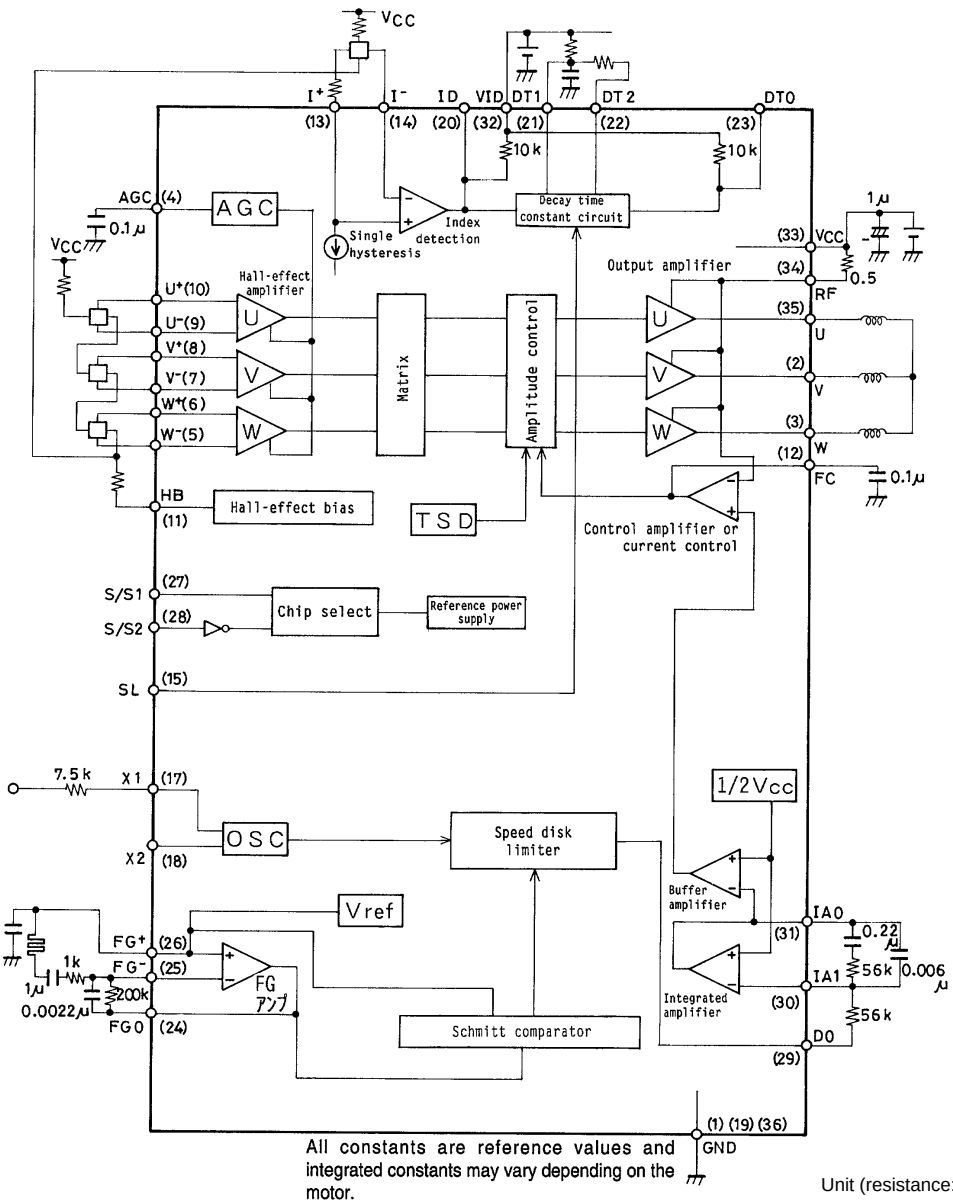
Note: *1) Marked values (*1) are guaranteed by the design itself and therefore do not require measurement.
*2) When hall-effect input becomes larger, kick-back occurs to the output waveform and for this reason, 200 m Vp-p or less is recommended.

Pin Assignment



[Top view]

Block Diagram

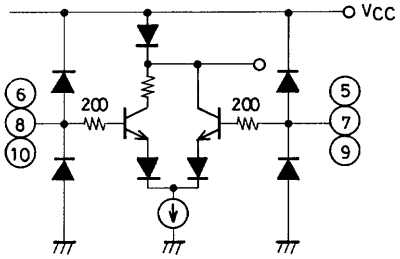
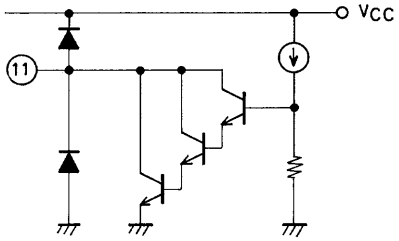
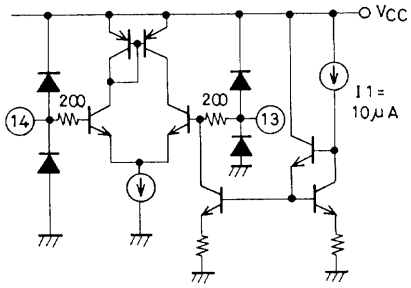
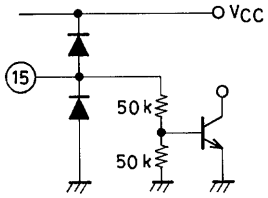
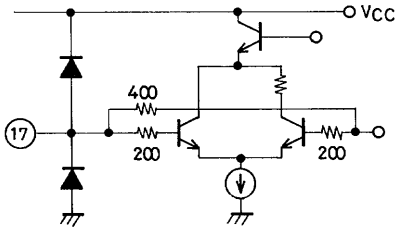
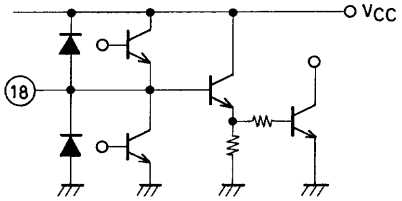


All constants are reference values and integrated constants may vary depending on the motor.

Unit (resistance: Ω, capacitance: F)

Pin Description

Unit (resistance: Ω)

Pin No.	Symbol	Pin voltage	Equivalent circuit	Pin description
5 6 7 8 9 10	W^- W^+ V^- V^+ U^- U^+	2.2V min V_{CC} –0.7V max		• W-phase hall-effect input pin. $W^+ > W^-$ is established when logic is at an “H” level. • V-phase hall-effect input pin. $V^+ > V^-$ is established when logic is at an “H” level. • U-phase hall-effect input pin. $U^+ > U^-$ is established when logic is at an “H” level.
11	HB	1.5V typ (I_H = 5mA)		• Minus pin for hall-effect bias. When stopped, switches open and hall-effect bias severs.
12	FC			• Frequency characteristics revision pin By installing a capacitor between this pin and GND, close-loop oscillation for the current control system halts.
13 14	I^+ I^-	1.5V min V_{CC} –0.5V max		• Index input pin. When the I^+ pin is at an “L” level, I1 operates with the fixed current of I1 = 10 μA and when at an “H” level, I1 does not flow. Hysteresis width is determined by the resistor attached externally to the I^+ pin.
15	SL	“L”: 0.8V max “H”: 2.0V min		• Time changeover pin. 1 : 1.2 “L” level : “H” level
17	X1			• Reference clock generating pin.
18	X2			
19	GND			• Ground pin. Grounded as with pins 1 and 36.

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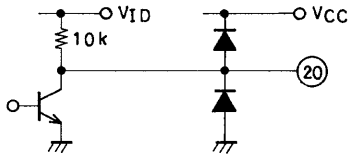
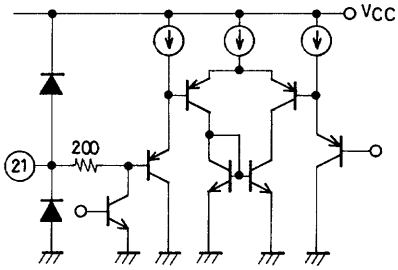
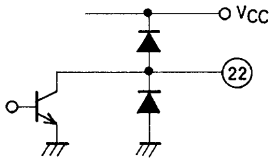
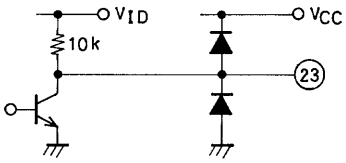
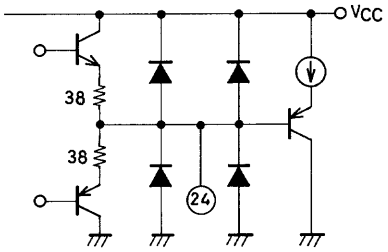
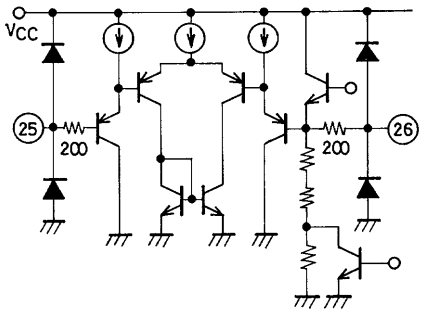
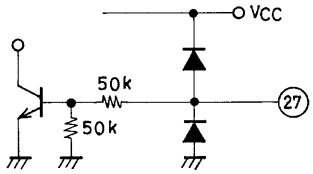
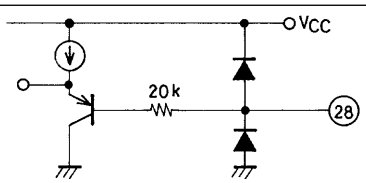
Unit (resistance: Ω)

Pin No.	Symbol	Pin voltage	Equivalent circuit	Pin description
20	ID	"L": 0.4V max "H": 4.5V min (When V_{ID} equals 5 V)		• Index pulse output pin.
21	DT1			• Pin connecting the external CR for the delay time constant circuit.
22	DT2			• Break-down current setting pin for the delay time constant circuit.
23	DTO	"L": 0.4V max "H": 4.5V min (When V_{ID} equals 5 V)		• Index delay pulse output pin.
24	FG0			• FG amplifier output pin.
25	FG⁻			• FG amplifier negative input pin.
26	FG⁺	2.48V (When V_{ID} equals 5 V)		• FG amplifier positive input pin. Generates reference voltage within IC.
27	S/S1	"L": 0.8V max "H": 2.0V min		• Start/stop changeover pin. "H" level active.
28	S/S2	"L": 0.8V max "H": 2.0V min		• Start/stop changeover pin. "L" level active.

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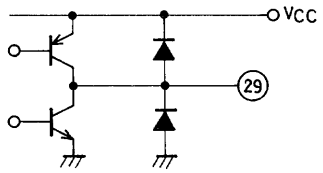
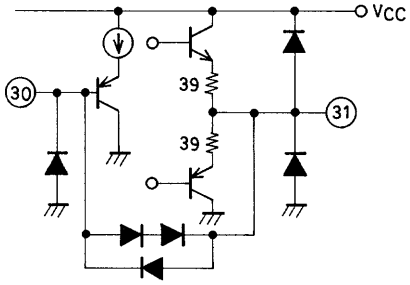
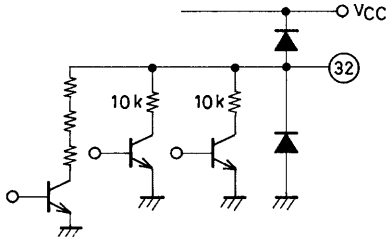
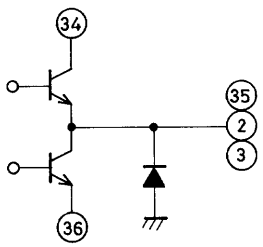
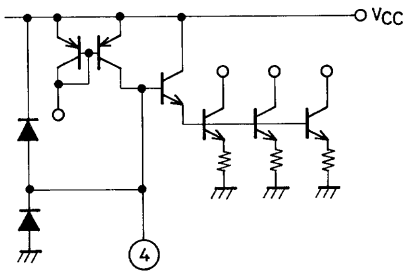
Unit (resistance: Ω)

Pin No.	Symbol	Pin voltage	Equivalent circuit	Pin description
29	DO			• Speed discriminator output pin.
30	IAI			• Integrated amplifier input pin.
31	IAO			• Integrated amplifier output pin.
32	VID			• Index pulse output and index delay pulse output power supply pin. For applications when V_{CC} equals 5 V, V_{CC} = V_{ID} = 5 V.
33	V_{CC}			• Total power supply voltage pin except for V_{ID}. Voltage must be stable and free of ripple and noise interference.
34	R_f			• Output current detection pin. By installing an R_f resistor between this pin and V_{CC}, output current is detected as voltage. Voltage detection at this pin activates the current limiter.
35	U_{OUT}			• U-phase output pin.
36	Pow GND			• Output transistor ground pin.
1	Sub GND			• Ground pin. Grounded as with pins 19 and 36.
2 3	V_{OUT} W_{OUT}			• V-phase output pin. • W-phase output pin.
4	AGC			• AGC pin. Controls hall-effect amplifier gain in response to hall-effect input frequency.

Truth Table

	Source → Sink	Hall-Effect Input		
		U	V	W
1	V-phase → W-phase	H	H	L
2	V-phase → U-phase	L	H	L
3	W-phase → U-phase	L	H	H
4	W-phase → V-phase	L	L	H
5	U-phase → V-phase	H	L	H
6	U-phase → W-phase	H	L	L

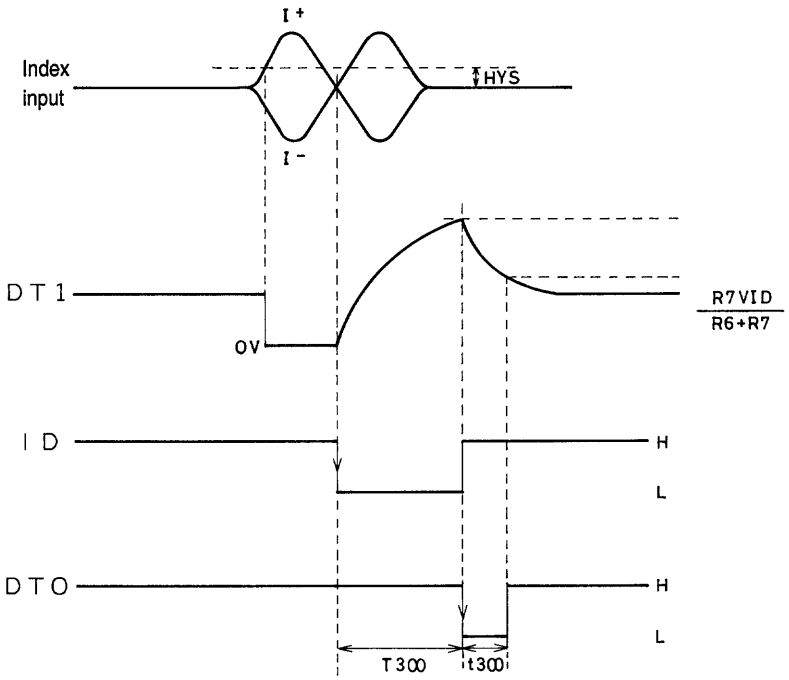
When an “H” level exists for hall-effect input,

$U^+ > U^-$

$V^+ > V^-$

$W^+ > W^-$

Index and Timing Chart



When SL equals an “H” level,

- $T' \approx 0.693CR6$
- $t' \approx \frac{CR6R7}{R6 + R7}\left\{0.405 + 1n\left(\frac{R6 - R7}{R6 - 2R7}\right)\right\}$

When SL equals an “L” level,

- $T' \approx 0.577CR6$
- $t' \approx \frac{CR6R7}{R6 + R7}\left\{0.522 + 1n\left(\frac{0.781R6 - R7}{R6 - 2R7}\right)\right\}$

Using only the ID pulse involves shorting DT1 and DT2.