

SANYO	No. 4863	LC7536R
		High Breakdown Voltage Serial Control Electronic Volume Control

Overview

The LC7536R is an electronic volume control IC that implements volume and balance functions with a minimum number of external components.

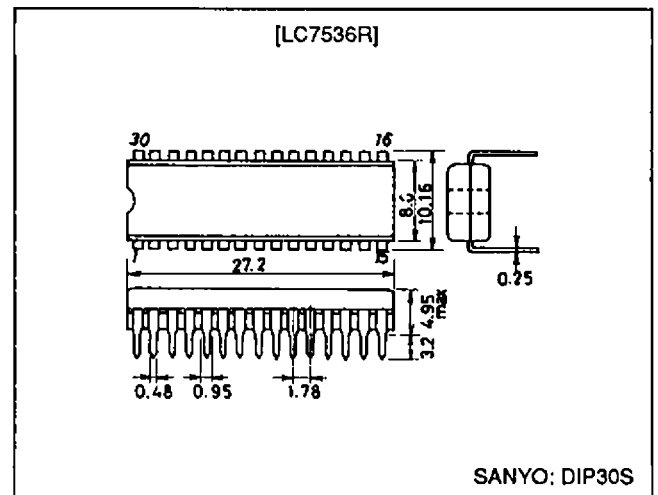
Features

- The LC7536R is controlled by a 3-wire (DI, CL and CE) serial data control scheme that can be shared with other ICs. Up to two LC7536Rs can be used on the same bus by using the S (select) pin.
- Eighty positions in 1 dB steps plus mute ($-\infty$), maximum attenuation is over 80 dB
- Input impedance (5 dB inputs): 47 k Ω (typical)
- High breakdown voltage: ± 16 V

Package Dimensions

unit: mm

3047A-DIP30S



Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$, $V_{SS} = 0$ V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD \text{ max}}$	$V_{EE} \leq V_{SS} < V_{CC} < V_{DD}$	$V_{SS} \text{ to } V_{SS} + 18$	V
	$V_{EE \text{ max}}$	$V_{EE} \leq V_{SS} < V_{CC} < V_{DD}$	$V_{SS} - 18 \text{ to } V_{SS}$	V
	$V_{CC \text{ max}}$	$V_{EE} \leq V_{SS} < V_{CC} < V_{DD}$	$V_{SS} \text{ to } V_{SS} + 7$	V
Input voltage	V_{I1}	CL, DI, CE	0 to $V_{DD} + 0.3$	V
	V_{I2}	IN1, IN2	$V_{EE} - 0.3 \text{ to } V_{DD} + 0.3$	V
	V_{I3}	S	$V_{CC} - 0.3 \text{ to } V_{DD} + 0.3$	V
Allowable power dissipation	$P_d \text{ max}$	$T_a \leq 75^\circ\text{C}$	250	mW
Operating temperature	T_{opr}		$-30 \text{ to } +75$	$^\circ\text{C}$
Storage temperature	T_{stg}		$-40 \text{ to } +125$	$^\circ\text{C}$

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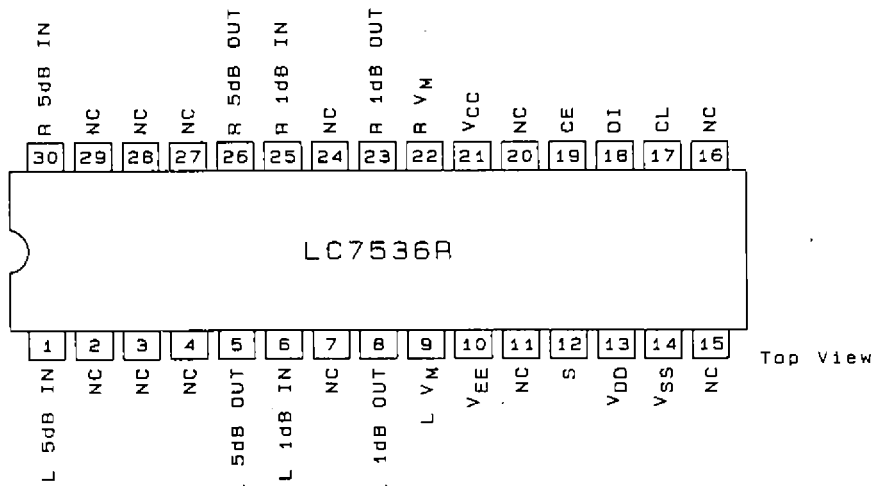
Allowable Operating Ranges at Ta = 25°C, VSS = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V _{DD}		V _{CC} + 4.5		16	V
	V _{EE}		-16		0	V
	V _{CC}		4.5	5	5.5	V
Input high level voltage	V _{IH1}	CL, DI, CE	0.8 V _{CC}		V _{CC}	V
Input low level voltage	V _{IL1}	CL, DI, CE	V _{SS}		0.2 V _{CC}	V
Input high level voltage	V _{IH2}	S	$0.8 \times (V_{DD} - V_{CC}) + V_{CC}$		V _{DD}	V
Input low level voltage	V _{IL2}	S	V _{CC}		$0.2 \times (V_{DD} - V_{CC}) + V_{CC}$	V
Input pulse width	t _{pw}	CL	1			μs
Setup time	t _{set up}	CL, DI, CE	1			μs
Hold time	t _{hold}	CL, DI, CE	1			μs
Operating frequency	f _{opg}	CL			500	kHz
Input signal amplitude	V _{IN}	IN1, IN2	V _{EE}		V _{DD}	V
Input leakage current	I _{IN}	CL, DI, CE, S	-10		+10	μA

Electrical Characteristics at Ta = 25°C, VSS = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Current drain	I _{DD}				1	mA
	I _{CC}				1	mA
Output off leakage current	I _{OFF}	IN1, IN2, V _{M1} , V _{M2} , CT1, CT2, OUT1, OUT2, analog switch off	-10		+10	μA
Total harmonic distortion	THD1	V _{IN} = 1 Vrms, f = 1 kHz, V _{DD} - V _{EE} = 32 V, V _R = max		0.004		%
	THD2	V _{IN} = 0.1 Vrms, f = 1 kHz, V _{DD} - V _{EE} = 32 V, V _R = max		0.02		%
Inter-channel crosstalk	C _T	OUT1 and OUT2, with a 20 kHz 1 Vrms input to one channel		-75	-60	dB
Output at maximum attenuation	V _O	f = 20 kHz, V _{IN} = 1 Vrms		-98		dB

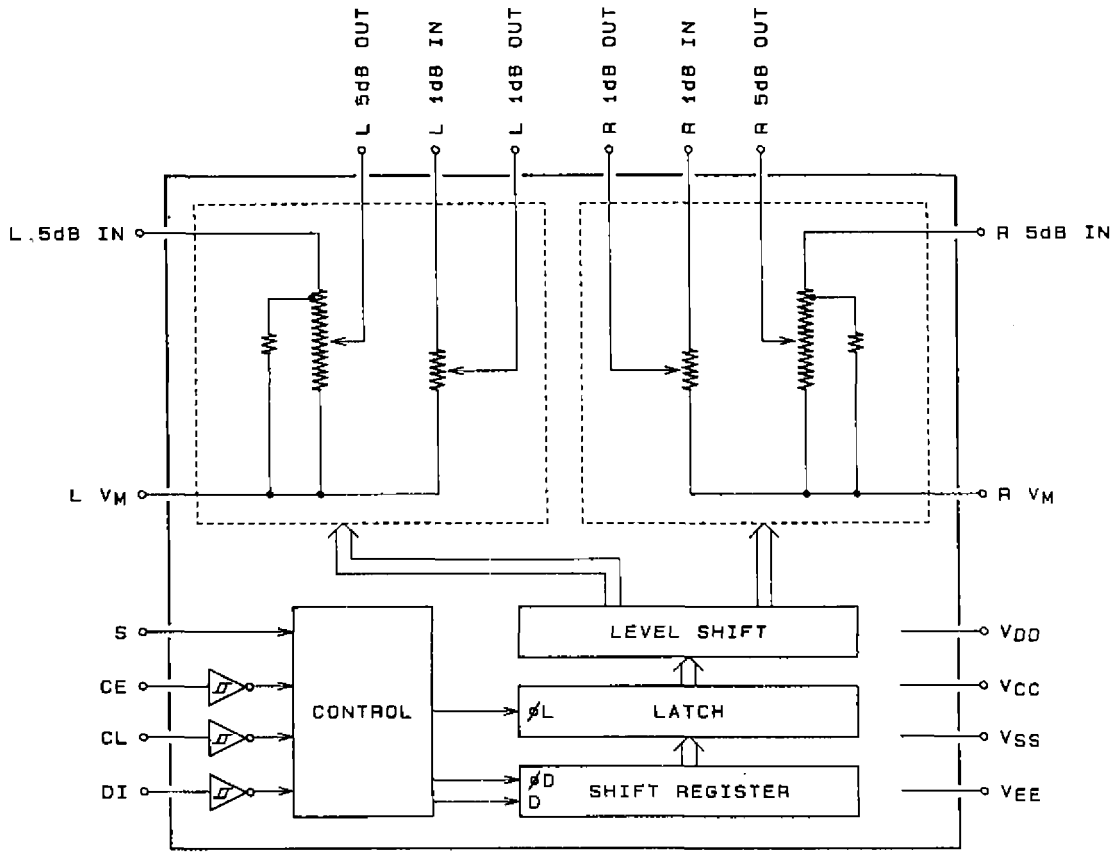
Pin Assignment



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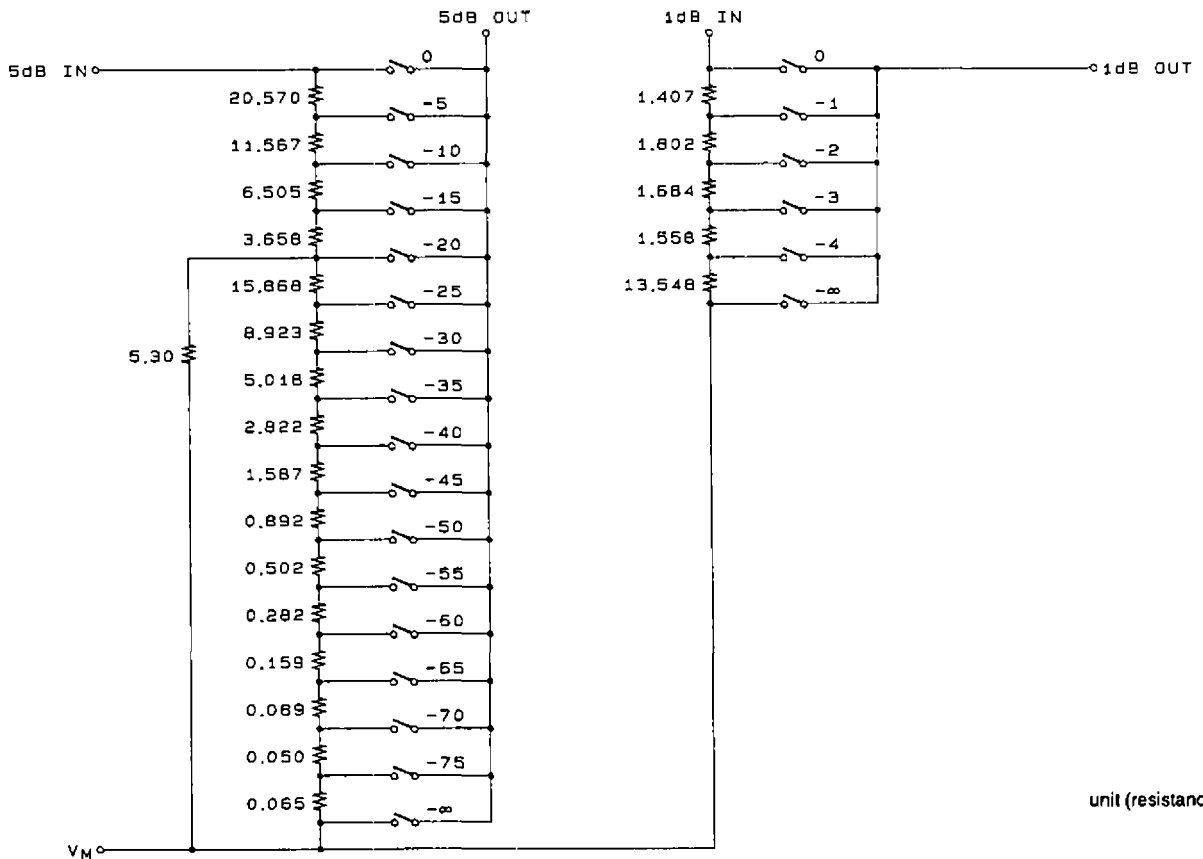
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Equivalent Circuit Block Diagram



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Internal Resistor Equivalent Circuit Diagram

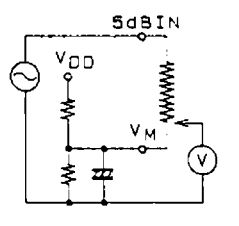


unit (resistance: KΩ)

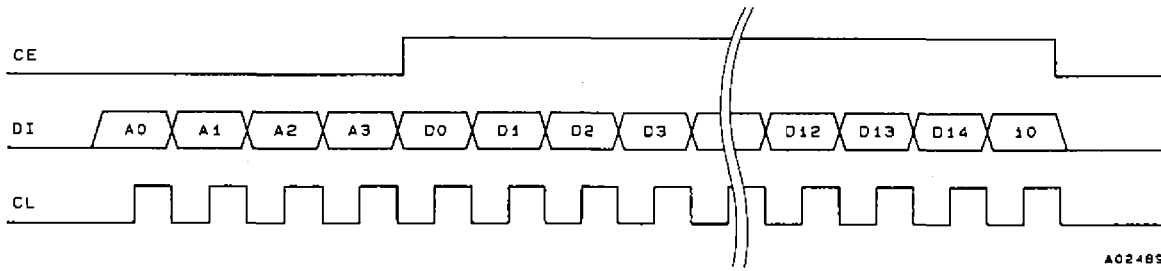
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Pin Functions

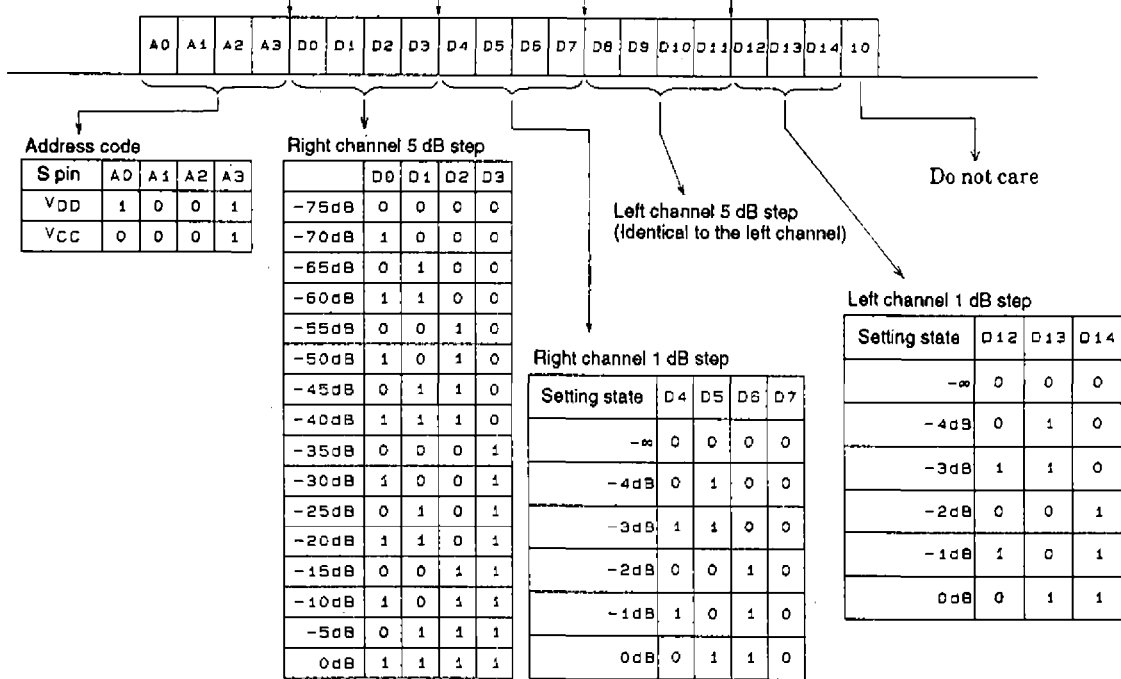
Pin No.	Symbol	Function	Note
1	L 5dBIN	Inputs to the 5 dB step attenuator. Must be driven by low impedance outputs.	
30	R 5dBIN		
3	NC	No connection	
4	NC		
28	NC		
27	NC		
5	L 5dBOUT	Outputs from the 5 dB step attenuator. Outputs should be received by a load of about 1 MΩ.	
26	R 5dBOUT		
6	L 1dBIN	Inputs to the 1 dB step attenuator. Must be driven by low impedance outputs.	
25	R 1dBIN		
8	L 1dBOUT	Outputs from the 1 dB step attenuator. Outputs should be received by a load in the range 47 kΩ to 1 MΩ.	
23	R 1dBOUT		
9	L V _M	Volume control common connections. The impedance of the pattern connected to these pins should be lowered as far as possible. Since LV _M , RV _M and V _{SS} are not connected internally, they should be connected externally according to their respective specifications. In particular, when a single-sided power supply is used, the capacitor connected between V _M and V _{SS} appears as the residual resistance when the volume is attenuated. Thus care is required when selecting the value for this capacitor.	
22	R V _M		
12	S	Selection pin for the address code in the data format. When this pin is connected to V _{DD} , the LC7536R will accept data when the address code is 9 and when connected to V _{CC} , the LC7536R will accept data when the address code is 8.	
17	CL	Inputs for controlling the LC7536R from serial data. Signals should have an amplitude of 0 to 5 V.	
18	DI		
19	CE		
10	V _{EE}	Power supply connections. Do not bring up the V _{CC} voltage before the V _{DD} voltage when powering up the LC7536R.	
13	V _{DD}		
14	V _{SS}		
21	V _{CC}		
2, 7, 11, 15, 16, 20, 24, 29	NC	No connection	

Data Format

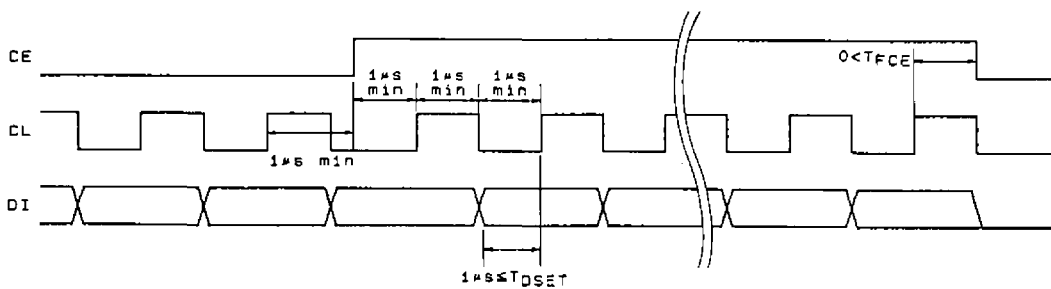


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Data consists of a total of 20 bits.



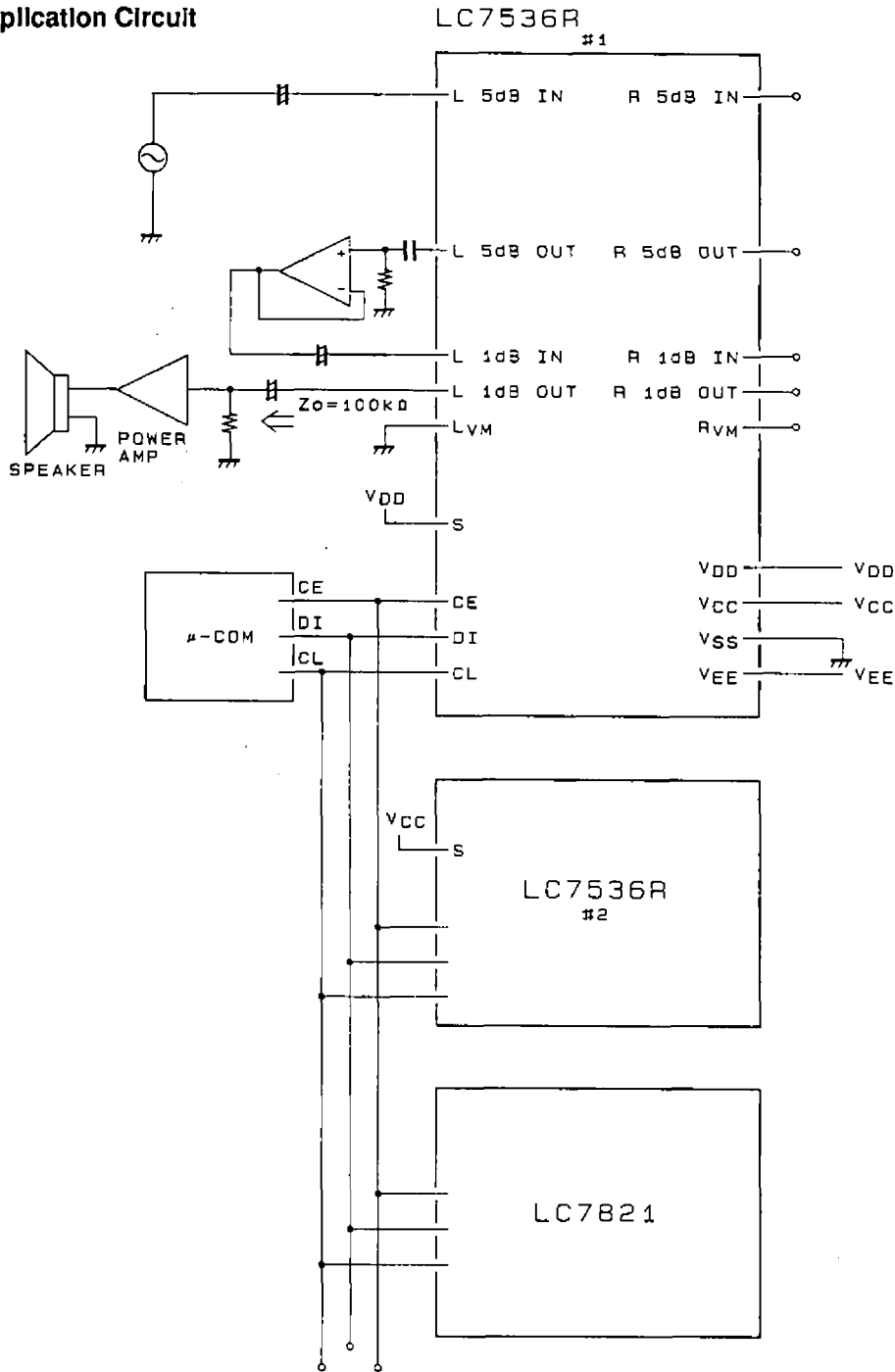
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Sample Application Circuit



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