Ordering number : EN *5194D

CMOS LSI (P-sub)

LC4104C

LCD Dot Matrix Segment Driver for STN Displays

Preliminary

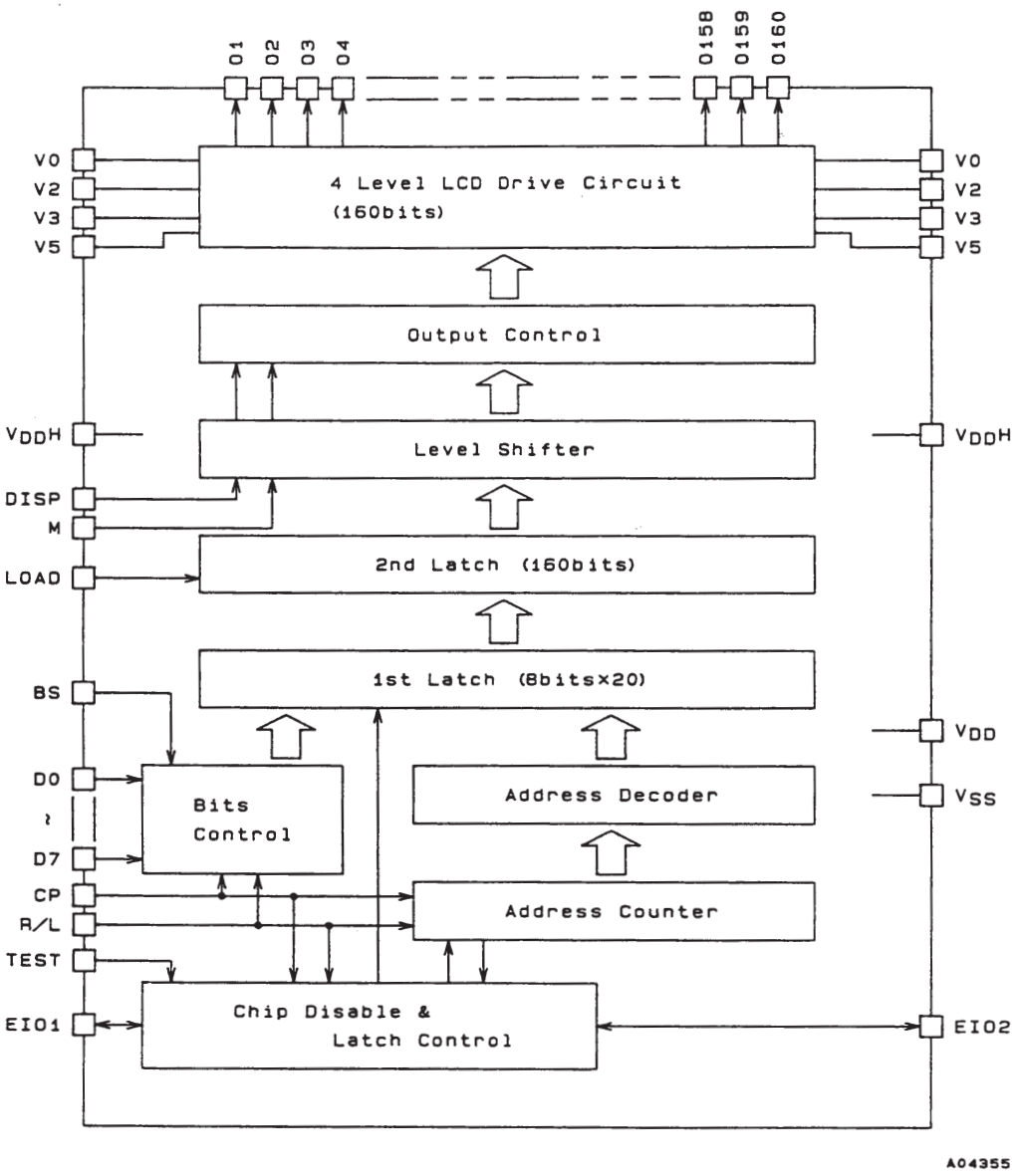
Overview

The LC4104 is a segment driver LSI for large-scale dot matrix LCD displays. The LC4104 latches 160-bits of display data transferred from the controller over a 4- or 8-bit parallel interface and generates the LCD drive signals. In conjunction with the LC4102 common driver, the LC4104 forms a chip set that can drive large-screen LCD panels.

Features

- High-voltage CMOS (P-sub) process
- LCD drive voltage: 36 V
- Logic system power-supply voltage: 2.7 to 5.5 V
- Maximum fcp: 12 MHz (V_{DD} = 5 V ±10%),
  10 MHz (V_{DD} = 2.7 to 4.5 V)
- Slim chip (The output pads are located along one of the long sides.)
- Parallel input circuit can be switched between 4 and 8 bits.
- Output directionality switching
- DISPOFF function (Holds the LCD drive voltage at a fixed level.)
- Display duty ratios: 1/160 to 1/480
- Appropriate for COG (chip on glass) mounting. (A gold bump structure is adopted in the pad areas.)
- LC4104C: Chip product

Block Diagram



Specifications

The following electrical characteristics apply when sealed in a Sanyo standard PGA-208 package.

Absolute Maximum Ratings at V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Maximum supply voltage	V_{DD} max		–0.3		7	V
Maximum supply voltage	V_{DDH} max		–0.3		40	V
Maximum supply voltage	V_{SS} max		–0.3		+0.3	V
Input voltage	V_{IN}	D0 to D7, LOAD, CP, R/L, TEST, DISP, M, EIO1, EIO2, BS	–0.3		V_{DD} + 0.3	V
Input voltage	V0, V2	V0, V2	V_{DDH} – 7		V_{DDH} + 0.3	V
Input voltage	V3	V3	–0.3		V_{SS} + 7	V
Input voltage	V5	V5	–0.3		+0.3	V
Operating temperature	Topr		–20		+75	°C
Storage temperature	Tstg		–55		+125	°C

Note: V0, V2, V3, and V5 must obey the following inequalities: $V_{DDH} \geq V0 \geq V2 \geq V_{DDH} - 7$ V, and 7 V ≥ V3 ≥ V5 ≥ V_{SS}.

Allowable Operating Ranges at Ta = –20 to +75°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}		2.7		5.5	V
Supply voltage	V_{DDH}		20		36	V
Supply voltage	V_{SS}			0		V
Input high-level voltage	V_{IH}	D0 to D7, LOAD, CP, R/L, M, TEST, DISP, BS, EIO1, EIO2	0.8 V_{DD}		V_{DD}	V
Input low-level voltage	V_{IL}	D0 to D7, LOAD, CP, R/L, M, TEST, DISP, BS, EIO1, EIO2	0		0.2 V_{DD}	V
Input voltage	V0, V2	V0, V2	V_{DDH} – 7		V_{DDH}	V
Input voltage	V3	V3	0		V_{SSH} + 7	V
Input voltage	V5	V5		0		V

Note: V0, V2, V3, and V5 must obey the following inequalities: $V_{DDH} \geq V0 \geq V2 \geq V_{DDH} - 7$ V, and $7 \text{ V} \geq V3 \geq V5 \geq V_{SS}$.
At power on: First turn on the logic system power supply and then turn on the high-voltage system power supply.
At power off: First turn off the high-voltage system power supply and then turn off the logic system power supply.

Allowable Operating Ranges at Ta = –20 to +75°C, V_{SS} = 0 V, V_{DD} = 5 V ± 10%

Parameter	Symbol	Conditions	min	typ	max	Unit
CP clock frequency	fcp	CP			12	MHz
High-level load pulse width	tw (ldH)	LOAD	50			ns
High-level clock pulse width	tw (cpH)	CP	20			ns
Low-level clock pulse width	tw (cpL)	CP	20			ns
LOAD/CP setup time	tsu (ld)	LOAD, CP	100			ns
LOAD/CP hold time	tho (ld)	LOAD, CP	200			ns
DATA/CP setup time	tsu (cp)	CP, D0 to D7	10			ns
DATA/CP hold time	tho (cp)	CP, D0 to D7	10			ns
EIO input setup time	tsu (ei)	CP, EIO1, EIO2	24			ns
Clock rise time	tr	LOAD, CP*			50	ns
Clock fall time	tf	LOAD, CP*			50	ns

Note: * The clock rise time (tr) and fall time (tf) must obey inequalities ① and ② below.

① : $\text{tr, tf} < \dfrac{\dfrac{1}{\text{fcp}} - \text{tw (cph)} - \text{tw (cpl)}}{2}$

② : tr, tf ≤ 50 ns

Allowable Operating Ranges at Ta = –20 to +75°C, V_{SS} = 0 V, V_{DD} = 2.7 to 4.5 V

Parameter	Symbol	Conditions	min	typ	max	Unit
CP clock frequency	fcp	CP			10	MHz
High-level load pulse width	tw (ldH)	LOAD	50			ns
High-level clock pulse width	tw (cpH)	CP	37			ns
Low-level clock pulse width	tw (cpL)	CP	37			ns
LOAD/CP setup time	tsu (ld)	LOAD, CP	100			ns
LOAD/CP hold time	tho (ld)	LOAD, CP	200			ns
DATA/CP setup time	tsu (cp)	CP, D0 to D7	35			ns
DATA/CP hold time	tho (cp)	CP, D0 to D7	35			ns
EIO input setup time	tsu (ei)	CP, EIO1, EIO2	30			ns
Clock rise time	tr	LOAD, CP*			50	ns
Clock fall time	tf	LOAD, CP*			50	ns

Note: * The clock rise time (tr) and fall time (tf) must obey inequalities ① and ② below.

① : $\text{tr, tf} < \dfrac{\dfrac{1}{\text{fcp}} - \text{tw (cph)} - \text{tw (cpl)}}{2}$

② : tr, tf ≤ 50 ns

Electrical Characteristics at Ta = –20 to +75°C, V_{DD} = 2.7 to 5.5 V, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Input high-level current	I_{IH}	$V_{IN} = V_{DD}$: D0 to D7, LOAD, CP, R/L, M, DISP, EIO1, EIO2, BS, TEST			5	µA
Input low-level current	$I_{IL}1$	$V_{IN} = V_{SS}$: D0 to D7, LOAD, CP, R/L, M, TEST, DISP, EIO1, EIO2, BS	–5			µA
	$I_{IL}2$	$V_{IN} = V_{SS}$: TEST	–500			
Output high-level voltage	V_{OH}	I_O = –0.4 mA: EIO1, EIO2	V_{DD} – 0.4		V_{DD}	V
Output low-level voltage	V_{OL}	I_O = 0.4 mA: EIO1, EIO2	V_{SS}		0.4	V
Output on resistance	R_{OUT}	V_{DDH} = 36 V*1, V0 – V_O = 0.5 V, V2 – V_O = 0.5 V, V_O – V3 = 0.5 V, V_O – V5 = 0.5 V: O1 to O160		1	3	kΩ
Current drain	I_{DD}	V_{DD} = 2.7 to 5.5 V			5.0	mA
	I_{DDH}	V_{DD} = 2.7 to 5.5 V, V_{DDH} = 32 V*2,			2.0	mA
		V_{DD} = 5 V ± 10%, V_{DDH} = 36 V			2.0	mA
	I_{ST}	*3			500	µA

Note: 1. V_O is the voltage applied for an on output, V0 = V_{DDH}, V2 = 18/20 (V_{DDH} – V_{SS}), V3 = 2/20 (V_{DDH} – V_{SS}), V5 = V_{SS}
2. LOAD = 28 kHz, CP = 10 MHz, M = 75 Hz
Alternatively: No output load and with the inputs $V_{IH} = V_{DD}$ and $V_{IL} = V_{SS}$.
3. The current drain in standby mode. Note that the EIOn pins must be held at V_{DD}.

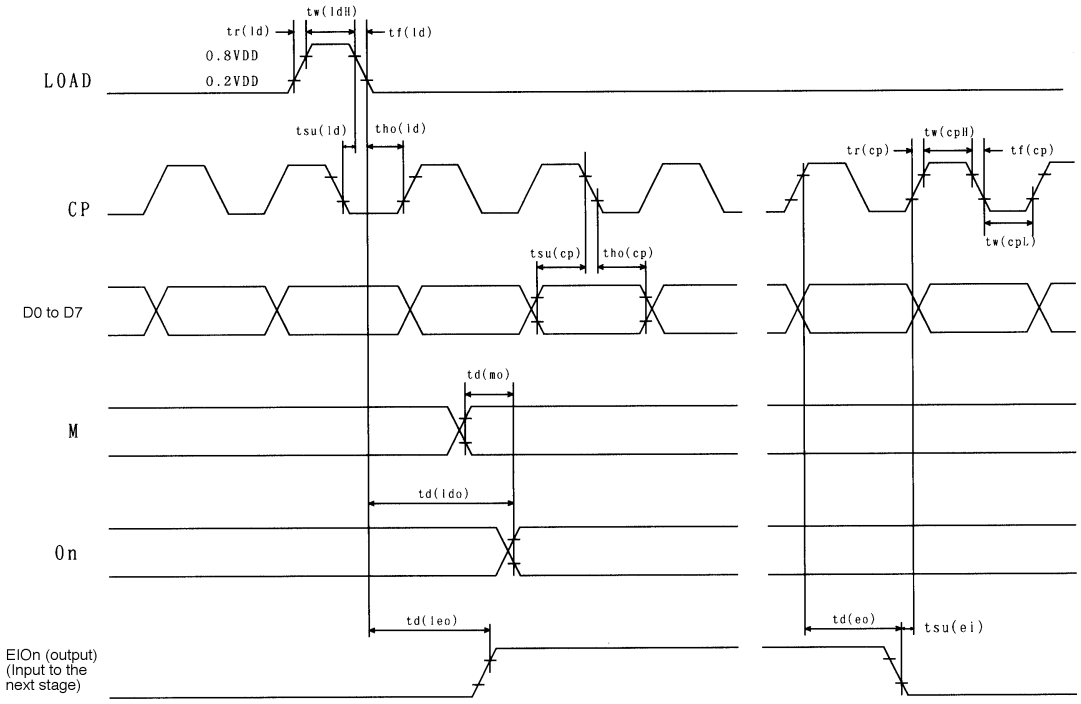
Switching Characteristics at Ta = –20 to +75°C, V_{SS} = 0 V, V_{DD} = 5 V ± 10%

Parameter	Symbol	Conditions	min	typ	max	Unit
EIO output delay time	td (eo)	30 pF capacitive load: CP, EIO1, EIO2			40	ns
LD/EIO output delay time	td (leo)	30 pF capacitive load: LOAD, EIO1, EIO2			70	ns
LOAD/on delay time	td (ldo)	100 pF capacitive load: LOAD, O1 to O160			700	ns
M/on delay time	td (mo)	100 pF capacitive load: M, O1 to O160			700	ns

Switching Characteristics at Ta = –20 to +75°C, V_{SS} = 0 V, V_{DD} = 2.7 to 4.5 V

Parameter	Symbol	Conditions	min	typ	max	Unit
EIO output delay time	td (eo)	30 pF capacitive load: CP, EIO1, EIO2			80	ns
LD/EIO output delay time	td (leo)	30 pF capacitive load: LOAD, EIO1, EIO2			130	ns
LOAD/on delay time	td (ldo)	100 pF capacitive load: LOAD, O1 to O160			3	µs
M/on delay time	td (mo)	100 pF capacitive load: M, O1 to O160			3	µs

Timing Chart

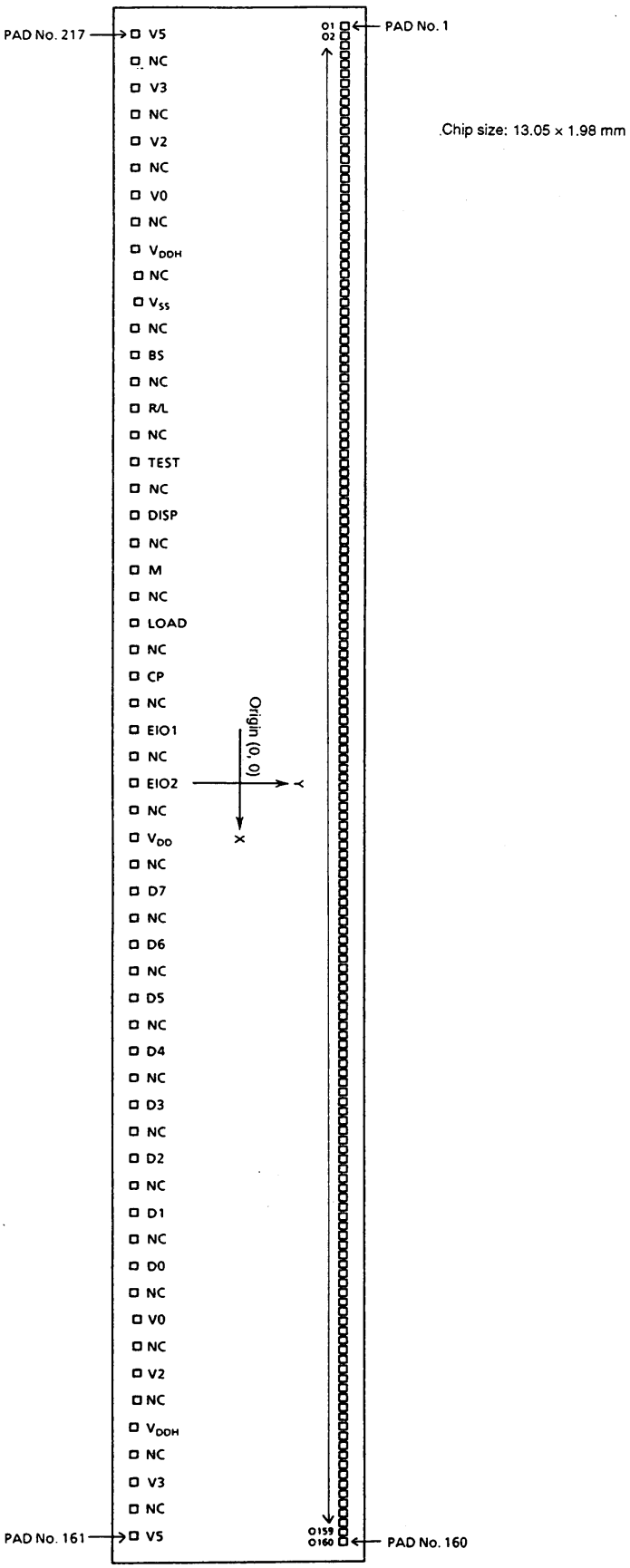


Pin Functions

<table>
<tr><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>O1 to O160</td><td>O</td><td>LCD drive outputs
<table>
<tr><th>M</th><th>Data</th><th>DISP</th><th>On</th></tr>
<tr><td>H</td><td>H</td><td>H</td><td>V0</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>V2</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>V3</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>V5</td></tr>
<tr><td>*</td><td>*</td><td>L</td><td>V5</td></tr>
</table>
*: Don’t care. (Must be held either high or low.)</td></tr>
<tr><td>V0
V2
V3
V5</td><td>I
I
I
I</td><td>V0 level drive voltage supply (selected level)
V2 level drive voltage supply (unselected level)
V3 level drive voltage supply (unselected level)
V5 level drive voltage supply (selected level)
} Pins with the same name must be set to the same potential.</td></tr>
<tr><td>V_{DDH}</td><td>—</td><td>High-voltage system power supply. Pins with the same name must be set to the same potential.</td></tr>
<tr><td>V_{DD}</td><td>—</td><td>Logic system power supply.</td></tr>
<tr><td>V_{SS}</td><td>—</td><td>GND</td></tr>
<tr><td>DISP</td><td>I</td><td>LCD off function. All outputs go to the V5 level when this pin is low.</td></tr>
<tr><td>M</td><td>I</td><td>Alternation signal input</td></tr>
<tr><td>EIO1
EIO2</td><td>I/O
I/O</td><td>Enable I/O
<table>
<tr><th>R/L</th><th>EIO1</th><th>EIO2</th></tr>
<tr><td>L</td><td>In</td><td>Out</td></tr>
<tr><td>H</td><td>Out</td><td>In</td></tr>
</table>
Enable input: The enable input at the first stage is fixed at V_{SS}. For succeeding stages, the enable input is connected to the enable output from the preceding stage.
Enable output: Connected to the enable input of the next stage when cascode connection is used.</td></tr>
<tr><td>CP</td><td>I</td><td>Data acquisition clock (falling edge)</td></tr>
<tr><td>LOAD</td><td>I</td><td>Data load clock (falling edge)</td></tr>
<tr><td>TEST</td><td>I</td><td>Test input. Must be tied high in normal use.*</td></tr>
<tr><td>R/L</td><td>I</td><td>Data shift direction setting
<table>
<tr><th>R/L</th><th>BS</th><th colspan="10">O1 to O160 outputs</th></tr>
<tr><td>L</td><td rowspan="2">H</td><td>O1
↑
D7</td><td>O2
↑
D6</td><td>O3
↑
D5</td><td>O4
↑
D4</td><td>→ . . .</td><td>O157
↑
D3</td><td>O158
↑
D2</td><td>O159
↑
D1</td><td>O160
↑
D0</td></tr>
<tr><td>H</td><td>O1
↑
D0</td><td>O2
↑
D1</td><td>O3
↑
D2</td><td>O4
↑
D3</td><td>. . .←</td><td>O157
↑
D4</td><td>O158
↑
D5</td><td>O159
↑
D6</td><td>O160
↑
D7</td></tr>
<tr><td>L</td><td rowspan="2">L</td><td>O1
↑
D3</td><td>O2
↑
D2</td><td>O3
↑
D1</td><td>O4
↑
D0</td><td>→ . . .</td><td>O157
↑
D3</td><td>O158
↑
D2</td><td>O159
↑
D1</td><td>O160
↑
D0</td></tr>
<tr><td>H</td><td>O1
↑
D0</td><td>O2
↑
D1</td><td>O3
↑
D2</td><td>O4
↑
D3</td><td>. . .←</td><td>O157
↑
D0</td><td>O158
↑
D1</td><td>O159
↑
D2</td><td>O160
↑
D3</td></tr>
</table></td></tr>
<tr><td>D0 to D7</td><td>I</td><td>Parallel data inputs</td></tr>
<tr><td>BS</td><td>I</td><td>Input bus setting. Set high for 8-bit input, low for 4-bit input. For 4-bit input, D0 to D3 are used for data input and D4 to D7 must be tied to ground.</td></tr>
</table>

Note: * This IC is sensitive to ESD care must be used when handling this device.

Pin Assignment



Pad Coordinates

PAD No.	Signal	X coordinate	Y coordinate	PAD No.	Signal	X coordinate	Y coordinate
1	O1	–6360.0	825.0	41	O41	–3160.0	825.0
2	O2	–6280.0	825.0	42	O42	–3080.0	825.0
3	O3	–6200.0	825.0	43	O43	–3000.0	825.0
4	O4	–6120.0	825.0	44	O44	–2920.0	825.0
5	O5	–6040.0	825.0	45	O45	–2840.0	825.0
6	O6	–5960.0	825.0	46	O46	–2760.0	825.0
7	O7	–5880.0	825.0	47	O47	–2680.0	825.0
8	O8	–5800.0	825.0	48	O48	–2600.0	825.0
9	O9	–5720.0	825.0	49	O49	–2520.0	825.0
10	O10	–5640.0	825.0	50	O50	–2440.0	825.0
11	O11	–5560.0	825.0	51	O51	–2360.0	825.0
12	O12	–5480.0	825.0	52	O52	–2280.0	825.0
13	O13	–5400.0	825.0	53	O53	–2200.0	825.0
14	O14	–5320.0	825.0	54	O54	–2120.0	825.0
15	O15	–5240.0	825.0	55	O55	–2040.0	825.0
16	O16	–5160.0	825.0	56	O56	–1960.0	825.0
17	O17	–5080.0	825.0	57	O57	–1880.0	825.0
18	O18	–5000.0	825.0	58	O58	–1800.0	825.0
19	O19	–4920.0	825.0	59	O59	–1720.0	825.0
20	O20	–4840.0	825.0	60	O60	–1640.0	825.0
21	O21	–4760.0	825.0	61	O61	–1560.0	825.0
22	O22	–4680.0	825.0	62	O62	–1480.0	825.0
23	O23	–4600.0	825.0	63	O63	–1400.0	825.0
24	O24	–4520.0	825.0	64	O64	–1320.0	825.0
25	O25	–4440.0	825.0	65	O65	–1240.0	825.0
26	O26	–4360.0	825.0	66	O66	–1160.0	825.0
27	O27	–4280.0	825.0	67	O67	–1080.0	825.0
28	O28	–4200.0	825.0	68	O68	–1000.0	825.0
29	O29	–4120.0	825.0	69	O69	–920.0	825.0
30	O30	–4040.0	825.0	70	O70	–840.0	825.0
31	O31	–3960.0	825.0	71	O71	–760.0	825.0
32	O32	–3880.0	825.0	72	O72	–680.0	825.0
33	O33	–3800.0	825.0	73	O73	–600.0	825.0
34	O34	–3720.0	825.0	74	O74	–520.0	825.0
35	O35	–3640.0	825.0	75	O75	–440.0	825.0
36	O36	–3560.0	825.0	76	O76	–360.0	825.0
37	O37	–3480.0	825.0	77	O77	–280.0	825.0
38	O38	–3400.0	825.0	78	O78	–200.0	825.0
39	O39	–3320.0	825.0	79	O79	–120.0	825.0
40	O40	–3240.0	825.0	80	O80	–40.0	825.0

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PAD No.	Signal	X coordinate	Y coordinate	PAD No.	Signal	X coordinate	Y coordinate
81	O81	40.0	825.0	121	O121	3240.0	825.0
82	O82	120.0	825.0	122	O122	3320.0	825.0
83	O83	200.0	825.0	123	O123	3400.0	825.0
84	O84	280.0	825.0	124	O124	3480.0	825.0
85	O85	360.0	825.0	125	O125	3560.0	825.0
86	O86	440.0	825.0	126	O126	3640.0	825.0
87	O87	520.0	825.0	127	O127	3720.0	825.0
88	O88	600.0	825.0	128	O128	3800.0	825.0
89	O89	680.0	825.0	129	O129	3880.0	825.0
90	O90	760.0	825.0	130	O130	3960.0	825.0
91	O91	840.0	825.0	131	O131	4040.0	825.0
92	O92	920.0	825.0	132	O132	4120.0	825.0
93	O93	1000.0	825.0	133	O133	4200.0	825.0
94	O94	1080.0	825.0	134	O134	4280.0	825.0
95	O95	1160.0	825.0	135	O135	4360.0	825.0
96	O96	1240.0	825.0	136	O136	4440.0	825.0
97	O97	1320.0	825.0	137	O137	4520.0	825.0
98	O98	1400.0	825.0	138	O138	4600.0	825.0
99	O99	1480.0	825.0	139	O139	4680.0	825.0
100	O100	1560.0	825.0	140	O140	4760.0	825.0
101	O101	1640.0	825.0	141	O141	4840.0	825.0
102	O102	1720.0	825.0	142	O142	4920.0	825.0
103	O103	1800.0	825.0	143	O143	5000.0	825.0
104	O104	1880.0	825.0	144	O144	5080.0	825.0
105	O105	1960.0	825.0	145	O145	5160.0	825.0
106	O106	2040.0	825.0	146	O146	5240.0	825.0
107	O107	2120.0	825.0	147	O147	5320.0	825.0
108	O108	2200.0	825.0	148	O148	5400.0	825.0
109	O109	2280.0	825.0	149	O149	5480.0	825.0
110	O110	2360.0	825.0	150	O150	5560.0	825.0
111	O111	2440.0	825.0	151	O151	5640.0	825.0
112	O112	2520.0	825.0	152	O152	5720.0	825.0
113	O113	2600.0	825.0	153	O153	5800.0	825.0
114	O114	2680.0	825.0	154	O154	5880.0	825.0
115	O115	2760.0	825.0	155	O155	5960.0	825.0
116	O116	2840.0	825.0	156	O156	6040.0	825.0
117	O117	2920.0	825.0	157	O157	6120.0	825.0
118	O118	3000.0	825.0	158	O158	6200.0	825.0
119	O119	3080.0	825.0	159	O159	6280.0	825.0
120	O120	3160.0	825.0	160	O160	6360.0	825.0

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PAD No.	Signal	X coordinate	Y coordinate	PAD No.	Signal	X coordinate	Y coordinate
161	V5	6300.0	–825.0	191	EIO1	–450.0	–825.0
162	NC	6075.0	–825.0	192	NC	–675.0	–825.0
163	V3	5850.0	–825.0	193	CP	–900.0	–825.0
164	NC	5625.0	–825.0	194	NC	–1125.0	–825.0
165	V_{DDH}	5400.0	–825.0	195	LOAD	–1350.0	–825.0
166	NC	5175.0	–800.0	196	NC	–1575.0	–825.0
167	V2	4950.0	–800.0	197	M	–1800.0	–825.0
168	NC	4725.0	–800.0	198	NC	–2025.0	–825.0
169	V0	4500.0	–800.0	199	DISP	–2250.0	–825.0
170	NC	4275.0	–825.0	200	NC	–2475.0	–825.0
171	D0	4050.0	–825.0	201	TEST	–2700.0	–825.0
172	NC	3825.0	–825.0	202	NC	–2925.0	–825.0
173	D1	3600.0	–825.0	203	R/L	–3150.0	–825.0
174	NC	3375.0	–825.0	204	NC	–3375.0	–825.0
175	D2	3150.0	–825.0	205	BS	–3600.0	–825.0
176	NC	2925.0	–825.0	206	NC	–3825.0	–825.0
177	D3	2700.0	–825.0	207	V_{SS}	–4050.0	–800.0
178	NC	2475.0	–825.0	208	NC	–4275.0	–800.0
179	D4	2250.0	–825.0	209	V_{DDH}	–4500.0	–825.0
180	NC	2025.0	–825.0	210	NC	–4725.0	–825.0
181	D5	1800.0	–825.0	211	V0	–4950.0	–825.0
182	NC	1575.0	–825.0	212	NC	–5175.0	–825.0
183	D6	1350.0	–825.0	213	V2	–5400.0	–825.0
184	NC	1125.0	–825.0	214	NC	–5625.0	–825.0
185	D7	900.0	–825.0	215	V3	–5850.0	–825.0
186	NC	675.0	–825.0	216	NC	–6075.0	–825.0
187	V_{DD}	450.0	–825.0	217	V5	–6300.0	–825.0
188	NC	225.0	–825.0				
189	EIO2	0.0	–825.0				
190	NC	–225.0	–825.0				

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