

## SANYO Semiconductors DATA SHEET

An ON Semiconductor Company

# LC709201F — Battery Monitor IC

#### Overview

The LC709201F is an IC that measures the remaining power level of 1-cell lithium-ion secondary batteries by monitoring the battery voltage without an external sense resistor, and detects the remaining battery power level by current prediction. It monitors the battery voltage and realizes a function that precisely measures the remaining battery charge. In addition, the IC realizes the function for calculating the remaining battery power level even more accurately by utilizing a temperature correction function that makes use of the temperature input from a thermistor.

#### Features

Accuracy of remaining battery power level measurement

• Accuracy of ±5% during discharging from 100% to 0% (at an ambient operating temperature of 0°C to 50°C)

■Measurement of remaining battery power level

• The remaining power level is measured four times a second and calculated with each measurement undertaken.

■Interface

• I<sup>2</sup>Cbus, communication in slave mode up to 100kHz supported

#### ■Ports

• I <sup>2</sup> C-bus communication pin	2 (SDA, SCL)
Battery temperature reading control pin	1 (TSW)
• Analog voltage input pin for battery temperature	1 (TSENSE)
• Reset pin	1 (RESB)
• TEST pin	1 (TEST)
• Power supply pin	$2(V_{SS}, V_{DD})$

#### ■Package form

- MFP10S (225 mil): LC709201FM-01/02/03
- VCT16 (2.6×2.6): LC709201FRD-01/02/03
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## Applications

• Cell phones, PDA devices, MP3 players, cordless phones, digital cameras, USB-related devices, etc.

(Note) Depending on the kinds of battery, applicable model differs (LC709201F-01/02/03). Please contact us for more detail information.

## **Package Dimensions**

unit : mm (typ) 3086B



## **Package Dimensions**

unit : mm (typ)

3318



## **Pin Assignment**



SANYO: MFP10S (225mil) "Lead-free Type"



SANYO: VCT16 (2.6×2.6) "Lead-free Type"

## **Block Diagram**



### **Pin Function**

Pin Name	I/O	Description
V <sub>SS</sub>	-	- power pin
V <sub>DD</sub>	-	+ power pin
RESB	Ι	Reset pin
TEST	I/O	Test pin
		*Connect an external 100kΩ pull-down resistor.
SDA	I/O	l <sup>2</sup> C data pin
SCL	I/O	l <sup>2</sup> C clock pin
TSW	0	Battery temperature reading control pin
		*Set high when reading in the temperature, held low at other times.
TSENSE	I	Battery temperature analog voltage input pin

#### Absolute Maximum Ratings at Ta=25°C, $\mathrm{V}_{SS}{=}0\mathrm{V}$

Damanatan	Querra ha a l	Die /Deese alve	Quaditions		Specification			1.1	
Parameter	Symbol	Pin/Remarks	Conditions	V <sub>DD</sub> [V]	min	typ	max	Unit	
Maximum supply voltage	V <sub>DD</sub> max	V <sub>DD</sub>			-0.3		+6.5		
Input voltage	V <sub>I</sub> (1)	RESB, TSENSE			-0.3		V <sub>DD</sub> +0.3	V	
Output voltage	V <sub>O</sub> (1)	TSW			-0.3		V <sub>DD</sub> +0.3	V	
Input/output voltage	V <sub>IO</sub> (1)	SDA, SCL, TEST			-0.3		V <sub>DD</sub> +0.3		
Allowable power	Pd max	MFP10S	Ta=-40 to +85°C				110		
dissipation		VCT16					55	mvv	
Operating ambient temperature	Topr				-40		+85	ŝ	
Storage ambient temperature	Tstg				-55		-125	ι. ·	

#### Allowable Operating Conditions at Ta=-40 to +85°C, $V_{SS}{=}0V$

Deremeter	Symbol	Din/Romarka	Conditions		S	unit		
Falameter	Symbol Pin/Remarks Conditions VDD[V]		V <sub>DD</sub> [V]	min	typ	max	unit	
Operating supply voltage	V <sub>DD</sub> (1)	V <sub>DD</sub>			2.25		5.5	
High level input voltage	V <sub>IH</sub> (1)	SDA, SCL		2.25 to 5.5	0.3V <sub>DD</sub> +0.7		V <sub>DD</sub>	V
Low level input voltage	V <sub>IL</sub> (1)	SDA, SCL		4.0 to 5.5	V <sub>SS</sub>		0.1V <sub>DD</sub> +0.4	
	V <sub>IL</sub> (2)			2.25 to 4.0	V <sub>SS</sub>		0.2V <sub>DD</sub>	

#### Electrical Characteristics at Ta=-40 to +85°C, V<sub>SS</sub>=0V

Devenueten	Quarket	Din/Bomorko	Oraclitica		S	LInit		
Parameter	Symbol	Pin/Remarks	Conditions	V <sub>DD</sub> [V]	min	typ	max	Unit
High level input current	l <sub>IH</sub> (1)	RESB, SDA, SCL	V <sub>IN</sub> =V <sub>DD</sub> (including output transistor off 2.25 t leakage current)				1	
Low level input current	կլ (1)	RESB, SDA, SCL	VIN=VSS (including output transistor off leakage current)	2.25 to 5.5	-1			μΑ
High level output	V <sub>OH</sub> (1)	TSW	I <sub>OH</sub> =-0.4mA	3.0 to 5.5	V <sub>DD</sub> -0.4			
voltage	V <sub>OH</sub> (2)		I <sub>OH</sub> =-0.2mA	2.25 to 5.5	V <sub>DD</sub> -0.4			
Low level output	V <sub>OL</sub> (1)	TSW,	I <sub>OL</sub> =3.0mA	3.0 to 5.5			0.4	V
voltage	V <sub>OL</sub> (2)	SDA, SCL	I <sub>OL</sub> =1.3mA	2.25 to 5.5			0.4	, i
Hysteresis voltage	VHYS	RESB, SDA, SCL		2.25 to 5.5		0.1V <sub>DD</sub>		
Pin capacitance	СР	All pins	Pins other than the pin under test VIN=VSS f=1 MHz Ta=25°C	2.25 to 5.5		10		pF
Consumption current	I <sub>DD</sub> (1)	V <sub>DD</sub>	When detecting remaining capacity	2.25 to 5.5		8	16	
	I <sub>DD</sub> (2)		When not detecting remaining capacity	2.25 to 5.5		5	12	μΑ

						Specification	า	
Parameter	Symbol	Pin/Remarks	Conditions	V <sub>DD</sub> [V]	min	typ	max	unit
Clock frequency	TSCL	SCL					100	kHz
Bus free time between	TBUF	SCL, SDA	See Fig. 1.					
STOP condition and					4.7			μs
START condition								
Hold time (repeated)	THD: STA	SCL, SDA	See Fig. 1.					
START condition								
First clock pulse is					4.0			μs
generated after this								
interval								
Repeated START	TSU: STA	SCL, SDA	See Fig. 1.	2 25 to 5 5	47			
condition setup time				2.23 10 3.3	4.7			μο
STOP condition setup	TSU: STO	SCL, SDA	See Fig. 1.		10			
time					4.0			μs
Data hold time	THD: DAT	SCL, SDA	See Fig. 1.		300			ns
Data setup time	TSU: DAT	SCL, SDA	See Fig. 1.		250			ns
Clock low period	TLOW	SCL			4.7			μs
Clock high period	THIGH	SCL			4.0			μs
Clock/data fall time	TF	SCL, SDA					300	ns
Clock/data rise time	TR	SCL, SDA					1000	ns





## **Discharge Characteristics**



Figure 2 Discharge Characteristics by Temperature Change



Figure 3 Discharge Characteristics by Load Change

## **Communication Protocol**

Communication protocol type: I<sup>2</sup>C Frequency: 100kHz Address: 0x16

#### **Bus Protocols**

S	:	Start Condition
Sr	:	Repeated Start Condition
Rd	:	Read (bit value of 1)
Wr	:	Write (bit value of 0)
А	:	ACK (bit value of 0)
Ν	:	NACK (bit value of 1)
Р	:	Stop Condition
CRC-8	:	Slave Address to Last Data (ex.3778mV: 0x16, 0x09, 0x17, 0xC2, 0x0E $\rightarrow$ 0x86)
	:	Master-to-Slave
	:	Slave-to-Master
	:	Continuation of protocol

#### **Read Word Protocol**

S	Slave Address	Wr	А	Command Code	A		
Sr	Slave Address	Rd	А	Data Byte Low	Α	Data Byte High	
Α	CRC-8	Ν	Р				

#### Write Word Protocol

S	Slave Add	ress	Wr	А	Command Code		A				
Data Byte Low		Α	Da	ata Byte	e High	А	С	CRC-8	А	Р	]

Slave Functions	Command Code	Range	Access	Unit
Cell Temperature	0x08	0 to 65535	R	0.1°K
Cell Voltage	0x09	0 to 65535	R	mV
Current	0x0A	-32768 to 32767	R	mA
Adjustment Pack	0x0B	0 to 255	R	Value
Relative State Of Charge	0x0D	0 to 100	R	%
Remaining Capacity	0x0F	0 to 65535	R	mAh
Full Charge Capacity	0x10	0 to 65535	R	mAh
IC Version	0x11	0 to 65535	R	Version
Adjustment Thermistor	0x12	0 to 255	R	Value
Set Relative State Of Charge	0x08	0xA500 + 0 to 100	W	0xA500 + %
Adjustment Pack	0x08	0x5A00 + 0 to 255	W	0x5A00 + Value
Adjustment Thermistor	0x08	0xAA00 + 0 to 255	W	0xAA00 + Value
Initial Relative State Of Charge	0x09	0xAA55	W	-

## **Application Circuit Example**

Figure 4 Example of an application schematic using LC709201F



Figure 5 Conceptual diagram using LC709201F



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