Ordering number : EN4841C

CMOS LSI

LC74723, 74723M

On-Screen Display Controller

Overview

The LC74723 and LC74723M are on-screen display controller CMOS LSIs that display characters and patterns on a TV screen under microprocessor control. Characters are 8 × 8 dots, and a dot interpolation function is provided. The LC74723 can display 24 characters × 10 lines of text.

Features

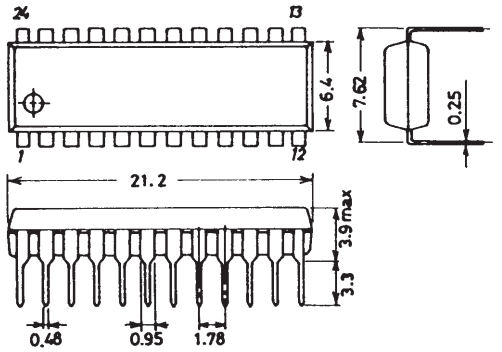
- Screen structure: 24 characters × 10 lines (up to 240 characters)
- Character structure: 8 (horizontal) × 8 (vertical) (interpolation function supported)
- Character sizes: Two horizontal and two vertical sizes
- Number of characters: 64
- Display start position: 64 horizontal and 64 vertical positions
- Blinking: In character units
- Blinking types: Two, with periods of 0.5 and 1.0 seconds
- Blue background screen display: (in internal synchronization mode)
- External control inputs: 8-bit serial input interface
- Built-in sync separator circuit
- Video output: Compound NTSC and PAL-M output
- Packages: 24-pin plastic MFP (375 mil)
  24-pin plastic DIP (300 mil)

Package Dimensions

unit: mm

3067-DIP24S

[LC74723]

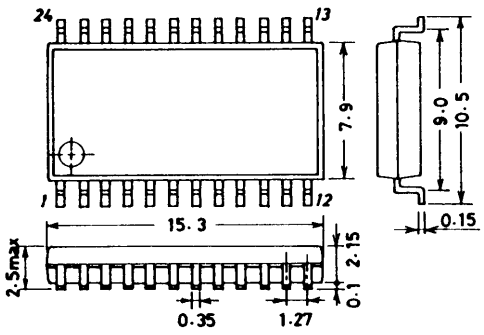


SANYO: DIP24S

unit: mm

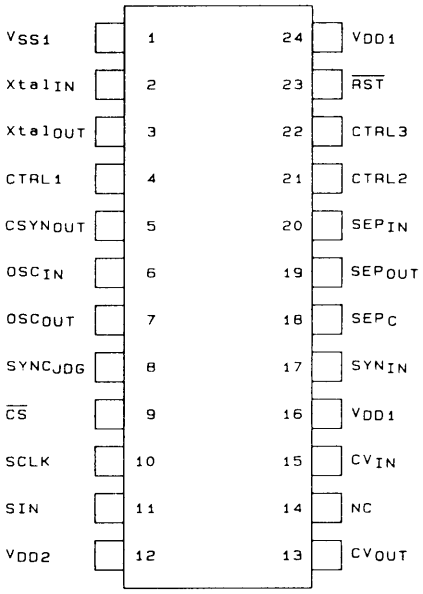
3045B-MFP24

[LC74723M]



SANYO: MFP24

Pin Assignment



Top view

Pin Functions

Pin No.	Symbol	Function	Description
1	$V_{SS}1$	Ground	Ground (digital system ground)
2	$Xtal_{IN}$	Crystal oscillator connection	Used either for connecting the external crystal and capacitor that are used for internal synchronization signal generation, or to input an external clock signal ($2f_{sc}$ or $4f_{sc}$).
3	$Xtal_{OUT}$		
4	CTRL1	Crystal oscillator input switching	Switches the LC74723 between external clock input mode and crystal oscillator mode. Low = crystal oscillator mode, high = external clock mode
5	$CSYN_{OUT}$	Composite synchronization signal output	Outputs a composite synchronization signal. Outputs the crystal oscillator clock on reset, i.e., when $\overline{RST}$ is low.
6	OSC_{IN}	LC oscillator	Connections for the coil and capacitor that form the oscillator used to generate the character output dot clock.
7	OSC_{OUT}		
8	$SYNC_{JDG}$	External synchronization signal judgment output	Outputs the result of judging whether or not there is an external synchronization signal. Outputs a high level when an external synchronization signal is present. Outputs the dot clock (LC oscillator) on reset, i.e., when $\overline{RST}$ is low. (The LC74723 can be set not to output this signal on reset using control data.)
9	$\overline{CS}$	Enable input	Enables serial data input. Serial data input is enabled when this input is low. There is a built-in pull-up resistor on this input (hysteresis input).
10	SCLK	Clock input	Inputs the clock signal used for serial data input. There is a built-in pull-up resistor on this input (hysteresis input).
11	SIN	Data input	Serial data input. There is a built-in pull-up resistor on this input (hysteresis input).
12	$V_{DD}2$	Power supply	Power supply (analog system power supply) for composite video signal level adjustment.
13	CV_{OUT}	Video signal output	Composite video signal output
14	NC		Must be either connected to ground or left open.
15	CV_{IN}	Video signal input	Composite video signal input
16	$V_{DD}1$	Power supply	Power supply (+5 V: digital system power supply)
17	SYN_{IN}	Sync separator circuit input	Video signal input for the built-in sync separator circuit (When the built-in sync separator circuit is not used, input either the horizontal synchronization signal or the composite synchronization signal.)
18	SEP_C	Sync separator circuit bias voltage	Built-in sync separator circuit bias voltage monitor
19	SEP_{OUT}	Composite synchronization signal output	Outputs the built-in sync separator circuit's composite synchronization signal. (Outputs the SYN_{IN} input signal when the built-in sync separator circuit is not used.)
20	SEP_{IN}	Vertical synchronization signal input	Inputs the vertical synchronization signal by integrating the output signal from the SEP_{OUT} pin. An integration circuit must be connected between the SEP_{OUT} pin and this pin. Hold at $V_{DD}1$ if this input is unused.

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Pin No.	Symbol	Function	Description
21	CTRL2	NTSC/PAL-M switch input	Switches the synchronization signal generation between NTSC and PAL-M. Low = NTSC, high = PAL-M
22	CTRL3	SEP_{IN} input control	Controls whether the $\overline{VSYNC}$ signal is input to SEP_{IN}. Low = Input $\overline{VSYNC}$, high = do not input.
23	$\overline{RST}$	Reset input	System reset input There is a built-in pull-up resistor on this input (hysteresis input).
24	$V_{DD}1$	Power supply (+5 V)	Power supply (+5 V: digital system power supply)

Note: * Both the $V_{DD}1$ pins (pins 16 and 24) must be connected.

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	$V_{DD}1$, $V_{DD}2$	V_{SS} – 0.3 to V_{SS} + 7.0	V
Maximum input voltage	V_{IN} max	All input pins	V_{SS} – 0.3 to V_{DD} + 0.3	V
Maximum output voltage	V_{OUT} max	$CSYN_{OUT}$, $SYNC_{JDG}$, SEP_{OUT}	V_{SS} – 0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd max	Ta = 25°C	350	mW
Operating temperature	Topr		–30 to +70	°C
Storage temperature	Tstg		–40 to +125	°C

Allowable Operating Ranges at Ta = –30 to +70°C

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	$V_{DD}1$	$V_{DD}1$	4.5	5.0	5.5	V
	$V_{DD}2$	$V_{DD}2$	4.5	5.0	1.27 $V_{DD}1$	V
Input high level voltage	$V_{IH}1$	$\overline{RST}$, $\overline{CS}$, SIN, SCLK	0.8 $V_{DD}1$		$V_{DD}1$ + 0.3	V
	$V_{IH}2$	CTRL1, CTRL2, CTRL3, SEP_{IN}	0.7 $V_{DD}1$		$V_{DD}1$ + 0.3	V
Input low level voltage	$V_{IL}1$	$\overline{RST}$, $\overline{CS}$, SIN, SCLK	V_{SS} – 0.3		0.2 $V_{DD}1$	V
	$V_{IL}2$	CTRL1, CTRL2, CTRL3, SEP_{IN}	V_{SS} – 0.3		0.3 $V_{DD}1$	V
Pull-up resistance	R_{PU}	Applies to the $\overline{RST}$, $\overline{CS}$, SIN, and SCLK pins and to the pins specified by options.	25	50	90	kΩ
Composite video input voltage	$V_{IN}1$	CV_{IN}; $V_{DD}1$ = 5 V		2.0		Vp-p
	$V_{IN}2$	SYN_{IN}; $V_{DD}1$ = 5 V		2.0	2.5	Vp-p
Input voltage	$V_{IN}3$	$Xtal_{IN}$ (when external clock input is used) $f_{in} = 2f_{sc}$ or $4f_{sc}$; $V_{DD}1$ = 5 V	0.1		5.0	Vp-p
Oscillator frequency	$f_{osc}1$	$Xtal_{IN}$ and $Xtal_{OUT}$ oscillator pins ($2f_{sc}$: NTSC)		7.159		MHz
	$f_{osc}1$	$Xtal_{IN}$ and $Xtal_{OUT}$ oscillator pins ($4f_{sc}$: NTSC)		14.318		MHz
	$f_{osc}1$	$Xtal_{IN}$ and $Xtal_{OUT}$ oscillator pins ($2f_{sc}$: PAL-M)		7.151		MHz
	$f_{osc}1$	$Xtal_{IN}$ and $Xtal_{OUT}$ oscillator pins ($4f_{sc}$: PAL-M)		14.302		MHz
	$f_{osc}2$	OSC_{IN} and OSC_{OUT} oscillator pins (LC oscillator)	5		12	MHz

Note: When the $Xtal_{IN}$ pin is used in clock input mode, be extremely careful of input noise.

Electrical Characteristics at Ta = –30 to +70°C, $V_{DD}1$ = 5 V unless otherwise specified

Parameter	Symbol	Conditions	min	typ	max	Unit
Input off leakage current	$I_{leak}1$	CV_{IN}			1	µA
Output off leakage current	$I_{leak}2$	CV_{OUT}			1	µA
Output high level voltage	$V_{OH}1$	$CSYN_{OUT}$, $SYNC_{JDG}$, SEP_{OUT}; $V_{DD}1$ = 4.5 V, I_{OH} = –1.0 mA	3.5			V
Output low level voltage	$V_{OL}1$	$CSYN_{OUT}$, $SYNC_{JDG}$, SEP_{OUT}; $V_{DD}1$ = 4.5 V, I_{OL} = 1.0 mA			1.0	V
Input current	I_{IH}	$\overline{RST}$, $\overline{CS}$, SIN, SCLK, CTRL1, CTRL2, CTRL3, SEP_{IN}; $V_{IN} = V_{DD}1$			1	µA
	I_{IL}	CTRL1, CTRL2, CTRL3, OSC_{IN}; $V_{IN} = V_{SS}1$	–1			µA
Current drain (operating)	$I_{DD}1$	$V_{DD}1$; All outputs open, Xtal: 7.159 MHz, LC: 8 MHz			15	mA
	$I_{DD}2$	$V_{DD}2$; $V_{DD}2$ = 5 V			20	mA

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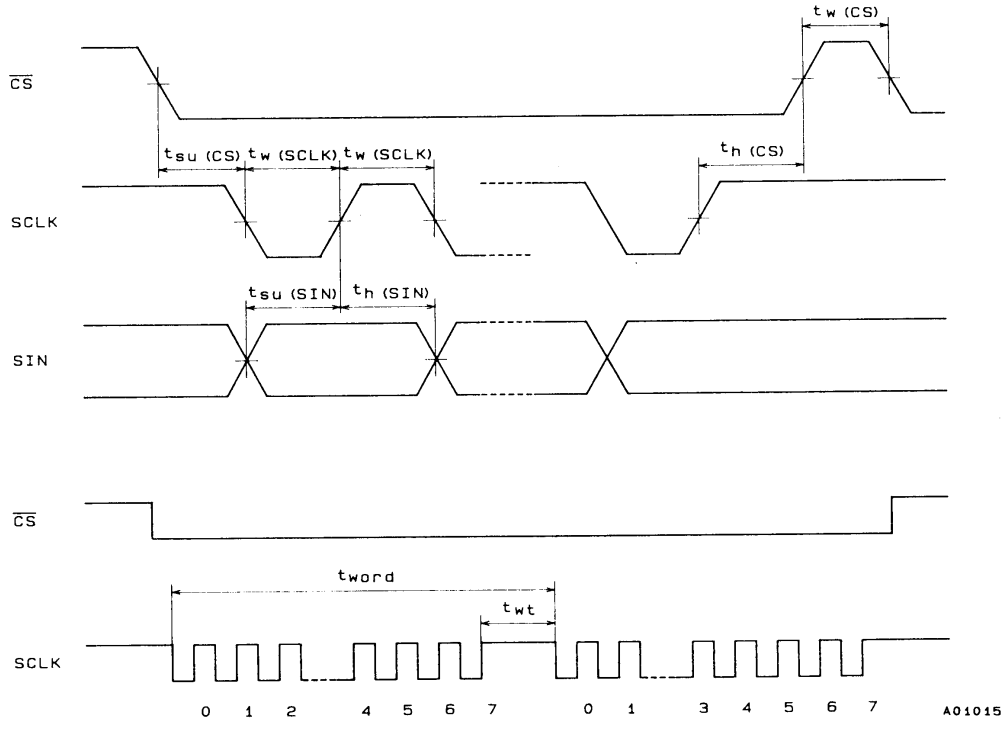
Parameter	Symbol	Conditions	min	typ	max	Unit
Sync level	V_{SN}	When the sync level is 0.8 V, CV_{OUT}: $V_{DD}1$, $V_{DD}2$ = 5 V	0.69	0.81	0.93	V
		When the sync level is 1.0 V, CV_{OUT}: $V_{DD}1$, $V_{DD}2$ = 5 V	0.89	1.01	1.13	V
Pedestal level	V_{PD}	When the sync level is 0.8 V, CV_{OUT}: $V_{DD}1$, $V_{DD}2$ = 5 V	1.28	1.40	1.52	V
		When the sync level is 1.0 V, CV_{OUT}: $V_{DD}1$, $V_{DD}2$ = 5 V	1.47	1.59	1.71	V
Color burst low level	V_{CBL}	When the sync level is 0.8 V, CV_{OUT}: $V_{DD}1$, $V_{DD}2$ = 5 V	0.97	1.09	1.21	V
		When the sync level is 1.0 V, CV_{OUT}: $V_{DD}1$, $V_{DD}2$ = 5 V	1.16	1.28	1.40	V
Color burst high level	V_{CBH}	When the sync level is 0.8 V, CV_{OUT}: $V_{DD}1$, $V_{DD}2$ = 5 V	1.60	1.72	1.84	V
		When the sync level is 1.0 V, CV_{OUT}: $V_{DD}1$, $V_{DD}2$ = 5 V	1.79	1.91	2.03	V
Background color low level	V_{RSL}	When the sync level is 0.8 V, CV_{OUT}: $V_{DD}1$, $V_{DD}2$ = 5 V	1.44	1.56	1.68	V
		When the sync level is 1.0 V, CV_{OUT}: $V_{DD}1$, $V_{DD}2$ = 5 V	1.63	1.75	1.87	V
Background color high level	V_{RSH}	When the sync level is 0.8 V, CV_{OUT}: $V_{DD}1$, $V_{DD}2$ = 5 V	1.96	2.08	2.20	V
		When the sync level is 1.0 V, CV_{OUT}: $V_{DD}1$, $V_{DD}2$ = 5 V	2.16	2.28	2.40	V
Trimming level 0	V_{BK0}	When the sync level is 0.8 V, CV_{OUT}: $V_{DD}1$, $V_{DD}2$ = 5 V	1.43	1.55	1.67	V
		When the sync level is 1.0 V, CV_{OUT}: $V_{DD}1$, $V_{DD}2$ = 5 V	1.61	1.73	1.85	V
Trimming level 1	V_{BK1}	When the sync level is 0.8 V, CV_{OUT}: $V_{DD}1$, $V_{DD}2$ = 5 V	2.01	2.13	2.25	V
		When the sync level is 1.0 V, CV_{OUT}: $V_{DD}1$, $V_{DD}2$ = 5 V	2.18	2.30	2.42	V
Character level	V_{CHA}	When the sync level is 0.8 V, CV_{OUT}: $V_{DD}1$, $V_{DD}2$ = 5 V	2.57	2.69	2.81	V
		When the sync level is 1.0 V, CV_{OUT}: $V_{DD}1$, $V_{DD}2$ = 5 V	2.76	2.88	3.00	V

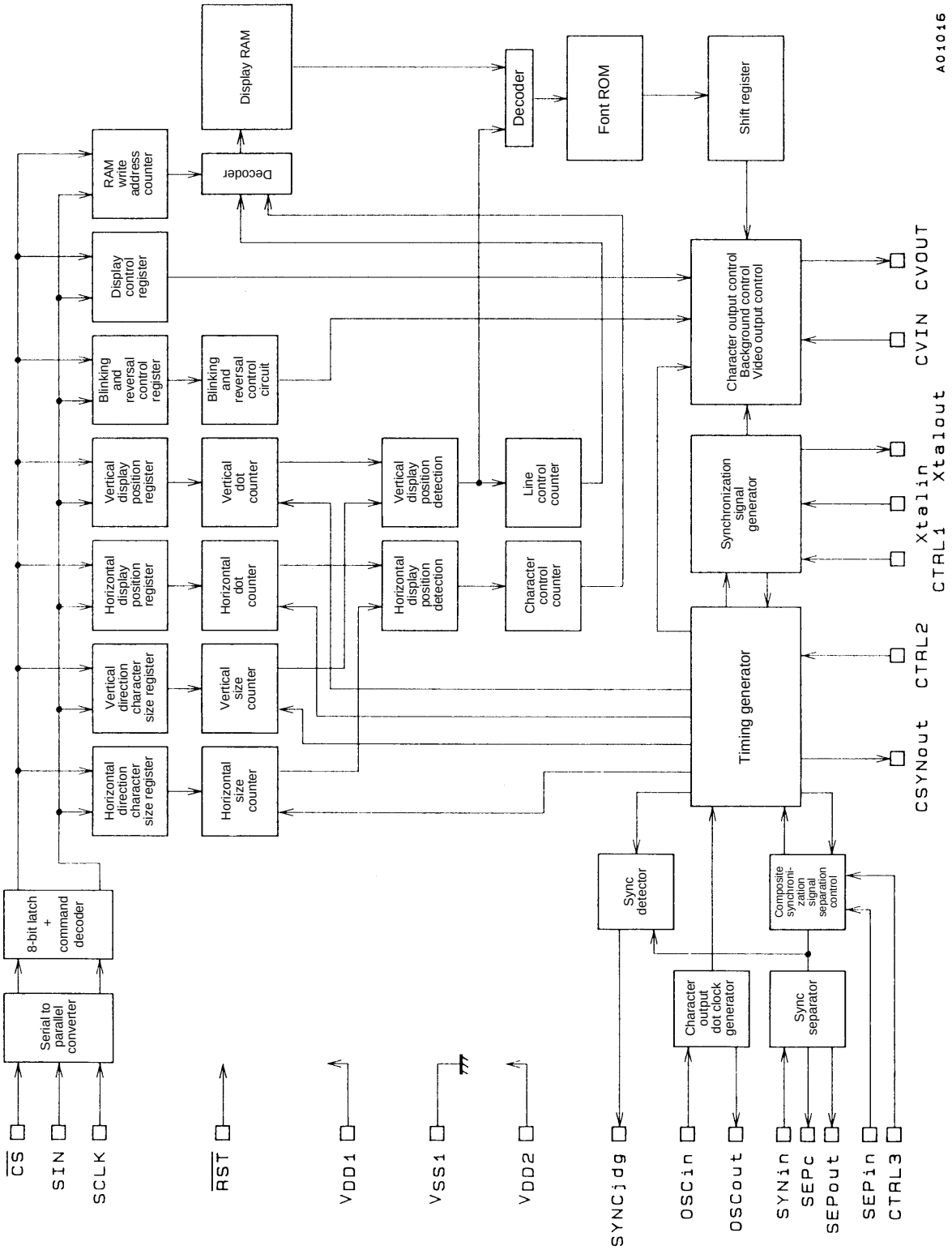
Timing Characteristics at Ta = –30 to +70°C, $V_{DD}1$ = 5 ± 0.5 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Minimum input pulse width	$t_{W\ (SCLK)}$	SCLK	200			ns
	$t_{W\ (CS)}$	$\overline{CS}$ (the period while $\overline{CS}$ is high)	1			µs
Data setup time	$t_{SU\ (CS)}$	$\overline{CS}$	200			ns
	$t_{SU\ (SIN)}$	SIN	200			ns
Data hold time	$t_{h\ (CS)}$	$\overline{CS}$	2			µs
	$t_{h\ (SIN)}$	SIN	200			ns
One word write time	t_{word}	The time to write 8 bits of data	4.2			µs
	t_{wt}	The RAM data write time	1			µs

Serial Data Input Timing



System Block Diagram



Display Control Commands

Display control commands are input as serial data in 8-bit units. Commands consist of a first byte that includes the command identifier code and data in the following second byte. The LC74723 supports the following six commands.

1. COMMAND0: Set display memory (VRAM) write address
2. COMMAND1: Set up display character data write
3. COMMAND2: Set vertical display start position and vertical character size
4. COMMAND3: Set horizontal display start position and horizontal character size
5. COMMAND4: Display control
6. COMMAND5: Display control

Display Control Command Table

Command	First byte								Second byte							
	Command identifier code				Data				Data							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
COMMAND0 (Set write address)	1	0	0	0	V3	V2	V1	V0	0	0	0	H4	H3	H2	H1	H0
COMMAND1 (Write character)	1	0	0	1	0	0	0	0	at	0	c5	c4	c3	c2	c1	c0
COMMAND 2 (Vertical display start position and vertical character size)	1	0	1	0	0	VS 20	0	VS 10	0	FS	VP 5	VP 4	VP 3	VP 2	VP 1	VP 0
COMMAND3 (Horizontal display start position and horizontal character size)	1	0	1	1	EGP	HS 20	0	HS 10	0	LC	HP 5	HP 4	HP 3	HP 2	HP 1	HP 0
COMMAND4 (Display control)	1	1	0	0	TST MOD	RAM ERS	OSC STP	SYS RST	0	EGL	NON	EG	BK 1	BK 0	RV	DSP ON
COMMAND5 (Synchronization signal control)	1	1	0	1	0	PH	RSN	INT	—	—	—	—	—	—	—	—

Once written, the command identifier code in the first byte is stored until the next first byte is written. However, when the display character data write command (COMMAND1) is written, the LC74723 locks into the display character data write mode, and another first byte cannot be written.
When a high level is input to the $\overline{CS}$ pin, the LC74723 is set to COMMAND0 (display memory write address setting mode).

1. COMMAND0 (Display memory write address setting command)
   - First byte

DA 0 to 7	Register name	Contents		Remarks
		State	Function	
7	—	1	Command 0 identification code Set display memory write address.	
6	—	0		
5	—	0		
4	—	0		
3	V3	0	Display memory address (0 to 9 hexadecimal)	
		1		
2	V2	0		
		1		
1	V1	0		
		1		
0	V0	0		
		1		

• Second byte

DA 0 to 7	Register name	Contents		Remarks
		State	Function	
7	—	0	Second byte identification code	
6	—	0		
5	—	0		
4	H4	0	Display memory address (0 to 17 hexadecimal)	
		1		
3	H3	0		
		1		
2	H2	0		
		1		
1	H1	0		
		1		
0	H0	0		
		1		

Note: The register states are all set to zero when the LC74723 is reset with the $\overline{\text{RST}}$ pin.

2. COMMAND1 (Display character data write setup command)

• First byte

DA 0 to 7	Register name	Contents		Remarks
		State	Function	
7	—	1	Command 1 identification code Set up display character data write.	When this command is input, the LC74723 locks into the display character data write mode until the $\overline{\text{CS}}$ pin goes high.
6	—	0		
5	—	0		
4	—	1		
3	—	0		
2	—	0		
1	—	0		
0	—	0		

• Second byte

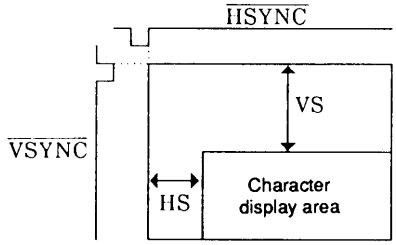
DA 0 to 7	Register name	Contents		Remarks
		State	Function	
7	at	0	Character attribute off	
		1	Character attribute on	
6	—	0		
5	c5	0	Character code (00 to 3F hexadecimal)	
		1		
4	c4	0		
		1		
3	c3	0		
		1		
2	c2	0		
		1		
1	c1	0		
		1		
0	c0	0		
		1		

Note: The register states are all set to zero when the LC74723 is reset with the $\overline{\text{RST}}$ pin.

3. COMMAND2 (Vertical display start position and vertical character size setting command)
   • First byte

DA 0 to 7	Register name	Contents		Remarks
		State	Function	
7	—	1	Command 2 identification code Set vertical display start position and vertical character size.	
6	—	0		
5	—	1		
4	—	0		
3	—	0		
2	VS20	0	1H per dot	Second line vertical character size
		1	2H per dot	
1	—	0		
0	VS10	0	1H per dot	First line vertical character size
		1	2H per dot	

   • Second byte

DA 0 to 7	Register name	Contents		Remarks
		State	Function	
7	—	0	Second byte identification code	
6	FS	0	Crystal oscillator frequency: $2f_{sc}$	
		1	Crystal oscillator frequency: $4f_{sc}$	
5	VP5 (MSB)	0	If VS is the vertical display start position then: $VS = H \times (2\sum_{n=0}^{5} 2^n VP_n)$ H: the horizontal synchronization pulse period  	The vertical display start position is set by the 6 bits VP0 to VP5. The weight of the low-order bit is 2H.
		1		
4	VP4	0		
		1		
3	VP3	0		
		1		
2	VP2	0		
		1		
1	VP1	0		
		1		
0	VP0 (LSB)	0		
		1		

Note: The register states are all set to zero when the LC74723 is reset with the $\overline{RST}$ pin.

4. COMMAND3 (Horizontal display start position and horizontal character size setting command)
   • First byte

DA 0 to 7	Register name	Contents		Remarks
		State	Function	
7	—	1	Command 3 identification code Set horizontal display start position and horizontal character size.	
6	—	0		
5	—	1		
4	—	1		
3	EGP	0	Correction: on	Trimming specifications when the horizontal character size is doubled
		1	Correction: off	
2	HS20	0	1Tc per dot	Second line horizontal character size
		1	2Tc per dot	
1	—	0		
0	HS10	0	1Tc per dot	First line horizontal character size
		1	2Tc per dot	

• Second byte

DA 0 to 7	Register name	Contents		Remarks
		State	Function	
7	—	0	Second byte identification code	Selects the dot clock used for horizontal direction character display.
6	LC	0	An LC oscillator is used for the dot clock	
		1	A crystal oscillator is used for the dot clock	
5	HP5 (MSB)	0	If HS is the horizontal display start position then: $HS = Tc \times (2\sum_{n=0}^{5} 2^n HP_n)$ Tc: The oscillator period of the OSCIN and OUT pin oscillator in operating mode	The horizontal display start position is set by the 6 bits HP0 to HP5. The weight of the low-order bit is 2Tc.
		1		
4	HP4	0		
		1		
3	HP3	0		
		1		
2	HP2	0		
		1		
1	HP1	0		
		1		
0	HP0 (LSB)	0		
		1		

Note: The register states are all set to zero when the LC74723 is reset with the $\overline{RST}$ pin.

5. COMMAND4 (Display control command)

• First byte

DA 0 to 7	Register name	Contents		Remarks
		State	Function	
7	—	1	Command 4 identification code Set display control.	
6	—	1		
5	—	0		
4	—	0		
3	TSTMOD	0	Normal operating mode	This bit must be zero.
		1	Test mode	
2	RAMERS	0		The RAM erase operation requires about 500 µs (It is executed in the DSPOFF state.)
		1	Erase display RAM (set to 3F hexadecimal)	
1	OSCSTP	0	Do not stop the crystal oscillator or LC oscillator circuits.	Valid when character display is off in external synchronization mode.
		1	Stop the crystal oscillator or LC oscillator circuits.	
0	SYSRST	0		Reset occurs when the $\overline{CS}$ pin is low, and the reset is cleared when $\overline{CS}$ is high.
		1	Reset all registers and turn the display off.	

• Second byte

DA 0 to 7	Register name	Contents		Remarks
		State	Function	
7	—	0	Second byte identification code	
6	EGL	0	Trimming level 0 (V_{BK0})	Trimming level switching
		1	Trimming level 1 (V_{BK1})	
5	NON	0	Interlace (256.5 H per field)	Interlace/non-interlace switching
		1	Non-interlace (263 H per field)	
4	EG	0	Trimming off	
		1	Trimming on	
3	BK1	0	Blinking period: about 0.5 s	Blinking state switching
		1	Blinking period: about 1.0 s	
2	BK0	0	Blinking off	When blinking is specified for reversed characters, the blinking will be between normal character and reversed character display.
		1	Blinking on	
1	RV	0	Reverse (character reversing) off	
		1	Reverse (character reversing) on	
0	DSPON	0	Character display off	
		1	Character display on	

Note: The register states are all set to zero when the LC74723 is reset with the $\overline{RST}$ pin.

6. COMMAND5 (Display control command)
   • First byte

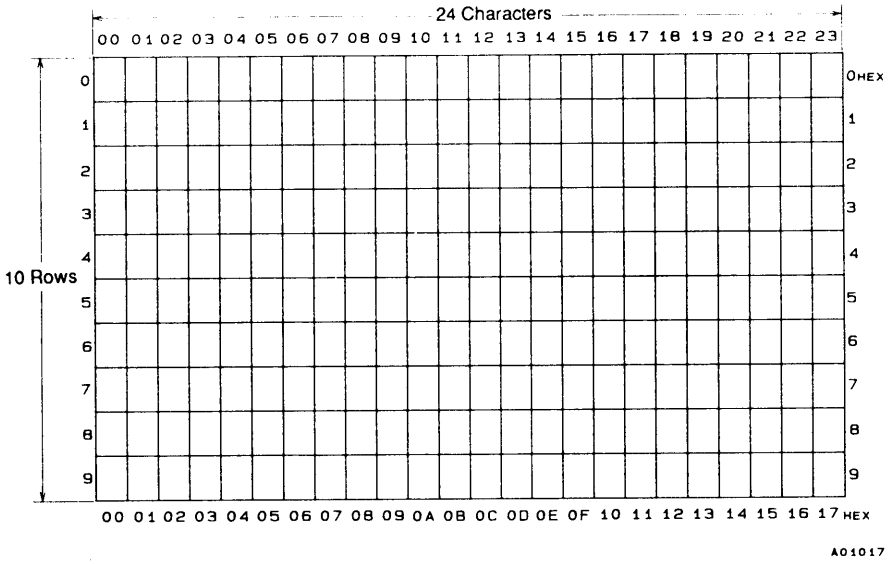
DA 0 to 7	Register name	Contents		Note
		State	Function	
7	—	1	Command 5 identification code Synchronization signal control setup	
6	—	1		
5	—	0		
4	—	1		
3	—	0		
2	PH	0	Green background	Background color switching (Only valid in NTSC mode, only a blue background color is supported in PAL-M mode.)
		1	Blue background	
1	RSN	0	External synchronization signal detection control: Disabled	External synchronization signal detection control Judges whether the signal has gone from present to absent or from absent to present.
		1	External synchronization signal detection control: Enabled	
0	INT	0	External synchronization	External/internal synchronization switching
		1	Internal synchronization	

Note: The register states are all set to zero when the LC74723 is reset with the $\overline{\text{RST}}$ pin.

Display Screen Structure

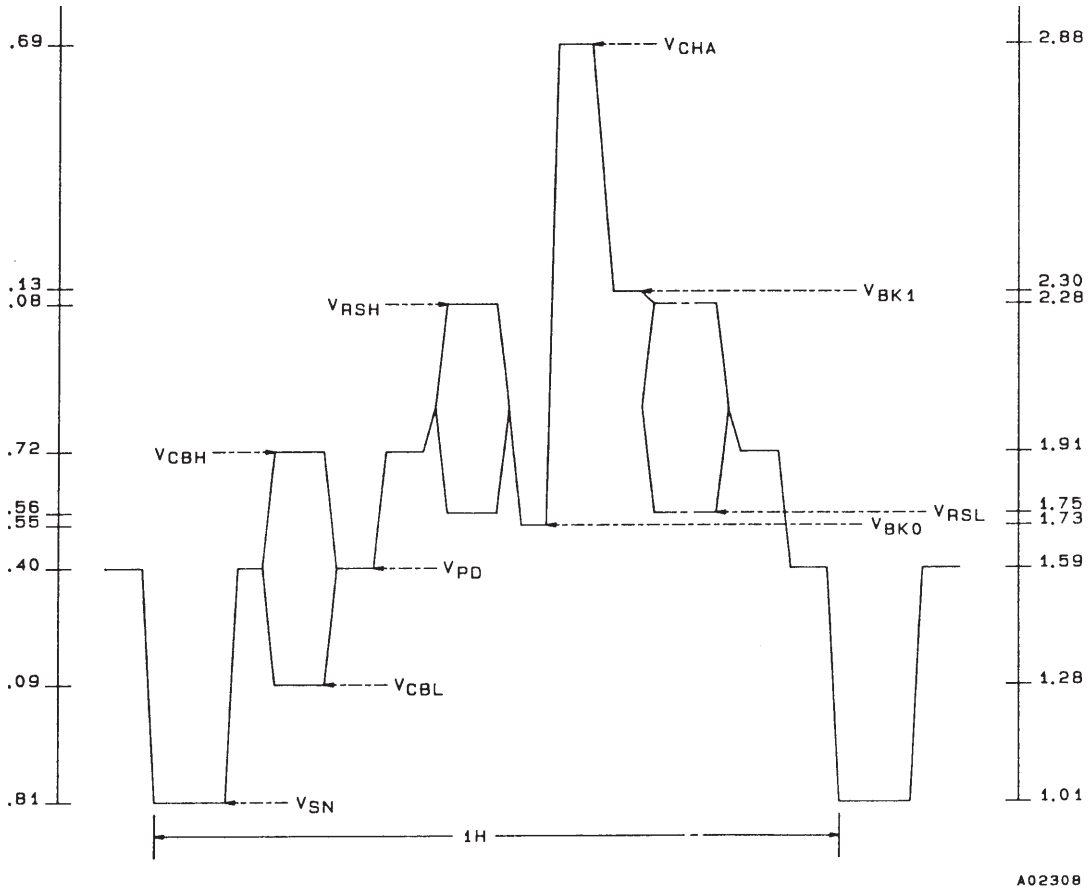
The display consists of 24 characters × 10 rows for a maximum of 240 characters. The maximum number of characters is reduced when the character size is enlarged.
Display memory addresses are specified as row (0 to 9 decimal) and column (0 to 23 decimal) addresses.

Display Screen Structure (display memory addresses)



Composite Video Signal Output Level (internally generated level)

CV_{OUT} output level waveform ($V_{DD}2$ = 5.00 V)



Output level	Output voltage ① [V]	Output voltage ② [V]
V_{CHA}: Character	2.69	2.88
V_{RSH}: Background color high	2.08	2.28
V_{CBH}: Color burst high	1.72	1.91
V_{RSL}: Background color low	1.56	1.75
V_{BK1}: Trimming	2.13	2.30
V_{BK0}: Trimming	1.55	1.73
V_{PD}: Pedestal	1.40	1.59
V_{CBL}: Color burst low	1.09	1.28
V_{SN}: Sync	0.81	1.01

Note: $V_{DD}2$ = 5.00 V