Ordering number : ENA1618

SANYO Semiconductors
DATA SHEET

An ON Semiconductor Company

CMOS IC

LC749402BG — Silicon gate LCD Picture Quality Improvement IC

Overview

LC749402BG is a picture quality improvement IC that processes the output signals to the LCD panel for high picture quality display. This IC performs various picture quality adjustments to provide the ideal correction for the display panel. It can support up to WVGA/SVGA panels. *

Features

(1) Digital input/output
- Digital YCbCr/YPbPr 24bit (4:4:4) or 16bit (4:2:2) or 8bit(ITU-R BT.656) signal input
- Digital RGB 24bit signal input
- Digital RGB 18bit/24bit signal output
- Digital YCbCr16bit (4:2:2)/24bit (4:4:4) signal output

(2) Image quality correction
- Y image quality correction: luminance adjustment, contour correction, CDEX (Color Depth Expander), dynamic-γ, black/white stretch
- C image quality correction: color exciter, flesh tone correction, hue, color gain
- RGB image quality correction: brightness, contrast, white balance, black balance, γ correction

(3) Panel interface
- Built-in panel driver timing controller
- Panel protection timing signal generation
- Backlight control PWM (video adaptive low power consumption processing)

*: The LC749402BG video input should satisfy the following conditions:
40MHz or less operating frequency, 896 dots or less horizontal size, 768 lines or less vertical size.

LSI Specifications

- Supply voltage Core: 1.2V
  I/O: 1.8V/2.85V/3.3V
- Maximum operating frequency: 40MHz
- Package: FBGA96

Principal Applications

- LCD display equipment

CDEX (Color Depth Expander)

Original

CDEX

Specifications

Absolute Maximum Ratings at Ta = 25°C, DV_{SS} = 0V, AV_{SS}_OSC = 0V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage (I/O)	DV_{DD}_IO		-0.3 to +3.96	V
Maximum supply voltage (core)	DV_{DD}_CORE AV_{DD}_OSC		-0.3 to +1.8	V
Digital input voltage	V_I		-0.3 to DV_{DD}_IO+0.3	V
Digital output voltage	V_O		-0.3 to DV_{DD}_IO+0.3	V
Operating temperature	Topr		-40 to +85	°C
Storage temperature	Tstg		-55 to +125	°C

Allowable Operating Ranges at Ta = -40 to +85°C, DV_{SS} = 0V, AV_{SS}_OSC = 0V

Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
Supply voltage (I/O)	DV_{DD}_IO		2.6	2.85	3.6	V
			1.7	1.8	1.9	V
Supply voltage (I/O)	DV_{DD}_CORE AV_{DD}_OSC		1.0	1.2	1.3	V
Input voltage range	V_{IN}		0		DV_{DD}_IO	V

DC Characteristics at Ta = -40 to +85°C, DV_{SS} = 0V, AV_{SS}_OSC = 0V,

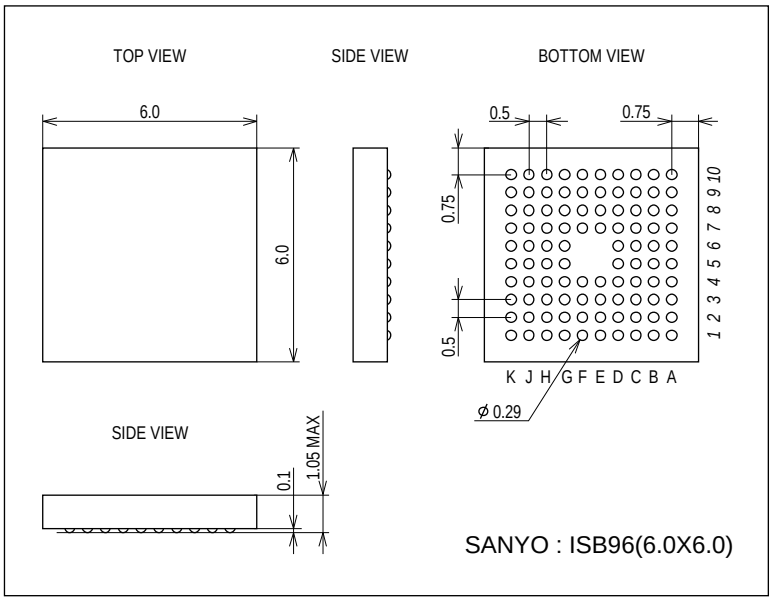
DV_{DD}_IO = 1.7V to 1.9V or 2.6V to 3.6V, DV_{DD}_CORE = 1.0V to 1.3V

Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
Input high-level voltage	V_{IH}	CMOS level inputs	0.7DV_{DD}_IO			V
		CMOS level Schmitt inputs	0.7DV_{DD}_IO			V
Input low-level voltage	V_{IL}	CMOS level inputs			0.3DV_{DD}_IO	V
		CMOS level Schmitt inputs			0.3DV_{DD}_IO	V
Input high-level current	I_{IH}	V_I=DV_{DD}_IO			10	µA
		V_I=DV_{DD}_IO, with pull-down resistance			100	µA
Input low-level current	I_{IL}	V_I=DV_{SS}	-10			µA
Output high-level voltage	V_{OH}	CMOS voltage: 2.6V to 3.6V Pin D: I_{OH}=-2mA Pin F: I_{OH}=-2mA (when set to 2mA) I_{OH}=-4mA (when set to 4mA) Pin G: I_{OH}=-4mA (when set to 4mA) I_{OH}=-8mA (when set to 8mA) Pin H: I_{OH}=-4mA	DV_{DD}_IO-0.4			V
		CMOS voltage: 1.7V to 1.9V Pin D: I_{OH}=-1mA Pin F: I_{OH}=-1mA (when set to 2mA) I_{OH}=-2mA (when set to 4mA) Pin G: I_{OH}=-2mA (when set to 4mA) I_{OH}=-4mA (when set to 8mA) Pin H: I_{OH}=-2mA	DV_{DD}_IO-0.45			V
Output low-level voltage	V_{OL}	CMOS			0.4	V
Output leak current	I_{OZ}	At output of high-impedance	-10		10	µA
Pull-down resistor	R_{DN}	Typical conditions: Ta=25°C DV_{DD}_IO=2.85V DV_{DD}_CORE=1.2V		98		kΩ
Dynamic supply current	I_{DDOP}	Typical conditions: Ta=25°C DV_{DD}_IO=2.85V DV_{DD}_CORE=1.2V tck=10MHz 10 steps		18		mA
		Typical conditions: Ta=25°C DV_{DD}_IO=2.85V DV_{DD}_CORE=1.2V tck=40MHz 10 steps		57		mA
Static supply current *1	I_{DDST}	Typical conditions: Ta=25°C DV_{DD}_IO=2.85V DV_{DD}_CORE=1.2V Outputs open V_I=DV_{SS} or DV_{DD}_IO		20		µA

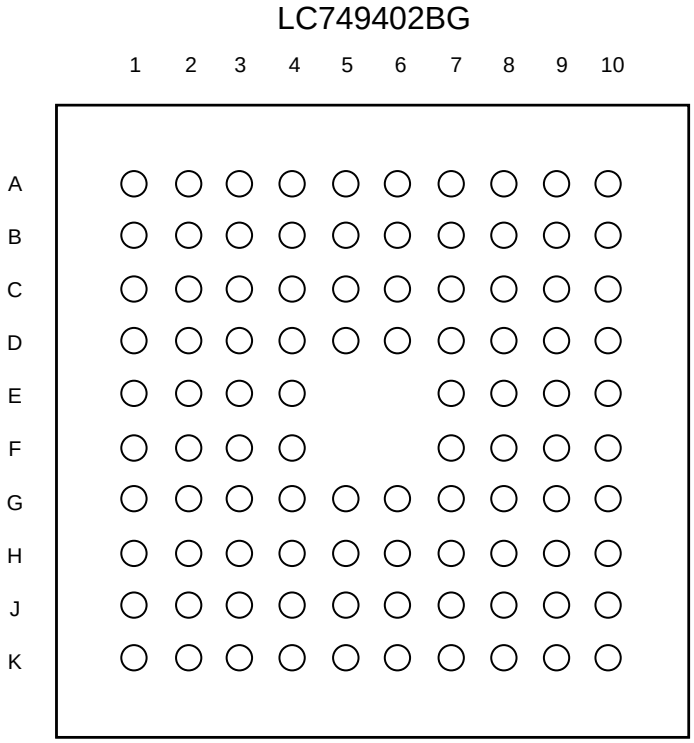
*1: There is a input terminal which builds in pull down resistance. Please note that there is no guarantee about static consumption current depending on circuit composition.

Package Dimensions FBGA96

unit:mm (typ)
3387

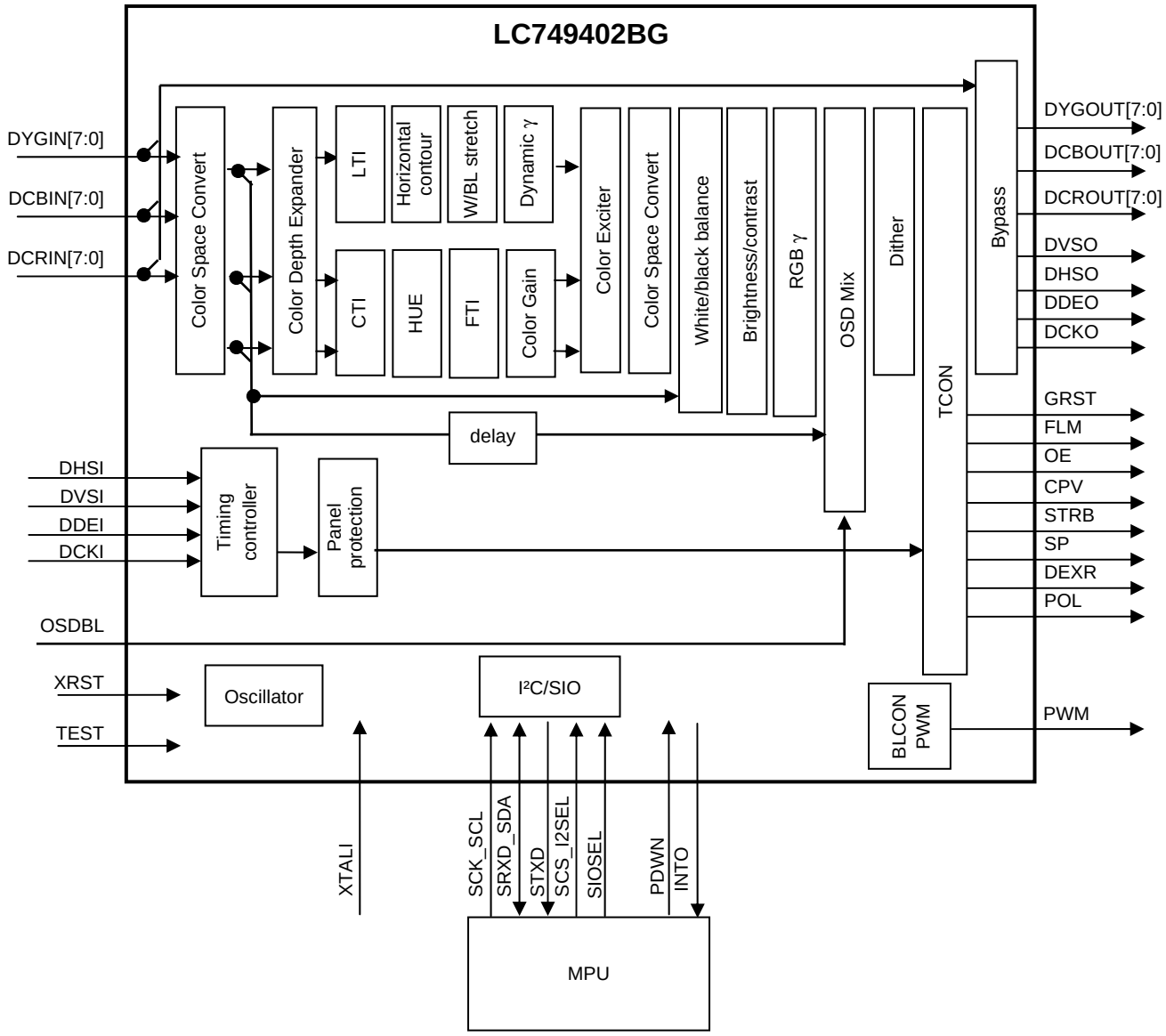


Pin Assignment



Top view

Block Diagram



Pin Functions

Pin No.	Pin symbol	In/output format		Connecting destination		Remarks
		I/O	Format			
A1	AV_{DD}_OSC	P	-	Core voltage	Analog	Connect this pin to B2 without fail.
A2	STXD	O	D	CMOS	Digital	SIO data
A3	SCK_SCL	I	C	CMOS	Digital	Bus clock (common to SIO and I^2C)
A4	DBOUT7	O	F	CMOS	Digital	B/Cb/C video (MSB)
A5	DBOUT4	O	F	CMOS	Digital	B/Cb/C video
A6	DBOUT1	O	F	CMOS	Digital	B/Cb/C video
A7	DGOUT6	O	F	CMOS	Digital	G/Y video
A8	DGOUT4	O	F	CMOS	Digital	G/Y video
A9	DGOUT3	O	F	CMOS	Digital	G/Y video
A10	DV_{DD}_IO	P	-	IO voltage	Digital	Connect this pin to B9 without fail
B1	RC_BIAS	I	J	resistor	Analog	Bias resistor connection (Connect this pin to GND with a 20kΩ)
B2	AV_{DD}_OSC	P	-	Core voltage	Analog	
B3	SRXD_SDA	I/O	H	CMOS	Digital	SIO data input/I^2C data I/O
B4	PWM	O	D	CMOS	Digital	Pulse width modulation waveform
B5	DBOUT5	O	F	CMOS	Digital	B/Cb/C video
B6	DBOUT2	O	F	CMOS	Digital	B/Cb/C video (6-bit output mode, LSB)
B7	DGOUT7	O	F	CMOS	Digital	G/Y video (MSB)
B8	DGOUT5	O	F	CMOS	Digital	G/Y video
B9	DV_{DD}_IO	P	-	IO voltage	Digital	
B10	DGOUT2	O	F	CMOS	Digital	G/Y video (6-bit output mode, LSB)
C1	DCRIN0	I	C	CMOS	Digital	R/Cr video. Connect this pin to GND when not to be used.
C2	DCRIN1	I	C	CMOS	Digital	R/Cr video. Connect this pin to GND when not to be used.
C3	AV_{SS}_OSC	P	-	GND	Analog	
C4	INTO	O	D	CMOS	Digital	Interrupt
C5	DBOUT6	O	F	CMOS	Digital	B/Cb/C video
C6	DBOUT3	O	F	CMOS	Digital	B/Cb/C video
C7	DBOUT0	O	F	CMOS	Digital	B/Cb/C video (8-bit output mode, LSB)
C8	DV_{DD}_IO	P	-	IO voltage	Digital	
C9	DGOUT1	O	F	CMOS	Digital	G/Y video
C10	DGOUT0	O	F	CMOS	Digital	G/Y video (8-bit output mode, LSB)
D1	DCRIN2	I	C	CMOS	Digital	R/Cr video. Connect this pin to GND when not to be used.
D2	DCRIN3	I	C	CMOS	Digital	R/Cr video. Connect this pin to GND when not to be used.
D3	DCRIN4	I	C	CMOS	Digital	R/Cr video. Connect this pin to GND when not to be used.
D4	TEST	I	B	CMOS	Digital	Test (Normally, connect this pin to GND)
D5	XRST	I	A	CMOS	Digital	System reset (“L” reset)
D6	DV_{DD}_IO	P	-	IO voltage	Digital	
D7	DV_{DD}_IO	P	-	IO voltage	Digital	
D8	DROUT7	O	F	CMOS	Digital	R/Cr video (MSB)
D9	DROUT6	O	F	CMOS	Digital	R/Cr video
D10	DROUT5	O	F	CMOS	Digital	R/Cr video

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Pin No.	Pin symbol	In/output format		Connecting destination		Remarks
		I/O	Format			
E1	DCRIN5	I	C	CMOS	Digital	R/Cr video. Connect this pin to GND when not to be used.
E2	DCRIN6	I	C	CMOS	Digital	R/Cr video. Connect this pin to GND when not to be used.
E3	DCRIN7	I	C	CMOS	Digital	R/Cr video (MSB). Connect this pin to GND when not to be used.
E4	DV_{SS}	P	-	GND	Digital	
E7	PDWN	I	A	CMOS	Digital	"H" power down. Connect this pin to GND when not to be used.
E8	DROUT4	O	F	CMOS	Digital	R/Cr video
E9	DROUT3	O	F	CMOS	Digital	R/Cr video
E10	DROUT2	O	F	CMOS	Digital	R/Cr video (6-bit output mode, LSB)
F1	DYGIN0	I	C	CMOS	Digital	G/Y/656 video (LSB). Connect this pin to GND when not to be used.
F2	DYGIN1	I	C	CMOS	Digital	G/Y/656 video. Connect this pin to GND when not to be used.
F3	DYGIN2	I	C	CMOS	Digital	G/Y/656 video. Connect this pin to GND when not to be used.
F4	DV_{SS}	P	-	GND	Digital	
F7	DV_{DD}_CORE	P	-	Core voltage	Digital	
F8	DROUT1	O	F	CMOS	Digital	R/Cr video
F9	DROUT0	O	F	CMOS	Digital	R/Cr video (8-bit output mode, LSB)
F10	DCKO	O	G	CMOS	Digital	Video clock
G1	DYGIN3	I	C	CMOS	Digital	G/Y/656 video. Connect this pin to GND when not to be used.
G2	DYGIN4	I	C	CMOS	Digital	G/Y/656 video. Connect this pin to GND when not to be used.
G3	DYGIN5	I	C	CMOS	Digital	G/Y/656 video. Connect this pin to GND when not to be used.
G4	DV_{SS}	P	-	GND	Digital	
G5	SCS_I2SEL	I	A	CMOS	Digital	SIO chip enable/I^2C slave address switching
G6	SIOSEL	I	C	CMOS	Digital	"L": I^2C slave, "H": 4-wire SIO
G7	DV_{DD}_CORE	P	-	Core voltage	Digital	
G8	DHSO/SP2	O	F	CMOS	Digital	Horizontal synchronizing signal/start pulse signal for source driver
G9	DVSO/FLM2	O	F	CMOS	Digital	Vertical synchronizing signal/start pulse signal for gate driver
G10	DDEO	O	F	CMOS	Digital	Data enable signal
H1	DYGIN6	I	C	CMOS	Digital	G/Y/656 video. Connect this pin to GND when not to be used.
H2	DYGIN7	I	C	CMOS	Digital	G/Y/656 video (MSB). Connect this pin to GND when not to be used.
H3	DV_{SS}	P	-	GND		
H4	DCBIN6	I	C	CMOS	Digital	B/Cb/C video. Connect this pin to GND when not to be used.
H5	DVSI	I	C	CMOS	Digital	Vertical synchronizing signal
H6	OSDBL	I	C	CMOS	Digital	Data enable signal for external OSD. Connect this pin to GND when not to be used.
H7	FLM	O	F	CMOS	Digital	Start pulse signal for gate driver
H8	DV_{DD}_CORE	P	-	Core voltage	Digital	
H9	DEXR	O	F	CMOS	Digital	Reversed video signal output for DTR. Low output when the DTR is OFF.
H10	POL	O	F	CMOS	Digital	Voltage polarity selection signal for source driver

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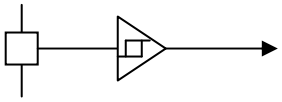
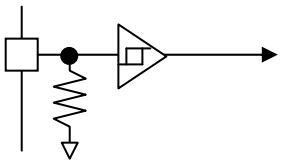
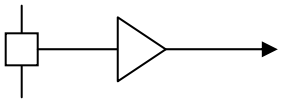
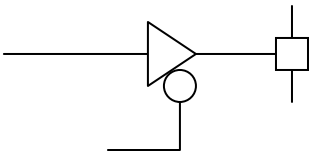
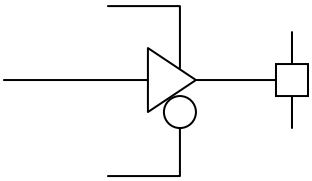
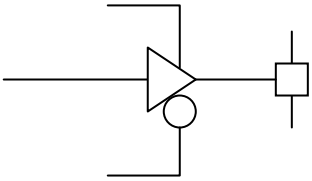
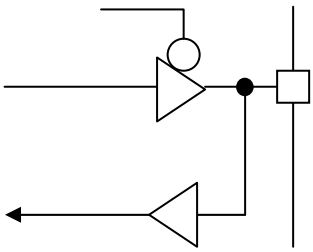
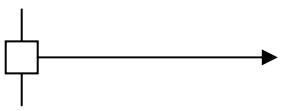
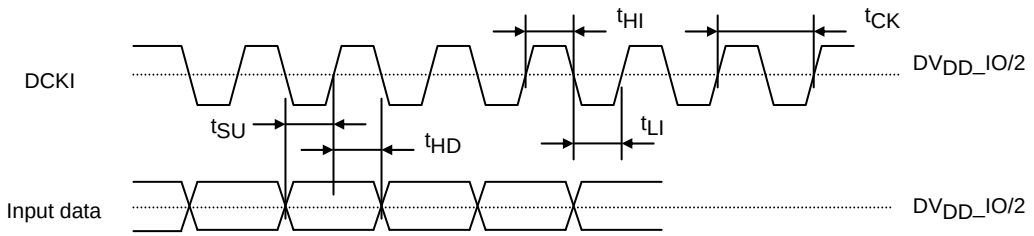
Pin No.	Pin symbol	In/output format		Connecting destination		Remarks
		I/O	Format			
J1	DCBIN0	I	C	CMOS	Digital	B/Cb/C video (LSB). Connect to GND when not to be used.
J2	DV_{SS}	P	-	GND	Digital	
J3	DCBIN3	I	C	CMOS	Digital	B/Cb/C video. Connect this pin to GND when not to be used.
J4	DCBIN5	I	C	CMOS	Digital	B/Cb/C video. Connect this pin to GND when not to be used.
J5	DDEI	I	C	CMOS	Digital	Data enable signal, Connect this pin to GND in the internal generation mode
J6	DHSI	I	C	CMOS	Digital	Horizontal synchronizing signal
J7	GRST	O	F	CMOS	Digital	Reset signal for gate driver
J8	CPV	O	F	CMOS	Digital	Clock signal for gate driver
J9	DV_{DD}_CORE	P	-	Core voltage	Digital	
J10	SP	O	F	CMOS	Digital	Start pulse signal for source driver
K1	DV_{SS}	P	-	GND	Analog	Connect this pin to J2 without fail
K2	DCBIN1	I	C	CMOS	Digital	B/Cb/C video. Connect this pin to GND when not to be used.
K3	DCBIN2	I	C	CMOS	Digital	B/Cb/C video. Connect this pin to GND when not to be used.
K4	DCBIN4	I	C	CMOS	Digital	B/Cb/C video. Connect this pin to GND when not to be used.
K5	DCBIN7	I	C	CMOS	Digital	B/Cb/C video (MSB). Connect this pin to GND when not to be used.
K6	DCKI	I	C	CMOS	Digital	Video clock
K7	XTAL1	I	C	CMOS	Digital	Panel protection, PWM generation clock. Connect this pin to GND when not to be used.
K8	OE	O	F	CMOS	Digital	Output enable signal for gate driver
K9	STRB	O	F	CMOS	Digital	Data strobe signal for source driver
K10	DV_{DD}_CORE	P	-	Core voltage	Digital	Connect this pin to J9 without fail

Pin Type

In/Output form	Function	Equivalent circuit	Application Terminal
A	Schmitt trigger CMOS input		XRST, PDWN, SCS_I2SEL
B	CMOS input with built-in pull-down resistor		TEST
C	CMOS input		SCK_SCL, SIOSEL, DVSI, DHSI, DDEI, OSDBL, DYGIN7, DYGIN6, DYGIN5, DYGIN4, DYGIN3, DYGIN2, DYGIN1, DYGIN0, DCBIN7, DCBIN6, DCBIN5, DCBIN4, DCBIN3, DCBIN2, DCBIN1, DCBIN0, DCRIN7, DCRIN6, DCRIN5, DCRIN4, DCRIN3, DCRIN2, DCRIN1, DCRIN0
D	2mA 3-STATE drive CMOS output		STXD, PWM, INTO
F	2mA/4mA switching 3-STATE drive CMOS output		DBOUT7, DBOUT6, DBOUT5, DBOUT4, DBOUT3, DBOUT2, DBOUT1, DBOUT0, DROUT7, DROUT6, DROUT5, DROUT4, DROUT3, DROUT2, DROUT1, DROUT0 DGOUT7, DGOUT6, DGOUT5, DGOUT4, DGOUT3, DGOUT2, DGOUT1, DGOUT0, DHSO/SP2, DVSO/FLM2, DDEO FLM, DEXR, POL, GRST, CPV, SP, OE, STRB
G	4mA/8mA switching 3-STATE drive CMOS output		DCKO
H	4mA 3-STATE drive CMOS input/output		SRXD_SDA
J	Analog input/output		RC_BIAS

I/O Timing

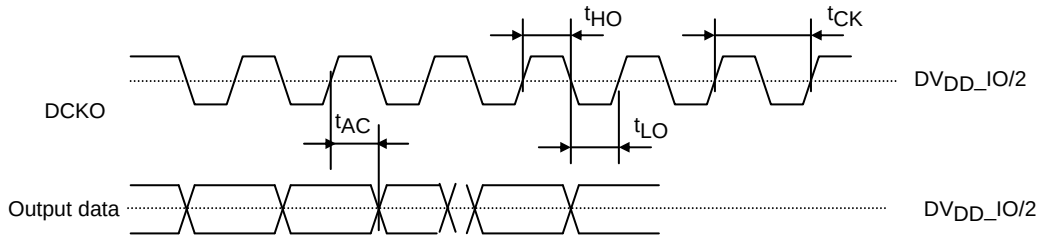
(1) Input data timing



Pin name	Parameter	Symbol	min	typ	max	unit
DCKI	Clock cycle	t_{CK}	25			ns
	Duty			50		%
DCRIN*, DYGIN*, DCBIN*, DVSI, DHSI, DDEI, OSDBL	Input data setup time (DV_{DD}_IO=2.6 to 3.6V)	t_{SU}	3			ns
	Input data setup time (DV_{DD}_IO=1.7 to 1.9V)	t_{SU}	3			ns
	Input data hold time (DV_{DD}_IO=2.6 to 3.6V)	t_{HD}	2			ns
	Input data hold time (DV_{DD}_IO=1.7 to 1.9V)	t_{HD}	2			ns

*: The recommended duty cycle of input clock is 50%

(2) Output data timing



Pin name	Parameter	Symbol	min	typ	max	unit
DCKO	Clock cycle	t_{CK}	25			ns
	Duty			50		%
DROUT*, DGOUT*, DBOUT*, DVSO, DHSO, DDEO, DEXR, POL, SP, STRB, CPV, OE, FLM, GRST	Output data delay time (DV_{DD}_IO=2.6 to 3.6V) Pin F: when set to 4mA Pin G: when set to 8mA	t_{AC}	-3		3	ns
	Output data delay time (DV_{DD}_IO=2.6 to 3.6V) Pin F: when set to 2mA Pin G: when set to 4mA	t_{AC}	-3		6	ns
	Output data delay time (DV_{DD}_IO=1.7 to 1.9V) Pin F: when set to 4mA Pin G: when set to 8mA	t_{AC}	-5		4	ns
	Output data delay time (DV_{DD}_IO=1.7 to 1.9V) Pin F: when set to 2mA Pin G: when set to 4mA	t_{AC}	-6		9	ns

* When DCKO is set to the forward rotation output. Output load capacity: 5pF