Ordering number : EN3586A

CMOS LSI

LC7574NE, 7574NW

1/2 Duty VFD Driver for Frequency Display

Overview

The LC7574NE and LC7574NW are 1/2 duty VFD drivers that can be used for electronic tuning frequency display and other applications under the control of a controller. These products can directly drive VFDs with up to 74 segments.

Features

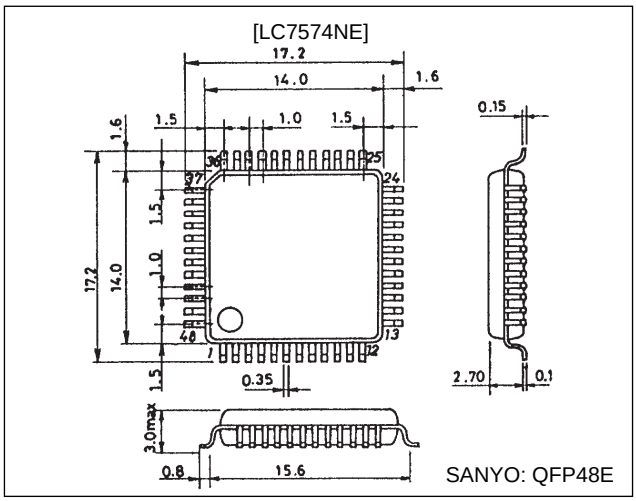
- 74 segment outputs
- Noise reduction circuits are built into the output drivers.
- Serial data input supports CCB* format communications with the system controller.
- Switching between digital and analog dimmers under serial data control
- High generality since display data is displayed without the intervention of a decoder
- All segments can be turned off with the $\overline{\text{BLK}}$ pin

- **CCB is a trademark of SANYO ELECTRIC CO., LTD.**
- **CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.**

Package Dimensions

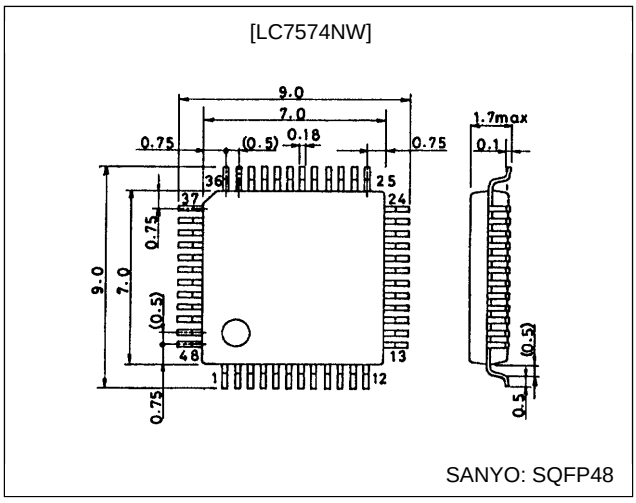
unit: mm

3156-QFP48E



unit: mm

3163A-SQFP48



Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}	–0.3 to +6.5	V
	V_{FL} max	V_{FL}	–0.3 to +21.0	V
Input voltage	$V_{IN}1$	DI, CL, CE, $\overline{BLK}$, DIM	–0.3 to +6.5	V
	$V_{IN}2$	OSC	–0.3 to V_{DD} + 0.3	V
Output voltage	$V_{OUT}1$	S1 to S37, G1, G2	–0.3 to V_{FL} + 0.3	V
	$V_{OUT}2$	OSC	–0.3 to V_{DD} + 0.3	V
Output current	$I_{OUT}1$	S1 to S37	5	mA
	$I_{OUT}2$	G1, G2	67	mA
Allowable power dissipation	Pd max	Ta = 85°C (LC7574NE)	250	mW
		Ta = 85°C (LC7574NW)	150	mW
Operating temperature	Topr		–40 to +85	°C
Storage temperature	Tstg		–50 to +125	°C

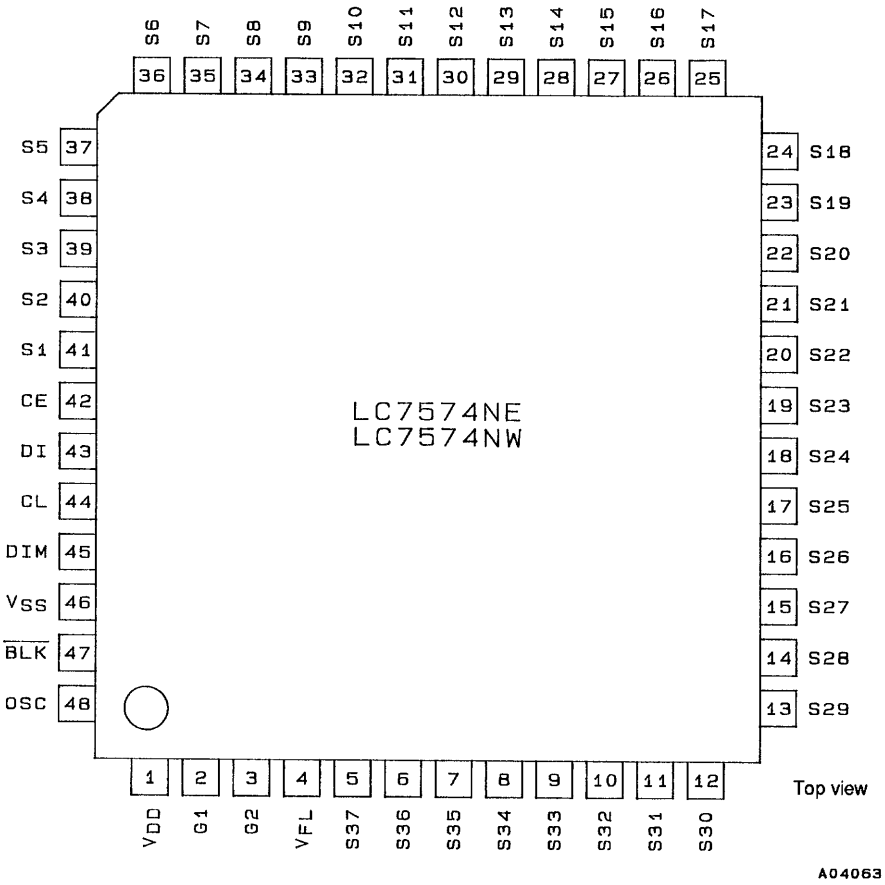
Allowable Operating Ranges at Ta = –40 to +85°C, V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}	V_{DD}	4.5	5.0	5.5	V
	V_{FL}	V_{FL}	8	12	18	V
Input high level voltage	V_{IH}	DI, CL, CE, $\overline{BLK}$	0.8 V_{DD}		5.5	V
Input low level voltage	V_{IL}	DI, CL, CE, $\overline{BLK}$	0		0.2 V_{DD}	V
Guaranteed oscillator range	f_{OSC}	OSC	0.4	1.6	3.0	MHz
Recommended external resistance	R_{OSC}	OSC		12		kΩ
Recommended external capacitance	C_{OSC}	OSC		50		pF
Low level clock pulse width	$t_{øL}$	CL: Figure 1	0.5			µs
High level clock pulse width	$t_{øH}$	CL: Figure 1	0.5			µs
Data setup time	t_{ds}	DI, CL: Figure 1	0.5			µs
Data hold time	t_{dh}	DI, CL: Figure 1	0.5			µs
CE wait time	t_{cp}	CE, CL: Figure 1	0.5			µs
CE setup time	t_{cs}	CE, CL: Figure 1	0.5			µs
CE hold time	t_{ch}	CE, CL: Figure 1	0.5			µs
$\overline{BLK}$ switching time	t_c	$\overline{BLK}$, CE: Figure 3	10			µs
Input voltage range	V_{IN}	DIM	0		+5.5	V

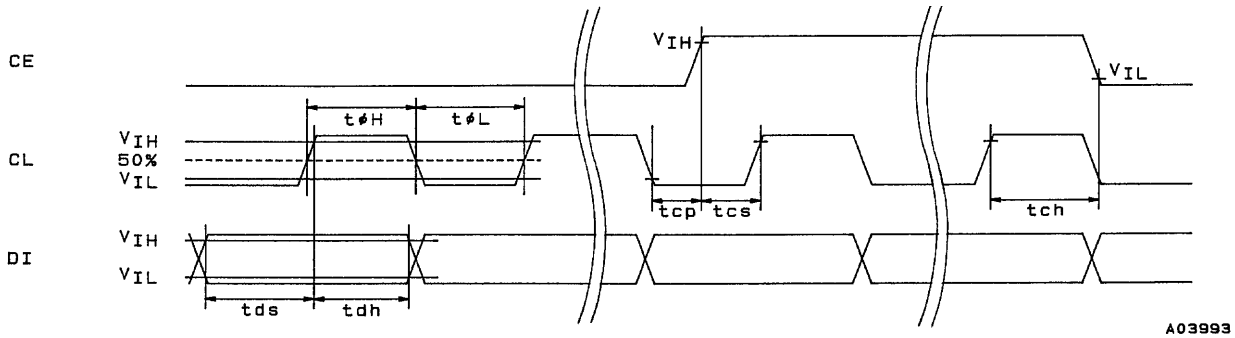
Electrical Characteristics in the Allowable Operating Ranges

Parameter	Symbol	Conditions	min	typ	max	Unit
Input high level current	I_{IH}	DI, CL, CE, $\overline{BLK}$, DIM: V_I = 5.5 V			5	µA
Input low level current	I_{IL}	DI, CL, CE, $\overline{BLK}$, DIM: V_I = 0 V	–5			µA
Output high level voltage	$V_{OH}1$	S1 to S37: I_O = 2 mA	V_{FL} – 0.6			V
	$V_{OH}2$	G1, G2: I_O = 25 mA	V_{FL} – 0.6			V
	$V_{OH}3$	G1, G2: I_O = 50 mA	V_{FL} – 1.3			V
Output low level voltage	V_{OL}	S1 to S37, G1, G2: I_O = –5 µA, Ta = 25°C	0.125	0.25	0.5	V
Oscillator frequency	f_{OSC}	R_{OSC} = 12 kΩ, C_{OSC} = 50 pF		1.6		MHz
Hysteresis voltage	V_H	DI, CL, CE, $\overline{BLK}$	0.5			V
A/D converter linearity error	Err	DIM	–1/2		+1/2	LSB
Current drain	I_{DD}	Outputs open: f_{OSC} = 1.6 MHz			10	mA

Pin Assignment



1. When CL is stopped at the low level



2. When CL is stopped at the high level

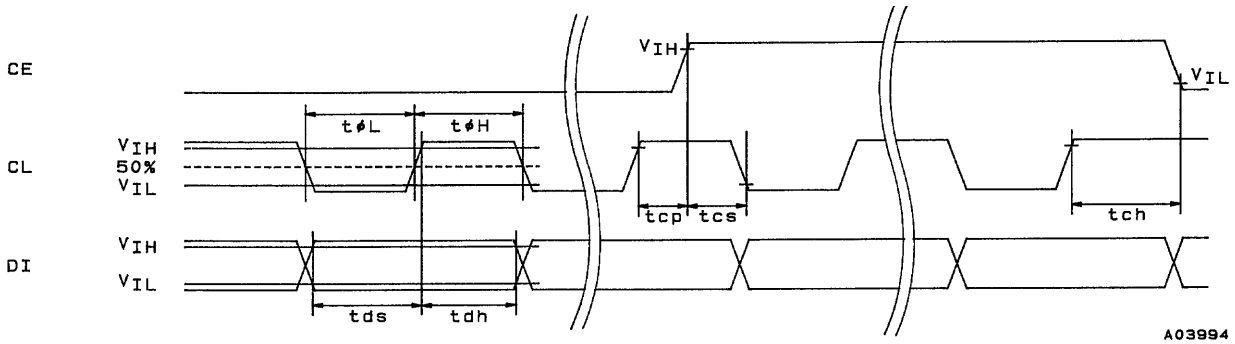
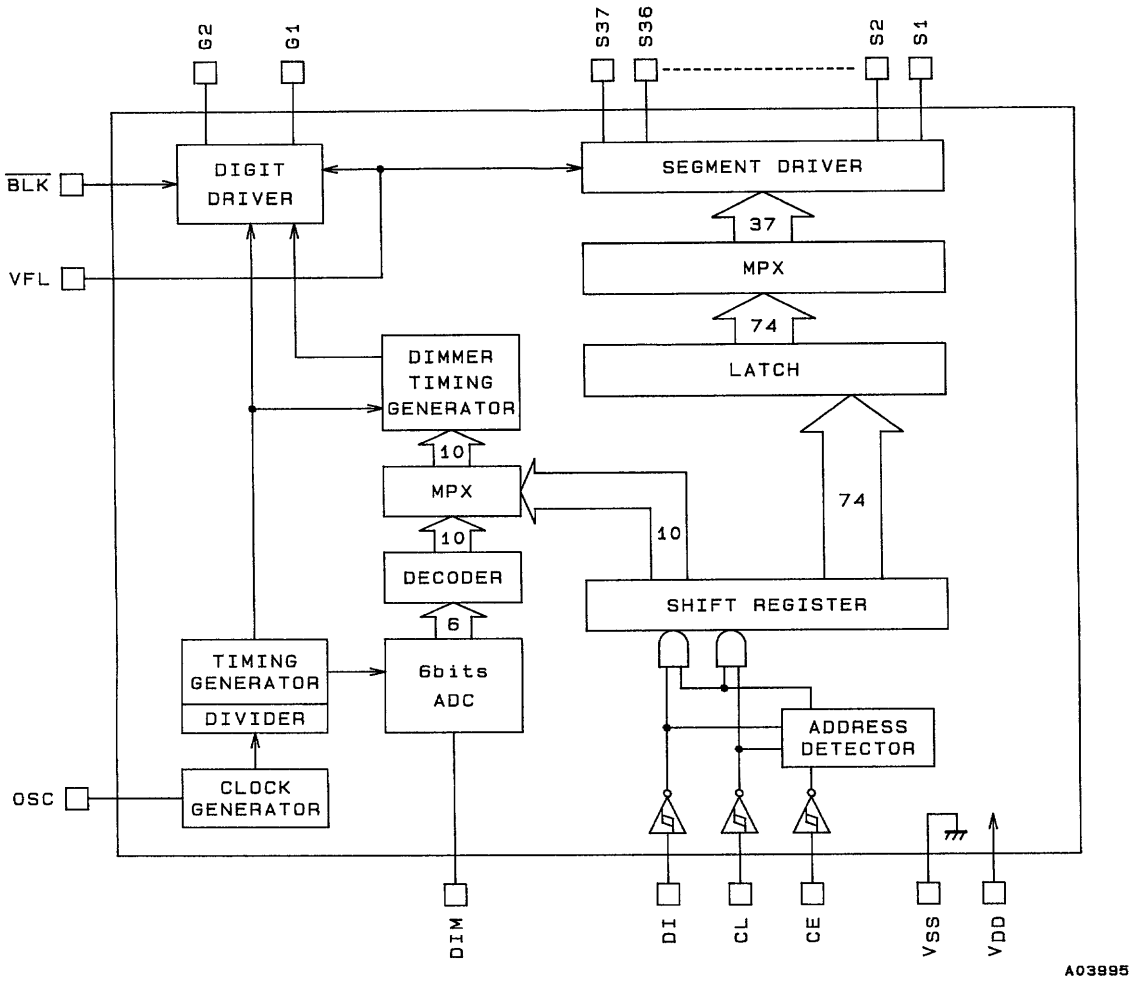


Figure 1

Block Diagram

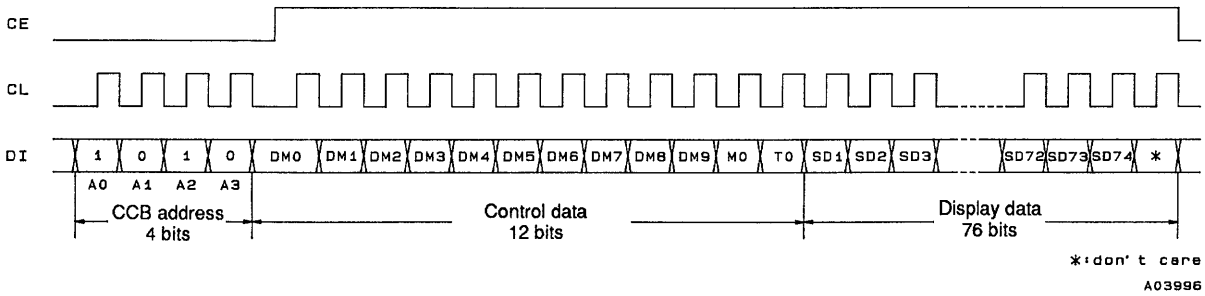


Pin Functions

Pin No.	Pin	I/O	Function		Handling when unused
4	V_{FL}	—	Driver block power supply. A voltage of between 8.0 and 18.0 V must be supplied.		—
1	V_{DD}	—	Logic block power supply. A voltage of between 4.5 and 5.5 V must be supplied.		—
46	V_{SS}	—	Ground. Must be connected to the system ground.		—
48	OSC	I/O	Oscillator connection. An oscillator circuit is formed by connecting an external resistor and capacitor to this pin.		V_{DD}
47	$\overline{BLK}$	I	Display off control input $\overline{BLK}$ = low (V_{SS}): Display off (G1 and G2 = low) $\overline{BLK}$ = high (V_{DD}): Display on Note that serial data can be transferred while the display is turned off.		GND
44	CL	I	Serial data transfer inputs. These pins must be connected to the system controller.	CL: synchronization clock DI: transfer data CE: chip enable	GND
43	DI				
42	CE				
45	DIM	I	When the analog dimmer is selected, the analog voltage applied to this pin controls the duty of the G1 and G2 digit output pins. Since a 6-bit A/D converter is applied to this analog voltage and that result is input to a decoder that provides a built-in dimmer curve, the relationship between the analog voltage and the duty can be specified as a mask program. Note that 63/96 · V_{DD} is the full-scale level for the 6-bit A/D converter.		GND
2, 3	G1, G2	O	Digit outputs. The frame frequency f_O is (f_{OSC}/4096) Hz		Open
41 to 5	S1 to S37	O	Segment outputs for displaying the display data transferred by serial data input.		Open

Serial Data Transfer Format

1. When CL is stopped at the low level



2. When CL is stopped at the high level

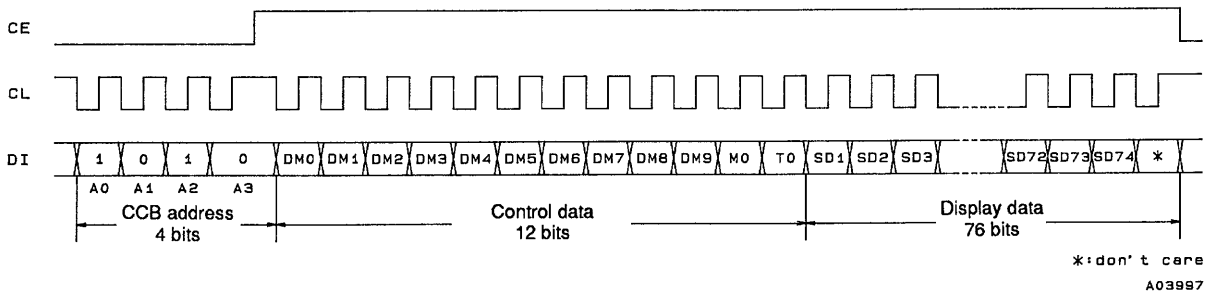


Figure 2

CCB address: Transfer 1010_B, as shown in Figure 2.

M0: Digital/analog dimmer selection data
- M0 = 0 .....Digital dimmer
- M0 = 1 .....Analog dimmer

DM0 to DM9: Dimmer data

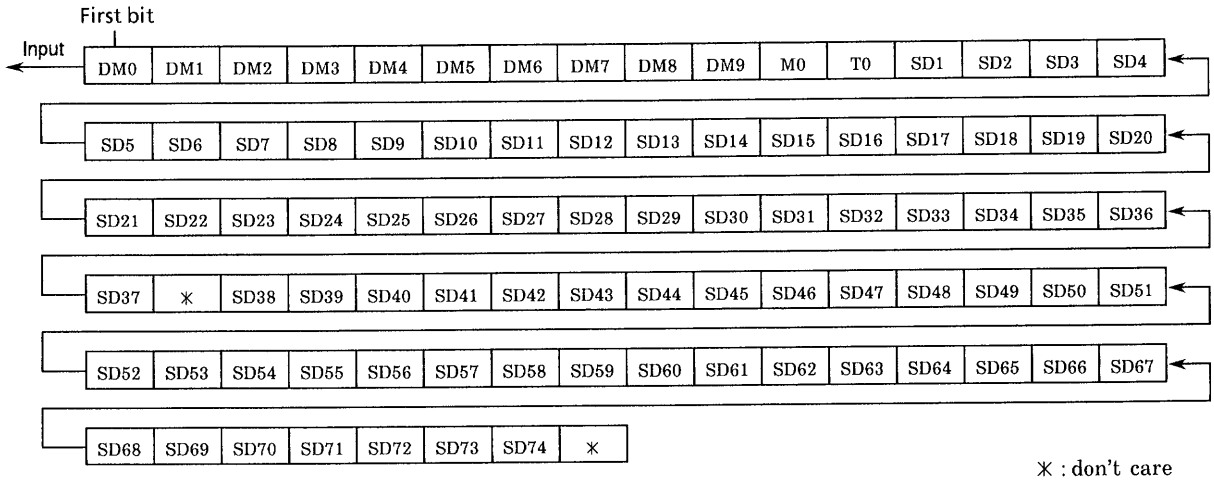
This data controls the duty of the G1 and G2 digit output pins when the digital dimmer is selected. This data consists of 10 bits, of which DM0 is the LSB. Note that display intensity can be adjusted by controlling the duty of the G1 and G2 digit output pins. (The DM0 to DM9 dimmer data is ignored when the analog dimmer is selected.)

SD1 to SD74: Display data
- SD1 to SD37.....Display data for the G1 digit output pin
- SD38 to SD74.....Display data for the G2 digit output pin
- SDn (n = 1 to 74) = 1.....Display on
- SDn (n = 1 to 74) = 0.....Display off

T0: Test data

The T0 bit must be set to 0.

Serial Data Format



Correspondence between Display Data (SD1 to SD74) and Segment Output Pins

Segment output pin	G1	G2
S1	SD1	SD38
S2	SD2	SD39
S3	SD3	SD40
S4	SD4	SD41
S5	SD5	SD42
S6	SD6	SD43
S7	SD7	SD44
S8	SD8	SD45
S9	SD9	SD46
S10	SD10	SD47
S11	SD11	SD48
S12	SD12	SD49
S13	SD13	SD50
S14	SD14	SD51
S15	SD15	SD52
S16	SD16	SD53
S17	SD17	SD54
S18	SD18	SD55
S19	SD19	SD56

Segment output pin	G1	G2
S20	SD20	SD57
S21	SD21	SD58
S22	SD22	SD59
S23	SD23	SD60
S24	SD24	SD61
S25	SD25	SD62
S26	SD26	SD63
S27	SD27	SD64
S28	SD28	SD65
S29	SD29	SD66
S30	SD30	SD67
S31	SD31	SD68
S32	SD32	SD69
S33	SD33	SD70
S34	SD34	SD71
S35	SD35	SD72
S36	SD36	SD73
S37	SD37	SD74

Example: Segment output pin S11 is controlled as follows:

Display data		Segment output pin S11 state
SD11	SD48	
0	0	The segments corresponding to both the G1 and G2 digit output pins are off.
0	1	The segment corresponding to the G2 digit output pin is on.
1	0	The segment corresponding to the G1 digit output pin is on.
1	1	The segments corresponding to both the G1 and G2 digit output pins are on.

$\overline{\text{BLK}}$ and the Display Control

Since the LSI internal data (SD1 to SD74 and the control data) is undefined when power is first applied, the display is off (G1 and G2 = low) by setting the $\overline{\text{BLK}}$ pin low at the same time as power is applied. Then, meaningless display at power on can be prevented by transferring all 92 bits of serial data from the controller while the display is off and setting $\overline{\text{BLK}}$ pin high after the transfer completes. (See Figure 3.)

Power Supply Sequence

The following sequences must be observed when power is turned on and off. (See Figure 3)

- Power on: Logic block power supply (V_{DD}) on → Driver block power supply (V_{FL}) on
- Power off: Driver block power supply (V_{FL}) off → Logic block power supply (V_{DD}) off

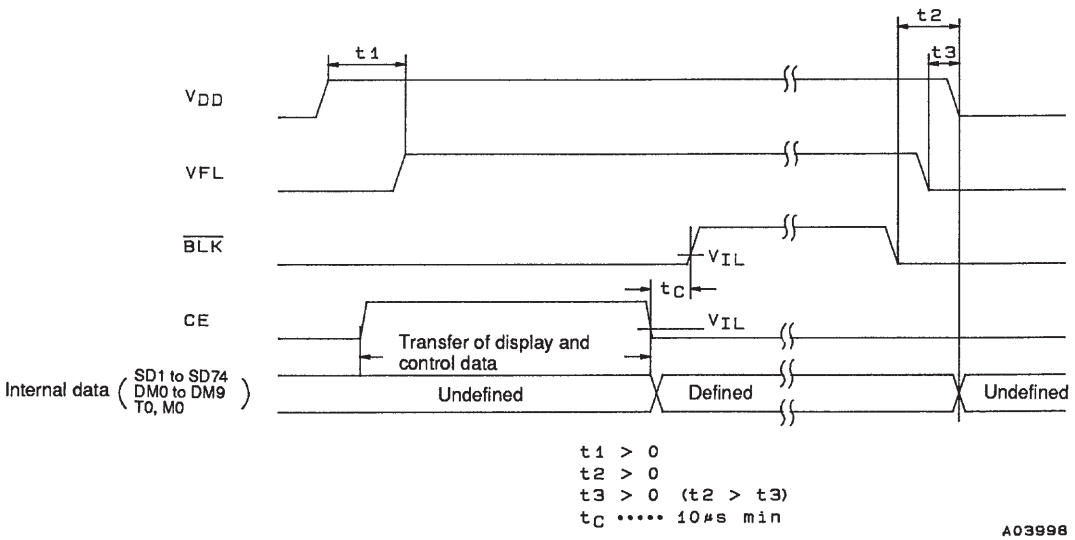
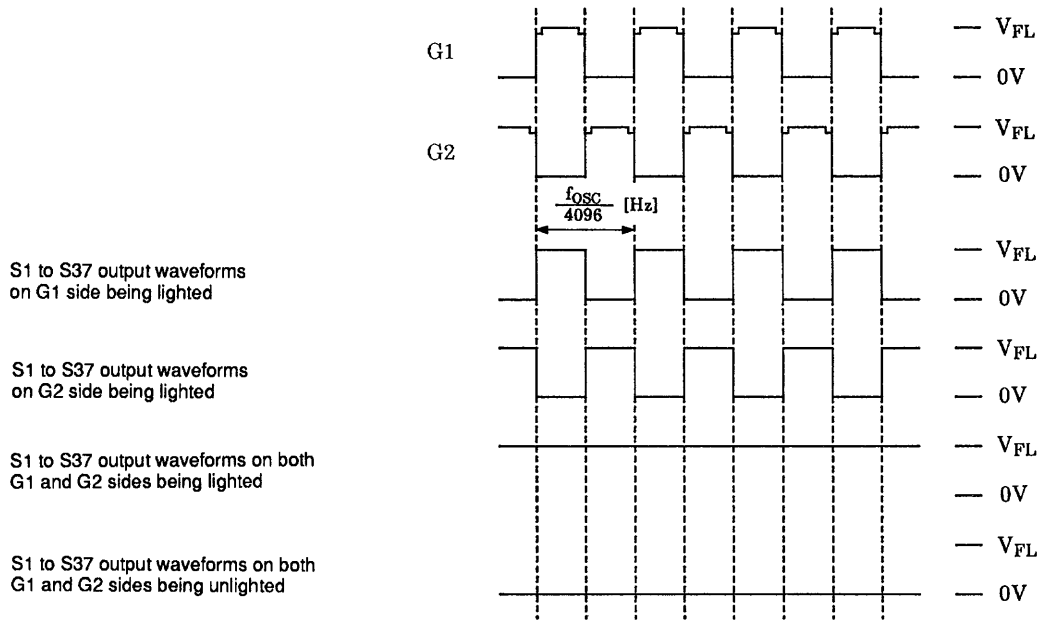


Figure 3

Output Waveforms (S1 to S37)



Relation between Segment and Digit Outputs

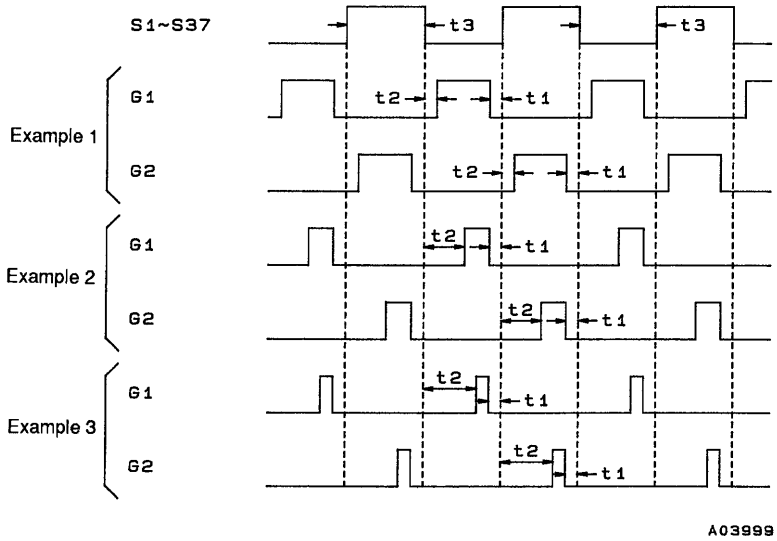


Figure 4

Descriptions

1. Consider the examples shown in Figure 4, where data is set up so that the segment outputs S1 to S37 output a low level on the G1 digit output timing and a high level on the G2 digit output timing. (Here, the G2 side being lighted)
2. The digit output G1 and G2 waveforms in Example 1 are output when the 10 bits of dimmer data (DM0 to DM9) are set to $3FE_H$. The relation between t1 and the oscillator frequency f_{OSC} is:

   $t1 = 2/f_{OSC}$.

   For example, if f_{OSC} = 1.6 [MHz], then

   t1 = 2/1.6 [MHz] = 1.25 [μs].

   Note that t1 and t2 are the same period in Example 1.
3. The digit output G1 and G2 waveforms in Example 2 are those when the dimmer data (DM0 to DM9) are set to a smaller value. Although the time t1, which is from the point where digit output falls to segment output changes, does not change, the time t2, which is from the point where segment output changes to the time the digit output rises, becomes longer. When the dimmer data (DM0 to DM9) are set to $0FF_H$ and f_{OSC} is 1.6 [MHz], then the frame frequency f_O is:

   $f_O = 1/(t3 \times 2)$
   $= f_{OSC}/4096$
   = 391 [Hz],

   and,

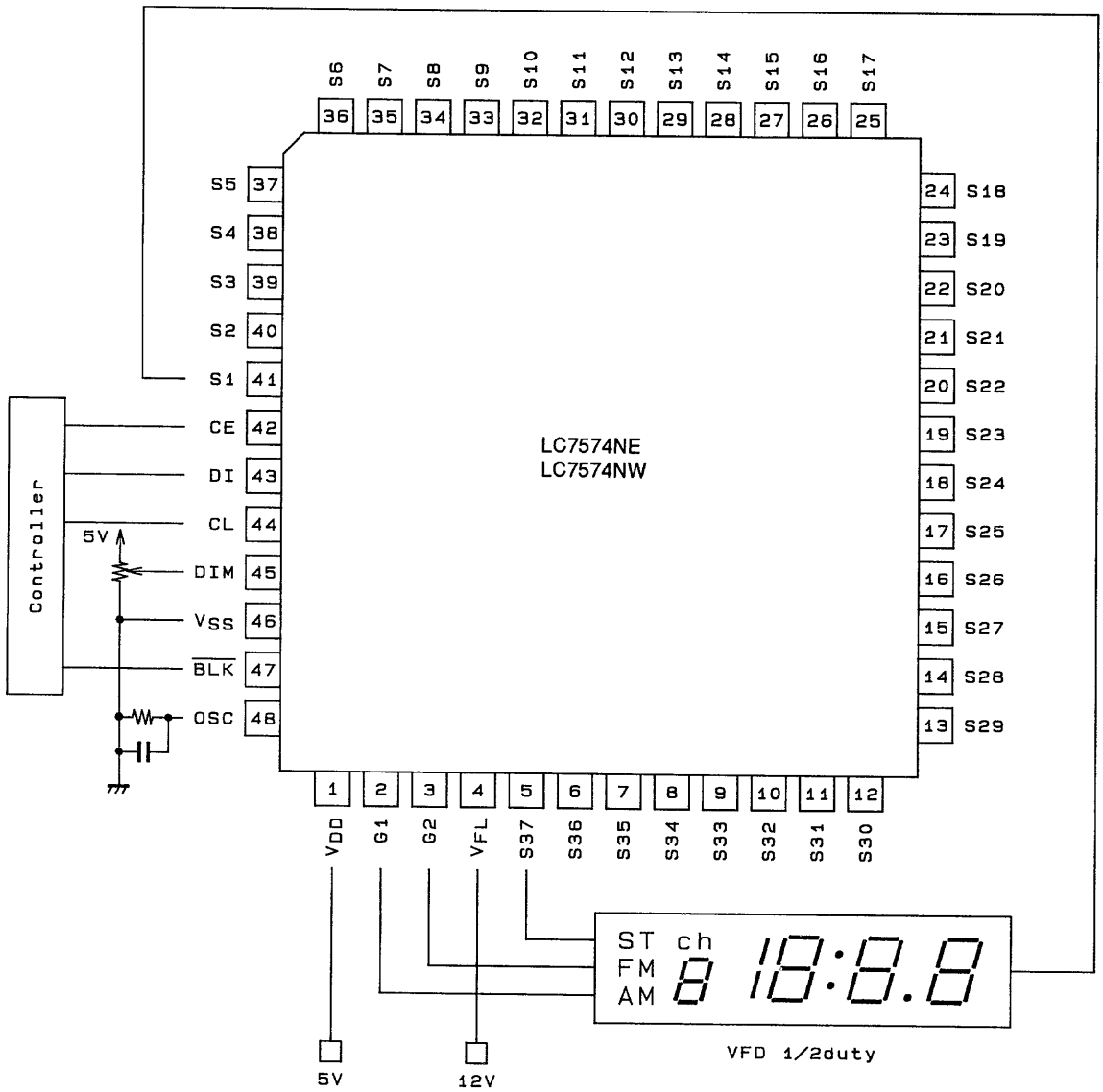
   t3 = 1.28 [ms].

   Therefore,

   $$t2 = \frac{(1.28\ [\text{ms}] - 1.25\ [\mu\text{s}] \times 2) \times (3FF_H - 0FF_H)}{1023} = 0.96\ [\text{ms}].$$

4. When the dimmer data (DM0 to DM9) are set to an even smaller value, the time t2, which is from the point where segment output changes to the time the digit output rises, becomes even longer, as in Example 3. Note that t1 does not change here, either.

Sample Application Circuit



Usage Notes

1. Notes on the segment and digit waveforms

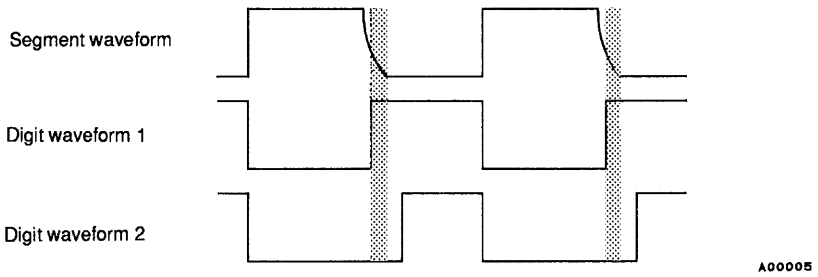


Figure 5

The segment waveform is distorted by the VFD panel used and the wiring, and furthermore, in the case of being used with essentially no dimming as in the digit waveform 1, as shown in Figure 5, the VFD panel glow dimly. By carefully considering the segment waveform, it can be seen that this problem can be resolved by applying an adequate amount of dimming, as shown in Digit waveform 2. When f_{OSC} is 1.6 [MHz], we recommend using 10 bits of dimmer data in the range 000_H to $3E0_H$.