Ordering number : EN※4910

CMOS LSI

No. ※4910

LC8230

MPEG Audio Decoder LSI

Preliminary

Overview

The LC8230 audio decoder decodes coded data that was compressed in conformance with layers 1 and 2 of the MPEG 1 audio standard (ISO/IEC 11172-3). It outputs a PCM signal that can be directly transferred to a D/A converter.

Features

- Support for intensity stereo
- Direct connection to either a 68000 or and 8086 family CPU
- Direct connection to either an 8- or 16-bit bus
- Built-in output attenuator that conforms to the CD-I specifications
- Coded data is temporarily stored in an external SRAM (8 kwords × 8 bits, 100 ns access time). The external SRAM is connected directly to the LC8230. No external control circuits are required since the LC8230 performs all buffer management and address generation for the SRAM.
- Support for two coded data transfer techniques: DMA (direct memory access) and writing by the external CPU (software transfer).
- Power-down mode in which power dissipation is significantly reduced when the chip is not operating.
- The external clock input frequency depends on the sampling frequency (fs). The input clock frequency is 384 fs.

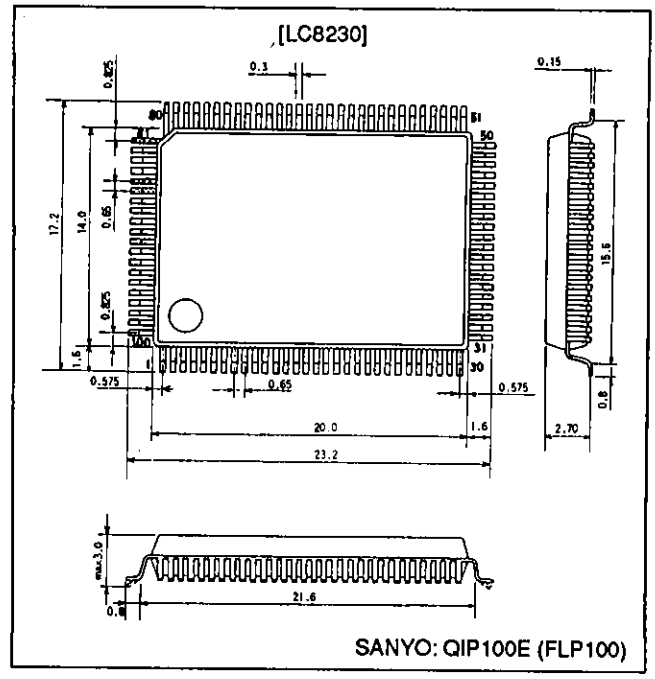
Sampling frequency	External clock input frequency
32 kHz	12.2880 MHz
44.1 kHz	16.9344 MHz
48 kHz	18.4320 MHz

- Extraction of up to 1 kbyte of ancillary data
- 100-pin QFP package
- Low power dissipation: 200 mW (operating)

Package Dimensions

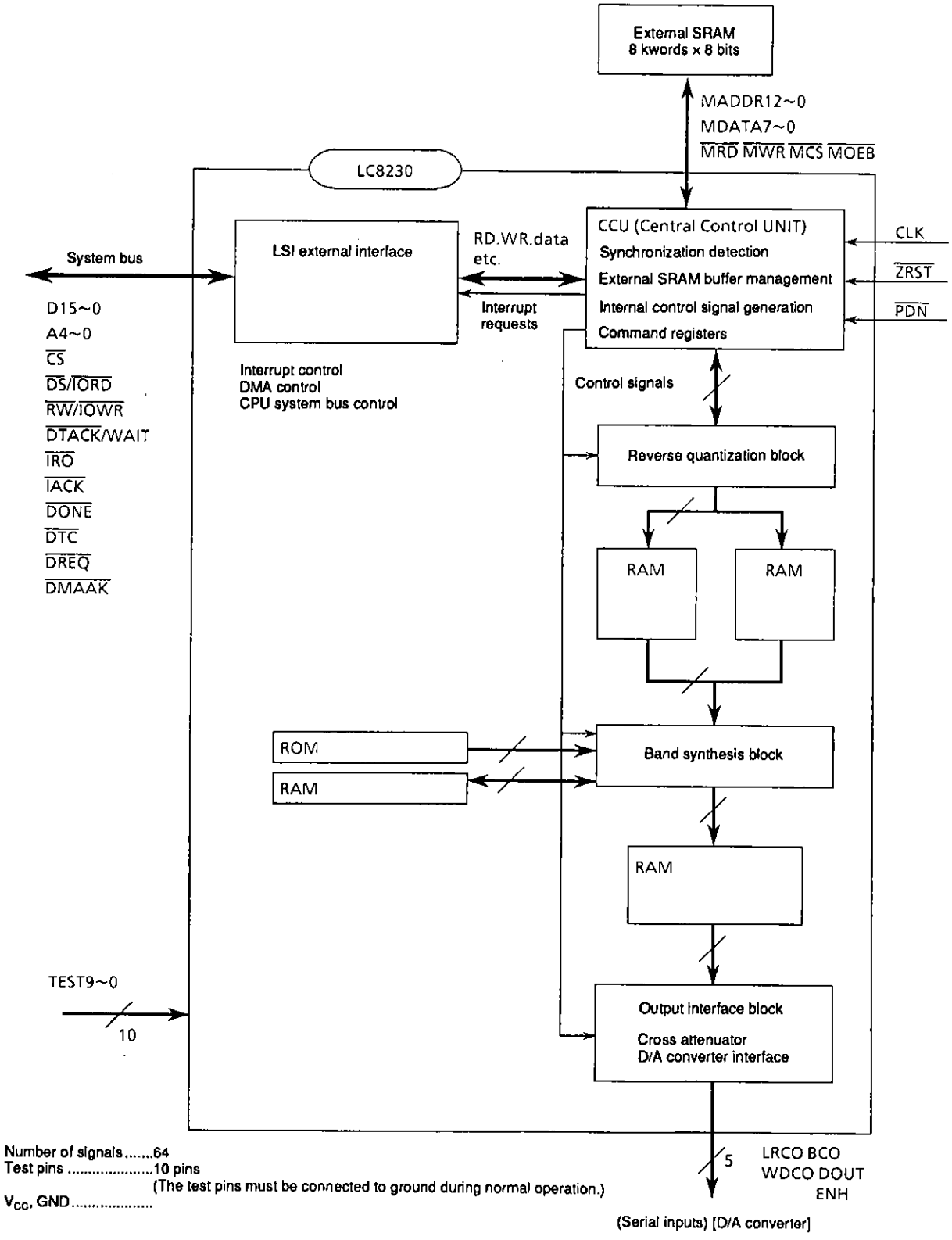
unit: mm

3151-QIP100E (FLP100)



SANYO Electric Co., Ltd. Semiconductor Business Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

Circuit Block Organization



Number of signals.....64
Test pins .....10 pins
(The test pins must be connected to ground during normal operation.)
V_{CC}, GND.....

Pin Functions

Pin No.	Symbol	Type	Definition
1	A0	I	Register address, A0 is used only by 8-bit CPUs
2	A1	I	
3	A2	I	
4	A3	I	
5	A4	I	
6	V_{SS}	P	
7	D0	B	Data port (8-bit CPUs use D0 to D7)
8	D1	B	
9	D2	B	
10	D3	B	
11	V_{DD}	P	
12	D4	B	Data port (8-bit CPUs use D0 to D7)
13	D5	B	
14	D6	B	
15	D7	B	
16	V_{SS}	P	
17	D8	B	Data port (8-bit CPUs use D0 to D7)
18	D9	B	
19	D10	B	
20	D11	B	
21	V_{DD}	P	
22	D12	B	Data port (8-bit CPUs use D0 to D7)
23	D13	B	
24	D14	B	
25	D15	B	
26	V_{SS}	P	
27	$\overline{CS}$	I	Chip select
28	$\overline{DS}$/$\overline{IORD}$	I	68000 data strobe, 8086 I/O read
29	$\overline{RW}$/$\overline{IOWR}$	I	68000 read/write, 8086 I/O read
30	$\overline{DTACK}$/WAIT	O	68000 data acknowledge, 8086 wait
31	ENH	O	De-emphasis applied
32	DOUT	O	PCM data serial output
33	BCO	O	64 fs output for the 32-slot case and 48 fs output for the 24-slot case
34	WDCO	O	2 fs clock output
35	LRCO	O	fs clock output
36	NC	NC	
37	NC	NC	
38	TEST1	I	LSI test pins
39	TEST4	I	
40	V_{SS}	P	
41	V_{DD}	P	
42	TEST6	I	LSI test pins
43	TEST3	I	
44	TEST8	I	
45	NC	NC	
46	$\overline{PDN}$	I	Power-down mode
47	NC	NC	
48	NC	NC	
49	CLK	I	Input clock
50	V_{SS}	P	
51	$\overline{MOEB}$	O	External SRAM output enable
52	$\overline{MWR}$	O	External SRAM write
53	$\overline{MCS}$	O	External SRAM chip select
54	$\overline{MRD}$	O	External SRAM read

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Pin No.	Symbol	Type	Definition
55	V_{DD}	P	
56	MDATA7	B	External SRAM data
57	MDATA6	B	
58	MDATA5	B	
59	MDATA4	B	
60	V_{SS}	P	
61	MDATA3	B	External SRAM data
62	MDATA2	B	
63	MDATA1	B	
64	MDATA0	B	
65	V_{DD}	P	
66	MADDR12	O	External SRAM address
67	MADDR11	O	
68	MADDR10	O	
69	MADDR9	O	
70	V_{SS}	P	
71	MADDR8	O	External SRAM address
72	MADDR7	O	
73	MADDR6	O	
74	MADDR5	O	
75	MADDR4	O	
76	V_{DD}	P	
77	MADDR3	O	External SRAM address
78	MADDR2	O	
79	MADDR1	O	
80	MADDR0	O	
81	V_{SS}	P	
82	NC	NC	
83	NC	NC	
84	$\overline{ZRST}$	I	Reset
85	NC	NC	
86	TEST9	I	LSI test pins
87	TEST2	I	
88	TEST5	I	
89	V_{DD}	P	
90	V_{SS}	P	
91	NC	NC	
92	TEST0	I	LSI test pins
93	TEST7	I	
94	$\overline{IRQ}$	O	Interrupt request
95	$\overline{IACK}$	I	Interrupt acknowledge
96	$\overline{DONE}$	I	DMA transfer complete
97	$\overline{DTC}$	I	Data latch signal used by the 68450 DMAC
98	$\overline{DREQ}$	O	DMA request
99	$\overline{DMAAK}$	I	DMA acknowledge
100	NC	NC	

Registers

Register overview (16-bit units)

Address	Type	Register	Function
0h	W	CD	Code data (for software writes)
2h	R	STA1	Status information (header information) 1
4h	R	STA2	Status information (header information) 2
6h	W	CTL	Control register
8h	W	ITV	Interrupt vector
Ah	W	ITM	Interrupt mask
Ch	R	ITS	Interrupt status
Eh	R/W	MCF	68000/8086 switching, 8/16-bit switching
10h	R	ACD	Ancillary data read
12h	W	BUF	Buffer size (transfer byte count)
14h	W	ATN1	Left input attenuation parameter
16h	W	ATN2	Right input attenuation parameter

Address: byte address, Type: W = write, R = read, R/W = read/write

Register Functions

Register	Function/bit allocation
CD (code data)	When software data transfer is used, data is written to this register. In 8-bit mode it is possible to continuously write to even addresses using only this register. This register can also be written in 16-bit mode.
STA1 (status1)	Bits 1, 0; Expansion mode, intensity stereo 0 0 bound = 4 0 1 bound = 8 1 0 bound = 12 1 1 bound = 16 Bits 3, 2; Mode 0 0 Stereo 0 1 Intensity stereo 1 0 Dual channel 1 1 Single channel Bit 4; Private Bit 5; Padding Bits 7, 6; Sampling frequency 0 0 44.1 kHz 0 1 48 kHz 1 0 32 kHz 1 1 Reserved Bits 11, 10, 9, 8; Bit rate index Bit 12; Protection Bits 14, 13; Mode 0 0 Reserved 0 1 Layer 3 1 0 Layer 2 1 1 Layer 1 Bit 15; ID, 1: MPEG
STAT2 (status2)	Bits 6 to 0; Ancillary data byte count Bit 7; 1: Ancillary data present, 0: No ancillary data Bit 8; 1:CRC error, 0: CRC no error Bits 10, 9; 00: No emphasis, 01: 50/15 emphasis used Bit 11; Original Bit 12; Copyright

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Register	Function/bit allocation
CTL (control)	Bit 0; 1: Software reset Bit 1; Start (expansion processing)] Bit 2; 1: Stop Bit 3; 1: Pulse interrupt, 0: Level interrupt Bit 4; 1: Interrupt signal clear Bit 5; 1: DMA start Bit 6; Reserved Bit 7; Reserved Bits 10 to 8; Output format selection 0 0 0: 32-slot, MSB first, left justified 0 0 1: 32-slot, LSB first, left justified 0 1 0: 32-slot, MSB first, left justified 0 1 1: Reserved 1 0 0: 24-slot, MSB first, left justified 1 0 1: 24-slot, LSB first, left justified 1 1 0: 24-slot, MSB first, left justified 1 1 1: Reserved
ITV (interrupt vector)	Interrupt vector
ITM (interrupt mask)	Bit 0; 1: Status ready interrupt enable Bit 1; 1: Buffer ready interrupt enable Bit 2; 1: End code detection interrupt enable (Interrupts are initially disabled following a reset.)
ITS (interrupt status)	Bit 0; 1: Status ready Bit 1; 1: Buffer ready Bit 2; 1: End code detected
MCF (microprocessor I/F conf)	Bit 0; 1: 16 bits, 0: 8 bits Bit 1; 1: 68000, 0: 8086 Bit 2; 1: MCF register lock Bit 4; Register byte order inversion Bit 5; Code byte order inversion
ACD (ancillary data)	Ancillary data read
BUF (transfer buffer size)	Transfer byte count specification
ATN1 (attenuator Lch input)	Bits 7 to 0; Left input/right output attenuator parameter Bits 15 to 8; Left input/right output attenuator parameter
ATN2 (attenuator Rch input)	Bits 7 to 0; Right input/left output attenuator parameter Bits 15 to 8; Right input/left output attenuator parameter

Specifications

DC Characteristics at Ta = –30 to 70°C, V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Input high level voltage	V_{IH}	TTL compatible: *4, 5	2.2			V
Input low level voltage	V_{IL}	TTL compatible: *4, 5			0.8	V
Input high level voltage	V_{IH}	CMOS compatible: *1, 3	0.7 V_{DD}			V
Input low level voltage	V_{IL}	CMOS compatible: *1, 3			0.3 V_{DD}	V
Input high level voltage	V_{IH}	CMOS compatible Schmitt inputs: *2	0.8 V_{DD}			V
Input low level voltage	V_{IL}	CMOS compatible Schmitt inputs: *2			0.2 V_{DD}	V
Input high level voltage	V_{IH}	I_{OH} = –3 mA: *5, 6	V_{DD} – 2.1			V
Input low level voltage	V_{IL}	I_{OL} = 3 mA: *5, 6			0.4	V
Input leakage current	I_L	V_I = V_{SS}, V_{DD}: *1, 2, 3, 4, 5	–10		+10	µA
Output leakage current	I_{OZ}	For high impedance outputs: *5	–10		+10	µA

Note: The applicable pin sets are listed below.

(Input)

1. CLK
2. PDN, $\overline{ZRST}$
3. TEST0 to 9
4. A0 to 4, $\overline{CS}$, $\overline{DMAAK}$, $\overline{DONE}$, DS, $\overline{DTC}$, $\overline{IACK}$, RW

(Input)

5. D0 to 15, MD0 to 7

(Output)

6. BCO, DOUT, DREQ, DTACK, ENH, IRQ, LRCO, MA0 to 12, MCS, MOEB, MRD, MWR, WDCO