Ordering number : EN*5239A

CMOS LSI

LE28F4001M, T, R-15/20

4 MEG (524288 words × 8 bits) Flash Memory

Preliminary

Overview

The LE28F4001 Series ICs are 524288-word × 8-bit flash memory products that support on-board reprogramming and feature 5 V single-voltage power supply operation. CMOS peripheral circuits were adopted for high speed, low power, and ease of use. These products support a sector (256 bytes) erase function for fast data rewriting.

Features

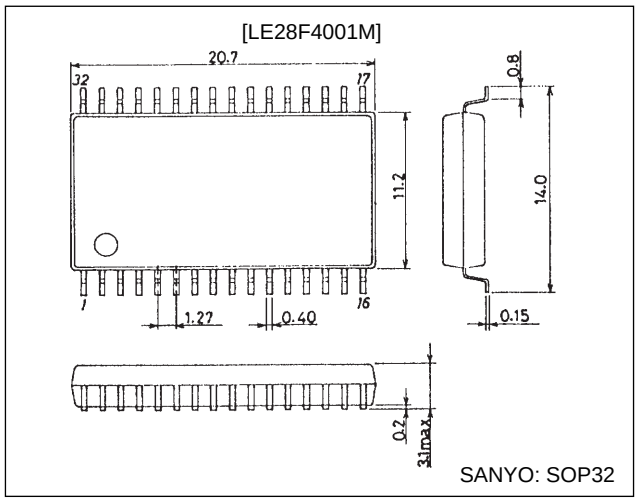
- Fabricated in a highly reliable 2-layer polysilicon CMOS flash EEPROM process.
- Read and write operation from a 5 V single-voltage power supply
- Sector erase function: 256 bytes per sector
- Fast access time: 150/200 ns
- Low power
  - — Operating current (read): 25 mA (maximum)
  - — Standby current: 20 µA (maximum)
- Highly reliable read and write operations
  - — Sector write cycles: 10^4 cycles
  - — Data retention time: 10 years
- Address and data latches
- Self-timer erase and programming
- Byte programming time: 35 µs (maximum)
- Write complete detection: Toggle bit and data polling
- Hardware and software data protection
- Pin assignment conforms to the JEDEC byte-wide EEPROM standard
- Packages

  SOP 32-pin (525 mil) plastic package :LE28F4001M
  TSOP 40-pin (10 × 14 mm) plastic package :LE28F4001T
  TSOP 40-pin (10 × 14 mm) plastic package :LE28F4001R

Package Dimensions

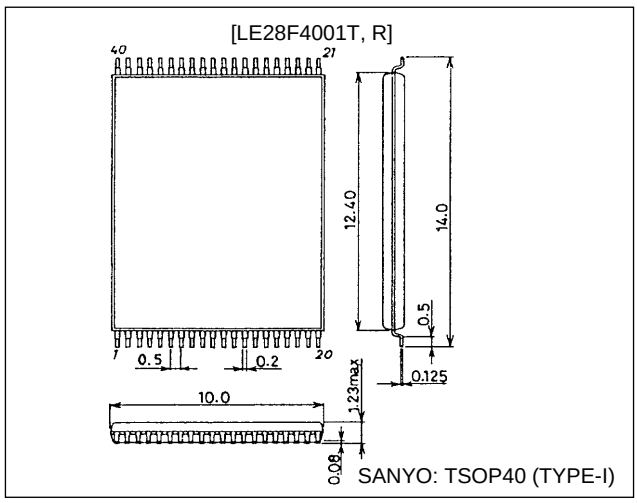
unit: mm

3205-SOP32



unit: mm

3087A-TSOP40



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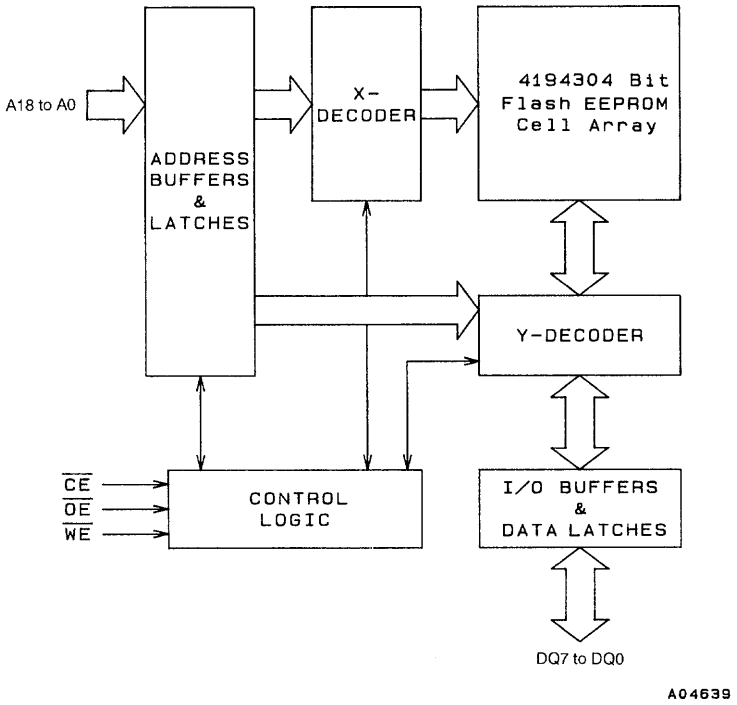
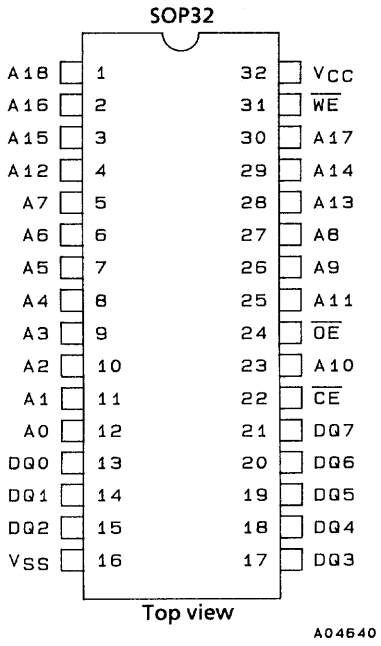
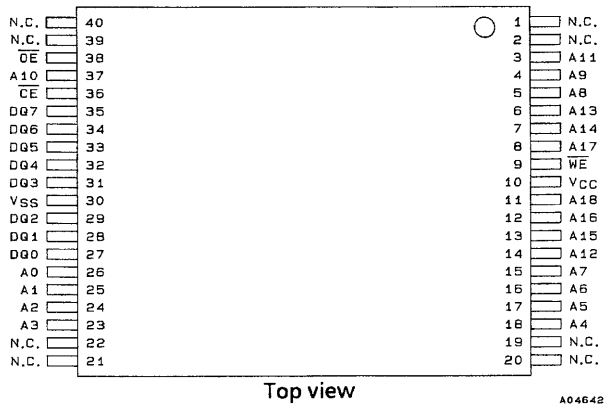
Block Diagram



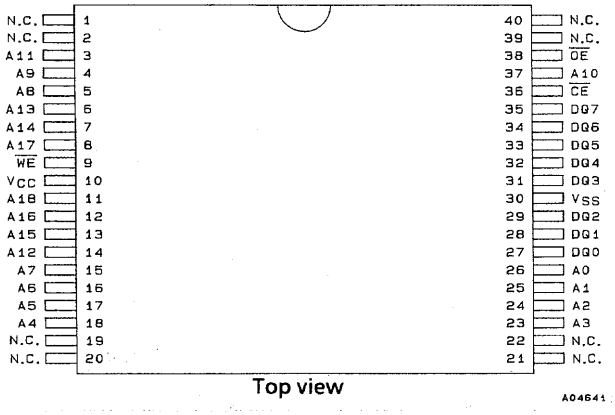
Pin Assignments



TSOP40 Standard



TSOP40 Reversed



Pin Functions

Symbol	Pin	Functions
A18 to A0	Address input	Supply the memory address to these pins. The address is latched internally during a write cycle.
DQ7 to DQ0	Data input and output	These pins output data during a read cycle and input data during a write cycle. Data is latched internally during a write cycle. Outputs go to the high-impedance state when either $\overline{OE}$ or $\overline{CE}$ is high.
$\overline{CE}$	Chip enable	The device is active when $\overline{CE}$ is low. When $\overline{CE}$ is high, the device becomes unselected and goes to the standby state.
$\overline{OE}$	Output enable	Makes the data output buffers active. $\overline{OE}$ is a low-active input.
$\overline{WE}$	Write enable	Makes the write operation active. $\overline{WE}$ is a low-active input.
V_{CC}	Power supply	Apply 5 V (±10%) to this pin.
V_{SS}	Ground	
N.C.	No connection	These pins must be left open.

Function Logic

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A18 to A0	DQ7 to DQ0
Read	V_{IL}	V_{IL}	V_{IH}	A_{IN}	D_{OUT}
Write	V_{IL}	V_{IH}	V_{IL}	A_{IN}	D_{IN}
Standby or write inhibit	V_{IH}	X	X	X	High-Z
Write inhibit	X	V_{IL}	X	X	High-Z/D_{OUT}
	X	X	V_{IH}	X	High-Z/D_{OUT}
Product identification	V_{IL}	V_{IL}	V_{IH}	A18 to A10 = V_{IL}, A8 to A1 = V_{IL}, A9 = 12 V, A0 = V_{IL}	Manufacturer code (BF)
				A18 to A10 = V_{IL}, A8 to A1 = V_{IL} A9 = 12 V, A0 = V_{IH}	Device code (04)

Command Settings

Command	Request cycle	Setup command cycle			Execute command cycle			SDP
		Operation	Address	Data	Operation	Address	Data	
Sector erase	2	Write	X	20H	Write	SA	D0H	N
Byte program	2	Write	X	10H	Write	PA	PD	N
Reset	1	Write	X	FFH				Y
Read ID	3	Write	X	90H	Read	(7)	(7)	Y
Software data unprotect	7	See Figure 9.						
Software data protect	7	See Figure 10.						

Notes on Command Settings

1. Type definitions: X = Don't care
2. Address definitions: SA = Sector Address = A18 to A8; sector size = 256 bytes; A7 to A0 = X for this command.
3. Address definitions: PA = Program Address = A18 to A0.
4. Data definition: PD = Program Data, H = number in hex.
5. SDP = Software Data Protect mode using 7-read-cycle sequence.
   Y = the operation can be executed with software data protect enabled. N = the operation cannot be executed with software data protect enabled.
6. Refer to figures 9 and 10 for the 7-read-cycle sequence software data protection.
7. Address 0000H retrieves the manufacturer code of BF (hex), address 0001H retrieves the device code of 04 (hex).

Product Overview

The LE28F4001 Series products are EEPROMs that support sector erase and byte programming functions and that feature a 512K × 8 organization. These products support both erase and programming from a 5-V single-voltage power supply, conform to the JEDEC standards for byte-wide memory pin assignments, and are pin compatible with industry standard EPROMs, flash EPROMs, and EEPROMs.
The LE28F4001 Series products, provide a 35 μs maximum byte programming time and a 4 ms sector erase time. Programming and erase operations can both be optimized by using the toggle bit and $\overline{\text{Data}}$ polling functions that indicate the completion of the write cycle. To protect data against unintentional writes, these products provide both hardware and software data protection schemes. The LE28F4001 Series products, guarantee 10^4 sector write cycles. The data retention time is ten years or longer.
The LE28F4001 Series functional block diagram and the 40-pin TSOP and 32-pin SOP package pin assignments are shown on page 2, and the pin functions and command settings are listed on page 3.

Device Operation

Commands are used to execute the device's memory functions. Commands are written to the command register with standard microprocessor write timing. Commands are written by setting $\overline{\text{WE}}$ low while $\overline{\text{CE}}$ is held low. The address is latched on the falling edge of either $\overline{\text{CE}}$ or $\overline{\text{WE}}$, whichever occurs later. Data is latched on the rising edge of either $\overline{\text{CE}}$ or $\overline{\text{WE}}$, whichever occurs first. However, the address is latched on the rising edge of either $\overline{\text{OE}}$ or $\overline{\text{CE}}$, whichever occurs first during the software write protect sequence.

Command Definition

The "Command Settings" section provided an overview and list of the LE28F4001 commands. This section describes the functions provided by those commands in detail.
Before executing the LE28F4001 Series byte programming or erase functions, the application system must execute the software data unprotect sequence.

1. Sector erase operation
   The sector erase operation consists of a setup command and an execute command. The setup commands sets the device to a state where all the bytes in the sector can be erased electrically. A single sector has 256 bytes. Since almost all applications use erase operations that are not whole-chip erase operations but rather are single sector erase operations, this sector erase function significantly increases the flexibility and ease of use of the LE28F4001 Series. The setup command is executed by writing 20H to the command register.
   An execute command (D0H) must be written to the command register to execute the sector erase operation. The sector erase operation starts on the rising edge of the $\overline{WE}$ pulse and is automatically completed under internal timing control. Figure 6 shows the timing waveforms for this operation.
   This two stage sequence in which a setup command and a following execute command are required guarantees that the memory at the sector specified by the address data will not be erased accidentally.
2. Sector erase flowchart
   The quick and reliable erasure of up to 256 bytes of memory can be achieved by following the sector erase flowchart shown in Figure 1. The whole operation consists of executing two commands. A sector erase operation completes in a maximum of 4 ms. Although the erase operation can be completed by executing a reset operation, the sector may not be completely erased if that reset is executed before the 4 ms time out period elapses. The erase command can be re-executed as many times as required before the erase completes. Excessive erasure cannot cause problems with the LE28F4001 Series products.
3. Byte programming operation
   The byte programming operation is started by writing a setup command (10H) to the command register.
   Once the setup command is executed, the execute command is started by the next $\overline{WE}$ pulse transition. Figure 7 shows the timing waveforms for this operation. The address and the data are latched internally on the falling edge and rising edge of the $\overline{WE}$ pulse, respectively. The $\overline{WE}$ rising edge also corresponds to the start of the programming operation. The programming operation is automatically completed under internal timing control. Figures 2 and 7 show the programming characteristics and waveforms.
   As mentioned previously, this two stage sequence in which a setup command and a following execute operation are required guarantees that the memory cells will not be programmed accidentally.
4. Byte programming flowchart
   Figure 2 shows the device data programming operation. This is effected by following the byte programming flowchart. The byte programming command sets up the byte to be written. The address is latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever is later. The data bus is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever is earlier, and the programming operation starts at that point. The completion of the write operation can be detected using either the toggle bit or by polling a $\overline{Data}$ pin.
5. Reset operation
   The reset command is a procedure for safely terminating an erase or programming command sequence. Writing FFH to the command register after issuing an erase or programming setup command will safely cancel that operation. The contents of memory will not be changed. The device goes to read mode after executing a reset command. The reset command cannot activate the software data protect function. Figure 8 shows the timing waveforms.
6. Read operation
   A read operation is performed by setting $\overline{CE}$ and $\overline{OE}$, and then $\overline{WE}$, to read mode. Figure 3 shows the read mode timing waveforms, and the read mode conditions are shown as “functional logic”. A read cycle from the host searches for the memory array data. The device remains in the read state until another command is written to the command register.
   As a default, the device will be in read mode in the write protect state from the time power is first applied until a command is written to the command register. The unprotect sequence must be executed to perform a write operation (erase or programming).
   The read operation is controlled by $\overline{CE}$ and $\overline{OE}$, and both must be set to the logic low level to activate the read function. When $\overline{CE}$ is at the logic high level, the chip is in the unselected state and only draws the standby current. $\overline{OE}$ controls the output pins. The device output pins will be in the high-impedance state if either $\overline{CE}$ or $\overline{OE}$ is at the logic high level.

7. Read ID operation
   The read ID (identifier) operation consists of a single command, 90H. A read operation from address 0000H will then return the manufacturer code (BFH) and a read operation from address 0001H will return the device code (04H). This operation is terminated by writing any other valid command to the command register.

Protecting Data from Unintentional Writes

To protect the accumulated stored data that the user intends to be nonvolatile, the LE28F4001 Series products provide both hardware and software functions to prevent unintentional writes when power is applied or cut off.

1. Hardware data protection
   The LE28F4001 Series products incorporate a hardware data function that prevents unintentional writes.
   - Write inhibit mode: Write operations are disabled if either $\overline{OE}$ is at the low logic level, $\overline{CE}$ is at the high logic level, or $\overline{WE}$ is at the high logic level.
   - Noise and glitch protection: $\overline{WE}$ pulses shorter than 15 ns will not execute a write operation.
   - The LE28F4001 Series products were designed to hold unintentional writes to a minimum by setting the device to read mode as the default when power is first applied.
2. Software data protection
   As mentioned earlier, the LE28F4001 Series is designed to provide even more protection from unintentional writes in software. To avoid unintentional erasure or programming of sector or device cells, when the application system attempts to execute a sector erase or programming operation it must execute that operation as a two-stage sequence consisting of first of a setup command and then an execute command.
   As a default, the LE28F4001 Series products go to the write protected state after power is applied. The device goes to the unprotected state after reads to seven specific addresses are executed consecutively. Those addresses are 1823H, 1820H, 1822H, 0418H, 041BH, 0419H, and 041AH. The address is latched on the rise of either $\overline{OE}$ or $\overline{CE}$, whichever is earlier. Similarly, the device can be set to the write protect state by reading from the following 7 addresses consecutively: 1823H, 1820H, 1822H, 0418H, 041BH, 0419H, and 040AH. Figures 9 and 10 show the software data protection waveforms for this 7-read-cycle sequence. The I/O pins can go to any state (high, low, or high impedance).

Detection of Write Operation Completion

To acquire the maximum performance from the device, the application must detect the completion of the programming cycle. The completion of the programming cycle can be detected by either $\overline{Data}$ polling or the toggle bit. This section describes these two detection mechanisms.

Actually, the completion of a nonvolatile memory write operation is asynchronous with respect to the application system. Therefore, it is possible that readout of either $\overline{Data}$ polling or toggle bit data could occur at the same time as the completion of the write cycle. If this happens the application system might get an incorrect result. That is, valid data could appear to contradict either DQ7 or DQ6. To prevent artificial rejections, if an incorrect result occurs, the software routine must include a loop to read the accessed location another 2 times. If both these readout cycles acquire valid data the device will have completed the write cycle. All other reject states are correct.

1. $\overline{Data}$ polling (DQ7)
   The LE28F4001 Series products provide a $\overline{Data}$ polling function that detects the completion of the programming cycle. During the program cycle, DQ7 reads out data that is the negation of the most recently loaded data. When the programming cycle has completed, DQ7, along with DQ0 to DQ6, reads out the last loaded data. Figure 11 shows the timing chart for this operation. For $\overline{Data}$ polling to function correctly, data must be erased before programming.
2. Toggle bit (DQ6)
   The DQ6 toggle bit is another technique for detecting the end of the erase or programming cycle. During an erase or programming operation the value of the DQ6 output alternates between 0 and 1, that is, the DQ6 output toggles between 0 and 1. When the erase or programming cycle completes, the toggling stops and the device goes to a normal read cycle. The toggle bit can be continuously monitored during an erase or programming cycle. Figure 12 shows the timing chart for toggle bit operation.
3. Continuous read
   One more technique for detecting the end of an erase or programming cycle is to read the same address twice in a row. If the same data is read twice in a row the erase or programming cycle has completed.

Product Identifier

Product identifier read is a mode provided so that applications can confirm that the device was manufactured by SANYO Electric Co., Ltd. This mode can be accessed by both hardware and software operations. A ROM writer is normally used with this hardware operation to recognize the correct algorithm for the SANYO LE28F4001 Series. We recommend that user use the software operation for recognizing this device. The "Functional Logic" section describes the hardware operation in detail. The manufacturer and device code are accessed in the same manner.

Decoupling Capacitors

Ceramic capacitors (0.1 μF) must be added between V_{CC} and V_{SS} for each device to assure stabile flash memory operation.

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Ratings	Unit	Note
Supply voltage	V_{CC}	–0.5 to +6.0	V	1
Input pin voltage	V_{IN}	–0.5 to V_{CC} + 0.5	V	1, 2
DQ pin voltage	$V_{I/O}$	–0.5 to V_{CC} + 0.5	V	1, 2
A9 pin voltage	V_{A9}	–0.5 to +14.0	V	1, 3
Power dissipation	Pd max	600	mW	1, 4
Operating temperature	Topr	0 to +70	°C	1
Storage temperature	Tstg	–65 to +150	°C	1

Note: 1. Stresses greater than the above listed maximum values may result in damage to the device.
2. –1.0 to V_{CC} + 1.0 V for pulse widths less than 20 ns.
3. –1.0 to V_{CC} + 14.0 V for pulse widths less than 20 ns.
4. Ta = 25 °C

DC Recommended Operating Ranges at Ta = 0 to +70°C, V_{CC} = 5 V ± 10%

Parameter	Symbol	min	typ	max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input low-level voltage	V_{IL}			0.8	V
Input high-level voltage	V_{IH}	2.0			V

DC Electrical Characteristics at Ta = 0 to +70°C, V_{CC} = 5 V ± 10%

Parameter	Symbol	Conditions	min	typ	max	Unit
Current drain during read	I_{CCR}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, all DQ pins open, Address inputs = V_{IH} or V_{IL}, operating frequency = $1/t_{RC}$ (minimum), V_{CC} = V_{CC} max			25	mA
Current drain during write	I_{CCW}	$\overline{CE}$ = $\overline{WE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, V_{CC} = V_{CC} max			40	mA
TTL standby current	I_{SB1}	$\overline{CE}$ = V_{IH}, V_{CC} = V_{CC} max			3	mA
CMOS standby current	I_{SB2}	$\overline{CE}$ = V_{CC} – 0.3 V, V_{CC} = V_{CC} max			20	μA
Input leakage current	I_{LI}	V_{IN} = V_{SS} to V_{CC}, V_{CC} = V_{CC} max			10	μA
Output leakage current	I_{LO}	V_{IN} = V_{SS} to V_{CC}, V_{CC} = V_{CC} max			10	μA
Output low-level voltage	V_{OL}	I_{OL} = 2.1 mA, V_{CC} = V_{CC} min			0.4	V
Output high-level voltage	V_{OH}	I_{OH} = –400 μA, V_{CC} = V_{CC} min	2.4			V

Input/Output Capacitances at Ta = 25°C, V_{CC} = 5 V ± 10%, f = 1 MHz

Parameter	Symbol	Conditions	max	Unit
I/O capacitance	C_{DQ}	V_{DQ} = 0 V	12	pF
Input capacitance	C_{IN}	V_{IN} = 0 V	6	pF

Power on Timing

Parameter	Symbol	max	Unit
Time from power on until first read operation	$t_{PU-READ}$	10	ms
Time from power on until first write operation	$t_{PU-WRITE}$	10	ms

AC Electrical Characteristics at Ta = 0 to +70°C, V_{CC} = 5 V ± 10%

AC Test Conditions

Input rise and fall times: .....10 ns (max.)
Output load: .....1 TTL gate + 30 pF

Read Cycle

Parameter	Symbol	LE28F4001M, T, R				Unit
		-15		-20		
		min	max	min	max	
Read cycle time	t_{RC}	150		200		ns
$\overline{CE}$ access time	t_{CE}		150		200	ns
Address access time	t_{AA}		150		200	ns
$\overline{OE}$ access time	t_{OE}		70		75	ns
$\overline{CE}$ to output low impedance time	t_{CLZ}	0		0		ns
$\overline{OE}$ to output low impedance time	t_{OLZ}	0		0		ns
$\overline{CE}$ to output high impedance time	t_{CHZ}		40		50	ns
$\overline{OE}$ to output high impedance time	t_{OHZ}		40		50	ns
Address to output valid time	t_{OH}	0		0		ns

Erase/Programming Cycle

Parameter	Symbol	LE28F4001M, T, R				Unit
		-15		-20		
		min	max	min	max	
Sector erase cycle time	t_{SE}		4		4	ns
Byte programming cycle time	t_{BP}		35		35	µs
Address setup time	t_{AS}	0		0		ns
Address hold time	t_{AH}	50		50		ns
$\overline{CE}$ and $\overline{WE}$ setup time	t_{CS}	0		0		ns
$\overline{CE}$ and $\overline{WE}$ hold time	t_{CH}	0		0		ns
$\overline{OE}$ setup time	t_{OES}	10		10		ns
$\overline{OE}$ hold time	t_{OEH}	10		10		ns
$\overline{CE}$ pulse width	t_{CP}	80		100		ns
$\overline{WE}$ pulse width	t_{WP}	80		100		ns
$\overline{WE}$ standby pulse width	t_{WPH}	50		50		ns
$\overline{CE}$ standby pulse width	t_{CPH}	50		50		ns
Data setup time	t_{DS}	50		50		ns
Data hold time	t_{DH}	10		10		ns
Reset recovery time	t_{RST}		4		4	µs
Protect mode $\overline{CE}$ pulse width	t_{PCP}	100		100		ns
Protect mode $\overline{CE}$ hold time	t_{PCH}	150		150		ns
Protect mode address setup time	t_{PAS}	20		30		ns
Protect mode address hold time	t_{PAH}	100		100		ns

Note: All signals must hold valid logic levels during the setup and hold times.

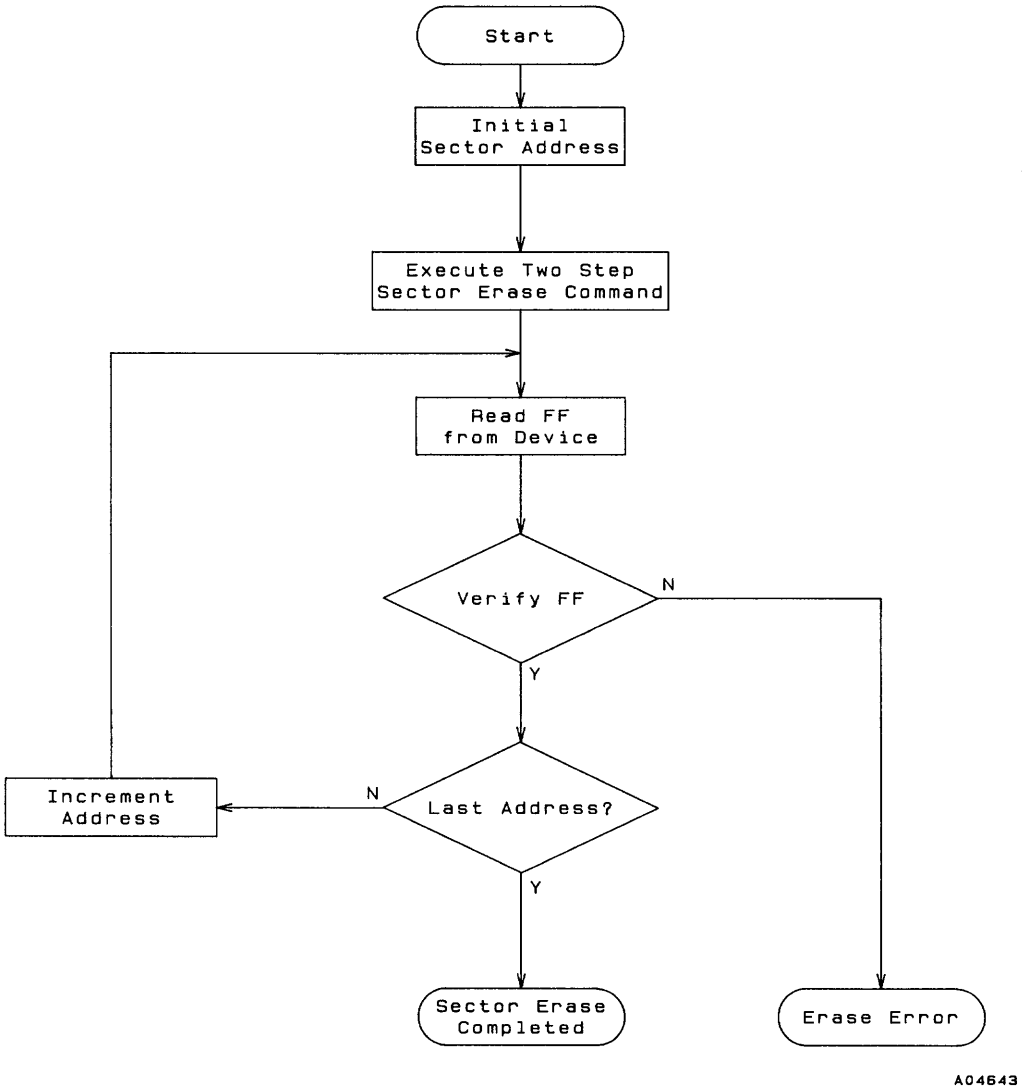


Figure 1 Sector Erase Flowchart

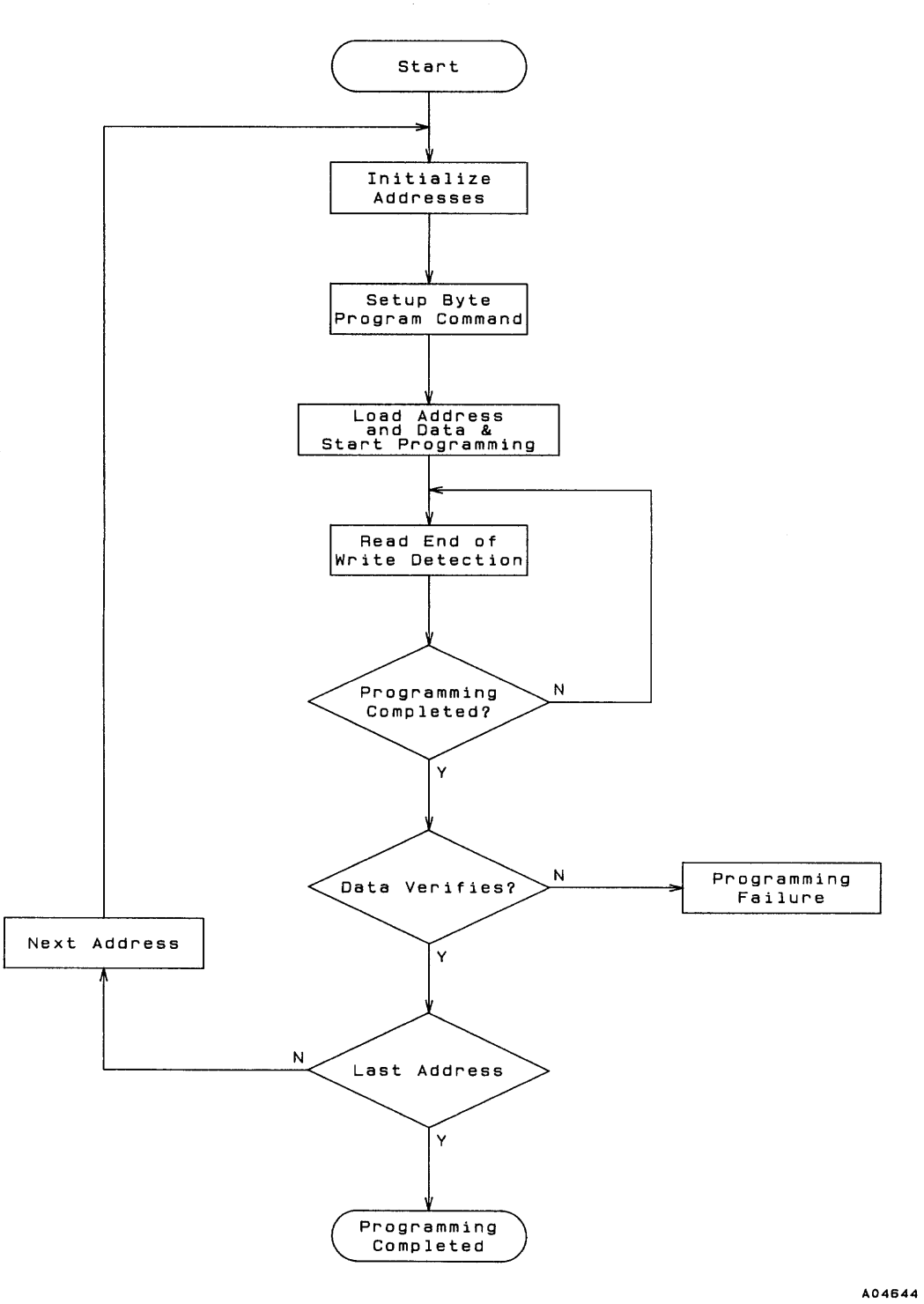


Figure 2 Byte Programming Flowchart

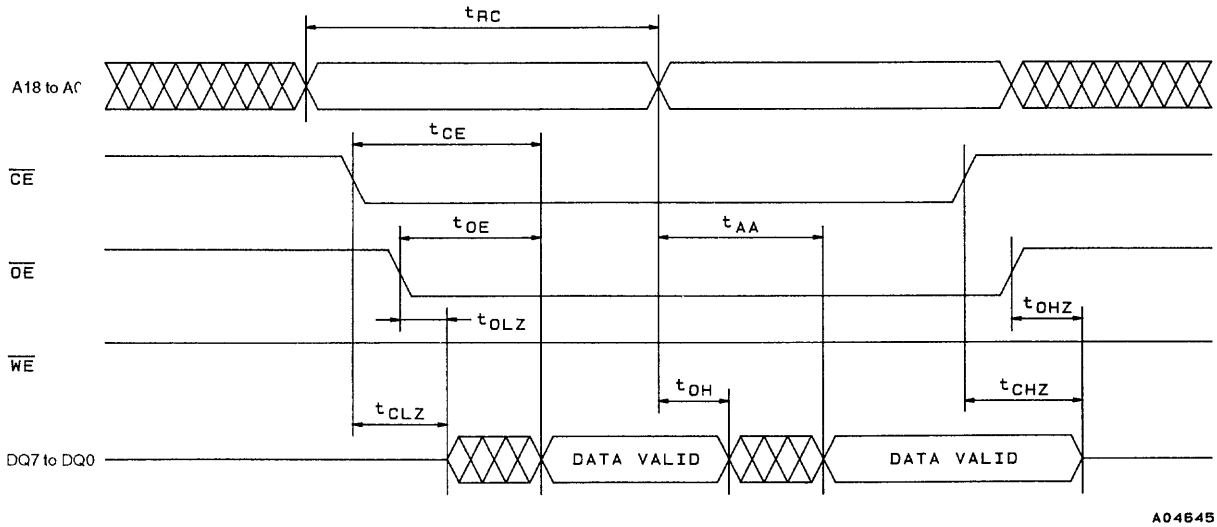


Figure 3 Read Cycle

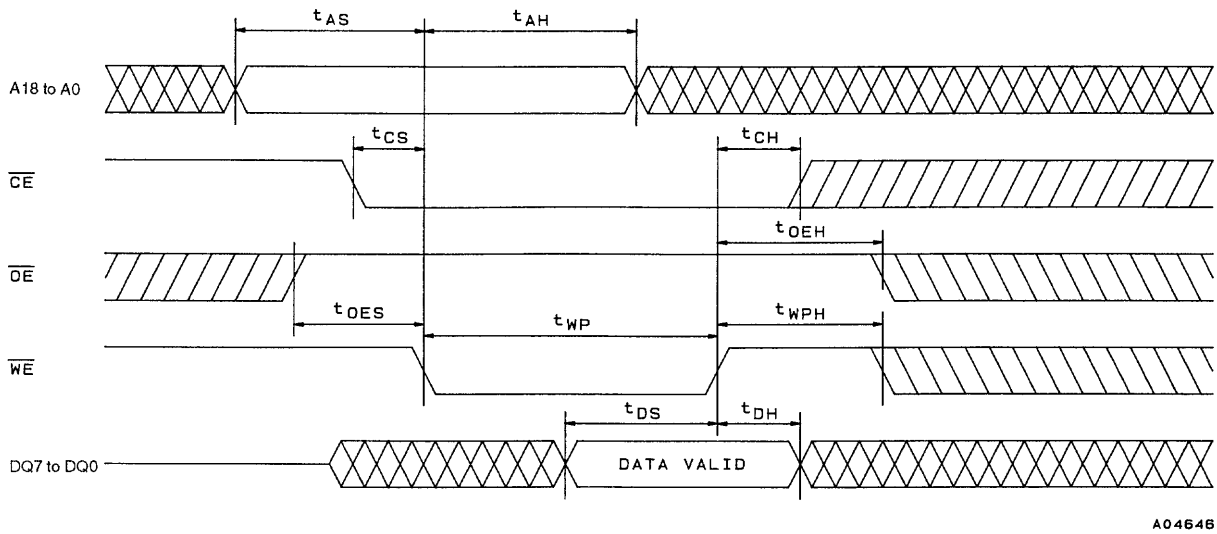


Figure 4 $\overline{WE}$ Control Write Cycle

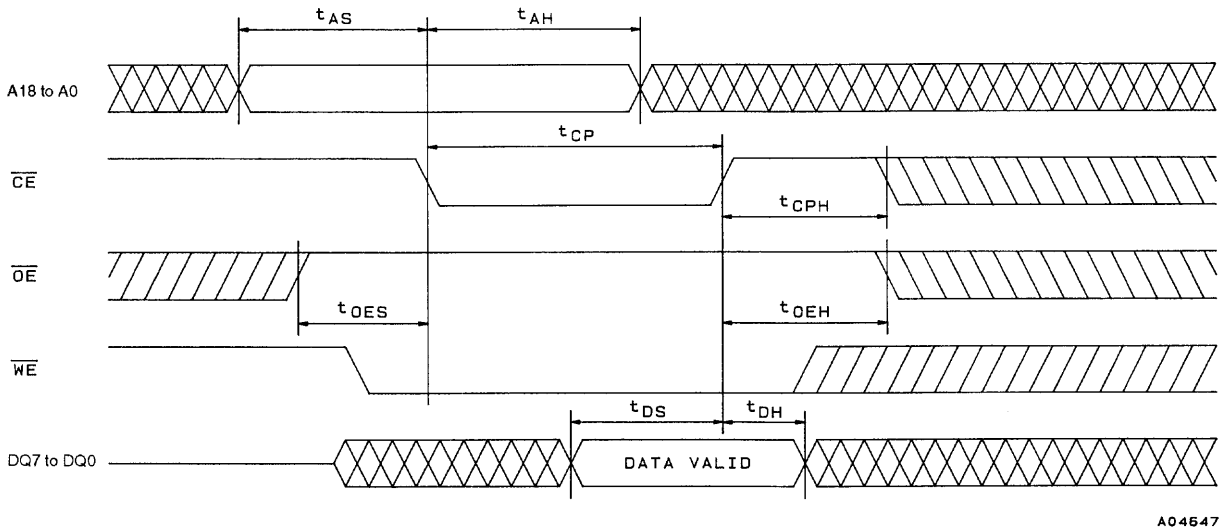


Figure 5 $\overline{CE}$ Control Write Cycle

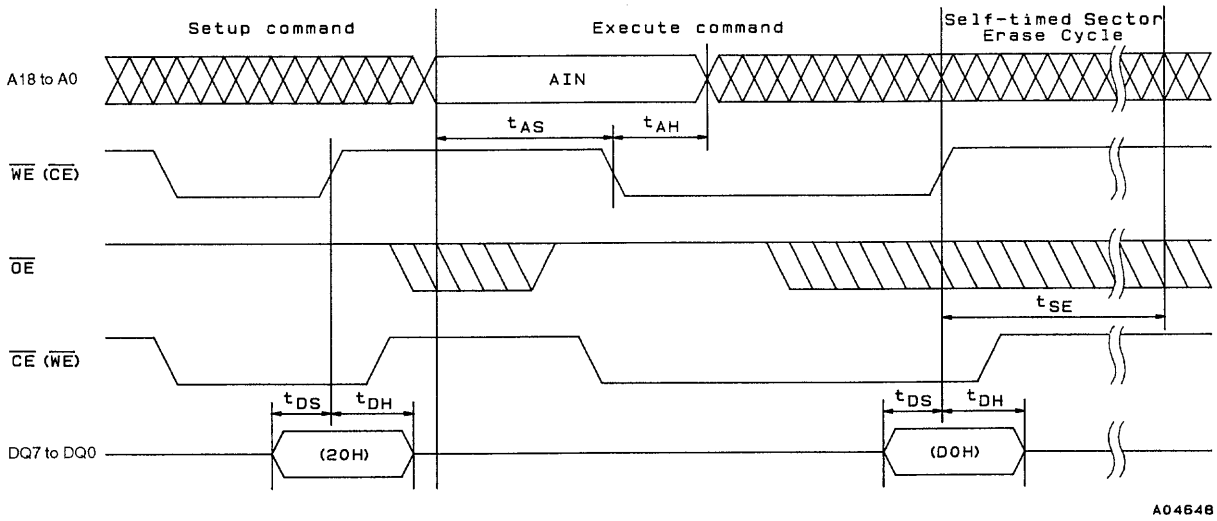


Figure 6 Sector Erase

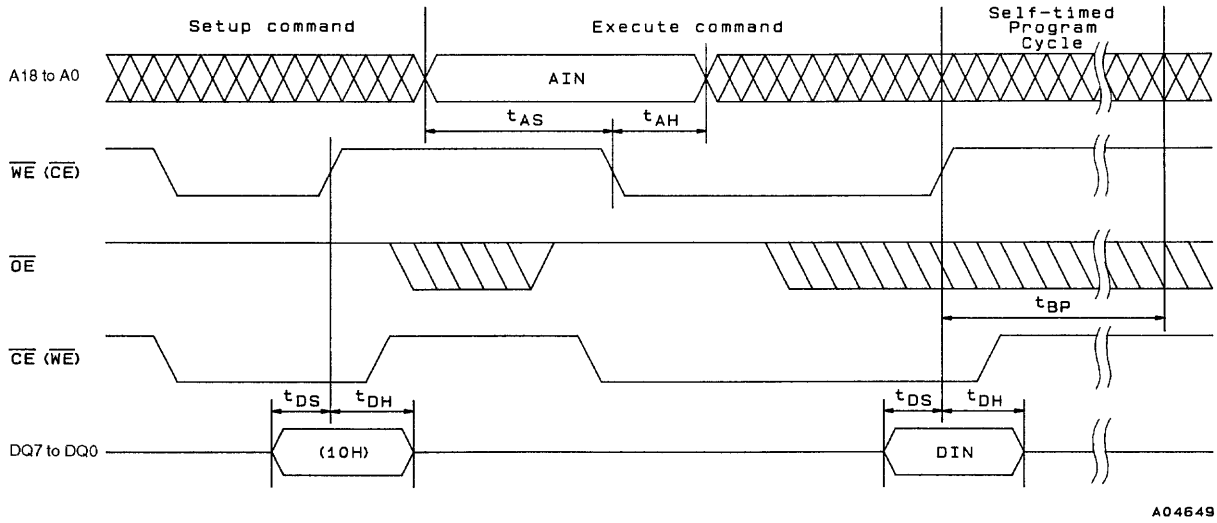


Figure 7 Byte Programming

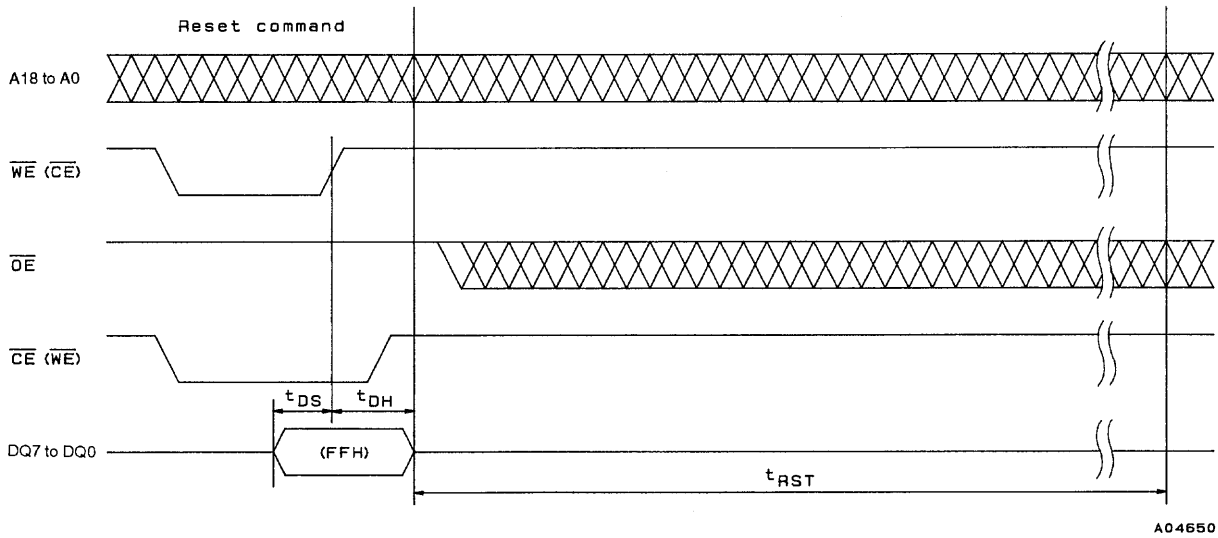
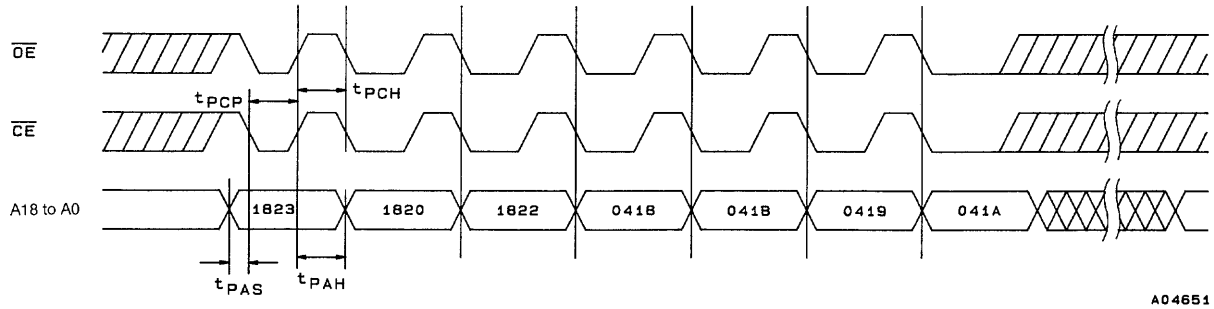


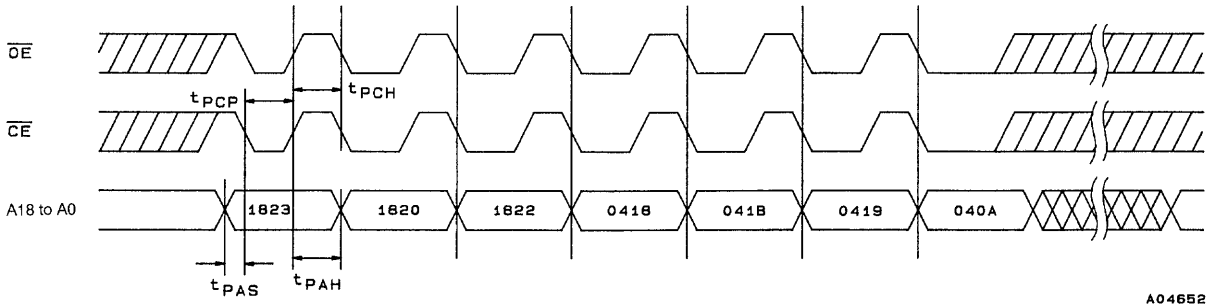
Figure 8 Reset



Note: 1. Addresses are latched internally on the rising edge of:
- $\overline{OE}$ if $\overline{CE}$ is kept low all time.
- $\overline{CE}$ if $\overline{OE}$ is kept low all time.
- The first pin to go high if both are togglet.

2. Above address values are in hex.

Figure 9 Software Data Unprotect Sequence



Note: 1. Addresses are latched internally on the rising edge of:
- $\overline{OE}$ if $\overline{CE}$ is kept low all time.
- $\overline{CE}$ if $\overline{OE}$ is kept low all time.
- The first pin to go high if both are togglet.

2. Above address values are in hex.

Figure 10 Software Data Protect Sequence

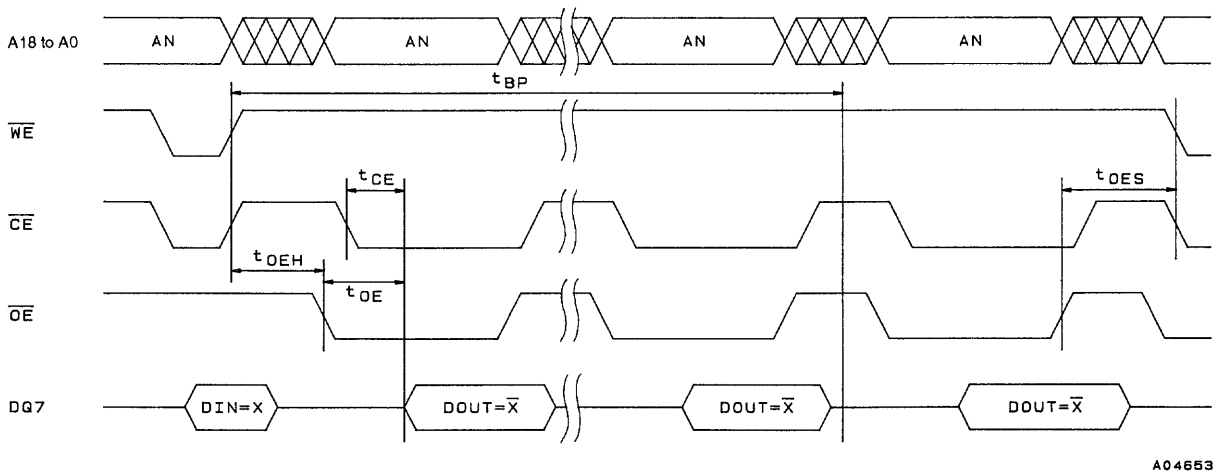
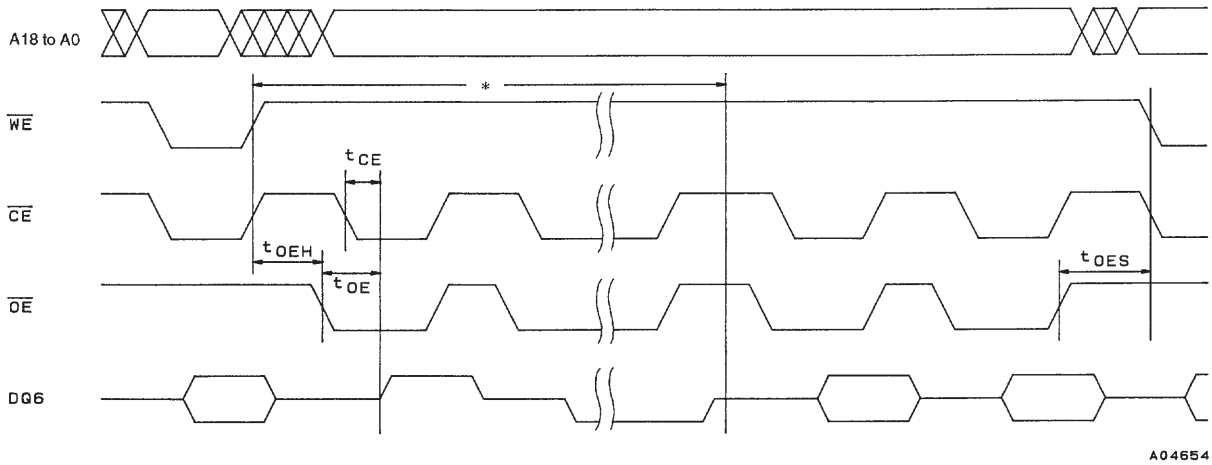
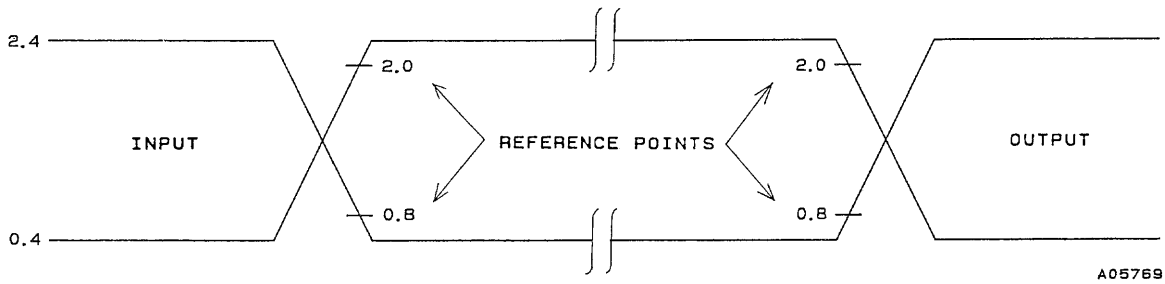


Figure 11 Data polling(DQ7)



Note: The timings stipulated here differ with the mode used. Either t_{SE} or t_{BP} applies.

Figure 12 Toggle Bit (DQ6)



Note: AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for a logic 1 and VOL (0.4 V_{TTL}) for a logic 0. The I/O measurement reference points are V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). The input rise and fall times (10% ↔ 90%) must be 10 ns or shorter.

Figure 13 AC I/O Reference Waveform