Ordering number : EN*5468

CMOS LSI

LE28FV4001M, T, R-20/25

4MEG (52488 × 8 Bits) Flash Memory

Preliminary

Overview

The LE28FV4001M, T, R Series are 4 MEG flash memory products that feature a 542488-word × 8-bit organization and 3.3 V single-voltage power supply operation. CMOS peripheral circuits were adopted for high speed, low power, and ease of use. The LE28FV4001M also supports high-speed data rewriting by providing a sector (256 bytes) erase function.

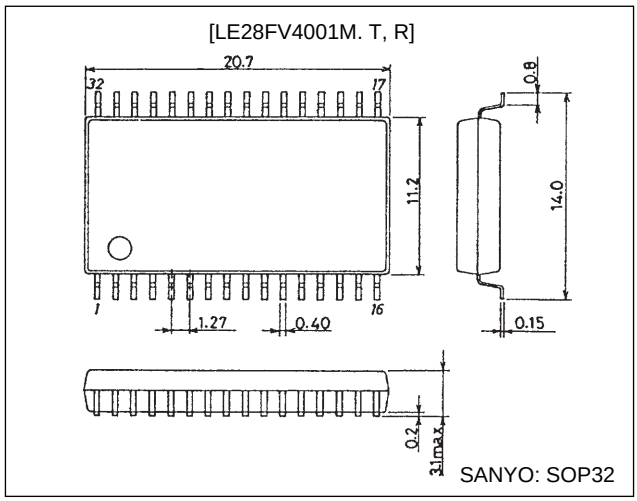
Features

- Highly reliable 2 layer polysilicon CMOS flash EEPROM process
- Read and write operations using a 3.3 V single-voltage power supply
- High-speed access: 200 and 250 ns
- Low power
  - — Operating (read): 10 mA (maximum)
  - — Standby: 20 µA (maximum)
- Highly reliable read write
  - —Number of sector write cycles: 10^4 cycles
  - — Data retention: 10 years
- Address and data latches
- Sector erase function: 256 bytes per sector
- Self-timer erase/program
- Byte program time: 35 µs (maximum)
- Write complete detection function: Toggle bit/$\overline{\text{Data}}$ poling
- Hardware and software data protection functions
- Pin assignment conforms to the JEDEC byte-wide EEPROM standard.
- Package
  SOP 32-pin (525 mil) plastic package: LE28FV4001M
  TSOP 42-pin (10 × 14 mm) plastic package: LE28FV4001T
  TSOP 40-pin (10 × 14 mm) plastic package: LE28FV4001R

Package Dimensions

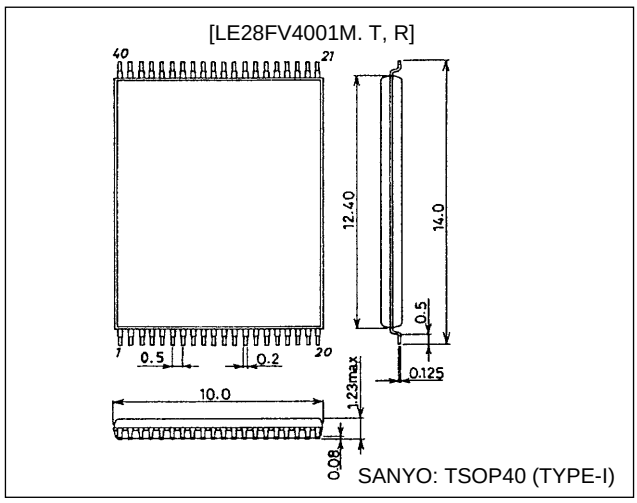
unit: mm

3205-SOP32



unit: mm

3087A-TSOP40



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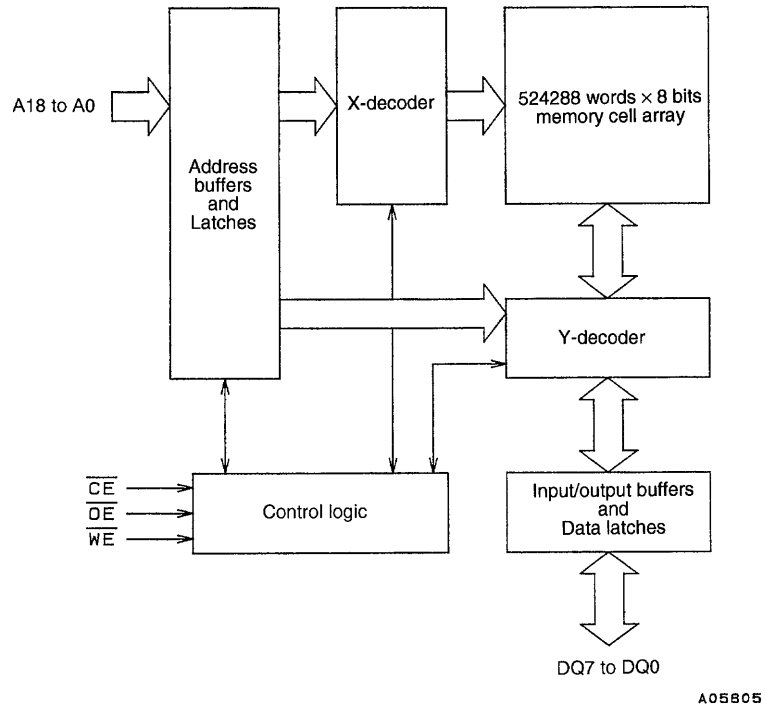
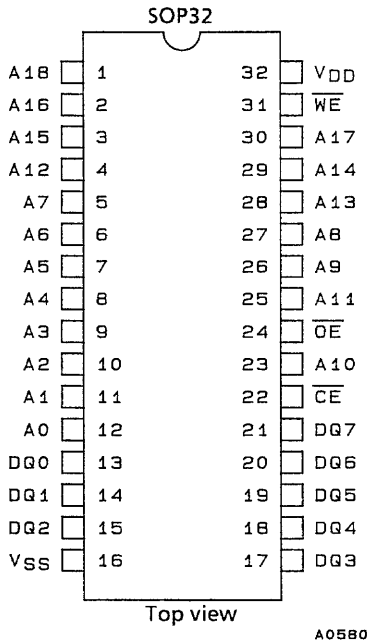
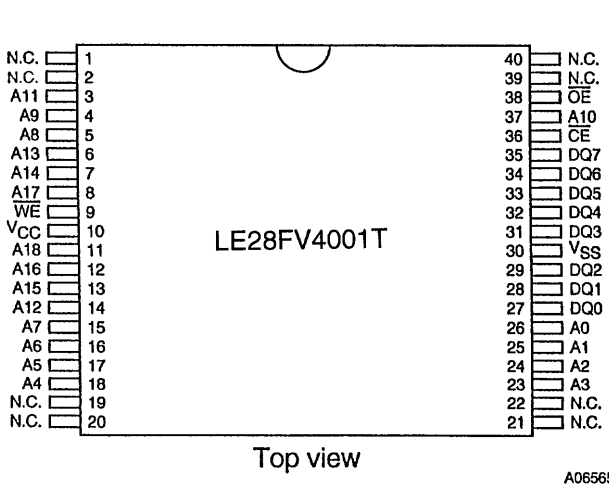
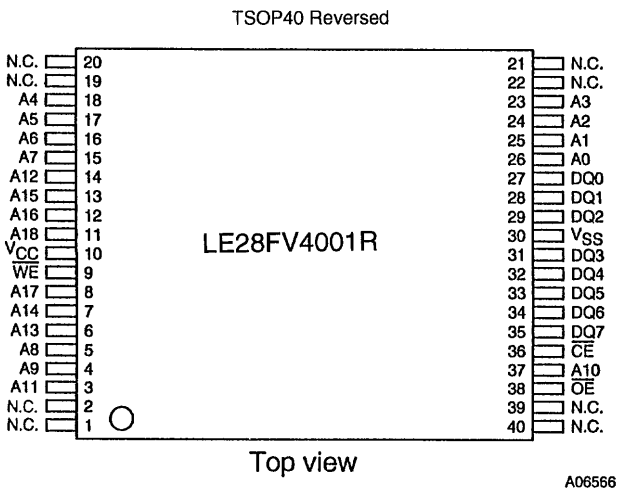
Block Diagram



Pin Assignments







Pin Functions

Symbol	Pin	Functions
A18 to A0	Address input	Supply the memory address to these pins. The address is latched internally during a write cycle.
DQ7 to DQ0	Data input and output	These pins output data during a read cycle and input data during a write cycle. Data is latched internally during a write cycle. Outputs go to the high-impedance state when either $\overline{OE}$ or $\overline{CE}$ is high.
$\overline{CE}$	Chip enable	The device is active when $\overline{CE}$ is low. When $\overline{CE}$ is high, the device becomes unselected and goes to the standby state.
$\overline{OE}$	Output enable	Makes the data output buffers active. $\overline{OE}$ is a low-active input.
$\overline{WE}$	Write enable	Makes the write operation active. $\overline{WE}$ is an active-low input.
V_{DD}	Power supply	Apply 3.3 V ±0.3 V to this pin.
V_{SS}	Ground	
N.C.	No connection	These pins are not connected to the chip internally.

Function Logic

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A18 to A0	DQ7 to DQ0
Read	V_{IL}	V_{IL}	V_{IH}	A_{IN}	D_{OUT}
Write	V_{IL}	V_{IH}	V_{IL}	A_{IN}	D_{IN}
Standby or write inhibit	V_{IH}	X	X	X	High-Z
Write inhibit	X	V_{IL}	X	X	High-Z/D_{OUT}
	X	X	V_{IH}	X	High-Z/D_{OUT}
Product identification	V_{IL}	V_{IL}	V_{IH}	A18 to A10 = V_{IL}, A8 to A1 = V_{IL}, A9 = 12 V, A0 = V_{IL}	Manufacturer code (BF)
				A18 to A10 = V_{IL}, A8 to A1 = V_{IL}, A9 = 12 V, A0 = V_{IH}	Device code (04)

Command Settings

Command	Request cycles	Setup command cycle			Execute command cycle			SDP
		Operation	Address	Data	Operation	Address	Data	
Sector erase	2	Write	X	20H	Write	Sector address	D0H	N
Byte program	2	Write	X	10H	Write	Program address	Program data	N
Reset	1	Write	X	FFH				Y
Read ID	3	Write	X	90H	Read	(7)	(7)	Y
Software data unprotect	7	See Figure 9.						
Software data protect	7	See Figure 10.						

Notes on command settings

1. X = high or low
2. The sector address is taken from A8 to A18, the sector size is 256 bytes, and A0 to A7 can be high or low during a sector erase operation.
3. The program address is taken from A0 to A18.
4. Data is displayed in hexadecimal.
5. SDP refers to the software data protect function, which uses a 7-byte read cycle sequence.
   Y = Can be executed even when the software data protect function is enabled.
   N = Cannot be executed when the software data protect function is enabled.
6. Figures 9 and 10 show the operation of the software data protect function using 7-byte read cycle sequences.
7. When an address of 0000 is specified, the manufacturer code, BF, is output, and when the address is 0001, the device code, 04, is output.

Product Overview

The LE28FV4001M, LE28FV4001T, and LE28FV4001R are 524288-word × 8-bit flash memory products that provide sector erase and byte programming functions. These flash memories can be erased and programmed using a 3.3-volt single-voltage power supply, they conform to the JEDEC standards for byte-wide memory pin assignments, and are pin compatible with industry standard EPROM, flash EPROM, and EEPROM memories.
The maximum byte programming time for the LE28FV4001M, LE28FV4001T, and LE28FV4001R is 35 μs, and the maximum sector erase time is 4 ms. Optimization is possible using the toggle bit and $\overline{\text{Data}}$ polling functions, which indicate the completion of the write cycle for both programming and erase operations. These products provide both hardware and software protection functions to protect data from being overwritten unintentionally. These products guarantee 10,000 rewrite cycles in sector units. Data is retained for at least 10 years.
The block diagram for these products as well as the pin assignments for the 40-pin TSOP and 32-pin SOP packages are shown on page 2. The pin functions and command settings are listed on page 3.

Device Operation

Commands are provided to access the device memory operation functions. The commands are written to a command register with standard microprocessor write timing. Commands are written by setting $\overline{\text{WE}}$ to the low level while $\overline{\text{CE}}$ is held low. The address is latched on the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CE}}$, whichever falls last. Data is latched on the rising edge of $\overline{\text{WE}}$ or $\overline{\text{CE}}$, whichever rises first. However, during the software write protect sequence, the address is latched on the rising edge of $\overline{\text{OE}}$ or $\overline{\text{CE}}$, whichever rises first.

Command Definition

The Command Settings section on page 3 presents a list of the commands and an overview of their functions. This section describes those functions in detail.
To execute the LE28FV4001M, LE28FV4001T, and LE28FV4001R byte program or erase function, the software protect function must be executed first.

1. Sector erase operation
   The sector erase operation consists of a setup command and an execute command. The setup command sets the device to a state where all the bytes within the sector can be erased electrically. A sector has 256 bytes. Since almost all applications use erase operations that are not whole chip erase operations but rather are single sector erase operations, this sector erase operation significantly increases the flexibility and ease-of-use of the LE28F4001 Series.
   The setup command is executed by writing 20H to the command register.
   An execute command (DDH) must be written to the command register to execute the sector erase operation. The sector erase operation starts on the rising edge of $\overline{\text{WE}}$ pulse and is automatically completed by an internal timer. Figure 6 shows the timing and waveforms for this operation.
   This two-stage sequence in which a setup command and a following execute command are required guarantees that the memory at the sector specified by the address data will not be erased accidentally.
2. Sector erase flowchart
   The quick and reliable erasure of up to 256 bytes of memory can be achieved by following the sector erase flowchart shown in Figure 1. The whole operation consists of executing two commands. A sector erase operation completes in a maximum of 4 ms. Although the erase operation can be terminated by executing a reset operation, the sector may not be completely erased if that reset is executed before the 4 ms time-out period elapses. The erase command can be re-executed as many times as required before the erase completes. Excessive erasure cannot cause problems with the LE28FV4001 Series products.

3. Byte programming operation
   The byte programming operation is started by writing a setup command (10H) to the command register.
   Once the setup command is executed, the execute command is started by the next $\overline{WE}$ pulse transition. Figure 7 shows the timing waveforms for this operation. The address and the data are latched internally on the falling edge and rising edge of the $\overline{WE}$ pulse, respectively. The $\overline{WE}$ rising edge also corresponds to the start of the programming operation. The programming operation is automatically completed under internal timing control. Figures 2 and 7 show the programming characteristics and waveforms.
   As mentioned previously, this two-stage sequence in which a setup command and a following execute operation, are required guarantees that memory cells will not be programmed accidentally.
4. Byte programming flowchart
   Data is stored into the device (i.e., the device is programmed) by the byte programming flowchart shown in Figure 2. The byte programming command sets up the byte for writing. The address is latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever falls last. The data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever rises first, and the programming operation starts. The application can detect the completion of the write by $\overline{Data}$ polling or by using the toggle bit.
5. Reset operation
   The reset command is a procedure for safely terminating an erase or programming command sequences. Writing FFH to the command register after issuing an erase or programming setup command will safely cancel that operation. The contents of memory will not be changed. The device goes to read mode after executing a reset command. The reset command cannot activate the software data protect function. Figure 8 shows the timing wavefroms.
6. Read operation
   A read operation is performed by setting $\overline{CE}$ and $\overline{OE}$, and then $\overline{WE}$ to read mode. Figure 3 shows the read mode timing waveforms, and the read mode conditions are shown as “function logic”. A read cycle from the host searches for the memory array data. The device remains in the read state until another command is written to the command register.
   As a default, the device will be in read mode in the write protect state from the time power is first applied until a command is written to the command register. The unprotect sequence must be executed to perform a write operation (erase or programming).
   The read operation is controlled by $\overline{CE}$ and $\overline{OE}$, and both must be set to the logic low level to activate the read function. When $\overline{CE}$ is at the logic high level, the chip is in the unselected state and only draws the standby current. $\overline{OE}$ controls the output pins. The device output pins will be in the high-impedance state if either $\overline{CE}$ or $\overline{OE}$ is at the logic high level.
7. Read ID operation
   The read ID operation consists of a single command, 90H. A read operation from address 0000H will then return the manufacturer code, BFH and a read operation from address 0001H will return the device code, 04H. This operation is terminated by writing any other valid command to the command register.

Protecting Data from Unintentional Writes

To protect the accumulated stored data that the user intends to be nonvolatile, the LE28FV4001 Series products provide both hardware and software functions to prevent unintentional writes when power is applied or cut off.

1. Hardware data protection
   The LE28FV4001 Series products incorporate a hardware data function that prevents unintentional writes.
   - Write inhibit mode: Write operations are disabled if either $\overline{OE}$ is at the low logic level, $\overline{CE}$ is at the high logic level, or $\overline{WE}$ is at the high logic level.
   - Noise and glitch protection: $\overline{WE}$ pulses shorter than 15 ns will not execute a write operation.
   - The LE28FV4001 Series products were designed to hold unintentional writes to a minimum by setting the device to read mode as the default when power is first applied.

2. Software data protection
   As mentioned earlier, the LE28FV4001 Series is designed to provide even more protection from unintentional writes in software. To avoid unintentional erasure or programming of sector or device cells, when the application system attempts to execute a sector erase or programming operation it must execute that operation as a two-stage sequence consisting of first of a setup command and then an execute command.
   As a default, the LE28FV4001 Series products go to the write protected state after power is applied. The device goes to the unprotected state after reads to seven specific addresses are executed consecutively. Those addresses are 1823H, 1820H, 1822H, 0418H, 041BH, 0419H, and 041AH. The address is latched on the rise of either $\overline{OE}$ or $\overline{CE}$, whichever is earlier. Similarly, the device can be set to the write protect state by reading from the following 7 addresses consecutively: 1823H, 1820H, 1822H, 0418H, 041BH, 0419H, and 040AH. Figures 9 and 10 show the software data protection waveforms for these 7-read-cycle sequences. The I/O pins can go to any state (high, low, or high impedance).

Detection of Write Operation Completion

To acquire the maximum performance from the device, applications must detect the completion of the programming cycle. The completion of the programming cycle can be detected by either $\overline{Data}$ polling or the toggle bit. This section describes these two detection mechanisms.
Actually, the completion of a nonvolatile memory write operation is asynchronous with respect to the application system. Therefore, it is possible that readout of either $\overline{Data}$ polling or toggle bit data could occur at the same time as the completion of the write cycle. If this happens the application system could receive an incorrect result. That is, valid data could appear to contradict either DQ7 or DQ6. To prevent false negatives, if an incorrect result occurs the software routine must include a loop to read the accessed location another 2 times. If both these readout cycles acquire valid data the device will have completed the write cycle. All other reject states are correct.

1. $\overline{Data}$ polling (DQ7)
   The LE28FV4001M, LE28FV4001T, and LE28FV4001R products provide a $\overline{Data}$ polling function that detects the completion of the programming cycle. During the program cycle, DQ7 reads out $\overline{Data}$ that is the negation of the most recently loaded data. When the programming cycle has complete, DQ7, along with DQ0 to DQ6, reads out the last loaded data. Figure 11 shows the timing chart for this operation. For data polling to function correctly, data must be erased before programming.
2. Toggle bit (DQ6)
   The DQ6 toggle bit is another technique for detecting the end of the erase or programming cycle. During an erase or programming operation the value of the DQ6 output alternates between 0 and 1, that is, the DQ6 output toggles between 0 and 1. When the erase or programming cycle completes, the toggling stops and the device goes to a normal read cycle. The toggle bit can be continuously monitored during an erase or programming cycle. Figure 12 shows the timing chart for toggle bit operation.
3. Continuous read
   One more technique for detecting the end of an erase or programming cycle is to read the same address twice in a row. If the same data is read twice in a row the erase or programming cycle has completed.

Product Identifier

Product identifier read is a mode provided so that applications can confirm that the device was manufactured by Sanyo Electric Co., Ltd. This mode can be accessed by both hardware and software operations. A ROM writer is normally used with this hardware operation to recognize the correct algorithm for these products. We recommend that users use the software operation for recognizing this device. The “Functional Logic” section describes the hardware operation in detail. The manufacturer and device code are accessed in the same manner.

Decoupling Capacitors

A 0.1-µF ceramic capacitors must be inserted between V_{DD} and V_{SS} for each device to assure stabile flash memory operation.

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Ratings	Unit	Note
Supply voltage	V_{DD}	–0.5 to +6.0	V	1
Input pin voltage	V_{IN}	–0.5 to V_{DD} + 0.5	V	1, 2
DQ pin voltage	V_{DQ}	–0.5 to V_{DD} + 0.5	V	1, 2
A9 pin voltage	V_{A9}	–0.5 to +14.0	V	1, 3
Allowable power dissipation	Pd max	600	mW	1, 4
Operating temperature	Topr	0 to +70	°C	1
Storage temperature	Tstg	–65 to +150	°C	1

Note: 1. The device may be destroyed by the application of stresses in excess of the absolute maximum ratings.
2. –1.0 V to V_{DD} + 1.0 V for pulses less than 20 ns
3. –1.0 V to +14 V for pulses less than 20 ns
4. Ta = 25 °C

DC Recommended Operating Ranges at Ta = 0 to +70°C

Parameter	Symbol	min	typ	max	Unit
Supply voltage	V_{DD}	3.0	3.3	3.6	V
Input low-level voltage	V_{IL}			0.6	V
Input high-level voltage	V_{IH}	2.0			V

DC Electrical Characteristics at Ta = 0 to +70°C, V_{DD} = 3.3 V ± 0.3 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Current drain during read	I_{DDR}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, all DQ pins open, address inputs = V_{IH} or V_{IL}, operating frequency = $1/t_{RC}$ (minimum), V_{DD} = V_{DD} max			10	mA
Current drain during write	I_{DDW}	$\overline{CE}$ = $\overline{WE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, V_{DD} = V_{DD} max			25	mA
TTL standby current	I_{SB1}	$\overline{CE}$ = V_{IH}, V_{DD} = V_{DD} max			1	mA
CMOS standby current	I_{SB2}	$\overline{CE}$ = V_{DD} – 0.3 V, V_{DD} = V_{DD} max			20	µA
Input leakage current	I_{LI}	V_{IN} = V_{SS} to V_{DD}, V_{DD} = V_{DD} max			10	µA
Output leakage current	I_{LO}	V_{IN} = V_{SS} to V_{DD}, V_{DD} = V_{DD} max			10	µA
Output low-level voltage	V_{OL}	I_{OL} = 100 µA, V_{DD} = V_{DD} min			0.4	V
Output high-level voltage	V_{OH}	I_{OH} = –100 µA, V_{DD} = V_{DD} min	2.4			V

Input/output Pin Capacitances at Ta = 25°C, V_{DD} = 3.3 V ± 0.3 V, f = 1 MHz

Parameter	Symbol	Conditions	max	Unit
Input/output capacitance	C_{DQ}	V_{DQ} = 0 V	12	pF
Input capacitance	C_{IN}	V_{IN} = 0 V	6	pF

Note: These items are only tested for random samples, i.e. they are not tested for all devices.

Power on Timing

Parameter	Symbol	Conditions	max	Unit
Time from power on until first read operation	$t_{PU-READ}$		10	ms
Time from power on until first write operation	$t_{PU-WRITE}$		10	ms

AC Electrical Characteristics at Ta = 0 to +70°C, V_{DD} = 3.3 V ± 0.3 V

AC Testing Conditions (See Figure 13)

Input rise and fall times: .....10 ns (max)
Output load: .....1 TTL gate + 30 pF

Read Cycle

Parameter	Symbol	LE28FV4001M, T, R				Unit
		-20		-25		
		min	max	min	max	
Read cycle time	t_{RC}	200		250		ns
$\overline{CE}$ access time	t_{CE}		200		250	ns
Address access time	t_{AA}		200		250	ns
$\overline{OE}$ access time	t_{OE}		100		120	ns
Output low-impedance time from $\overline{CE}$	t_{CLZ}	0		0		ns
Output low-impedance time from $\overline{OE}$	t_{OLZ}	0		0		ns
Output high-impedance time from $\overline{CE}$	t_{CHZ}		60		60	ns
Output high-impedance time from $\overline{OE}$	t_{OHZ}		60		60	ns
Output valid time from address input	t_{OH}	0		0		ns

Erase/Programming Cycles

Parameter	Symbol	LE28FV4001M, T, R				Unit
		-20		-25		
		min	max	min	max	
Sector erase cycle time	t_{SE}		4		4	ms
Byte programming cycle time	t_{BP}		35		35	µs
Address setup time	t_{AS}	0		0		ns
Address hold time	t_{AH}	50		100		ns
$\overline{CE}$ and WE setup time	t_{CS}	0		0		ns
$\overline{CE}$ and WE hold time	t_{CH}	0		0		ns
$\overline{OE}$ setup time	t_{OES}	10		20		ns
$\overline{OE}$ hold time	t_{OEH}	10		20		ns
$\overline{CE}$ pulse width	t_{CP}	100		160		ns
$\overline{WE}$ pulse width	t_{WP}	100		160		ns
$\overline{WE}$ standby pulse width	t_{WPH}	50		50		ns
$\overline{CE}$ standby pulse width	t_{CPH}	50		50		ns
Data setup time	t_{DS}	50		100		ns
Data hold time	t_{DH}	10		20		ns
Reset recovery time	t_{RST}		4		4	µs
$\overline{CE}$ pulse width in protect mode	t_{PCP}	100		100		ns
$\overline{CE}$ hold time in protect mode	t_{PCH}	150		150		ns
Address setup time in protect mode	t_{PAS}	30		30		ns
Address hold time in protect mode	t_{PAH}	100		100		ns

Note: All signals must hold valid logic levels during the setup and hold periods.

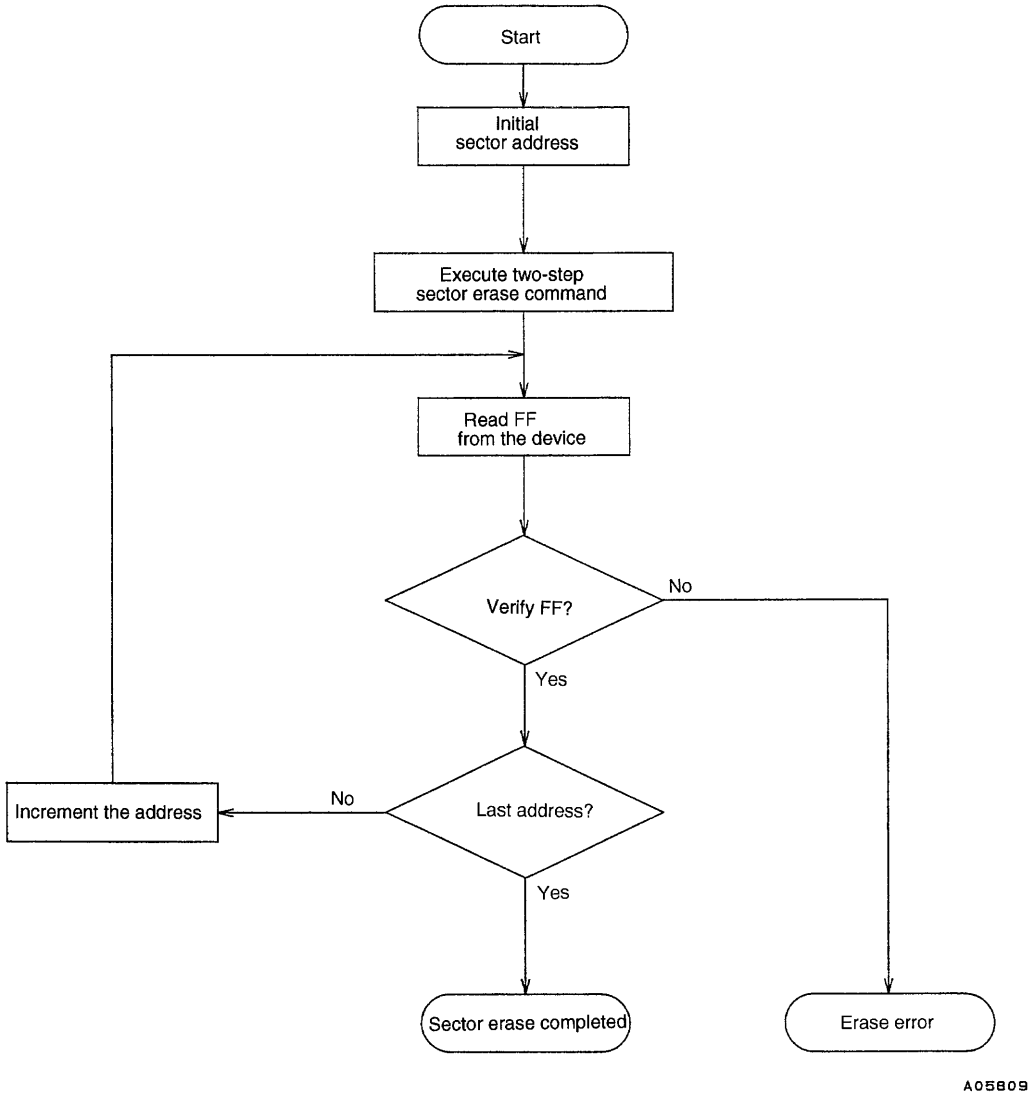


Figure 1 Sector Erase Flowchart

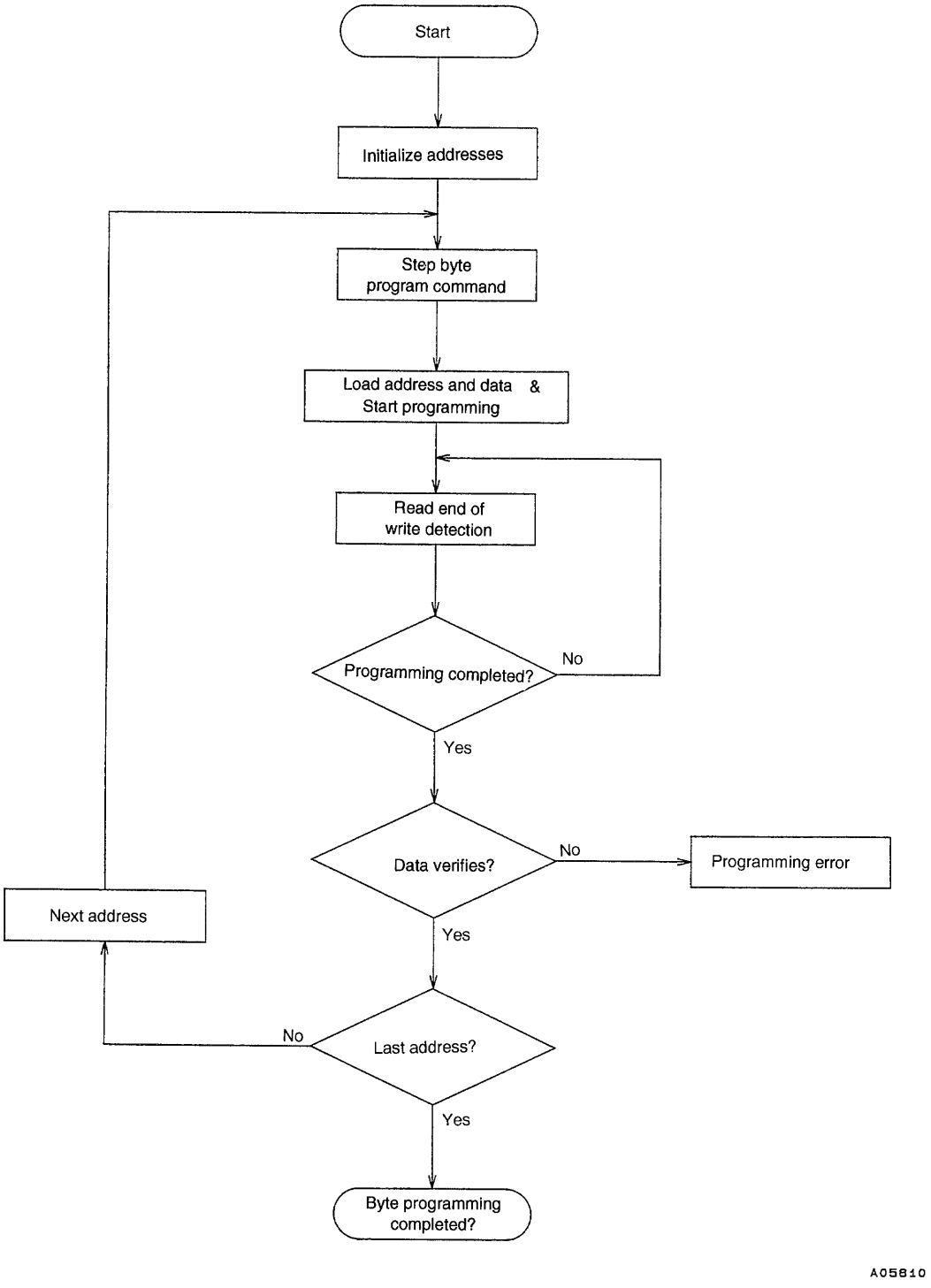


Figure 2 Byte Program Flowchart

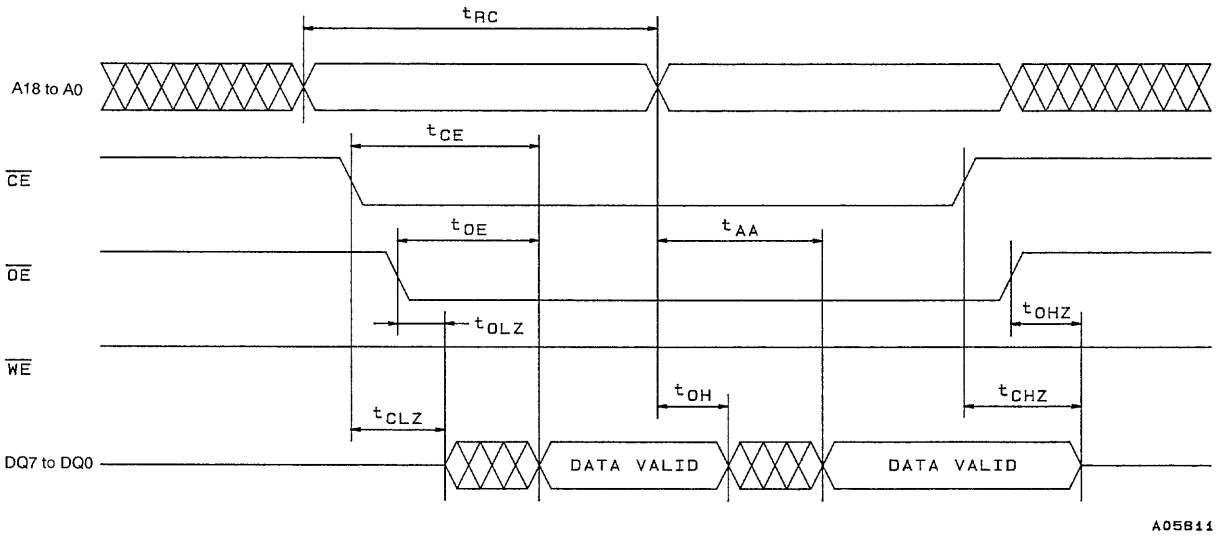


Figure 3 Read Cycle

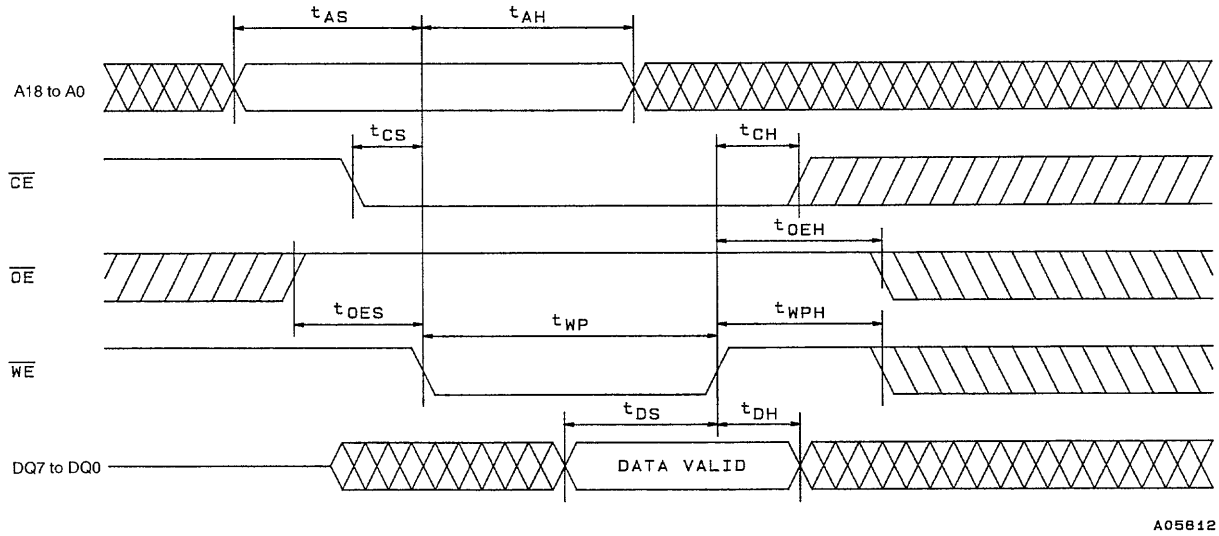


Figure 4 $\overline{WE}$ Control Write Cycle

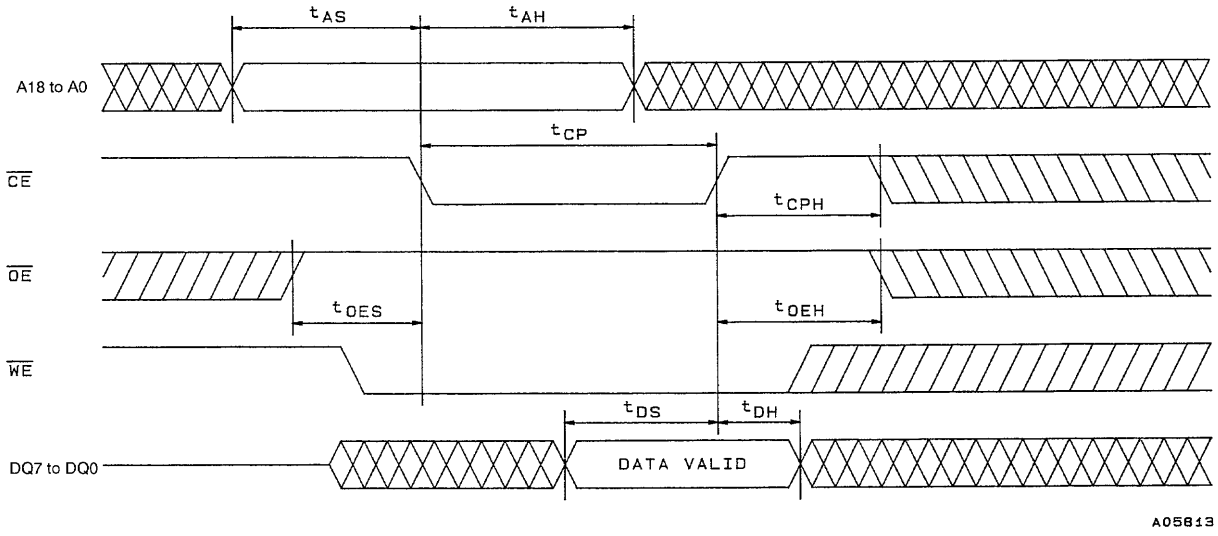


Figure 5 $\overline{CE}$ Control Write Cycle

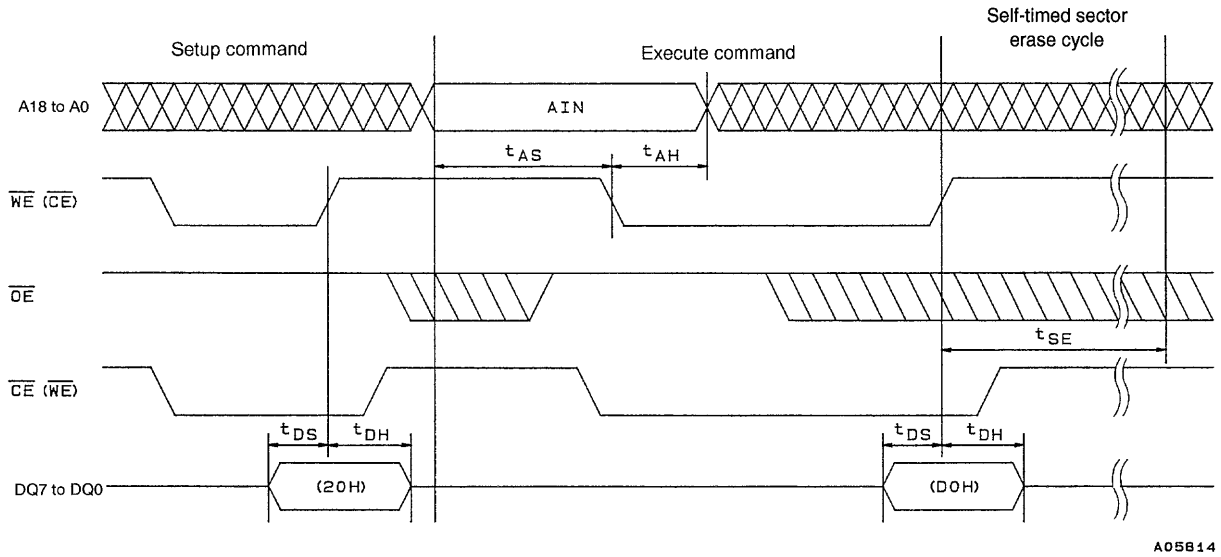


Figure 6 Sector Erase

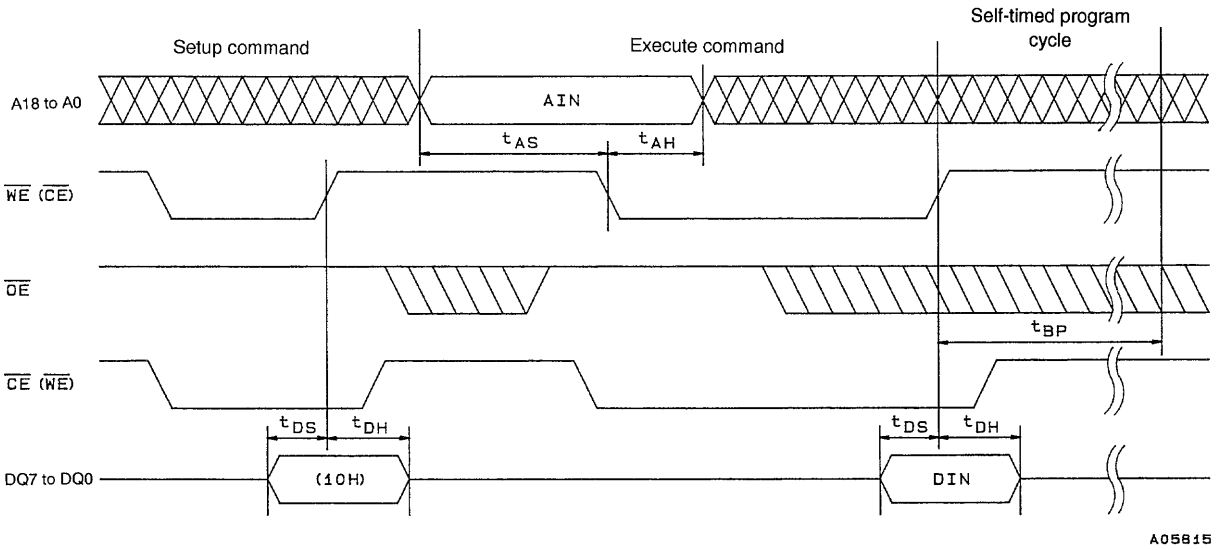


Figure 7 Byte Program

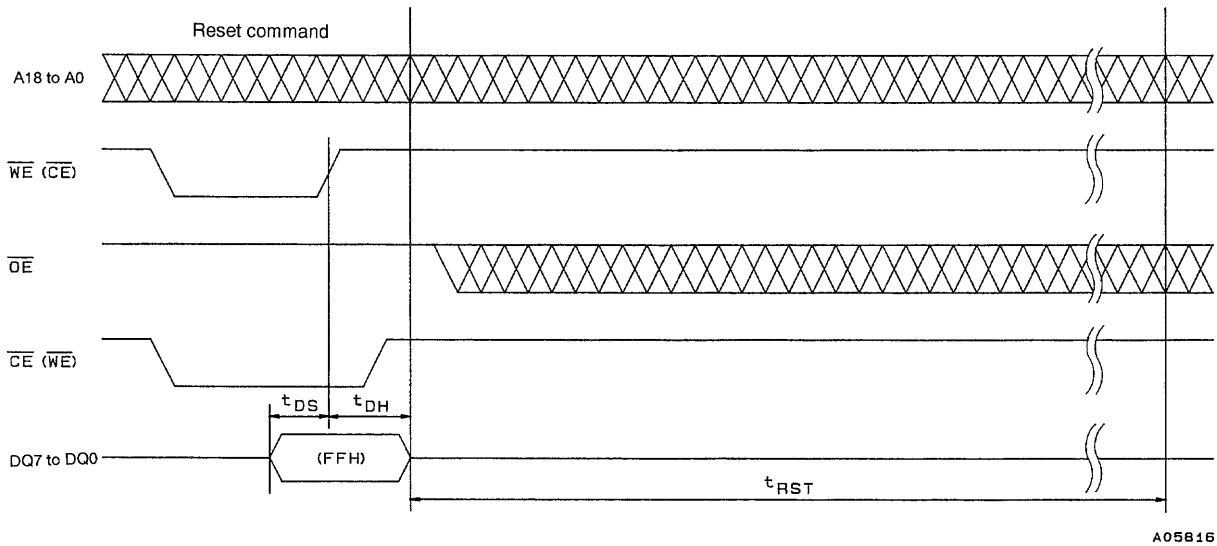


Figure 8 Reset

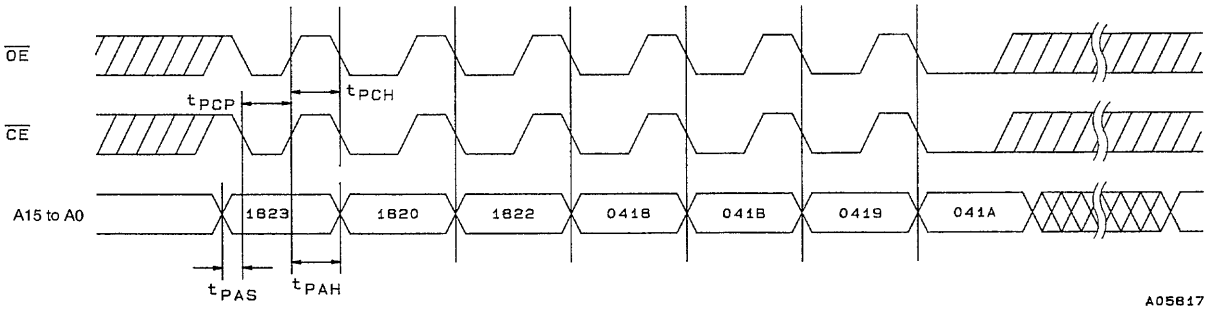


Figure 9 Software Data Unprotect Sequence

Notes on Figure 9
1. The address is latched on the rising edge of $\overline{CE}$ or $\overline{OE}$, whichever is earlier.
2. Pins A16 to A18 should be at either V_{IL} or V_{IH}.
3. The address is expressed in hexadecimal.

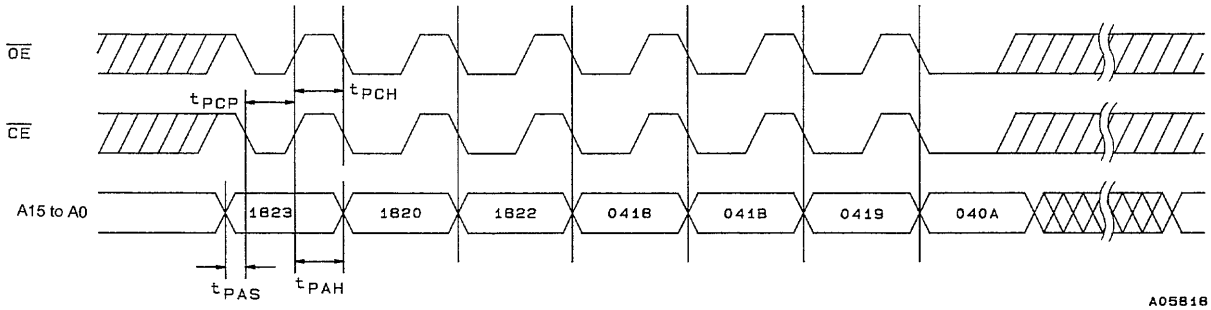


Figure 10 Software Data Protect Sequence

Notes on Figure 10
1. The address is latched on the rising edge of $\overline{CE}$ or $\overline{OE}$, whichever is earlier.
2. Pins A16 to A18 should be at either V_{IL} or V_{IH}.
3. The address is expressed in hexadecimal.

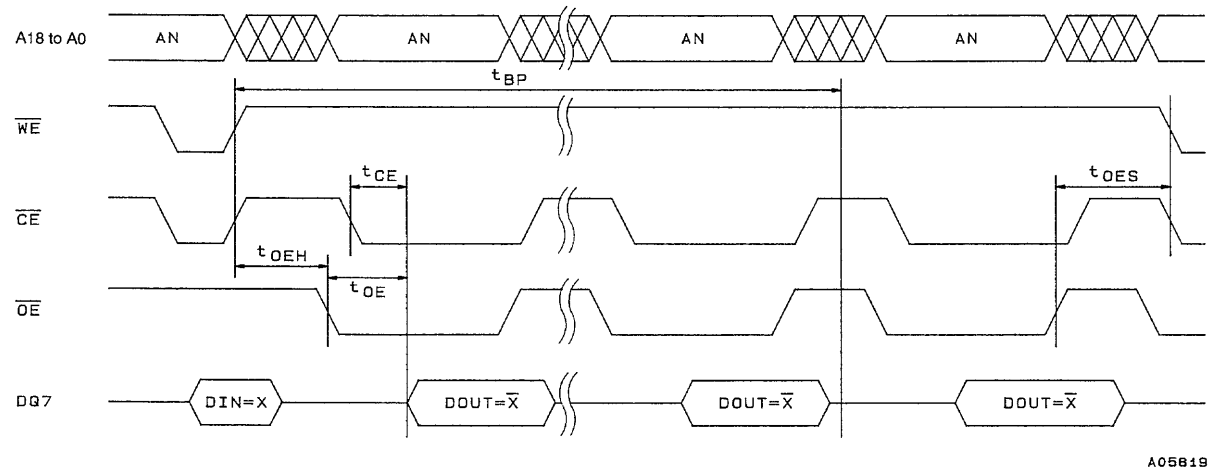


Figure 11 $\overline{\text{Data}}$ Polling (DQ7)

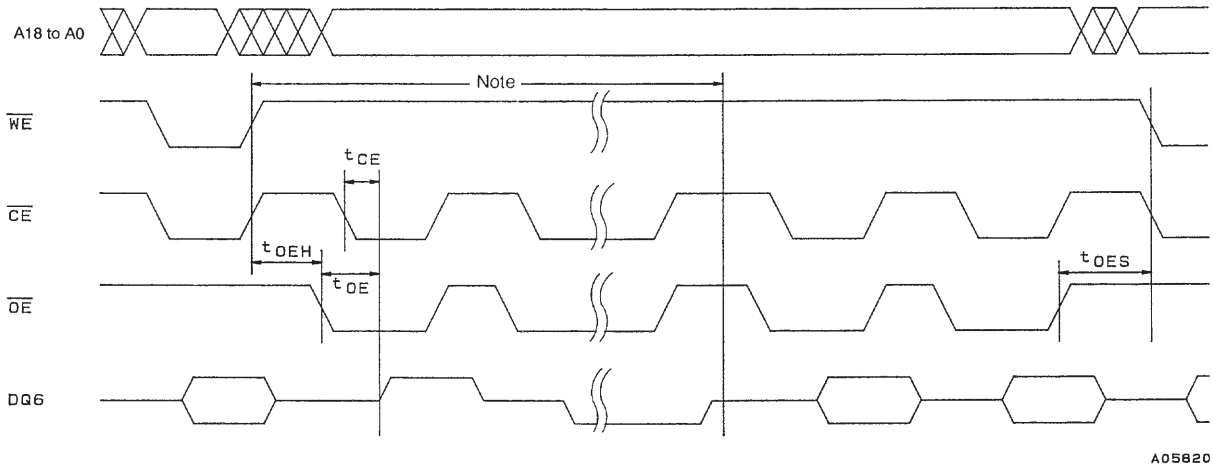


Figure 12 Toggle Bit (DQ6)

Note: The prescription of this timing differs depending on the operating mode used. Either tSE or tBP applies.

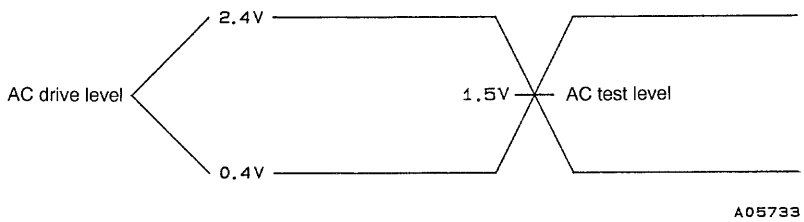


Figure 13 AC Input/Output Reference Waveform

The input rise and fall times (10% ↔ 90%) must not exceed 10 ns.