Migration from LH28F016SA/SU to LH28F160S3/S5

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INTRODUCTION

To convert the LH28F016SA/SU to a LH28F160S3/S5, some hardware and software changes are necessary and precautions must be taken. This is an overview of the main differences between the the LH28F016SA/SU and LH28F160S3/S5. For more detailed information, please refer to the product specification sheets.

HARDWARE COMPATIBILITY

Figure 1 shows the pin lay-out. Pin 1 becomes NC (No Connect) from $3/\overline{5}$ and pin 53 becomes STS (Status) from $\overline{RY/BY}$.

The NC can be either driven or floated. The STS can be configured in two different modes, level mode (default mode) or pulse mode. In level mode, it acts as a $\overline{RY/BY}$ pin. For pulse mode, please see the STS Configuration Command table in the data sheets for further information.

Tables 1, 2 and 3 show the comparison of SA/SU and S3/S5 on V_{PP} Voltage Comparison, V_{CC} Voltage Comparison, and V_{PP}/V_{CC} Voltage Combination, respectively. Please note, the 12 V of V_{PP} on LH28F160S3/S5 is no longer available.

To protect data from being accidentally erased on S3/S5, V_{PP} should be pulled lower than V_{PPLK}. The $V_{PP} = V_{CC}$ is no longer applied for such protection.

LH28F160S3/S5					LH28F160S3/S5
LH28F016SA/SU				LH28F016SA/SU	
NC	$3/\overline{5}$	1	56	$\overline{WP}$	$\overline{WP}$
$\overline{CE_1}$	$\overline{CE_1}$	2	55	$\overline{WE}$	$\overline{WE}$
NC	NC	3	54	$\overline{OE}$	$\overline{OE}$
A_{20}	A_{20}	4	53	$\overline{RY/BY}$	STS
A_{19}	A_{19}	5	52	DQ_{15}	DQ_{15}
A_{18}	A_{18}	6	51	DQ_7	DQ_7
A_{17}	A_{17}	7	50	DQ_{14}	DQ_{14}
A_{16}	A_{16}	8	49	DQ_6	DQ_6
V_{CC}	V_{CC}	9	48	GND	GND
A_{15}	A_{15}	10	47	DQ_{13}	DQ_{13}
A_{14}	A_{14}	11	46	DQ_5	DQ_5
A_{13}	A_{13}	12	45	DQ_{12}	DQ_{12}
A_{12}	A_{12}	13	44	DQ_4	DQ_4
$\overline{CE_0}$	$\overline{CE_0}$	14	43	V_{CC}	V_{CC}
V_{PP}	V_{PP}	15	42	GND	GND
$\overline{RP}$	$\overline{RP}$	16	41	DQ_{11}	DQ_{11}
A_{11}	A_{11}	17	40	DQ_3	DQ_3
A_{10}	A_{10}	18	39	DQ_{10}	DQ_{10}
A_9	A_9	19	38	DQ_2	DQ_2
A_8	A_8	20	37	V_{CC}	V_{CC}
GND	GND	21	36	DQ_9	DQ_9
A_7	A_7	22	35	DQ_1	DQ_1
A_6	A_6	23	34	DQ_8	DQ_8
A_5	A_5	24	33	DQ_0	DQ_0
A_4	A_4	25	32	A_0	A_0
A_3	A_3	26	31	$\overline{BYTE}$	$\overline{BYTE}$
A_2	A_2	27	30	NC	NC
A_1	A_1	28	29	NC	NC

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Figure 1. Pin-out Comparison of the LH28F160S3/S5 versus LH28F016SA/SU

Table 1. V_{PP} Voltage Comparison

V_{PP} VOLTAGE	LH28F016SA	LH28F016SU	LH28F160S3	LH28F160S5
12 V	Yes	No	No	No
5.0 V	No	Yes	Yes	Yes
3.3 V	No	Yes	Yes	No
2.7 V	No	No	Yes	No

Table 2. V_{CC} Voltage Comparison

V_{CC} VOLTAGE	LH28F016SA/SU	LH28F160S3	LH28F160S5
5.0 V	Yes	No	Yes
3.3 V	Yes	Yes	No
2.7 V	No	Yes	No

Table 3. V_{PP}/V_{CC} Voltage Combinations

DEVICE	V_{CC} VOLTAGE	V_{PP} VOLTAGE
LH28F160S3	2.7 V	2.7 V, 3.3 V or 5.0 V
LH28F160S3	3.3 V	3.3 V or 5.0 V
LH28F160S5	5.0 V	5.0 V

SOFTWARE COMPATIBILITY

The manufacture and device IDs need to be changed, please refer to Table 4.

LH28F016SA/SU and LH28F160S3/S5 have two command sets each, Compatible Command and Enhanced Command.

The Compatible Command performs the basic operations such as Array read, Word/Byte Write, Block Erase and Suspend etc. The S3/S5 has the same command set as SA/SU.

However the Enhanced Command is different from SA/SU and S3/S5. Table 5 shows the differences.

Furthermore, the S3/S5 supports CFI (Common Flash Interface). The CFI standardizes the software compatibility. It contains block size, density, command set information, etc. To accommodate such changes, some software modifications are necessary. Table 5 shows the changes between SA/SU and S3/S5. For additional information on software compatibility, please refer to the product data sheets.

Table 4. ID Codes Comparison

DEVICE	MANUFACTURE ID	DEVICE ID
LH28F016SA	89 H	A0 H
LH28F016SU	B0 H	88 H
LH28F160S3/S5	B0 H	D0 H

Table 5. Software Changes Between SA and S3/S5

ENHANCED COMMAND FUNCTION	COMMAND CODE	ENHANCED ON S3/S5	NEW ON S3/S5	NOT SUPPORTED ON S3/S5
Intelligent identifier	90 H	X		
Suspend	B0 H	X		
Lock Block/Confirm	77H/D0H			X
Set Block Lock-Bit/Confirm	60H/01H		X	
Clear Block Lock-Bits/Confirm	60H/D0H		X	
Single Load to Page Buffer	74 H			X
Sequential Load to Page Buffer	E0 H			X
Page Buffer Write to Flash	0C H			X
Write to Buffer/Confirm	E8H/D0H		X	
Erase All Unlocked Blocks/Confirm	A7H/D0H			X
Full Chip Erase/Confirm	30H/D0H		X	
Device Configuration	96 H			X
STS Configuration	B8 H		X	
Read Query	98 H		X	
Read Extended Status Register	71 H			X
Read Page Buffer	75 H			X
Page Buffer Swap	72 H			X
Two-Byte Program	FB H			X
Upload Status Bits	97 H			X
Upload Device Information	99 H			X
Sleep	F0 H			X
Abort	80 H			X

Because the command sets differ, some status register bits checking need to be changed accordingly. Please refer to Table 6 for those changes, and refer to product data sheets for detailed information.

Table 6. Status Register Bit Cross Reference

STATUS	S3/S5	SA/SU CSR	SA/SU GSR	SA/SU BSR
Write State Machine Status	SR.7	CSR.7	GSR.7	
Erase-Suspend Status	SR.6	CSR.6		
Program-Suspend Status	SR.2			
Operation Suspend Status	SR.6 or SR.2		GSR.6	
Erase Status	SR.5	CSR.5		
Data-Write Status	SR.4	CSR.4		
Device Operation Status	SR.5 or SR.4		GSR.5	
Improper Command sequence	SR.5 and SR.4	CSR.5 and CSR.4		
Device Sleep Status	N/A		GSR.4	
Block Status	SR.1			BSR.7
Block Lock Status	BSR.0			BSR.6
Block Operation Status	BSR.1, SR.5 or SR.4			BSR.5
Block Operation Abort Status	N/A			BSR.4
Queue Status	N/A (XSR.7)		GSR.3	BSR.3
V$_{PP}$ Status	SR.3	CSR.3		BSR.2
Page Buffer Available Status	XSR.7		GSR.2	
Page Buffer Status	N/A		GSR.1	
Page Buffer Select Status	N/A		GSR.0	
Reserved	XSR.0-6, BSR.2-7, SR.0	CSR.2-0		BSR.0

AC/DC SPECIFICATIONS

The comparison of electrical specifications between LH28F016SA/SU and LH28F160S3/S5 in shown in Table 7. Please note the power consumption of these devices varies, depending on the operation mode(s).

The programming and erase times have been improved. Therefore, the S3/S5 operates more effectively than the SA/SU. Please refer to the data sheets for further information.

Table 7. Comparison of Electrical Specification

PARAMETER		LH28F016SA/SU		LH28F160S5	LH28F160S3	
Supply Voltage (V_{CC}/V_{PP})		5 V/5 V (5 V/12 V)	3.3 V/5 V (3.3/12 V)	5 V/5 V	3.3 V/5 V	3.3 V/3.3 V
Read Current (MAX.)	$I_{CC}R$	60 mA (60 mA)	35 mA (35 mA)	50 mA	25 mA	25 mA
Write Current (MAX.)	$I_{PP}W$	60 mA (12 mA)	60 mA (15 mA)	80 mA	80 mA	80 mA
	$I_{CC}W$	35 mA (35 mA)	12 mA (12 mA)	35 mA	17 mA	17 mA
Erase Current (MAX.)	$I_{PP}E$	40 mA (10 mA)	40 mA (10 mA)	40 mA	40 mA	40 mA
	$I_{CC}E$	25 mA (25 mA)	12 mA (12 mA)	30 mA	17 mA	17 mA
Standby Current (MAX.)	IccS	10 µA (100 µA)	8 µA (100 µA)	100 µA	100 µA	100 µA
Deep Power Down Current (MAX.)	$I_{PP}D$	5 µA (5 µA)	5 µA (5 µA)	5 µA	5 µA	5 µA
	$I_{CC}P$	5 µA/50 µA (5 µA)	5 µA/50 µA (5 µA)	15 µA	15 µA	15 µA
Address Access Time (MAX.)		70 ns (70 ns)	120 ns (120 ns)	70 ns	100 ns	100 ns
$\overline{OE}$ Access Time (MAX.)		30 ns (30 ns)	45 ns (45 ns)	30 ns	45 ns	45 ns
Byte Write Time (TYP.)		8 µs (6 µs)	12 µs (9 µs)	9.24 µs	12.95 µs	19.51 µs
Byte Write time with page buffer (TYP.)		6.5us (5.5 µs)	9.5 µs (6.5 µs)	2 µs	2.7 µs	5.86 µs
Block Write Time (TYP.)		0.5 s (0.4 s)	0.8 s (0.6 s)	0.38 s	0.43 s	0.89 s
Block Erase Time (TYP.)		0.7 s (0.6 s)	0.9 s (0.8 s)	0.34 s	0.41 s	0.55 s
Access Time at 2.7 V at (MAX.)		160 ns			120 ns	

CONCLUSION

In addition to some hardware and software changes, DC/AC data modifications are necessary. Below is the summary of those changes. Please refer to the product data sheets for any further and detailed information.

- For any new designs, please contact your local representative, Sharp's field sales office or Sharp's distributions for Flash memory products information, or please visit Sharp's World Wide Web: http://www.sharpsma.com for latest information.

- For any existing designs, the following points need to be checked.
  - Hardware:
    - Covert 12 V_{PP} to be 5 V, 3.3 V or 2.7 V.
    - Become NC on pin 1 and STS on pin 53 from $3/\overline{5}$ and RY/$\overline{BY}$, respectively.
    - Pull V_{PP} below V_{CCLK} to protect data if it is used.

  - Software:
    - No software changes are required if the Enhanced Command Set and Status Registers are not used.
    - Refer Table 5, 6 and data sheets for detail information on software modifications.
  - AC/DC Characteristic Differences:
    - Block Erase Time and Block Program Time of S3/S5 are shorter than SA/SU.
    - S3/S5 Byte Wrtie Time without page buffer is longer than SA/SU.
    - Refer to Table 7 and product data sheets for additional information.

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