# Migration from LH28F032SUTD to LH28F320SKTD

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## INTRODUCTION

To convert a LH28F032SUTD to a LH28F320SKTD, the hardware and software changes are as follows.

## HARDWARE COMPATIBILITY

Figure 1 shows the pinout. Pin 1 becomes NC (No Connect) from 3/$\overline{5}$. Pin 53 becomes STS (Status) from RY/$\overline{BY}$.

The NC can be either driven or floated. The STS can be configured in two different modes: level mode (default mode) or pulse mode. In level mode, it acts as a RY/$\overline{BY}$ pin. For pulse mode, please refer to Table 12 of the STS Configuration Command in the data sheets for further information.

Table 1 shows a comparison between LH28F032SUTD and LH28F320SKTD. The LH28F320SKTD is available in 3.3 V $V_{PP}$ design. However, designers need to be aware that the size of the page buffer is smaller than what is available in the LH28F032SUTD model.

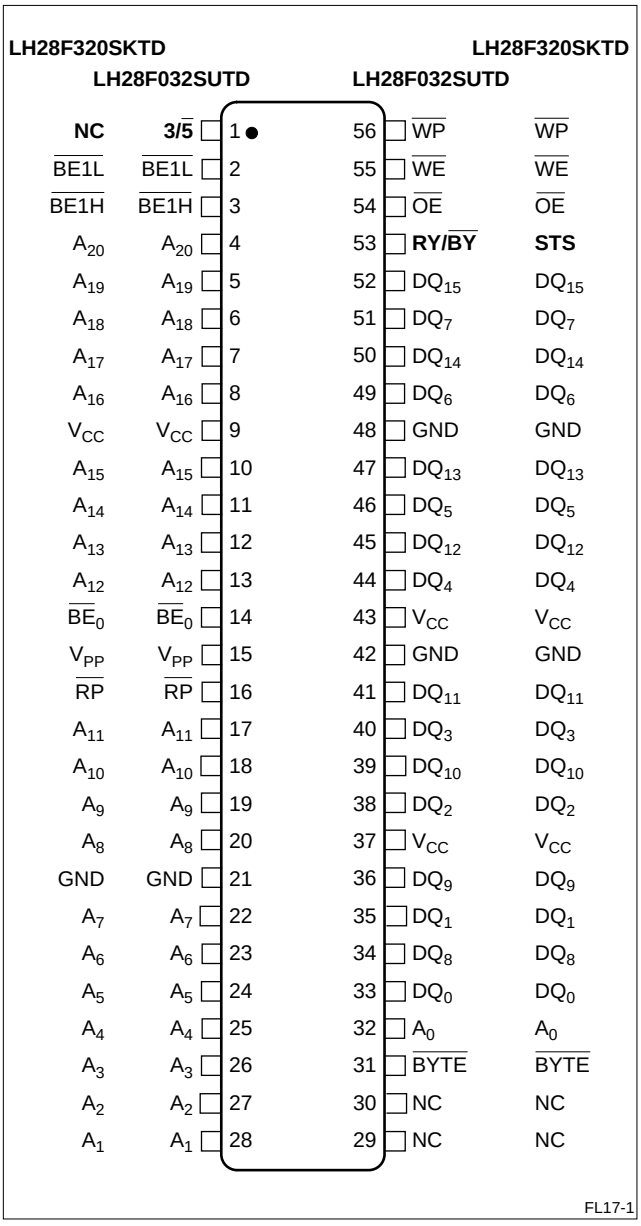


**Figure 1. Pinout Comparison of the LH28F032SUTD versus LH28F320SKTD**

**Table 1. Comparison of LH28F032SUTD and LH28F320SKTD**

| PARAMETER | LH28F032SUTD | LH28F320SKTD |
|---|---|---|
| Supply Voltage $V_{CC}/V_{PP}$ | 3.3 V/5 V, 5 V/5 V | 3.3 V/3.3 V, 3.3 V/5 V, 5 V/5 V |
| Configuration | x8/x16 | x8/x16 |
| Package | 56 TSOP | 56 TSOP |
| Block Size | 32 × 64KB × 2 banks | 32 × 64KB × 2 banks |
| Block Locking Feature | Any block | Any block |
| Buffer Size | 256 bytes × 2 | 32 bytes × 2 |
| CFI | No | Yes |

## SOFTWARE COMPATIBILITY

Table 2 shows the differences between the manufacture and device IDs. If any conversion takes place, the device ID has to be changed.

**Table 2. Comparison of IDs**

| DEVICE | MANUFACTURE ID | DEVICE ID |
|---|---|---|
| LH28F032SUTD | B0 | 88 |
| LH28F320SKTD | B0 | D0 |

LH28F032SU and LH28F320SK have two command sets: Compatible Command set and Enhanced Command set.

The Compatible Command performs the basic operations such as Array Read, Word/Byte Write, Block Erase and Suspend etc. While the Enhanced Command performs the enhanced features offered by the SK device. Table 3 and Table 4 show the compatible command set and enhanced command set, respectively.

Furthermore, the SK supports CFI (Common Flash Interface). The CFI is used to standardize the software compatibility and contains the block size, density, command set information, etc.

For detailed information on software compatibility and CFI, please refer to the data sheets for each part.

**Table 3. Compatible Command Set**

| COMPATIBLE COMMAND CODE | LH28F032SU | LH28F320SK |
|---|---|---|
| Read Array | FFH | FFH |
| Intelligent Identifier | 90H | 90H |
| Read Compatible Status Register | 70H | 70H |
| Clear Status Register | 50H | 50H |
| Word/Byte Write | 40H | 40H |
| Alternate Word/Byte Write | 10H | 10H |
| Erase Suspend/Resume | B0H/D0H | B0H/D0H |
| Block Erase/Confirm | 20H/D0H | 20H/D0H |

Table 4 shows the differences of the Enhanced Command Functions between the two devices. Because of those differences, the status register bits checking differs as well. The LH28F032SU has three registers, Compatible Status Register (CSR), Global Status Register (GSR), Block Status Register (BSR). However LH28F320SK has only two: the Status Register (SR) and Extended Status Register (XSR). Table 5 shows the status register bit cross references.

**Table 4. Enhanced Command Set**

| ENHANCED COMMAND FUNCTION | LH28F032SU | LH28F320SK |
|---|---|---|
| Lock Block/Confirm | 77H/D0H | |
| Set Block Lock-Bit/Confirm | | 60H/01H |
| Clear Block Lock-Bits/ Confirm | | 60H/D0H |
| Single Load to Page Buffer | 74H | |
| Sequential Load to Page Buffer | E0H | E8H |
| Page Buffer Write to Flash | 0CH | D0H |
| Byte Write Suspend/ Resume | | B0H/D0H |
| Erase All Unlocked Blocks/Confirm | A7H/D0H | |
| Full Chip Erase/Confirm | | 30H/D0H |
| Device Configuration | 96H | |
| STS Configuration | | B8H |
| Read Query | | 98H |
| Read Extended Status Register | 71H | |
| Read Page Buffer | 75H | |
| Page Buffer Swap | 72H | |
| Two-Byte Program | FBH | |
| Upload Status Bits | 97H | |
| Upload Device Information | 99H | |
| Sleep | F0H | |
| Abort | 80H | |

**Table 5. Comparison of Status Registers**

| STATUS | LH28F320SK SR/XSR | LH28F032SU CSR | LH28F032SU GSR | LH28F032SU BSR |
|---|---|---|---|---|
| Write State Machine Status | SR.7 | CSR.7 | GSR.7 | |
| Erase-Suspend Status | SR.6 | CSR.6 | | |
| Program-Suspend Status | SR.2 | | | |
| Operation Suspend Status | SR.6 or SR.2 | | GSR.6 | |
| Erase Status | SR.5 | CSR.5 | | |
| Data-Write Status | SR.4 | CSR.4 | | |
| Device Operation Status | SR.5 or SR.4 | | GSR.5 | |
| Improper Command Sequence | SR.5 and SR.4 | CSR.5 and CSR.4 | | |
| Device Sleep Status | N/A | | GSR.4 | |
| Block Status | SR.1 | | | BSR.7 |
| Block Lock Status | BSR.0 | | | BSR.6 |
| Block Operation Status | BSR.1, SR.5 or SR.4 | | | BSR.5 |
| Block Operation Abort Status | N/A | | | BSR.4 |
| Queue Status | N/A (XSR.7) | | GSR.3 | BSR.3 |
| $V_{PP}$ Status | SR.3 | CSR.3 | | BSR.2 |
| Page Buffer Available Status | XSR.7 | | GSR.2 | |
| Page Buffer Status | N/A | | GSR.1 | |
| Page Buffer Select Status | N/A | | GSR.0 | |
| Reserved | XSR.0-6, BSR.2-7, SR.0 | CSR.2-0 | | BSR.0 |

## AC/DC SPECIFICATIONS

The comparison of electrical specifications between LH28F032SU and LH28F320SK is shown in Table 6. Please note that the power consumption of these devices varies depending on which operation modes are in use. However, the programming and erase times have been greatly improved in the SK model. Please refer to the product data sheets for further information.

**Table 6. Comparison of AD/CD Characteristics**

| PARAMETER | | LH28F032SU | | LH28F320SK | | |
|---|---|---|---|---|---|---|
| Supply Voltage ($V_{CC}$/$V_{PP}$) | | 5 V/5 V | 3.3 V/5 V | 5 V/5 V | 3.3 V/5 V | 3.3 V/3.3 V |
| Read Current (MAX.) | $I_{CC}R$ | 60 mA | 35 mA | 50 mA | 25 mA | 25 mA |
| Write Current (MAX.) | $I_{PP}W$ | 60 mA | 60 mA | 80 mA | 80 mA | 80 mA |
| | $I_{CC}W$ | 35 mA | 12 mA | 35 mA | 17 mA | 17 mA |
| Erase Current (MAX.) | $I_{PP}E$ | 40 mA | 40 mA | 40 mA | 40 mA | 40 mA |
| | $I_{CC}E$ | 25 mA | 12 mA | 30 mA | 17 mA | 17 mA |
| Standby Current (MAX.) | $I_{CC}S$ | 40 µA | 30 µA | 100 µA | 100 µA | 100 µA |
| Deep Power Down Current (MAX.) | $I_{PP}D$ | 10 µA | 10 µA | 5 µA | 5 µA | 5 µA |
| | $I_{CC}D$ | 16 µA | 16 µA | 15 µA | 15 µA | 15 µA |
| Address Access Time (MAX.) | | 70 ns | 120 ns | 70 ns | 100 ns | 100 ns |
| $\overline{OE}$ Access Time (MAX.) | | 30 ns | 45 ns | 35 ns | 45 ns | 45 ns |
| Byte Write Time (TYP.) | | 8 µs(6 µs) | 12 µs (9 µs) | 9.24 µs | 12.95 µs | 19.51 µs |
| Byte Write time with page buffer (TYP.) | | 6.5 µs (5.5 µs) | 9.5 µs (6.5 µs) | 2 µs | 2.7 µs | 5.66 µs |
| Block Write Time (TYP.) | | 0.5 s | 0.8 s | 0.31 s | 0.43 s | 0.72 s |
| Block Erase Time (TYP.) | | 0.7 s | 0.9 s | 0.34 s | 0.41 s | 0.55 s |
| Access Time at 2.7 V at (MAX.) | | 160 ns | | | 120 ns | |

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