Ordering number: EN3035A

NMOS LSI

SANYO No.3035A

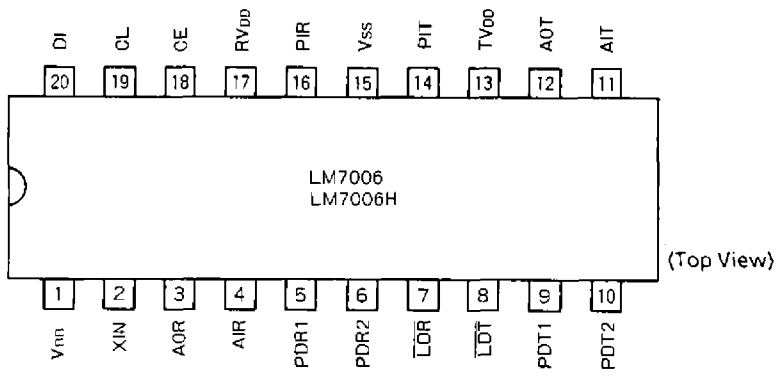
LM7006, 7006H

Dual PLL Frequency Synthesizer Circuit

Overview

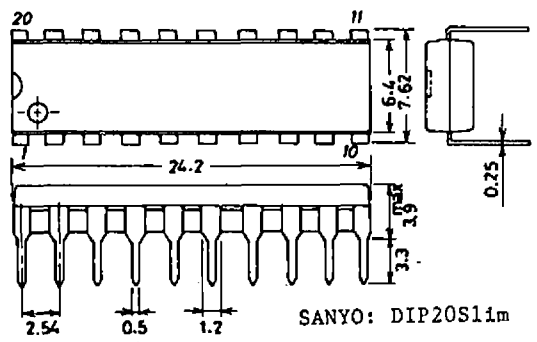
The LM7006, 7006H is a PLL Frequency Synthesizer circuit for use in cordless telephones. It incorporates separate programmable dividers, phase comparators and dual-gain charge pumps for the transmit and receive sides. (Transmit side is operated by an independent power supply for standby function.)
Device operation is controlled by a 40-bit serial input word, enabling simple control from a microcontroller by CCB.
The LM7006, 7006H is available in a 20-pin plastic DIP (300MIL). It operates from a single 4.0 to 5.5V supply.

Pin Assignment: DIP20S

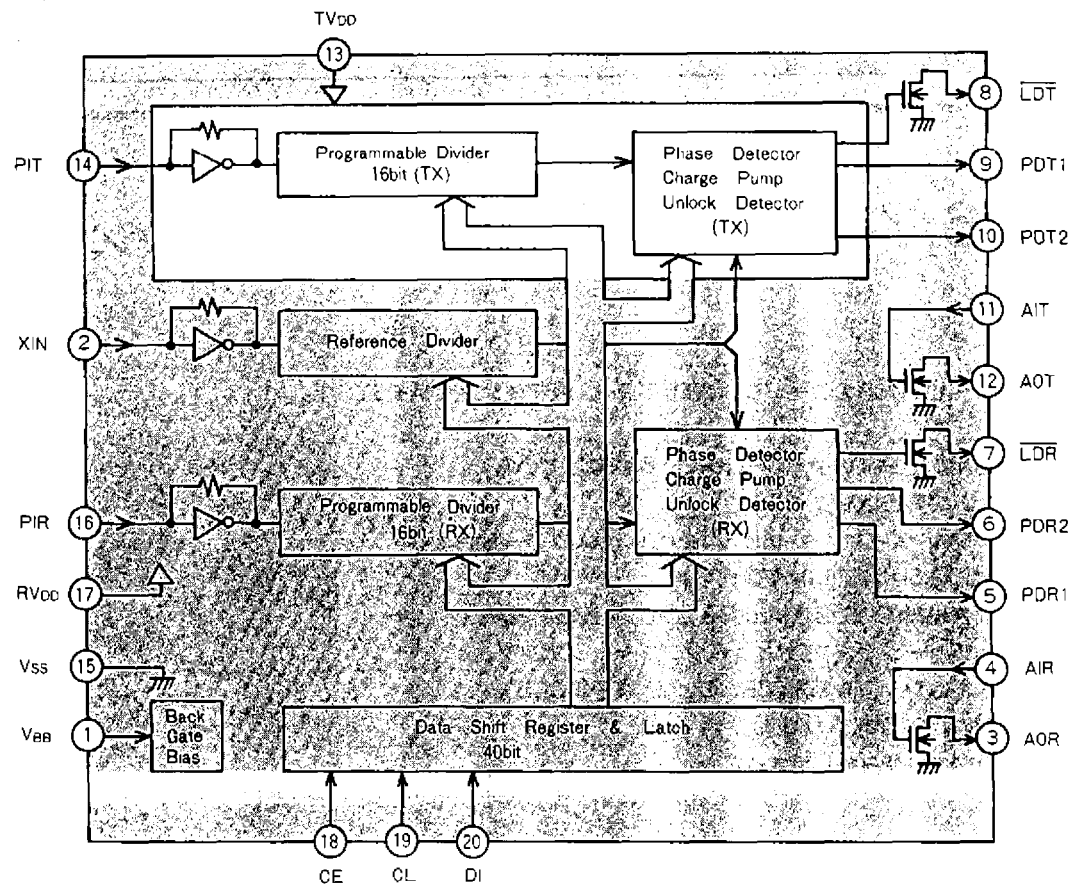


Package Dimensions 3021B-D20SIC

(unit : mm)



Equivalent Circuit Block Diagram



PIT : TX local OSC signal input
XIN : Reference OSC signal input (12.800MHz)
PIR : RX local OSC signal input
RV_{DD} : Power supply other than TV_{DD}
V_{SS} : Ground
V_{BB} : Back gate bias pin
CE,CL,DI : Serial data input
TV_{DD} : TX PLL supply (: [ ])

$\overline{LDT}$: TX unlock detection (open-drain)
PDT1 : TX Charge pump output (main)
PDT2 : TXCharge pump output (sub)
AIT,AOT : TX Tr for L.P.F amp
$\overline{LDR}$: RX unlock detection (open-drain)
PDR1 : RX Charge pump output (main)
PDR2 : RX Charge pump output (sub)
AIR,AOR : RX Tr for L.P.F amp

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0V

				unit
Supply Voltage	V_{DD} max	RV_{DD},TV_{DD}	−0.3 to +6.0	V
Back Gate Bias	V_{BB} max	V_{BB}	−4.0 to −2.0	V
Input Voltage	$V_{IN(1)}$ max	CE,CL,DI,AIR,AIT	−0.3 to +7.0	V
	$V_{IN(2)}$ max	All other input pins	−0.3 to V_{DD}+0.3	V
Output Voltage	$V_{OUT(1)}$ max	AOR,AOT,$\overline{LDR}$,$\overline{LDT}$	−0.3 to +7.0	V
	$V_{OUT(2)}$ max	All other output pins	−0.3 to V_{DD}+0.3	V
Output Current	$I_{OUT(1)}$ max	AOR,AOT,$\overline{LDR}$,$\overline{LDT}$	0 to 2.0	mA
Allowable Power Dissipation	Pd max	Ta≦75°C	350	mW
Operating Temperature	Topr		−40 to +75	°C
Storage Temperature	Tstg		−55 to +125	°C

Note : Pins PIR and PIT are susceptible to damage by static discharge. Appropriate precautions should be taken during handling and operation.

Allowable Operating Conditions at Ta = −40 to +75°C, V_{SS} = 0V				min	typ	max	unit
Supply Voltage	V_{DD}	RV_{DD}, TV_{DD}		4.0		5.5	V
Input 'H'-Level Voltage	V_{IH}	CE,CL,DI		2.5		5.5	V
Input 'L'-Level Voltage	V_{IL}	CE,CL,DI		0		0.5	V
Output Voltage	V_{OUT}	AOR,AOT, $\overline{LDR}$,$\overline{LDT}$		0		5.5	V
Input Frequency	$f_{IN(1)}$	XIN	Sine wave, capacitive coupling $V_{IN(1)}$ = 50mVrms	3.0	12.8	13.5	MHz
	$f_{IN(2)}$	PIR,PIT	Sine wave, capacitive coupling $V_{IN(2)}$ = 70mVrms	200		400	MHz
Input Voltage	$V_{IN(1)}$	XIN	Sine wave, capacitive coupling $f_{IN(1)}$ = 3.0 to 13.5MHz	50		1000	mVrms
	$V_{IN(2)}$	PIR,PIT	Sine wave, capacitive coupling $f_{IN(2)}$ = 200 to 400MHz	70		500	mVrms

Electrical Characteristics under Allowable Operating Conditions				min	typ	max	unit
Internal Feedback Resistor	Rf	XIN,PIR,PIT			500		kΩ
Hysteresis Width	Vh	CE,CL,DI		0.1	0.5		V
Input 'H'-Level Current	$I_{IH(1)}$	CE,CL,DI	V_I = 5.5V			5.0	μA
	$I_{IH(2)}$	XIN,PIR,PIT	$V_I = V_{DD}$			40	μA
	$I_{IH(3)}$	AIR,AIT	V_I = 5.5V		0.01	10.0	nA
Input 'L'-Level Current	$I_{IL(1)}$	CE,CL,DI	$V_I = V_{SS}$			5.0	μA
	$I_{IL(2)}$	X_{IN},PIR,PIT	$V_I = V_{SS}$			40	μA
	$I_{IL(3)}$	AIR,AIT	$V_I = V_{SS}$		0.01	10.0	nA
Output 'H'-Level Voltage	V_{OH}	PDR1,PDR2 PDT1,PDT2	I_O = 0.1mA	0.6V_{DD}			V
Output 'L'-Level Voltage	$V_{OL(1)}$	PDR1,PDR2 PDT1,PDT2	I_O = 0.1mA			0.3	V
	$V_{OL(2)}$	$\overline{LDR}$,$\overline{LDT}$	I_O = 1.0mA			1.0	V
	$V_{OL(3)}$	AOR,AOT	I_O = 0.5mA AIR/AIT = 1.2V			0.5	V
Output OFF-State Leakage Current	$I_{OFF(1)}$	$\overline{LDR}$,$\overline{LDT}$	V_O = 5.5V			5.0	μA
	$I_{OFF(2)}$	AOR,AOT	V_O = 5.5V			1.0	μA
	$I_{OFF(3)}$	PDR1,PDR2 PDT1,PDT2	V_O = 0.3V, V_O = 5.5V		0.01	10.0	nA
Input Capacitance	C_{IN}	XIN,PIR,PIT			2.5		pF
Supply Current	$I_{DD(1)}$	RV_{DD}	※1		23	32	mA
	$I_{DD(2)}$	RV_{DD} + TV_{DD}	※2		45	62	mA

LM7006 and LM7006H Difference				min	typ	max	unit
LM7006	I_{DD}	RV_{DD} + TV_{DD}	※2, Ta = 25°C			50	mA
LM7006H	I_{DD}	RV_{DD} + TV_{DD}	※2, Ta = 25°C	50		55	mA

※1 XIN = 12.8MHz,
PIR = 400MHz (70mVrms),
other inputs : V_{SS},
outputs : open

※2 XIN = 12.8MHz,
PIR = 400MHz (70mVrms),
PIT = 400MHz (70mVrms),
other inputs : V_{SS},
outputs : open

Note : The LM7006H is distinguished by an orange marking. I_{DD} is the only difference between the two devices.

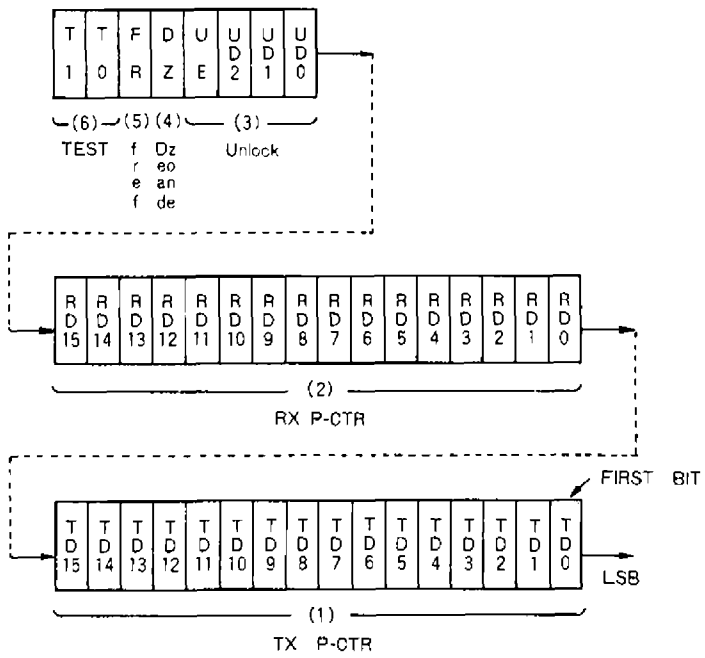
Pin Description

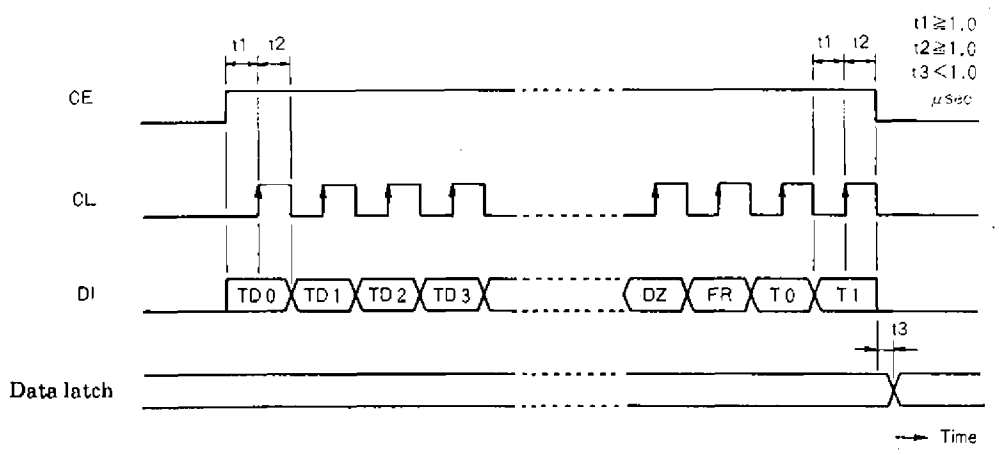
Pin Name	Pin No.	Input/Output	Description
XIN	2	Input	Reference OSC input 12.800MHz,50mVrms minimum (TCX0)
PIT	14	Input	Transmit VCO input 200 to 400MHz,70mVrms minimum. Division ratio of transmit programmable divider is set by the TD0 to TD15 control bits to between 256 and 65535.
PIR	16	Input	Receive VCO input 200 to 400MHz,70mVrms minimum. Division ratio of receive programmable divider is set by the RD0 to RD15 control bits to between 256 and 65535.
RV_{DD}	17	–	Receive section power supply 4.0 to 5.5V to data shift register latch, reference divider, RX programmable divider, RX phase detector, RX unlock detector.
TV_{DD}	13	– ※1	Transmit section power supply 4.0 to 5.5V to TX programmable divider, TX phase detector, TX unlock detector.
V_{BB}	1	Output	Back gate bias pin Requires a 0.01μF capacitor between V_{BB} and ground.
V_{SS}	15	–	Ground
$\overline{LDT}$ $\overline{LDR}$	8 7	Output [N-channel Open drain]	N-channel open-drain lock/unlock outputs for transmit and receive PLLs Lock : High-impedance Unlock : LOW The lock/unlock phase boundary is set by the UD0 to UD2 control bits. Extension of the phase difference signal is selected by the UE control flag.
PDT1 PDR1	9 5	Output (Tri-state)	Tri-state main charge pump outputs for transmit and receive PLLs Driven by the phase error signal obtained by comparing PLL frequency divided by N (fosc/N) with the reference frequency (fref) fosc/N > fref or leading: positive pulses fosc/N < fref or lagging: negative pulses fosc/N = fref: high-impedance
PDT2 PDR2	10 6	Output (Tri-state)	Tri-state auxiliary charge pump outputs for transmit and receive PLLs Driven by the PLLs phase error outputs only while PLL is out of lock, and high-impedance while PLL is in the lock range set by UD0 to UD2. Same polarity as main charge pump outputs.
AIT AOR	11 12	Input Ouptut	MOS N-channel transistor for TX PLL loop filter
AIR AOR	4 3	Input Output	MOS N-channel transistor for RX PLL loop filter
CE	18	Input ※2	Chip enable input A HIGH level enables serial data transfer into the LM7006.
CL	19	Input ※2	Serial input data clock
DI	20	Input ※2	Serial data input

※1 TV_{DD} Pin is connected to V_{SS} when transmit circuit is in power-off state (standby mode).
For instance, connect resistor (47kΩ to 100kΩ) between TV_{DD} and V_{SS}.

※2 High and Low input voltages on CE, CL, DI are held in the following range, respectively, regardless of the supply voltage (RV_{DD}).
V_{IH} = 2.5 to 5.5V, V_{IL} = 0 to 0.5V

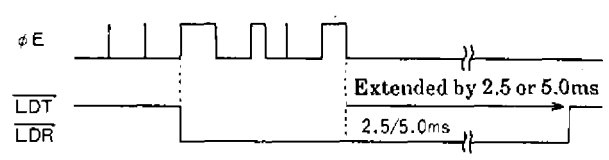
Device Control



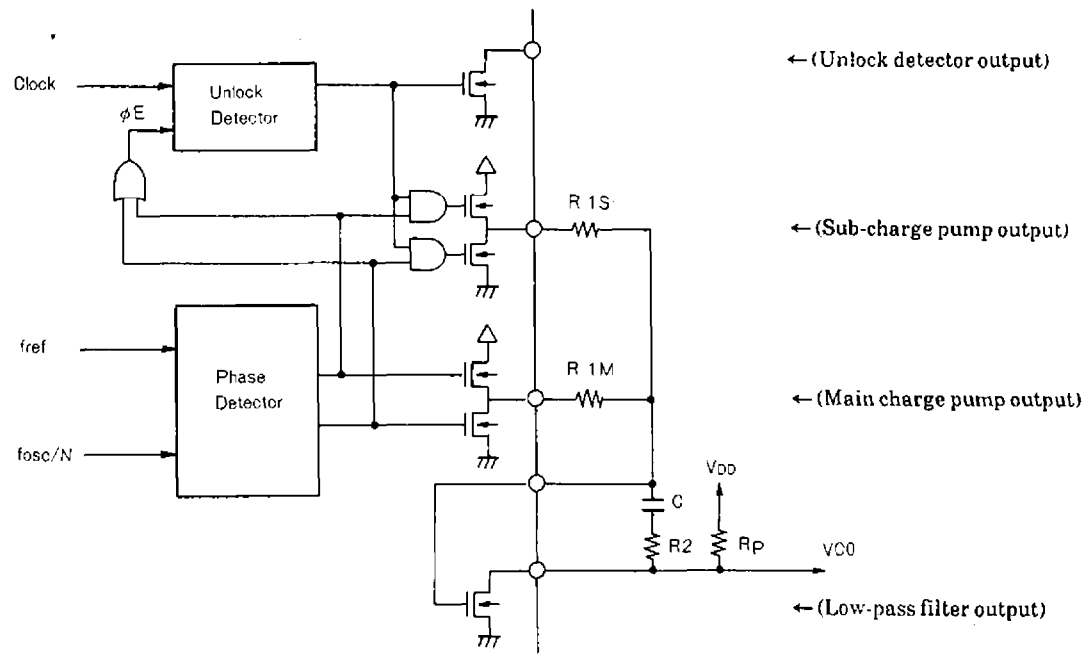


※ As the state of output pins of the LM7006 is unsettled when power is applied to them, the data must be sent from microcontroller as soon as possible.

<table>
<tr><th>No.</th><th>Data</th><th>Description</th><th>Associated data bits</th></tr>
<tr><td>(1)</td><td>TX Programmable Divider :
TD0 to TD15</td><td>TD0 to TD15 form the TX side programmable divider ratio. TD0 is the least significant bit, and TD15 the most significant bit. The divider ratio must be between 256 and 65535, inclusive.</td><td>FR</td></tr>
<tr><td>(2)</td><td>RX Programmable Divider :
RD0 to RD15</td><td>RD0 to RD15 form the RX side programmable divider ratio. RD0 is the least significant bit, and RD15 the most significant bit. The divider ratio must be between 256 and 65535, inclusive.</td><td>FR</td></tr>
<tr><td>(3)</td><td>UD0
UD1
UD2

Unlock Detector Control :
UE</td><td>UD0 to UD2 set the lock detector phase difference lock/unlock limit, as shown in the table below.
<table>
<tr><th>UD2</th><th>UD1</th><th>UD0</th><th>Signal Name</th><th>Phase Difference (øE) Detection Width (µsec)</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>ULD0</td><td>øE > 0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>ULD1</td><td>øE > 1.25</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>ULD2</td><td>øE > 0.30</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>ULD3</td><td>øE > 5.00</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>ULD4</td><td>øE > 0.15</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>ULD5</td><td>øE > 2.50</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>ULD6</td><td>øE > 0.60</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>ULD7</td><td>øE > 10.00</td></tr>
</table>
UE controls the format of the lock detector $\overline{LDT}$ and $\overline{LDR}$ output signals. The figure below illustrates this operation.
<table>
<tr><th>Signal Name</th><th>UE</th><th>$\overline{LDT}$/$\overline{LDR}$ Outputs</th></tr>
<tr><td>ULD0</td><td>0/1</td><td>Directly output the phase error signal</td></tr>
<tr><td rowspan="2">ULD0 to ULD7</td><td>0</td><td>The phase error signal is extended by 2.5ms</td></tr>
<tr><td>1</td><td>The phase error signal is extended by 5.0ms</td></tr>
</table>

</td><td></td></tr>
<tr><td>(4)</td><td>Dead Zone Control :
DZ</td><td>Selects the width of the phase comparator insensitive region.
DZ=0 : narrow
DZ=1 : wide</td><td></td></tr>
<tr><td>(5)</td><td>Reference frequency Select :
FR</td><td>FR=0 : reference frequency=25.0kHz
FR=1 : reference frequency=12.5kHz</td><td>TD0 to TD15
RD0 to RD15</td></tr>
<tr><td>(6)</td><td>Device Test Flags :
T0,T1</td><td>T0 and T1 are used to test the LM7006. They should both be set to "0" for normal operation.</td><td></td></tr>
</table>

Dual Charge Pump



The dual charge pump circuit ensures good performance during normal tracking and fast lock-in shown input frequency charges. During normal operation, only the main charge pump is employed to keep the PLL in sync. The auxiliary charge pump output is high-impedance. The loop filter time constant is relatively high, thus ensuring good sideband and modulation characteristics. When channels are changed, the PLL will lose lock and the auxiliary charge pump is activated. The filter resistor now consists of both R1S and R1M in parallel, reducing the filter time constant. PLL lock-in is thus accelerated.

Sample Application Circuit