

# LM9036 Ultra-Low Quiescent Current Voltage Regulator

Check for Samples: LM9036

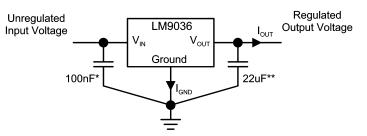
## FEATURES

- Ultra low Ground Pin Current (I<sub>GND</sub> ≤ 25µA for I<sub>OUT</sub> = 0.1mA)
- Fixed 5V, 3.3V, 50mA Output
- Output Tolerance ±5% Over Line, Load, and Temperature
- Dropout Voltage Typically 200mV @ I<sub>OUT</sub> = 50mA
- -45V Reverse Transient Protection
- Internal Short Circuit Current Limit
- Internal Thermal Shutdown Protection
- 40V Operating Voltage Limit

### **Typical Application**

## DESCRIPTION

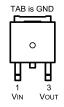
The LM9036 ultra-low quiescent current regulator features low dropout voltage and low current in the standby mode. With less than  $25\mu$ A Ground Pin current at a 0.1mA load, the LM9036 is ideally suited for automotive and other battery operated systems. The LM9036 retains all of the features that are common to low dropout regulators including a low dropout PNP pass device, short circuit protection, reverse battery protection, and thermal shutdown. The LM9036 has a 40V maximum operating voltage limit, a  $-40^{\circ}$ C to  $+125^{\circ}$ C operating temperature range, and  $\pm5\%$  output voltage tolerance over the entire output current, input voltage, and temperature range.



\* Required if regulator is located more than 2" from power supply filter capacitor.

\*\* Required for stability. Must be rated over intended operating temperature range. Effective series resistance (ESR) is critical, see Electrical Characteristics. Locate capacitor as close as possible to the regulator output and ground pins. Capacitance may be increased without bound.

## **Connection Diagram**



#### Figure 1. PFM Top View Order Number LM9036DT-5.0, LM9036DTX-5.0, LM9036DT-3.3, LM9036DTX-3.3 See NS Package Number NDP0003B

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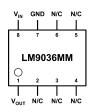
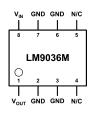


Figure 2. 8 Lead VSSOP
Top View
LM9036MM-3.3, , LM9036MMX-3.3, LM9036MM-5.0,
LM9036MMX-5.0
See NS Package Number DGK



#### Figure 3. 8 Lead SOIC Top View LM9036M-3.3, LM9036MX-3.3, LM9036M-5.0, LM9036MX-5.0 See NS Package Number D

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings<sup>(1)(2)</sup>

Input Voltage (Survival)	+55V, -45V
ESD Susceptibility <sup>(3)</sup>	±1.9kV
Power Dissipation <sup>(4)</sup>	Internally limited
Junction Temperature (T <sub>Jmax</sub> )	150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating ratings.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

(3) Human body model, 100pF discharge through a  $1.5k\Omega$  resistor.

(4) The maximum power dissipation is a function of T<sub>Jmax</sub>, θ<sub>JA</sub>, and T<sub>A</sub>. The maximum allowable power dissipation at any ambient temperature is P<sub>D</sub> = (T<sub>Jmax</sub> - T<sub>A</sub>)/θ<sub>JA</sub>. If this dissipation is exceeded, the die temperature will rise above 150°C and the LM9036 will go into thermal shutdown.

## **Operating Ratings**

Operating Temperature Range	-40°C to +125°C
Maximum Input Voltage (Operational)	40V
SOIC-8 (D) θ <sub>JA</sub> <sup>(1)</sup>	140°C/W
PFM (NDP0003B) θ <sub>JA</sub> <sup>(1)</sup>	125°C/W
PFM (NDP0003B) θ <sub>JA</sub> <sup>(2)</sup>	50°C/W
PFM (NDP0003B) θ <sub>JC</sub> <sup>(1)</sup>	11°C/W
MSO-8 (DGK) θ <sub>JA</sub> <sup>(1)</sup>	200°C/W

(1) Worst case (Free Air) per EIA / JESD51-3.

(2) Typical  $\theta_{JA}$  with 1 square inch of 2oz copper pad area directly under the ground tab.



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### **Electrical Characteristics - LM9036-5.0**

 $V_{IN}$  = 14V,  $I_{OUT}$  = 10 mA,  $T_J$  = 25°C, unless otherwise specified. **Boldface** limits apply over entire operating temperature range

Parameter	Conditions	Min (1)	Typical	Max (1)	Units
		4.80	5.00	5.20	
Output Voltage (V <sub>OUT</sub> )	$5.5V \le V_{IN} \le 26V$ , $0.1mA \le I_{OUT} \le 50mA^{(3)}$	4.75	5.00	5.25	V
	$I_{OUT} = 0.1 \text{mA}, 8\text{V} \le \text{V}_{IN} \le 24 \text{V}$		20	25	
Quieseent Quirrent (1)	$I_{OUT} = 1$ mA, 8V $\leq V_{IN} \leq 24$ V		50	100	μΑ
Quiescent Current (I <sub>GND</sub> )	$I_{OUT} = 10mA, 8V \le V_{IN} \le 24V$		0.3	0.5	
	$I_{OUT} = 50 \text{mA}, 8 \text{V} \le \text{V}_{IN} \le 24 \text{V}$		2.0	2.5	mA
Line Regulation ( $\Delta V_{OUT}$ )	$6V \le V_{IN} \le 40V, I_{OUT} = 1mA$		10	30	mV
Load Regulation ( $\Delta V_{OUT}$ )	0.1mA ≤ I <sub>OUT</sub> ≤ 5mA		10	30	mV
	5mA ≤ I <sub>OUT</sub> ≤ 50mA		10	30	mV
Dropout Voltage ( $\Delta V_{OUT}$ )	I <sub>OUT</sub> = 0.1mA		0.05	0.10	V
	I <sub>OUT</sub> = 50mA		0.20	0.40	V
Short Circuit Current (I <sub>SC</sub> )	V <sub>OUT</sub> = 0V	65	120	250	mA
Ripple Rejection (PSRR)	V <sub>ripple</sub> = 1V <sub>rms</sub> , F <sub>ripple</sub> = 120Hz	-40	-60		dB
Output Bypass Capacitance (C <sub>OUT</sub> )	$0.3\Omega \le \text{ESR} \le 8\Omega$ $0.1\text{mA} \le I_{OUT} \le 50\text{mA}$	10	22		μF

(1) Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level) and 100% tested.

(2) Typicals are at 25°C (unless otherwise specified) and represent the most likely parametric norm.

(3) To ensure constant junction temperature, pulse testing is used.

### **Electrical Characteristics - LM9036-3.3**

 $V_{IN} = 14V$ ,  $I_{OUT} = 10$  mA,  $T_J = 25^{\circ}$ C, unless otherwise specified. **Boldface** limits apply over entire operating temperature range

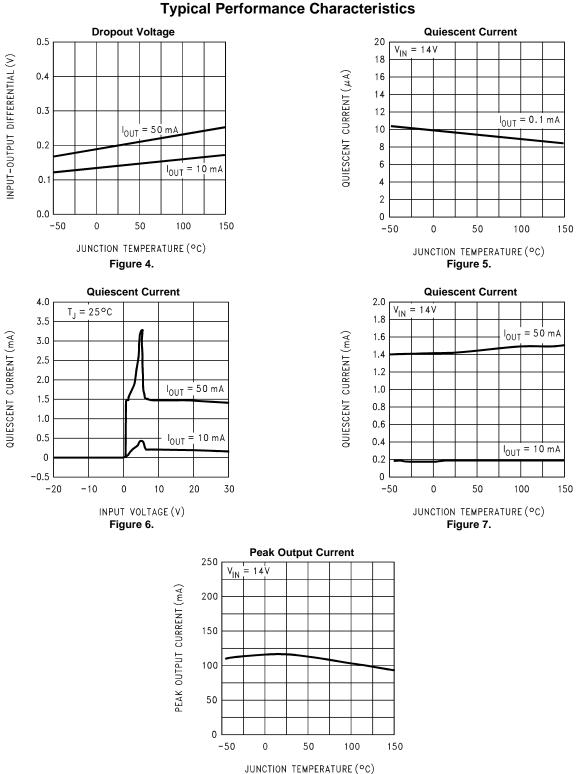
Parameter	Conditions	Min (1)	Typical	Max (1)	Units
		3.168	3.30	3.432	
Output Voltage (V <sub>OUT</sub> )	$5.5V \le V_{IN} \le 26V$ , $0.1mA \le I_{OUT} \le 50mA^{(3)}$	3.135	3.30	3.465	V
	$I_{OUT} = 0.1 \text{mA}, 8\text{V} \le \text{V}_{IN} \le 24 \text{V}$		20	25	۵
Outersent Outerset (I )	$I_{OUT} = 1$ mA, 8V $\leq V_{IN} \leq 24$ V		50	100	μA
Quiescent Current (I <sub>GND</sub> )	$I_{OUT} = 10$ mA, $8V \le V_{IN} \le 24V$		0.3	0.5	0
	$I_{OUT} = 50$ mA, 8V $\leq V_{IN} \leq 24$ V		2.0	2.5	mA
Line Regulation ( $\Delta V_{OUT}$ )	$6V \le V_{IN} \le 40V, I_{OUT} = 1mA$		10	30	mV
Load Regulation ( $\Delta V_{OUT}$ )	0.1mA ≤ I <sub>OUT</sub> ≤ 5mA		10	30	mV
	$5mA \le I_{OUT} \le 50mA$		10	30	mV
Dropout Voltage (Δ V <sub>OUT</sub> )	I <sub>OUT</sub> = 0.1mA		0.05	0.10	V
	I <sub>OUT</sub> = 50mA		0.20	0.40	V
Short Circuit Current (I <sub>SC</sub> )	V <sub>OUT</sub> = 0V	65	120	250	mA
Ripple Rejection (PSRR)	$V_{ripple} = 1V_{rms}, F_{ripple} = 120Hz$	-40	-60		dB
Output Bypass Capacitance (C <sub>OUT</sub> )	$0.3\Omega \le \text{ESR} \le 8\Omega$ $0.1\text{mA} \le I_{OUT} \le 50\text{mA}$	22	33		μF

(1) Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level) and 100% tested.

(2) Typicals are at 25°C (unless otherwise specified) and represent the most likely parametric norm.

(3) To ensure constant junction temperature, pulse testing is used.

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### **APPLICATIONS INFORMATION**

Unlike other PNP low dropout regulators, the LM9036 remains fully operational to 40V. Owing to power dissipation characteristics of the package, full output current cannot be guaranteed for all combinations of ambient temperature and input voltage.

The junction to ambient thermal resistance  $\theta_{JA}$  rating has two distinct components: the junction to case thermal resistance rating  $\theta_{JC}$ ; and the case to ambient thermal resistance rating  $\theta_{CA}$ . The relationship is defined as:  $\theta_{JA} = \theta_{JC} + \theta_{CA}$ .

On the PFM package the ground tab is thermally connected to the backside of the die. Adding 1 square inch of 2 oz. copper pad area directly under the ground tab will improve the  $\theta_{JA}$  rating to approximately 50°C/W.

While the LM9036 has an internally set thermal shutdown point of typically 150°C, this is intended as a safety feature only. Continuous operation near the thermal shutdown temperature should be avoided as it may have a negative affect on the life of the device.

Using the  $\theta_{JA}$  for a LM9036DT mounted on a circuit board as defined at, see<sup>(1)</sup>, and using the formula for maximum allowable dissipation given in, see<sup>(2)</sup>, for an ambient temperature (T<sub>A</sub>) of +85°C, we find that P<sub>DMAX</sub> = 1.3W. Including the small contribution of the quiescent current I<sub>Q</sub> to the total power dissipation, the maximum input voltage (while still delivering 50mA output current) is 29.5V. The LM9036DT will go into thermal shutdown when attempting to deliver the full output current of 50mA, with an ambient temperature of +85°C, and the input voltage is greater than 29.5V. Similarly, with an ambient temperature of 25°C the P<sub>DMAX</sub> = 2.5W, and the LM9036DT can deliver the full output current of 50mA with an input voltage of up to 40V.

While the LM9036 maintains regulation to 55V, it will not withstand a short circuit above 40V because of safe operating area limitations in the internal PNP pass device. Above 55V the LM9036 will break down with catastrophic effects on the regulator and possibly the load as well. Do not use this device in a design where the input operating voltage may exceed 40V, or where transients are likely to exceed 55V.

- (1) Typical  $\theta_{JA}$  with 1 square inch of 2oz copper pad area directly under the ground tab.
- (2) The maximum power dissipation is a function of  $T_{Jmax}$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any ambient temperature is  $P_D = (T_{Jmax} T_A)/\theta_{JA}$ . If this dissipation is exceeded, the die temperature will rise above 150°C and the LM9036 will go into thermal shutdown.



9-Mar-2013

## **PACKAGING INFORMATION**

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	•	Op Temp (°C)		Samples
LM9036DT-5.0	(1) ACTIVE	PFM	NDP	3	75	(2) TBD	Call TI	(3) Call TI	-40 to 125	(4) LM9036D T-5.0	Samples
LM9036DT-5.0/NOPB	ACTIVE	PFM	NDP	3	75	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	LM9036D T-5.0	Samples
LM9036DTX-5.0	ACTIVE	PFM	NDP	3	2500	TBD	Call TI	Call TI	-40 to 125	LM9036D T-5.0	Samples
LM9036DTX-5.0/NOPB	ACTIVE	PFM	NDP	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	LM9036D T-5.0	Samples
LM9036M-3.3	ACTIVE	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 125	LM903 6M-3	Samples
LM9036M-3.3/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM903 6M-3	Samples
LM9036M-5.0	ACTIVE	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 125	LM903 6M-5	Samples
LM9036M-5.0/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM903 6M-5	Samples
LM9036MM-3.3	ACTIVE	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 125	KDB	Samples
LM9036MM-3.3/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	KDB	Samples
LM9036MM-5.0	ACTIVE	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 125	KDA	Samples
LM9036MM-5.0/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	KDA	Samples
LM9036MMX-3.3	ACTIVE	VSSOP	DGK	8	3500	TBD	Call TI	Call TI	-40 to 125	KDB	Samples
LM9036MMX-5.0	ACTIVE	VSSOP	DGK	8	3500	TBD	Call TI	Call TI	-40 to 125	KDA	Samples
LM9036MX-3.3	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 125	LM903 6M-3	Samples
LM9036MX-3.3/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM903 6M-3	Samples
LM9036MX-5.0	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 125	LM903 6M-5	Samples
LM9036MX-5.0/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM903 6M-5	Samples



9-Mar-2013

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> Only one of markings shown within the brackets will appear on the physical device.

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## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



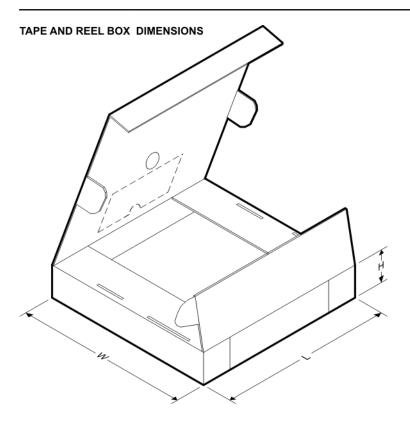
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM9036DTX-5.0	PFM	NDP	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
LM9036DTX-5.0/NOPB	PFM	NDP	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
LM9036MM-3.3	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM9036MM-3.3/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM9036MM-5.0	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM9036MM-5.0/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM9036MMX-3.3	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM9036MMX-5.0	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM9036MX-3.3	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM9036MX-3.3/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM9036MX-5.0	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM9036MX-5.0/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

TEXAS INSTRUMENTS

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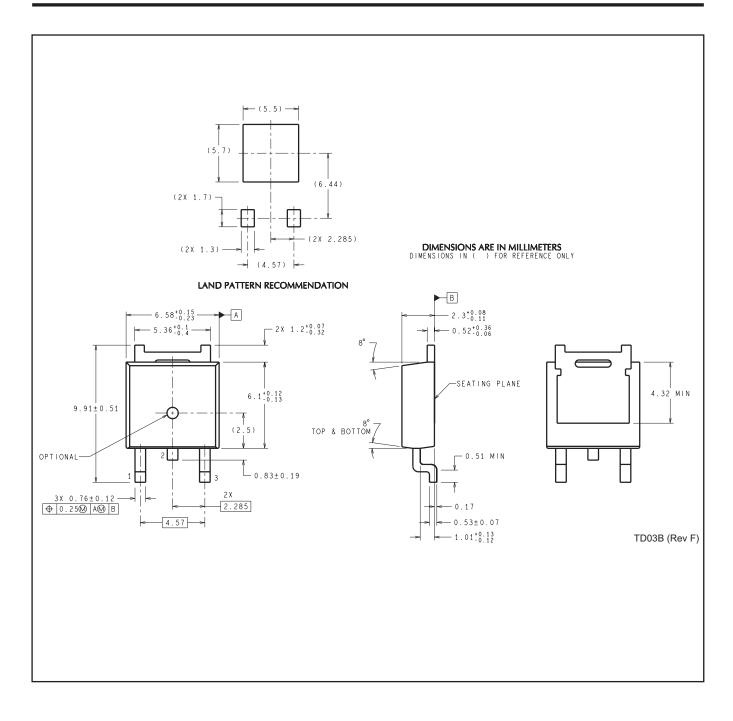
19-Feb-2013



*All dimensions are nominal							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM9036DTX-5.0	PFM	NDP	3	2500	354.0	340.0	35.0
LM9036DTX-5.0/NOPB	PFM	NDP	3	2500	358.0	343.0	63.0
LM9036MM-3.3	VSSOP	DGK	8	1000	203.0	190.0	41.0
LM9036MM-3.3/NOPB	VSSOP	DGK	8	1000	203.0	190.0	41.0
LM9036MM-5.0	VSSOP	DGK	8	1000	203.0	190.0	41.0
LM9036MM-5.0/NOPB	VSSOP	DGK	8	1000	203.0	190.0	41.0
LM9036MMX-3.3	VSSOP	DGK	8	3500	349.0	337.0	45.0
LM9036MMX-5.0	VSSOP	DGK	8	3500	349.0	337.0	45.0
LM9036MX-3.3	SOIC	D	8	2500	349.0	337.0	45.0
LM9036MX-3.3/NOPB	SOIC	D	8	2500	349.0	337.0	45.0
LM9036MX-5.0	SOIC	D	8	2500	349.0	337.0	45.0
LM9036MX-5.0/NOPB	SOIC	D	8	2500	349.0	337.0	45.0

# **MECHANICAL DATA**

# NDP0003B



DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.

- D Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.



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