

LMH6642EP, LMH6643EP, LMH6644EP

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LMH6642EP/LMH6643EP/LMH6644EP Enhanced Plastic Low Power, 130MHz, 75mA Railto-Rail Output Amplifiers

Check for Samples: LMH6642EP, LMH6643EP, LMH6644EP

FEATURES

- $(V_S = \pm 5V, T_A = 25^{\circ}C, R_L = 2k\Omega, A_V = +1.$ Typical values unless specified).
- $-3dB BW (A_V = +1) 130MHz$
- Supply voltage range 2.7V to 12.8V
- Slew rate ⁽¹⁾, (A_V = −1) 130V/µs
- Supply current (no load) 2.7mA/amp
- Output short circuit current +115mA/-145mA
- Linear output current ±75mA
- Input common mode volt. 0.5V beyond V⁻, 1V from V⁺
- · Output voltage swing 40mV from rails
- Input voltage noise (100kHz) 17nVI/√Hz
- Input current noise (100kHz) 0.9pA/√Hz
- (1) Slew rate is the average of the rising and falling slew rates.

- THD (5MHz, $R_L = 2k\Omega$, $V_O = 2V_{PP}$, $A_V = +2$) -62dBc
- Settling time 68ns
- Fully characterized for 3V, 5V, and ±5V
- Overdrive recovery 100ns
- Output short circuit protected (2)
- No output phase reversal with CMVR exceeded

APPLICATIONS

- Selected Military Applications
- Selected Avionics Applications
- Output short circuit duration is infinite for V_S < 6V at room temperature and below. For V_S > 6V, allowable short circuit duration is 1.5ms.

DESCRIPTION

The LMH664XEP family true single supply voltage feedback amplifiers offer high speed (130MHz), low distortion (-62dBc), and exceptionally high output current (approximately 75mA) at low cost and with reduced power consumption when compared against existing devices with similar performance.

Input common mode voltage range extends to 0.5V below V^- and 1V from V^+ . Output voltage range extends to within 40mV of either supply rail, allowing wide dynamic range especially desirable in low voltage applications. The output stage is capable of approximately 75mA in order to drive heavy loads. Fast output Slew Rate $(130V/\mu s)$ ensures large peak-to-peak output swings can be maintained even at higher speeds, resulting in exceptional full power bandwidth of 40MHz with a 3V supply. These characteristics, along with low cost, are ideal features for a multitude of industrial and commercial applications.

Careful attention has been paid to ensure device stability under all operating voltages and modes. The result is a very well behaved frequency response characteristic (0.1dB gain flatness up the 12MHz under 150 Ω load and A_V = +2) with minimal peaking (typically 2dB maximum) for any gain setting and under both heavy and light loads. This along with fast settling time (68ns) and low distortion allows the device to operate well in ADC buffer, and high frequency filter applications as well as other applications.

This device family offers professional quality video performance with low DG (0.01%) and DP (0.01°) characteristics. Differential Gain and Differential Phase characteristics are also well maintained under heavy loads (150 Ω) and throughout the output voltage range. The LMH664XEP family is offered in single (LMH6642EP), dual (LMH6643EP), and quad (LMH6644EP) options. See ordering information for packages offered.

ENHANCED PLASTIC

- Extended Temperature Performance of −40°C to +85°C
- Baseline Control Single Fab & Assembly Site
- Process Change Notification (PCN)
- Qualification & Reliability Data
- Solder (PbSn) Lead Finish is standard

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Enhanced Diminishing Manufacturing Sources (DMS) Support



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

2KV ⁽²⁾
200V ⁽³⁾
±2.5V
(4), (5)
13.5V
V ⁺ +0.8V, V [−] −0.8V
±10mA
−65°C to +150°C
+150°C
235°C
260°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.
- (2) Human body model, 1.5kΩ in series with 100pF.
- 3) Machine Model, 0Ω in series with 200pF.
- (4) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
- (5) Output short circuit duration is infinite for V_S < 6V at room temperature and below. For V_S > 6V, allowable short circuit duration is 1.5ms.
- (6) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Operating Ratings (1)

2.7V to 12.8V
−40°C to +85°C
265°C/W
190°C/W
235°C/W
145°C/W
155°C/W

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.
- (2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

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3V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for at $T_J = 25^{\circ}C$, $V^+ = 3V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$, and $R_L = 2k\Omega$ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ	Max (1)	Units
BW	-3dB BW	$A_V = +1, V_{OUT} = 200 \text{mV}_{PP}$	80	115		N 41 1
		A _V = +2, −1, V _{OUT} = 200mV _{PP}		46		MHz
BW _{0.1dB}	0.1dB Gain Flatness	$A_V = +2$, $R_L = 150\Omega$ to V+/2, $R_L = 402\Omega$, $V_{OUT} = 200 \text{mV}_{PP}$		19		MHz
PBW	Full Power Bandwidth	$A_V = +1$, $-1dB$, $V_{OUT} = 1V_{PP}$		40		MHz
e _n	Input-Referred Voltage Noise	f = 100kHz		17		\/\land
		f = 1kHz		48		nV/√Hz
i _n	Input-Referred Current Noise	f = 100kHz		0.90		pA√Hz
		f = 1kHz		3.3		
THD	Total Harmonic Distortion	$f = 5MHz$, $V_O = 2V_{PP}$, $A_V = -1$, $R_L = 100\Omega$ to $V^+/2$		-48		dBc
DG	Differential Gain	$V_{CM} = 1V$, NTSC, $A_V = +2$ $R_L = 150\Omega$ to $V^+/2$		0.17		%
		$R_L = 1k\Omega$ to V ⁺ /2		0.03		7
DP	Differential Phase	$V_{CM} = 1V$, NTSC, $A_V = +2$ $R_L = 150\Omega$ to $V^+/2$		0.05		deg
		$R_L = 1k\Omega$ to V ⁺ /2		0.03		
CT Rej.	Cross-Talk Rejection	f = 5MHz, Receiver: $R_f = R_g = 510\Omega$, $A_V = +2$		47		dB
T _S	Settling Time	V _O = 2V _{PP} , ±0.1%, 8pF Load, V _S = 5V		68		ns
SR	Slew Rate (3)	$A_V = -1$, $V_I = 2V_{PP}$	90	120		V/µs
V _{OS}	Input Offset Voltage			±1	±5 ±7	mV
TC V _{OS}	Input Offset Average Drift	(4)		±5		μV/°C
I _B	Input Bias Current	(5)		-1.50	-2.60 -3.25	μA
I _{OS}	Input Offset Current			20	800 1000	nA
R _{IN}	Common Mode Input Resistance			3		МΩ
C _{IN}	Common Mode Input Capacitance			2		pF
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 50dB		-0.5	-0.2 - 0.1	
			1.8 1.6	2.0		V
CMRR	Common Mode Rejection Ratio	V _{CM} Stepped from 0V to 1.5V	72	95		dB
A _{VOL}	Large Signal Voltage Gain	$V_O = 0.5V$ to 2.5V R _L = 2k Ω to V ⁺ /2	80 75	96		.10
		$V_{O} = 0.5V$ to 2.5V $R_{L} = 150\Omega$ to $V^{+}/2$	74 70	82		- dB
Vo	Output Swing	$R_L = 2k\Omega \text{ to V}^+/2, V_{ID} = 200\text{mV}$	2.90	2.98		.,
	High	$R_L = 150\Omega$ to V ⁺ /2, $V_{ID} = 200$ mV	2.80	2.93		V
	Output Swing	$R_L = 2k\Omega \text{ to V}^+/2, V_{ID} = -200\text{mV}$		25	75 m\/	.,
	Low	$R_L = 150\Omega$ to V ⁺ /2, $V_{ID} = -200$ mV		75	150	mV

All limits are guaranteed by testing or statistical analysis.

Typical values represent the most likely parametric norm. Slew rate is the average of the rising and falling slew rates.

Offset voltage average drift determined by dividing the change in VOS at temperature extremes by the total temperature change.

Positive current corresponds to current flowing into the device.



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3V Electrical Characteristics (continued)

Unless otherwise specified, all limits guaranteed for at $T_J = 25$ °C, $V^+ = 3V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$, and $R_L = 2k\Omega$ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
I _{SC}	Output Short Circuit Current	Sourcing to V ⁺ /2 V _{ID} = 200mV ⁽⁶⁾	50 35	95		A
		Sinking to V ⁺ /2 $V_{ID} = -200 \text{mV}^{(6)}$	55 40	110		- mA
I _{OUT}	Output Current	V _{OUT} = 0.5V from either supply		±65		mA
+PSRR	Positive Power Supply Rejection Ratio	$V^{+} = 3.0V$ to 3.5V, $V_{CM} = 1.5V$	75	85		dB
Is	Supply Current (per channel)	No Load		2.70	4.00 4.50	mA

⁽⁶⁾ Short circuit test is a momentary test. See Note 14.

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5V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for at $T_J = 25$ °C, $V^+ = 5V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$, and $R_L = 2k\Omega$ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ	Max (1)	Units	
BW	-3dB BW	$A_V = +1$, $V_{OUT} = 200 \text{mV}_{PP}$	90	120		NAL 1-	
		$A_V = +2, -1, V_{OUT} = 200 \text{mV}_{PP}$		46		MHz	
BW _{0.1dB}	0.1dB Gain Flatness	$A_V = +2$, $R_L = 150\Omega$ to V+/2, $R_f = 402\Omega$, $V_{OUT} = 200 \text{mV}_{PP}$		15		MHz	
PBW	Full Power Bandwidth	A _V = +1, −1dB, V _{OUT} = 2V _{PP}		22		MHz	
e _n	Input-Referred Voltage Noise	f = 100kHz		17		->4/11	
		f = 1kHz		48		nV/√Hz	
i _n	Input-Referred Current Noise	f = 100kHz		0.90		- A / /II-	
		f = 1kHz		3.3		pA/√Hz	
THD	Total Harmonic Distortion	$f = 5MHz, V_O = 2V_{PP}, A_V = +2$		-60		dBc	
DG	Differential Gain	NTSC, $A_V = +2$ $R_L = 150\Omega$ to $V^+/2$		0.16		%	
		$R_L = 1k\Omega$ to $V^+/2$		0.05			
DP	Differential Phase	NTSC, $A_V = +2$ $R_L = 150\Omega$ to $V^+/2$		0.05		deg	
		$R_L = 1k\Omega$ to V ⁺ /2		0.01			
CT Rej.	Cross-Talk Rejection	f = 5MHz, Receiver: $R_f = R_g = 510\Omega$, $A_V = +2$		47		dB	
T _S	Settling Time	V _O = 2V _{PP} , ±0.1%, 8pF Load		68		ns	
SR	Slew Rate (3)	$A_V = -1, V_I = 2V_{PP}$	95	125		V/µs	
V _{OS}	Input Offset Voltage			±1	±5 ±7	mV	
TC V _{OS}	Input Offset Average Drift	(4)		±5		μV/°C	
l _B	Input Bias Current	(5)		-1.70	-2.60 -3.25	μA	
I _{OS}	Input Offset Current			20	800 1000	nA	
R _{IN}	Common Mode Input Resistance			3		МΩ	
C _{IN}	Common Mode Input Capacitance			2		pF	
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 50dB		-0.5	-0.2 -0.1	V	
			3.8 3.6	4.0		V	
CMRR	Common Mode Rejection Ratio	V _{CM} Stepped from 0V to 3.5V	72	95		dB	
A _{VOL}	Large Signal Voltage Gain	$V_O = 0.5V$ to 4.50V $R_L = 2k\Omega$ to $V^+/2$	86 82	98		- dB	
		$V_{O} = 0.5V$ to 4.25V $R_{L} = 150\Omega$ to $V^{+}/2$	76 72	82		uв	
V _O	Output Swing	$R_L = 2k\Omega$ to V ⁺ /2, $V_{ID} = 200mV$	4.90	4.98		V	
	High	$R_L = 150\Omega$ to V ⁺ /2, $V_{ID} = 200$ mV	4.65	4.90			
	Output Swing	$R_L = 2k\Omega$ to V ⁺ /2, $V_{ID} = -200$ mV		25	100	m\/	
		Low	$R_L = 150\Omega$ to V ⁺ /2, $V_{ID} = -200$ mV		100	150	mV

⁽¹⁾ All limits are guaranteed by testing or statistical analysis.

⁽²⁾ Typical values represent the most likely parametric norm.

⁽³⁾ Slew rate is the average of the rising and falling slew rates.

⁽⁴⁾ Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes by the total temperature change.

⁽⁵⁾ Positive current corresponds to current flowing into the device.



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5V Electrical Characteristics (continued)

Unless otherwise specified, all limits guaranteed for at $T_J = 25^{\circ}C$, $V^+ = 5V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$, and $R_L = 2k\Omega$ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ	Max (1)	Units
I _{SC}	Output Short Circuit Current	Sourcing to V ⁺ /2 V _{ID} = 200mV ⁽⁶⁾	55 40	115		4
		Sinking to V ⁺ /2 $V_{ID} = -200 \text{mV}^{(6)}$	70 55	140		mA
I _{OUT}	Output Current	V _O = 0.5V from either supply		±70		mA
+PSRR	Positive Power Supply Rejection Ratio	V ⁺ = 4.0V to 6V	79	90		dB
Is	Supply Current (per channel)	No Load		2.70	4.25 5.00	mA

⁽⁶⁾ Short circuit test is a momentary test. See Note 14.



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±5V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for at $T_J = 25^{\circ}C$, $V^+ = 5V$, $V^- = -5V$, $V_{CM} = V_O = 0V$ and $R_L = 2k\Omega$ to ground. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units	
BW	-3dB BW	$A_V = +1, V_{OUT} = 200 \text{mV}_{PP}$	95	130		N 41 1-	
		A _V = +2, -1, V _{OUT} = 200mV _{PP}		46		MHz	
BW _{0.1dB}	0.1dB Gain Flatness	$A_V = +2$, $R_L = 150\Omega$ to V+/2, $R_f = 806\Omega$, $V_{OUT} = 200 \text{mV}_{PP}$		12		MHz	
PBW	Full Power Bandwidth	$A_V = +1, -1dB, V_{OUT} = 2V_{PP}$		24		MHz	
e _n	Input-Referred Voltage Noise	f = 100kHz		17			
		f = 1kHz		48		nV/√Hz	
i _n	Input-Referred Current Noise	f = 100kHz		0.90		A / /!!	
		f = 1kHz		3.3		pA/√Hz	
THD	Total Harmonic Distortion	$f = 5MHz, V_O = 2V_{PP}, A_V = +2$		-62		dBc	
DG	Differential Gain	NTSC, $A_V = +2$ $R_L = 150\Omega$ to $V^+/2$		0.15		%	
		$R_L = 1k\Omega$ to $V^+/2$		0.01			
DP	Differential Phase	NTSC, $A_V = +2$ $R_L = 150\Omega$ to $V^+/2$		0.04		deg	
		$R_L = 1k\Omega$ to $V^+/2$		0.01			
CT Rej.	Cross-Talk Rejection	f = 5MHz, Receiver: $R_f = R_g = 510\Omega$, $A_V = +2$		47		dB	
T _S	Settling Time	$V_{O} = 2V_{PP}, \pm 0.1\%, 8pF Load, V_{S} = 5V$		68		ns	
SR	Slew Rate (3)	$A_V = -1$, $V_I = 2V_{PP}$	100	135		V/µs	
V _{OS}	Input Offset Voltage			±1	±5 ±7	mV	
TC V _{OS}	Input Offset Average Drift	(4)		±5		μV/°C	
I _B	Input Bias Current	(5)		-1.60	-2.60 -3.25	μА	
I _{OS}	Input Offset Current			20	800 1000	nA	
R _{IN}	Common Mode Input Resistance			3		МΩ	
C _{IN}	Common Mode Input Capacitance			2		pF	
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 50dB		-5.5	-5.2 -5.1	V	
			3.8 3.6	4.0		V	
CMRR	Common Mode Rejection Ratio	V _{CM} Stepped from -5V to 3.5V	74	95		dB	
A _{VOL}	Large Signal Voltage Gain	$V_O = -4.5V$ to 4.5V, $R_L = 2k\Omega$	88 84	96		dB	
		$V_O = -4.0V$ to 4.0V, $R_L = 150\Omega$	78 74	82		UD	
Vo	Output Swing	$R_L = 2k\Omega$, $V_{ID} = 200mV$	4.90	4.96		V	
	High	$R_L = 150\Omega, V_{ID} = 200mV$	4.65	4.80		V	
	Output Swing	$R_L = 2k\Omega$, $V_{ID} = -200mV$		-4.96	-4.90	\/	
		Low	$R_L = 150\Omega, V_{ID} = -200 \text{mV}$		-4.80	-4.65	V

⁽¹⁾ All limits are guaranteed by testing or statistical analysis.

⁽²⁾ Typical values represent the most likely parametric norm.

⁽³⁾ Slew rate is the average of the rising and falling slew rates.

⁽⁴⁾ Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes by the total temperature change.

⁽⁵⁾ Positive current corresponds to current flowing into the device.

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±5V Electrical Characteristics (continued)

Unless otherwise specified, all limits guaranteed for at $T_J = 25^{\circ}C$, $V^+ = 5V$, $V^- = -5V$, $V_{CM} = V_O = 0V$ and $R_L = 2k\Omega$ to ground. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ	Max (1)	Units
I _{SC}	Output Short Circuit Current	Sourcing to Ground V _{ID} = 200mV ⁽⁶⁾	60 35	115		A
		Sinking to Ground V _{ID} = -200mV ⁽⁶⁾	85 65	145		- mA
I _{OUT}	Output Current	V _O = 0.5V from either supply	±75			mA
PSRR	Power Supply Rejection Ratio	$(V^+, V^-) = (4.5V, -4.5V)$ to $(5.5V, -5.5V)$	78	90		dB
Is	Supply Current (per channel)	No Load		2.70	4.50 5.50	mA

(6) Short circuit test is a momentary test. See Note 14.

Connection Diagram

SOT23-5 (LMH6642)

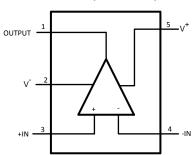


Figure 1. Top View

SOIC-8 (LMH6642)

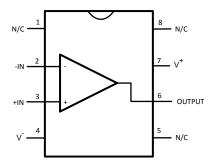


Figure 2. Top View

SOIC-8 and MSOP-8 (LMH6643)

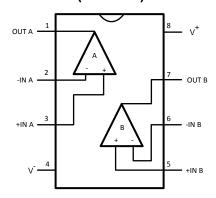


Figure 3. Top View

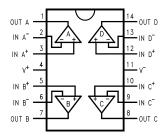


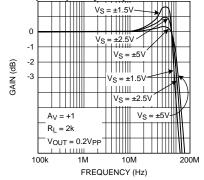
Figure 4. SOIC-14 and TSSOP-14, (LMH6644) - Top View



Typical Performance Characteristics

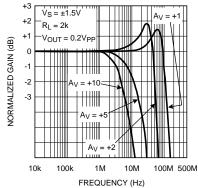
At $T_J = 25^{\circ}\text{C}$, $V^+ = +5$, $V^- = -5\text{V}$, $R_F = R_L = 2k\Omega$. Unless otherwise specified.

Closed Loop Frequency Response for Various Supplies

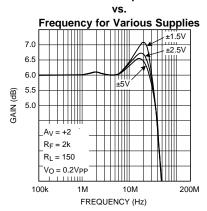


Closed Loop Gain

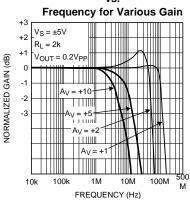
Frequency for Various Gain



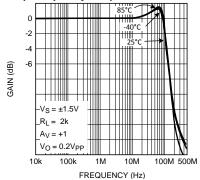
Closed Loop Gain



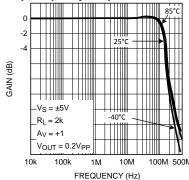
Closed Loop Gain vs.



Closed Loop Frequency Response for Various Temperature



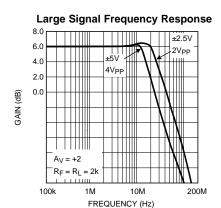
Closed Loop Frequency Response for Various Temperature



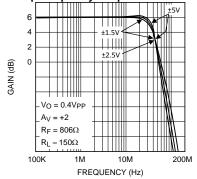
INSTRUMENTS

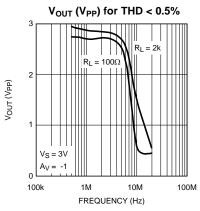


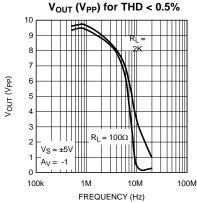
At $T_J = 25$ °C, $V^+ = +5$, $V^- = -5V$, $R_F = R_L = 2k\Omega$. Unless otherwise specified.



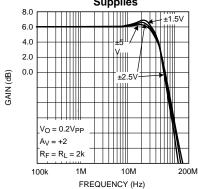
Closed Loop Frequency Response for Various Supplies



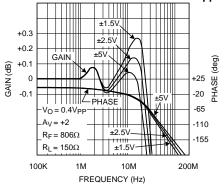


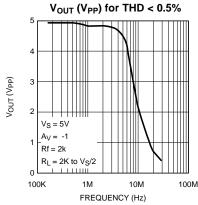


Closed Loop Small Signal Frequency Response for Various Supplies

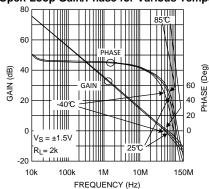


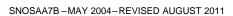
±0.1dB Gain Flatness for Various Supplies





Open Loop Gain/Phase for Various Temperature

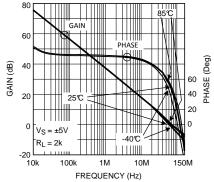




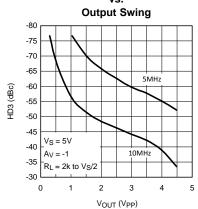


At $T_J = 25^{\circ}\text{C}$, $V^+ = +5$, $V^- = -5\text{V}$, $R_F = R_L = 2k\Omega$. Unless otherwise specified.

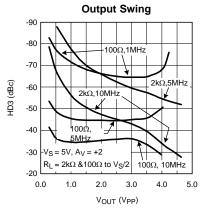
Open Loop Gain/Phase for Various Temperature



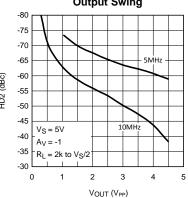




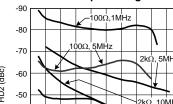
HD3 vs.

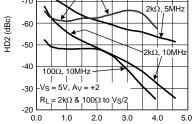


HD2 (dBc) vs. **Output Swing**



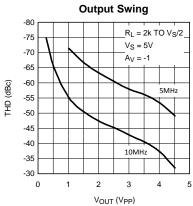
HD2 **Output Swing**





THD (dBc) vs.

V_{OUT} (V_{PP})



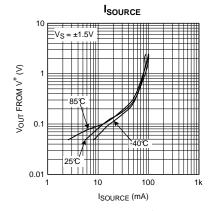
At $T_J = 25$ °C, $V^+ = +5$, $V^- = -5V$, $R_F = R_L = 2k\Omega$. Unless otherwise specified.

Settling Time

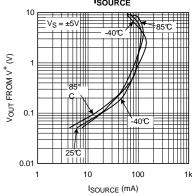
vs. Input Step Amplitude (Output Slew and Settle Time) 80 70 60 ±0.1% SETTLING TIME 50 40 30 20 A_V = -1 $R_f = R_L = 2k$ 10 $C_L = 8pF$ 0

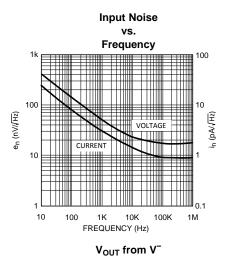
INPUT STEP AMPLITUDE (VPP) V_{OUT} from V⁺ vs.

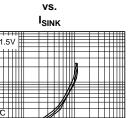
0.5

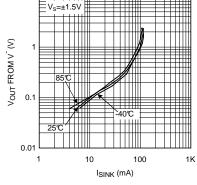


V_{OUT} from V⁺ vs. ISOURCE



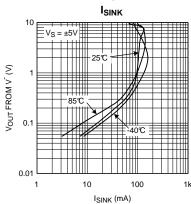


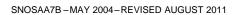




10

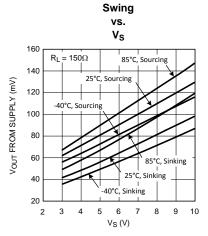
V_{OUT} from V vs.



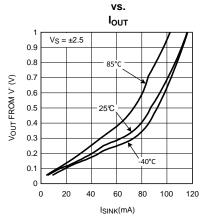




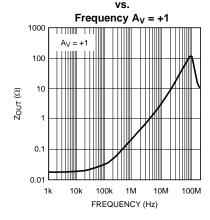
At $T_J = 25$ °C, $V^+ = +5$, $V^- = -5V$, $R_F = R_L = 2k\Omega$. Unless otherwise specified.



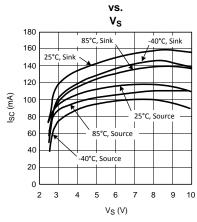
Output Sinking Saturation Voltage



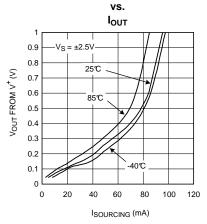
Closed Loop Output Impedance



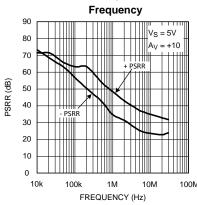
Short Circuit Current (to V_S/2)



Output Sourcing Saturation Voltage

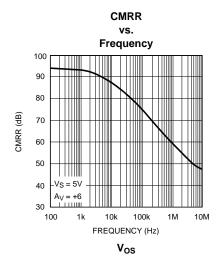


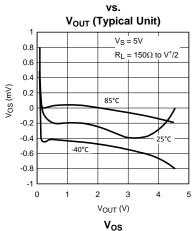
PSRR vs.

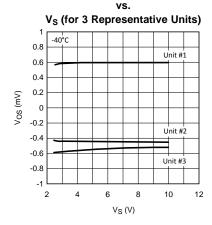


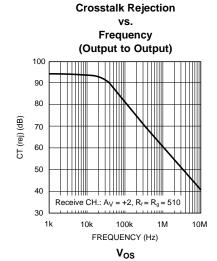
Typical Performance Characteristics (continued)

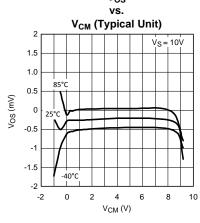
At $T_J = 25$ °C, $V^+ = +5$, $V^- = -5V$, $R_F = R_L = 2k\Omega$. Unless otherwise specified.

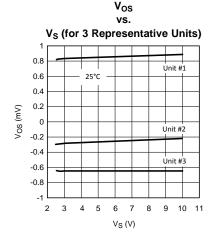








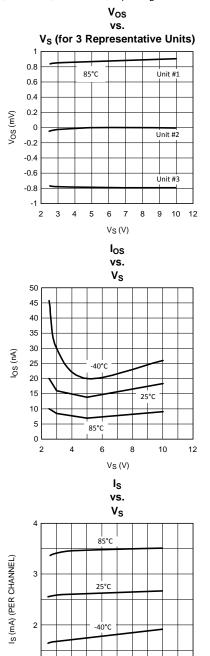




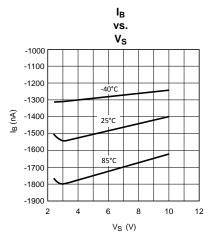


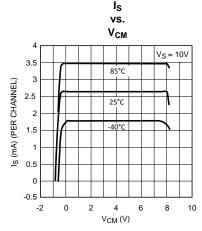


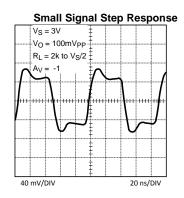
At $T_J = 25$ °C, $V^+ = +5$, $V^- = -5V$, $R_F = R_L = 2k\Omega$. Unless otherwise specified.



V_S (V)



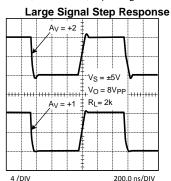




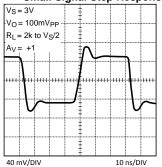
INSTRUMENTS

Typical Performance Characteristics (continued)

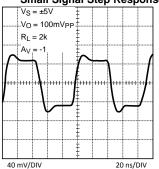
At $T_J = 25$ °C, $V^+ = +5$, $V^- = -5V$, $R_F = R_L = 2k\Omega$. Unless otherwise specified.



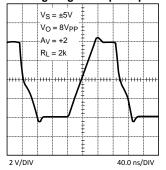




Small Signal Step Response



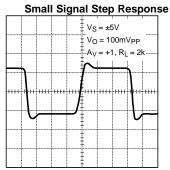
Large Signal Step Response



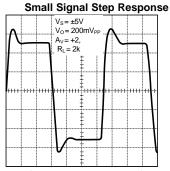
Large Signal Step Response



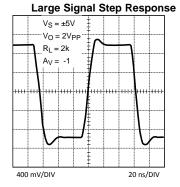
400 mV/DIV 40.0 nS/DIV



40 mV/DIV 10.0 ns/DIV



40 mV/DIV 20.0 ns/DIV

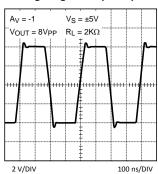


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Typical Performance Characteristics (continued)

At $T_J = 25$ °C, $V^+ = +5$, $V^- = -5V$, $R_F = R_L = 2k\Omega$. Unless otherwise specified.

Large Signal Step Response



Application Notes

CIRCUIT DESCRIPTION

The LMH664XEP family is based on National Semiconductor's proprietary VIP10 dielectrically isolated bipolar process.

This device family architecture features the following:

- Complimentary bipolar devices with exceptionally high f_t (~8GHz) even under low supply voltage (2.7V) and low bias current.
- A class A-B "turn-around" stage with improved noise, offset, and reduced power dissipation compared to similar speed devices (patent pending).
- Common Emitter push-push output stage capable of 75mA output current (at 0.5V from the supply rails) while
 consuming only 2.7mA of total supply current per channel. This architecture allows output to reach within
 milli-volts of either supply rail.
- Consistent performance from any supply voltage (3V-10V) with little variation with supply voltage for the most important specifications (e.g. BW, SR, I_{OUT}, etc.)
- Significant power saving (~40%) compared to competitive devices on the market with similar performance.

Application Hints

This Op Amp family is a drop-in replacement for the AD805X family of high speed Op Amps in most applications. In addition, the LMH664XEP will typically save about 40% on power dissipation, due to lower supply current, when compared to competition. All AD805X family's guaranteed parameters are included in the list of LMH664XEP guaranteed specifications in order to ensure equal or better level of performance. However, as in most high performance parts, due to subtleties of applications, it is strongly recommended that the performance of the part to be evaluated is tested under actual operating conditions to ensure full compliance to all specifications.

With 3V supplies and a common mode input voltage range that extends 0.5V below V $^-$, the LMH664XEP find applications in low voltage/low power applications. Even with 3V supplies, the -3dB BW (@ A $_V$ = +1) is typically 115MHz with a tested limit of 80MHz. Production testing guarantees that process variations with not compromise speed. High frequency response is exceptionally stable confining the typical -3dB BW over the industrial temperature range to $\pm 2.5\%$.

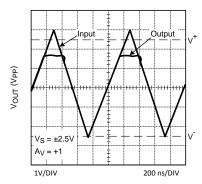
As can be seen from the typical performance plots, the LMH664XEP output current capability (~75mA) is enhanced compared to AD805X. This enhancement, increases the output load range, adding to the LMH664XEP's versatility.

Because of the LMH664XEP's high output current capability attention should be given to device junction temperature in order not to exceed the Absolute Maximum Rating.

This device family was designed to avoid output phase reversal. With input overdrive, the output is kept near supply rail (or as closed to it as mandated by the closed loop gain setting and the input voltage). See:

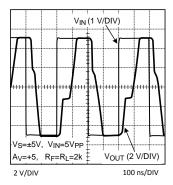
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However, if the input voltage range of −0.5V to 1V from V⁺ is exceeded by more than a diode drop, the internal ESD protection diodes will start to conduct. The current in the diodes should be kept at or below 10mA.

Output overdrive recovery time is less than 100ns as can be seen from the following plot:



SINGLE SUPPLY, LOW POWER PHOTODIODE AMPLIFIER

The circuit shown is used to amplify the current from a photo-diode into a voltage output. In this circuit, the emphasis is on achieving high bandwidth and the transimpedance gain setting is kept relatively low. Because of its high slew rate limit and high speed, the LMH664XEP family lends itself well to such an application.

This circuit achieves approximately 1V/mA of transimpedance gain and capable of handling up to $1mA_{pp}$ from the photodiode. Q1, in a common base configuration, isolates the high capacitance of the photodiode (C_d) from the Op Amp input in order to maximize speed. Input is AC coupled through C1 to ease biasing and allow single supply operation. With 5V single supply, the device input/output is shifted to near half supply using a voltage divider from V_{CC} . Note that Q1 collector does not have any voltage swing and the Miller effect is minimized. D1, tied to Q1 base, is for temperature compensation of Q1's bias point. Q1 collector current was set to be large enough to handle the peak-to-peak photodiode excitation and not too large to shift the U1 output too far from mid-supply.

No matter how low an R_f is selected, there is a need for C_f in order to stabilize the circuit. The reason for this is that the Op Amp input capacitance and Q1 equivalent collector capacitance together (C_{IN}) will cause additional phase shift to the signal fed back to the inverting node. C_f will function as a zero in the feedback path counteracting the effect of the C_{IN} and acting to stabilized the circuit. By proper selection of C_f such that the Op Amp open loop gain is equal to the inverse of the feedback factor at that frequency, the response is optimized with a theoretical 45° phase margin.

$$C_F = \sim SQRT \left[(C_{IN})/(2\pi \cdot GBWP \cdot R_F) \right]$$
 (1)

where GBWP is the Gain Bandwidth Product of the Op Amp

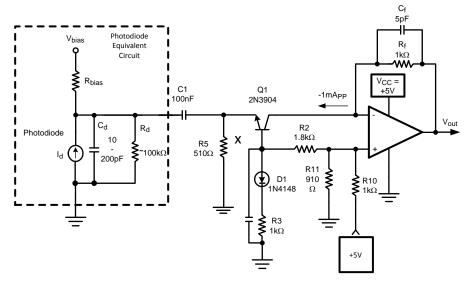
Optimized as such, the I-V converter will have a theoretical pole, fp, at:

$$f_P = SQRT \left[GBWP/(2\pi R_F \cdot C_{IN}) \right]$$
 (2)

With Op Amp input capacitance of 3pF and an estimate for Q1 output capacitance of about 3pF as well, C_{IN} = 6pF. From the typical performance plots, LMH6642EP/6643EP family GBWP is approximately 57MHz. Therefore, with R_f = 1k, from Equation 1 and 2 above.

TEXAS INSTRUMENTS

 $C_f = \sim 4.1 pF$, and $f_p = 39 MHz$



For this example, optimum C_f was empirically determined to be around 5pF. This time domain response is shown in Figure 5 below showing about 9ns rise/fall times, corresponding to about 39MHz for f_p . The overall supply current from the +5V supply is around 5mA with no load.

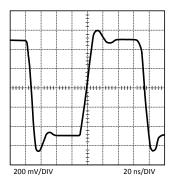


Figure 5.

PRINTED CIRCUIT BOARD LAYOUT AND COMPONENT VALUES SECTIONS

Generally, a good high frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitances on these nodes to ground will cause frequency response peaking and possible circuit oscillations (see Application Note OA-15 for more information). National Semiconductor suggests the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization:

Device	Package	Evaluation Board PN
LMH6642MF	SOT23-5	CLC730068
LMH6642MF	8-Pin SOIC	CLC730027
LMH6643MA	8-Pin SOIC	CLC730036
LMH6643MA	8-Pin MSOP	CLC730123
LMH6644MA	14-Pin SOIC	CLC730031
LMH6644MA	14-Pin TSSOP	CLC730131



LMH6642EP, LMH6643EP, LMH6644EP

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These free evaluation boards are shipped when a device sample request is placed with National Semiconductor.

Another important parameter in working with high speed/high performance amplifiers, is the component values selection. Choosing external resistors that are large in value will effect the closed loop behavior of the stage because of the interaction of these resistors with parasitic capacitances. These capacitors could be inherent to the device or a by-product of the board layout and component placement. Either way, keeping the resistor values lower, will diminish this interaction to a large extent. On the other hand, choosing very low value resistors could load down nodes and will contribute to higher overall power dissipation.

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