National Semiconductor

May 1997

# LMV8172
# Vertical Deflection Output Amplifier

## General Description

The LMV8172 is a monolithic amplifier for driving the vertical deflection yoke of a CRT. The IC is a differential input, single-ended output amplifier with a flyback generator. This architecture minimizes the power dissipation during forward scanning without slowing down the flyback.

The LMV8172 is packaged in a 7-pin TO-220 power package.

## Features

- High output current
- Flyback generator
- Minimum external part count
- Works with single or dual supplies
- Low cross-over distortion

## Applications

- Vertical deflection for monitors and TVs

## Connection Diagram

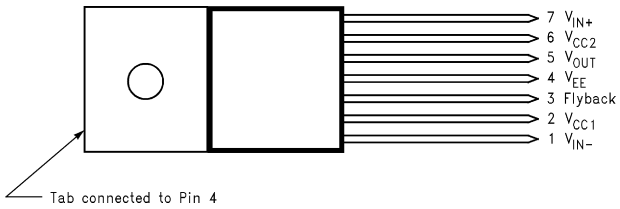


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**FIGURE 1. Top View**
**Order Number LMV8172T**
**See NS Package Number TA07B**

 

## Absolute Maximum Ratings (Notes 1, 3)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage, ($V_S = V_{CC1} - V_{EE}$) | 35V |
| Flyback Peak Voltage, | |
| ($V_{OUT} - V_{EE}$) | 60V |
| ($V_{CC2} - V_{EE}$) | 60V |
| Input Voltage, ($V_{DC}$) | |
| Pins 1, 7 | $V_{EE} \le V_{IN} \le V_{CC1}$ |
| Output Peak Current, ($I_O$) | |
| Pin 5 (Note 8) | 3.2 $A_{pp}$ |
| Power Dissipation ($P_D$) | |
| $T_C = 25^\circ C$ | 41W |
| $T_C = 90^\circ C$ | 20W |
| Above 25°C, derate based on $\theta_{JC}$ and $T_J$ (Note 4) | |
| Thermal Resistance ($\theta_{JC}$) | 3°C/W |
| Junction Temperature ($T_{JMAX}$) | 150°C |
| ESD Susceptibility (Note 5) | 2 kV |
| Storage Temperature | −65°C to +80°C |
| Lead Temperature (Soldering 10 seconds) | 265°C |

## Operating Ratings (Note 2)

| | |
|---|---|
| Junction Temperature Range | $-20^\circ C \le T_J \le +150^\circ C$ |

## Electrical Characteristics

$V_{CC1}$ = +17.5V; $V_{CC2}$ = +16.9V; $V_{EE}$ = −17.5V; $T_C$ = 25°C unless otherwise specified.

| Symbol | Parameter | Conditions | Typical (Note 6) | Limit (Note 7) | Units |
|---|---|---|---|---|---|
| $I_{2+6}$ | Total Quiescent Current ($I_2 + I_6$) | See Figure 2 | 11 | 20 | mA (max) |
| $I_1$ | Input Bias Current | | -0.5 | -2.0 | µA (max) |
| $I_{os}$ | Input Offset Current | | 0.5 | 3.0 | µA (max) |
| $V_{3L}$ | Pin 3 Saturation Voltage to $V_{EE}$ | See Figure 3, $I_3$ = 20 mA | 1.1 | 2.0 | V (max) |
| $V_{5L}$ | Output Saturation Voltage to $V_{EE}$ | See Figure 3, $I_5$ = 1.2A | 1.3 | 2.5 | V (max) |
| | | $I_5$ = 0.7A | 0.7 | 1.4 | V (max) |
| $V_{5H}$ | Output Saturation Voltage to $V_{CC2}$ | See Figure 4, $I_5$ = −1.2A | 2.6 | 3.3 | V (max) |
| | | $I_5$ = −0.7A | 2.1 | 2.8 | V (max) |

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

**Note 2:** Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

**Note 3:** All voltages are measured with respect to GND, unless otherwise specified.

**Note 4:** The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{JMAX}$, $\theta_{JC}$ and the case temperature, $T_C$. The maximum allowable power dissipation at any elevated temperature is $P_D = (T_{JMAX} - T_C) / \theta_{JC}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_{JMAX}$ = 150°C. The typical thermal resistance ($\theta_{JC}$) of the LMV8172 is 3°C/W.

**Note 5:** Human Body model, 100 pF capacitor discharged through a 1.5 kΩ resistor.

**Note 6:** Typicals are at $T_C$ = 25°C and represent most likely parametric norm.

**Note 7:** Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

**Note 8:** Maximum output current is tested with a load of 3 mH, $V_{CC1}$ = +15V and $V_{EE}$ = −15V, $V_{IN+}$ set so the device is drawing equal amounts of current from both supplies, and the sawtooth on $V_{IN-}$ set so the voltage waveform on pin 5 is as large as possible without distortion.

## Test Circuits

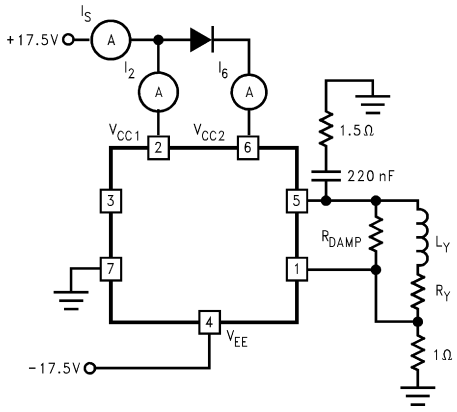


**FIGURE 2.**

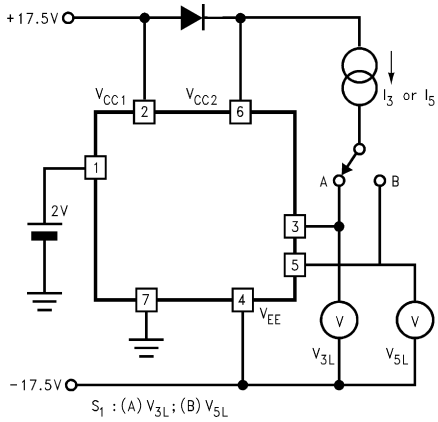


**FIGURE 3.**

## Test Circuits (Continued)

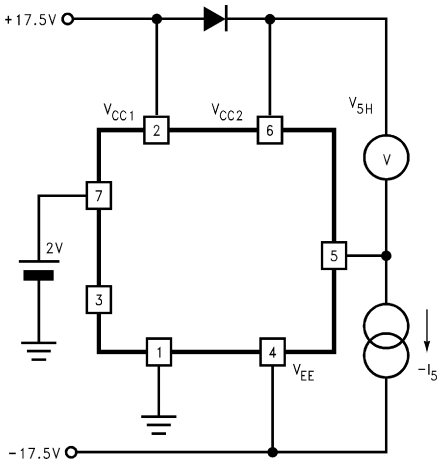


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**FIGURE 4.**

## Block Diagram

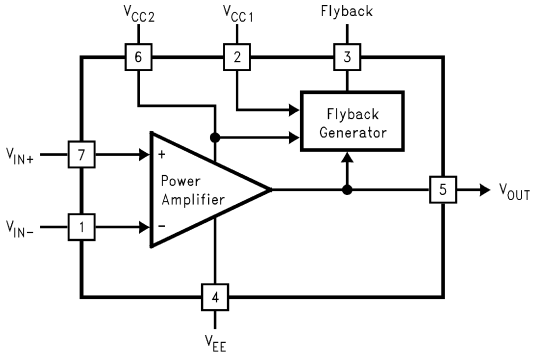


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**FIGURE 5.**

## Application Hints

To get the best possible performance from the LMV8172T it is important to use a good PCB layout and the correct components. The 0.1 µF and 470 µF capacitors on the $V_{CC1}$ and $V_{EE}$ lines should be as close as possible to their pins. The power traces should be wide and there should be no jumpers between the capacitors and the LMV8172T. The value of the electrolytic capacitors used on the $V_{CC1}$ and $V_{EE}$ lines should be 470 µF or greater. The ground traces should also be as wide as possible. The diode and optional capacitor should be located close to the LMV8172T. The diode should be a fast-recovery type, the 1N4937 recommended has a $t_{rr}$ of 150 ns. The capacitor is optional, it may be needed in some PCB layouts. A suggested layout is shown in *Figure 6*.

## Application Hints (Continued)

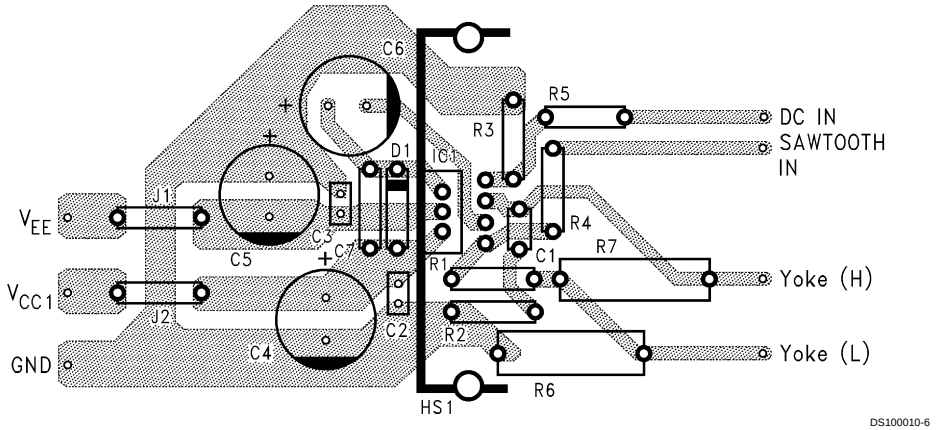



**FIGURE 6.**

## Typical Application

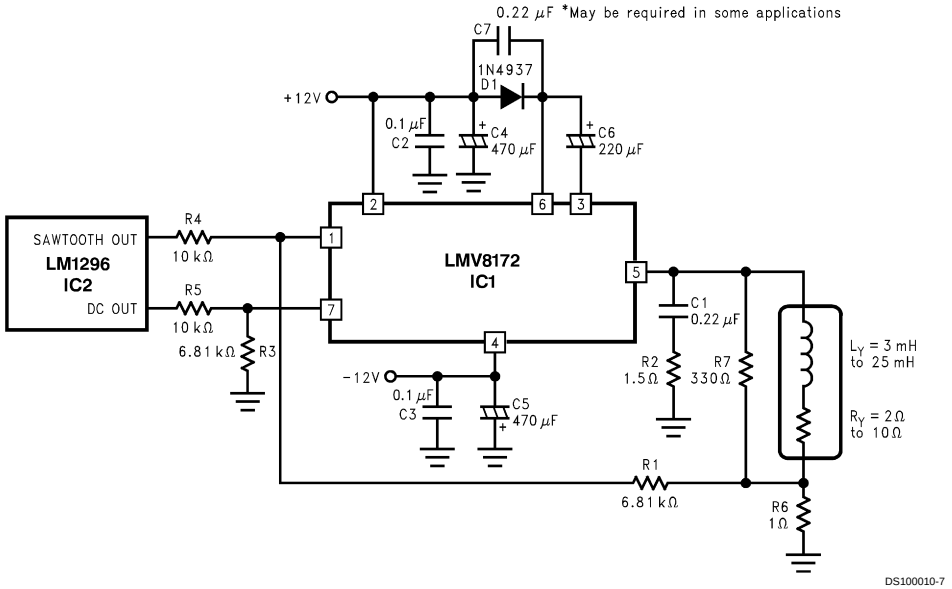
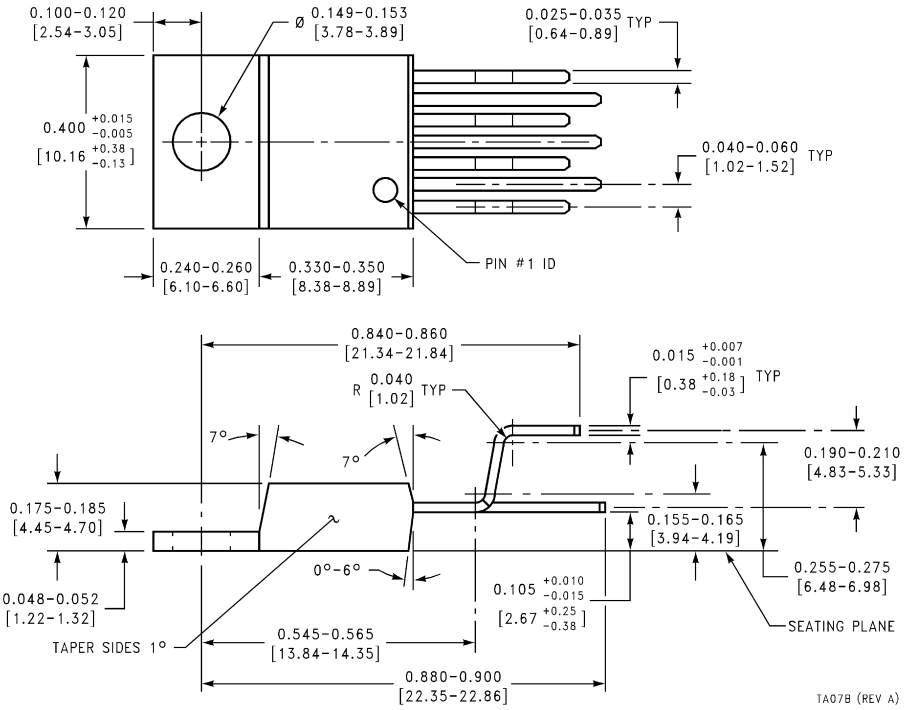



**FIGURE 7.**

## Physical Dimensions inches (millimeters) unless otherwise noted




**Order Number LMV8172T**
**NS Package Number TA07B**

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